Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	600
Number of Logic Elements/Cells	2700
Total RAM Bits	81920
Number of I/O	196
Number of Gates	128236
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	352-LBGA Exposed Pad, Metal
Supplier Device Package	352-MBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv100e-7bg352c

Eight I/O banks result from separating each edge of the FPGA into two banks, as shown in Figure 3. Each bank has multiple V_{CCO} pins, all of which must be connected to the same voltage. This voltage is determined by the output standards in use.

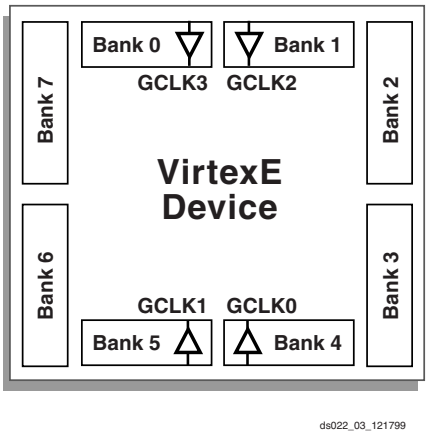

Figure 3: **Virtex-E I/O Banks**

Within a bank, output standards can be mixed only if they use the same V_{CCO}. Compatible standards are shown in Table 2. GTL and GTL+ appear under all voltages because their open-drain outputs do not depend on V_{CCO}.

Table 2: **Compatible Output Standards**

V_{CCO}	Compatible Standards
3.3 V	PCI, LVTTL, SSTL3 I, SSTL3 II, CTT, AGP, GTL, GTL+, LVPECL
2.5 V	SSTL2 I, SSTL2 II, LVCMOS2, GTL, GTL+, BLVDS, LVDS
1.8 V	LVCMOS18, GTL, GTL+
1.5 V	HSTL I, HSTL III, HSTL IV, GTL, GTL+

Some input standards require a user-supplied threshold voltage, V_{REF}. In this case, certain user-I/O pins are automatically configured as inputs for the V_{REF} voltage. Approximately one in six of the I/O pins in the bank assume this role.

The V_{REF} pins within a bank are interconnected internally and consequently only one V_{REF} voltage can be used within each bank. All V_{REF} pins in the bank, however, must be connected to the external voltage source for correct operation.

Within a bank, inputs that require V_{REF} can be mixed with those that do not. However, only one V_{REF} voltage can be used within a bank.

In Virtex-E, input buffers with LVTTL, LVCMOS2, LVCMOS18, PCI33_3, PCI66_3 standards are supplied by V_{CCO} rather than V_{CCINT}. For these standards, only input and output buffers that have the same V_{CCO} can be mixed together.

The V_{CCO} and V_{REF} pins for each bank appear in the device pin-out tables and diagrams. The diagrams also show the bank affiliation of each I/O.

Within a given package, the number of V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices, more I/O pins convert to V_{REF} pins. Since these are always a super set of the V_{REF} pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device if necessary. All the V_{REF} pins for the largest device anticipated must be connected to the V_{REF} voltage, and not used for I/O.

In smaller devices, some V_{CCO} pins used in larger devices do not connect within the package. These unconnected pins can be left unconnected externally, or can be connected to the V_{CCO} voltage to permit migration to a larger device if necessary.

Configurable Logic Blocks

The basic building block of the Virtex-E CLB is the logic cell (LC). An LC includes a 4-input function generator, carry logic, and a storage element. The output from the function generator in each LC drives both the CLB output and the D input of the flip-flop. Each Virtex-E CLB contains four LCs, organized in two similar slices, as shown in Figure 4. Figure 5 shows a more detailed view of a single slice.

In addition to the four basic LCs, the Virtex-E CLB contains logic that combines function generators to provide functions of five or six inputs. Consequently, when estimating the number of system gates provided by a given device, each CLB counts as 4.5 LCs.

Look-Up Tables

Virtex-E function generators are implemented as 4-input look-up tables (LUTs). In addition to operating as a function generator, each LUT can provide a 16 x 1-bit synchronous RAM. Furthermore, the two LUTs within a slice can be combined to create a 16 x 2-bit or 32 x 1-bit synchronous RAM, or a 16 x 1-bit dual-port synchronous RAM.

The Virtex-E LUT can also provide a 16-bit shift register that is ideal for capturing high-speed or burst-mode data. This mode can also be used to store data in applications such as Digital Signal Processing.

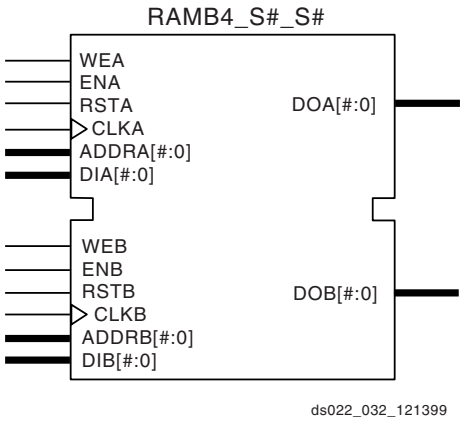

Figure 31: **Dual-Port Block SelectRAM+ Memory**

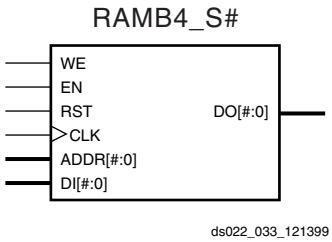

Figure 32: **Single-Port Block SelectRAM+ Memory**

Table 14: **Available Library Primitives**

Primitive	Port A Width	Port B Width
RAMB4_S1	1	N/A
RAMB4_S1_S1		1
RAMB4_S1_S2		2
RAMB4_S1_S4		4
RAMB4_S1_S8		8
RAMB4_S1_S16		16
RAMB4_S2	2	N/A
RAMB4_S2_S2		2
RAMB4_S2_S4		4
RAMB4_S2_S8		8
RAMB4_S2_S16		16
RAMB4_S4	4	N/A
RAMB4_S4_S4		4
RAMB4_S4_S8		8
RAMB4_S4_S16		16
RAMB4_S8	8	N/A
RAMB4_S8_S8		8
RAMB4_S8_S16		16
RAMB4_S16	16	N/A
RAMB4_S16_S16		16

Port Signals

Each block SelectRAM+ port operates independently of the others while accessing the same set of 4096 memory cells.

Table 15 describes the depth and width aspect ratios for the block SelectRAM+ memory.

Table 15: **Block SelectRAM+ Port Aspect Ratios**

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

Clock—CLK[A|B]

Each port is fully synchronous with independent clock pins. All port input pins have setup time referenced to the port CLK pin. The data output bus has a clock-to-out time referenced to the CLK pin.

Enable—EN[A|B]

The enable pin affects the read, write and reset functionality of the port. Ports with an inactive enable pin keep the output pins in the previous state and do not write data to the memory cells.

Write Enable—WE[A|B]

Activating the write enable pin allows the port to write to the memory cells. When active, the contents of the data input bus are written to the RAM at the address pointed to by the address bus, and the new data also reflects on the data out bus. When inactive, a read operation occurs and the contents of the memory cells referenced by the address bus reflect on the data out bus.

Reset—RST[A|B]

The reset pin forces the data output bus latches to zero synchronously. This does not affect the memory cells of the RAM and does not disturb a write operation on the other port.

Address Bus—ADDR[A|B]<#:0>

The address bus selects the memory cells for read or write. The width of the port determines the required width of this bus as shown in Table 15.

Data In Bus—DI[A|B]<#:0>

The data in bus provides the new data value to be written into the RAM. This bus and the port have the same width, as shown in Table 15.

Application Examples

Creating a design with the SelectI/O features requires the instantiation of the desired library symbol within the design code. At the board level, designers need to know the termination techniques required for each I/O standard.

This section describes some common application examples illustrating the termination techniques recommended by each of the standards supported by the SelectI/O features.

Termination Examples

Circuit examples involving typical termination techniques for each of the SelectI/O standards follow. For a full range of accepted values for the DC voltage specifications for each standard, refer to the table associated with each figure.

The resistors used in each termination technique example and the transmission lines depicted represent board level components and are not meant to represent components on the device.

GTL

A sample circuit illustrating a valid termination technique for GTL is shown in Figure 44.

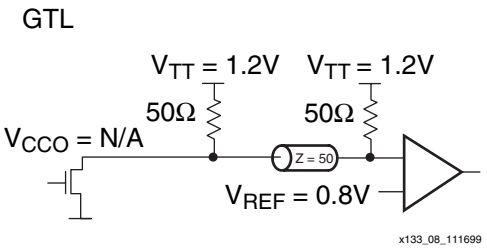

Figure 44: **Terminated GTL**

Table 23 lists DC voltage specifications.

Table 23: **GTL Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	-	N/A	-
$V_{REF} = N \times V_{TT}$[1]	0.74	0.8	0.86
V_{TT}	1.14	1.2	1.26
$V_{IH} = V_{REF} + 0.05$	0.79	0.85	-
$V_{IL} = V_{REF} - 0.05$	-	0.75	0.81
V_{OH}	-	-	-
V_{OL}	-	0.2	0.4
I_{OH} at V_{OH}(mA)	-	-	-
I_{OL}at V_{OL}(mA) at 0.4V	32	-	-
I_{OL}at V_{OL}(mA) at 0.2V	-	-	40

Notes:
1. N must be greater than or equal to 0.653 and less than or equal to 0.68.

GTL+

A sample circuit illustrating a valid termination technique for GTL+ appears in Figure 45. DC voltage specifications appear in Table 24.

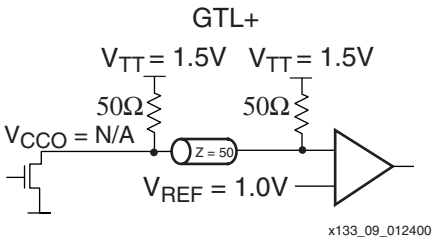

Figure 45: **Terminated GTL+**

Table 24: **GTL+ Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	-	-	-
$V_{REF} = N \times V_{TT}$[1]	0.88	1.0	1.12
V_{TT}	1.35	1.5	1.65
$V_{IH} = V_{REF} + 0.1$	0.98	1.1	-
$V_{IL} = V_{REF} - 0.1$	-	0.9	1.02
V_{OH}	-	-	-
V_{OL}	0.3	0.45	0.6
I_{OH} at V_{OH} (mA)	-	-	-
I_{OL}at V_{OL} (mA) at 0.6V	36	-	-
I_{OL}at V_{OL} (mA) at 0.3V	-	-	48

Notes:
1. N must be greater than or equal to 0.653 and less than or equal to 0.68.

SSTL3_I

A sample circuit illustrating a valid termination technique for SSTL3_I appears in Figure 49. DC voltage specifications appear in Table 28.

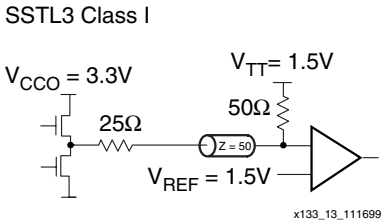

Figure 49: **Terminated SSTL3 Class I**

Table 28: **SSTL3_I Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	**3.0**	**3.3**	**3.6**
V_{REF} = 0.45 × V_{CCO}	1.3	1.5	1.7
V_{TT} = V_{REF}	1.3	1.5	1.7
V_{IH} = V_{REF} + 0.2	1.5	1.7	3.9(1)
V_{IL} = V_{REF} – 0.2	–0.3(2)	1.3	1.5
V_{OH} = V_{REF} + 0.6	1.9	-	-
V_{OL} = V_{REF} – 0.6	-	-	1.1
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL}at V_{OL} (mA)	8	-	-

Notes:
1. V_{IH} maximum is V_{CCO} + 0.3
2. V_{IL} minimum does not conform to the formula

SSTL3_II

A sample circuit illustrating a valid termination technique for SSTL3_II appears in Figure 50. DC voltage specifications appear in Table 29.

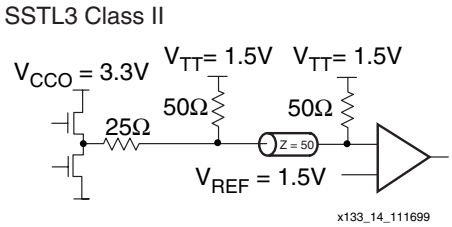

Figure 50: **Terminated SSTL3 Class II**

Table 29: **SSTL3_II Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
V_{REF} = 0.45 × V_{CCO}	1.3	1.5	1.7
V_{TT} = V_{REF}	1.3	1.5	1.7
V_{IH} = V_{REF} + 0.2	1.5	1.7	3.9(1)
V_{IL}= V_{REF} – 0.2	–0.3(2)	1.3	1.5
V_{OH} = V_{REF} + 0.8	2.1	-	-
V_{OL}= V_{REF} – 0.8	-	-	0.9
I_{OH} at V_{OH} (mA)	–16	-	-
I_{OL}at V_{OL} (mA)	16	-	-

Notes:
1. V_{IH} maximum is V_{CCO} + 0.3
2. V_{IL} minimum does not conform to the formula

SSTL2_I

A sample circuit illustrating a valid termination technique for SSTL2_I appears in Figure 51. DC voltage specifications appear in Table 30.

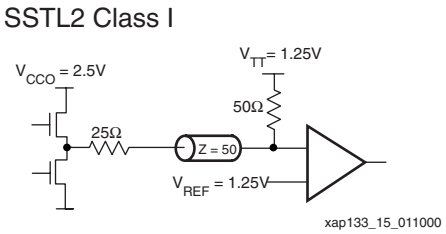

Figure 51: **Terminated SSTL2 Class I**

Table 30: **SSTL2_I Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
V_{REF} = 0.5 × V_{CCO}	1.15	1.25	1.35
V_{TT} = V_{REF} + N(1)	1.11	1.25	1.39
V_{IH} = V_{REF} + 0.18	1.33	1.43	3.0(2)
V_{IL} = V_{REF} – 0.18	–0.3(3)	1.07	1.17
V_{OH} = V_{REF} + 0.61	1.76	-	-
V_{OL}= V_{REF} – 0.61	-	-	0.74
I_{OH} at V_{OH} (mA)	–7.6	-	-
I_{OL}at V_{OL} (mA)	7.6	-	-

Notes:
1. N must be greater than or equal to -0.04 and less than or equal to 0.04.
2. V_{IH} maximum is V_{CCO} + 0.3.
3. V_{IL} minimum does not conform to the formula.

Virtex-E Data Sheet

The Virtex-E Data Sheet contains the following modules:

- DS022-1, Virtex-E 1.8V FPGAs:
  Introduction and Ordering Information (Module 1)
- DS022-2, Virtex-E 1.8V FPGAs:
  Functional Description (Module 2)
- DS022-3, Virtex-E 1.8V FPGAs:
  DC and Switching Characteristics (Module 3)
- DS022-4, Virtex-E 1.8V FPGAs:
  Pinout Tables (Module 4)

Virtex-E Pin Definitions

Pin Name	Dedicated Pin	Direction	Description
GCK0, GCK1, GCK2, GCK3	Yes	Input	Clock input pins that connect to Global Clock Buffers.
M0, M1, M2	Yes	Input	Mode pins are used to specify the configuration mode.
CCLK	Yes	Input or Output	The configuration Clock I/O pin: it is an input for SelectMAP and slave-serial modes, and output in master-serial mode. After configuration, it is input only, logic level = Don't Care.
PROGRAM	Yes	Input	Initiates a configuration sequence when asserted Low.
DONE	Yes	Bidirectional	Indicates that configuration loading is complete, and that the start-up sequence is in progress. The output can be open drain.
INIT	No	Bidirectional (Open-drain)	When Low, indicates that the configuration memory is being cleared. The pin becomes a user I/O after configuration.
BUSY/DOUT	No	Output	In SelectMAP mode, BUSY controls the rate at which configuration data is loaded. The pin becomes a user I/O after configuration unless the SelectMAP port is retained. In bit-serial modes, DOUT provides preamble and configuration data to downstream devices in a daisy-chain. The pin becomes a user I/O after configuration.
D0/DIN, D1, D2, D3, D4, D5, D6, D7	No	Input or Output	In SelectMAP mode, D0-7 are configuration data pins. These pins become user I/Os after configuration unless the SelectMAP port is retained. In bit-serial modes, DIN is the single data input. This pin becomes a user I/O after configuration.
WRITE	No	Input	In SelectMAP mode, the active-low Write Enable signal. The pin becomes a user I/O after configuration unless the SelectMAP port is retained.
CS	No	Input	In SelectMAP mode, the active-low Chip Select signal. The pin becomes a user I/O after configuration unless the SelectMAP port is retained.
TDI, TDO, TMS, TCK	Yes	Mixed	Boundary-scan Test-Access-Port pins, as defined in IEEE1149.1.
DXN, DXP	Yes	N/A	Temperature-sensing diode pins. (Anode: DXP, cathode: DXN)
V_{CCINT}	Yes	Input	Power-supply pins for the internal core logic.
V_{CCO}	Yes	Input	Power-supply pins for the output drivers (subject to banking rules)
V_{REF}	No	Input	Input threshold voltage pins. Become user I/Os when an external threshold voltage is not needed (subject to banking rules).
GND	Yes	Input	Ground

Pinout Differences Between Virtex and Virtex-E Families

The same device in the same package for the Virtex-E and Virtex families are pin-compatible with some minor exceptions, listed in Table 1.

XCV200E Device, FG456 Package

The Virtex-E XCV200E has two I/O pins swapped with the Virtex XCV200 to accommodate differential clock pairing.

XCV400E Device, FG676 Package

The Virtex-E XCV400E has two I/O pins swapped with the Virtex XCV400 to accommodate differential clock pairing.

All Devices, PQ240 and HQ240 Packages

The Virtex devices in PQ240 and HQ240 packages do not have V_{CCO} banking, but Virtex-E devices do. To achieve this, eight Virtex I/O pins (P232, P207, P176, P146, P116, P85, P55, and P25) are now VCCO pins in the Virtex-E family. This change also requires one Virtex I/O or VREF pin to be swapped with a standard I/O pin.

Additionally, accommodating differential clock input pairs in Virtex-E caused some IO_V_{REF} differences in the XCV400E and XCV600E devices only. Virtex IO_V_{REF} pins P215 and P87 are Virtex-E IO_V_{REF} pins P216 and P86, respectively. Virtex-E pins P215 and P87 are IO_DLL.

Table 1: **Pinout Differences Summary**

Part	Package	Pins	Virtex	Virtex-E
XCV200	FG456	E11, U11	I/O	No Connect
		B11, AA11	No Connect	IO_LVDS_DLL
XCV400	FG676	D13, Y13	I/O	No Connect
		B13, AF13	No Connect	IO_LVDS_DLL
XCV400/600	PQ240/HQ240	P215, P87	IO_V_{REF}	IO_LVDS_DLL
		P216, P86	I/O	IO_V_{REF}
All	PQ240/HQ240	P232, P207, P176, P146, P116, P85, P55, and P25	I/O	V_{CCO}
		P231	I/O	IO_V_{REF}

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P138	IO_D5_L26N_YY	3
P137	VCCINT	NA
P136	VCCO	3
P135	GND	NA
P134	IO_D6_L27P_Y	3
P133	IO_VREF_L27N_Y	3
P132	IO_VREF	3
P131	IO_L28P_Y	3
P130	IO_VREF_L28N_Y	3
P129	GND	NA
P128	IO_L29P_Y	3
P127	IO_L29N_Y	3
P126	IO_VREF_L30P_Y	3
P125	IO_L30N_Y	3
P124	IO_D7_L31P_YY	3
P123	IO_INIT_L31N_YY	3
P122	PROGRAM	NA
P121	VCCO	3
P120	DONE	3
P119	GND	NA
P118	IO_L32P_YY	4
P117	IO_L32N_YY	4
P116	VCCO	4
P115	IO_VREF	4
P114	IO_L33P_YY	4
P113	IO_L33N_YY	4
P112	GND	NA
P111	IO_VREF_L34P_YY	4
P110	IO_L34N_YY	4
P109	IO_VREF	4
P108	IO_VREF_L35P_YY	4
P107	IO_L35N_YY	4
P106	GND	NA
P105	VCCO	4
P104	VCCINT	NA
P103	IO_L36P_YY	4

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P102	IO_L36N_YY	4
P101[1]	IO_VREF	4
P100	IO_L37P_Y	4
P99	IO_L37N_Y	4
P98	GND	NA
P97	IO_VREF_L38P_Y	4
P96	IO_L38N_Y	4
P95	IO_L39P	4
P94	IO_VREF_L39N	4
P93	IO_LVDS_DLL_L40P	4
P92	GCK0	4
P91	GND	NA
P90	VCCO	4
P89	GCK1	5
P88	VCCINT	NA
P87	IO_LVDS_DLL_L40N	5
P86	IO_VREF	5
P85	VCCO	5
P84	IO_VREF_L41P	5
P83	GND	NA
P82	IO_L41N	5
P81	IO	5
P80[1]	IO_VREF	5
P79	IO_L42P_YY	5
P78	IO_L42N_YY	5
P77	VCCINT	NA
P76	VCCO	5
P75	GND	NA
P74	IO_L43P_YY	5
P73	IO_VREF_L43N_YY	5
P72	IO_VREF	5
P71	IO_L44P_YY	5
P70	IO_VREF_L44N_YY	5
P69	GND	NA
P68	IO_L45P_YY	5
P67	IO_L45N_YY	5

BG352 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A check (√) in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock

Table 11: **BG352 Differential Pin Pair Summary XCV100E, XCV200E, XCV300E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	AE13	AC13	NA	IO LVDS 55
1	5	AF14	AD14	NA	IO LVDS 55
2	1	B14	A13	NA	IO LVDS 9
3	0	D14	A15	NA	IO LVDS 9
IO LVDS Total Outputs: 87, Asynchronous Output Pairs: 43					
0	0	B23	D21	√	VREF_0
1	0	D20	A23	√	-
2	0	B22	C21	√	VREF_0
3	0	A21	B20	2	-
4	0	B19	C19	√	VREF_0
5	0	C18	D17	√	-
6	0	A18	C17	2	-
7	0	C16	B17	√	-
8	0	D15	A16	√	VREF_0
9	1	A13	A15	√	GCLK LVDS 3/2
10	1	A12	C13	2	-
11	1	C12	B12	√	VREF_1
12	1	B11	A11	√	-
13	1	D11	C11	2	-
14	1	C10	B9	√	-
15	1	C9	B8	√	VREF_1
16	1	A7	D9	1	-
17	1	B6	A6	√	VREF_1
18	1	A4	C7	√	-

Table 11: **BG352 Differential Pin Pair Summary XCV100E, XCV200E, XCV300E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
19	1	D6	C6	√	VREF_1
20	1	C4	D5	√	CS
21	2	E4	D3	√	DIN_D0
22	2	D2	C1	√	VREF_2
23	2	G4	F3	√	-
24	2	E2	F2	√	VREF_2
25	2	F1	J4	2	-
26	2	H2	G1	√	D1
27	2	J3	J2	√	D2
28	2	J1	L4	1	-
29	2	L3	L2	√	-
30	2	M4	M3	√	D3
31	2	M2	M1	2	-
32	2	N4	N2	√	-
33	3	R1	R2	2	-
34	3	R3	R4	√	VREF_3
35	3	T2	U2	√	-
36	3	T4	V1	1	-
37	3	U3	U4	√	D5
38	3	V3	V4	√	VREF_3
39	3	Y1	Y2	1	-
40	3	AA2	Y3	√	VREF_3
41	3	AC1	AB2	√	-
42	3	AA4	AC2	√	VREF_3
43	3	AC3	AD2	√	INIT
44	4	AC5	AD4	√	-
45	4	AE4	AF3	√	VREF_4
46	4	AC7	AD6	√	-
47	4	AE5	AE6	√	VREF_4
48	4	AF6	AC9	2	-
49	4	AE8	AF7	√	VREF_4
50	4	AD9	AE9	√	-
51	4	AF9	AC11	2	-
52	4	AD11	AE11	√	-
53	4	AC12	AD12	√	VREF_4
54	4	AE12	AF12	2	-

Table 12: **BG432 — XCV300E, XCV400E, XCV600E**

Bank	Pin Description	Pin #
2	IO_L41N_Y	H2
2	IO_VREF_L42P_Y	H1[1]
2	IO_L42N_Y	J4
2	IO_VREF_L43P_YY	J2
2	IO_D1_L43N_YY	K4
2	IO_D2_L44P_YY	K2
2	IO_L44N_YY	K1
2	IO_L45P_Y	L2
2	IO_L45N_Y	M4
2	IO_L46P_Y	M3
2	IO_L46N_Y	M2
2	IO_L47P_Y	N4
2	IO_L47N_Y	N3
2	IO_VREF_L48P_YY	N1
2	IO_D3_L48N_YY	P4
2	IO_L49P_Y	P3
2	IO_L49N_Y	P2
2	IO_VREF_L50P_Y	R3[2]
2	IO_L50N_Y	R4
2	IO_L51P_YY	R1
2	IO_L51N_YY	T3
3	IO	AA2
3	IO	AC2
3	IO	AE2
3	IO	U3
3	IO	W1
3	IO_L52P_Y	U4
3	IO_VREF_L52N_Y	U2[2]
3	IO_L53P_Y	U1
3	IO_L53N_Y	V3
3	IO_D4_L54P_YY	V4
3	IO_VREF_L54N_YY	V2
3	IO_L55P_Y	W3
3	IO_L55N_Y	W4
3	IO_L56P_Y	Y1

Table 12: **BG432 — XCV300E, XCV400E, XCV600E**

Bank	Pin Description	Pin #
3	IO_L56N_Y	Y3
3	IO_L57P_Y	Y4
3	IO_L57N_Y	Y2
3	IO_L58P_YY	AA3
3	IO_D5_L58N_YY	AB1
3	IO_D6_L59P_YY	AB3
3	IO_VREF_L59N_YY	AB4
3	IO_L60P_Y	AD1
3	IO_VREF_L60N_Y	AC3[1]
3	IO_L61P_Y	AC4
3	IO_L61N_Y	AD2
3	IO_L62P_YY	AD3
3	IO_VREF_L62N_YY	AD4
3	IO_L63P_Y	AF2
3	IO_L63N_Y	AE3
3	IO_L64P	AE4
3	IO_L64N	AG1
3	IO_L65P_Y	AG2
3	IO_VREF_L65N_Y	AF3
3	IO_L66P_Y	AF4
3	IO_L66N_Y	AH1
3	IO_L67P	AH2
3	IO_L67N	AG3
3	IO_D7_L68P_YY	AG4
3	IO_INIT_L68N_YY	AJ2
3	IO	T2
4	GCK0	AL16
4	IO	AH10
4	IO	AJ11
4	IO	AK7
4	IO	AL12
4	IO	AL15
4	IO_L69P_YY	AJ4
4	IO_L69N_YY	AK3
4	IO_L70P_Y	AH5

Table 13: **BG432 Differential Pin Pair Summary XCV300E, XCV400E, XC600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
112	6	AB29	AB28	√	VREF
113	6	AA29	AB31	√	-
114	6	Y29	Y28	4	-
115	6	Y31	Y30	1	-
116	6	W30	W29	1	-
117	6	V29	V28	√	VREF
118	6	U29	V30	4	-
119	6	U30	U28	1	VREF
120	7	R29	T31	√	-
121	7	R31	R30	1	VREF
122	7	P28	P29	4	-
123	7	N30	P30	√	VREF
124	7	N31	N28	1	-
125	7	M28	M29	1	-
126	7	L30	M30	4	-
127	7	K30	K31	√	-
128	7	J30	K28	√	VREF
129	7	J28	J29	1	VREF
130	7	G30	H30	4	-
131	7	F31	H28	√	VREF
132	7	G28	G29	1	-
133	7	E30	E31	5	-
134	7	F28	F29	1	VREF
135	7	D30	D31	4	-
136	7	E28	E29	3	-

Notes:
1. AO in the XCV300E, 600E.
2. AO in the XCV300E.
3. AO in the XCV400E, 600E.
4. AO in the XCV300E, 400E.
5. AO in the XCV600E.

BG560 Ball Grid Array Packages

XCV1000E, XCV1600E, and XCV2000E devices in BG560 Ball Grid Array packages have footprint compatibility. Pins labeled I0_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 14, see Table 15 for Differential Pair information.

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
0	GCK3	A17	
0	IO	A27	
0	IO	B25	
0	IO	C28	
0	IO	C30	
0	IO	D30	
0	IO_L0N	E28	
0	IO_VREF_L0P	D29	3
0	IO_L1N_YY	D28	
0	IO_L1P_YY	A31	
0	IO_VREF_L2N_YY	E27	
0	IO_L2P_YY	C29	
0	IO_L3N_Y	B30	
0	IO_L3P_Y	D27	
0	IO_L4N_YY	E26	
0	IO_L4P_YY	B29	
0	IO_VREF_L5N_YY	D26	
0	IO_L5P_YY	C27	
0	IO_L6N_Y	E25	
0	IO_VREF_L6P_Y	A28	1
0	IO_L7N_Y	D25	
0	IO_L7P_Y	C26	
0	IO_VREF_L8N_Y	E24	4
0	IO_L8P_Y	B26	
0	IO_L9N_Y	C25	
0	IO_L9P_Y	D24	
0	IO_VREF_L10N_YY	E23	
0	IO_L10P_YY	A25	
0	IO_L11N_YY	D23	

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
NA	GND	A29	
NA	GND	A32	
NA	GND	A33	
NA	GND	B1	
NA	GND	B6	
NA	GND	B9	
NA	GND	B15	
NA	GND	B23	
NA	GND	B27	
NA	GND	B31	
NA	GND	C2	
NA	GND	E1	
NA	GND	F32	
NA	GND	G2	
NA	GND	G33	
NA	GND	J32	
NA	GND	K1	
NA	GND	L2	
NA	GND	M33	
NA	GND	P1	
NA	GND	P33	
NA	GND	R32	
NA	GND	T1	
NA	GND	V33	
NA	GND	W2	
NA	GND	Y1	
NA	GND	Y33	
NA	GND	AB1	
NA	GND	AC32	
NA	GND	AD33	
NA	GND	AE2	
NA	GND	AG1	
NA	GND	AG32	
NA	GND	AH2	
NA	GND	AJ33	

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
NA	GND	AL32	
NA	GND	AM3	
NA	GND	AM7	
NA	GND	AM11	
NA	GND	AM19	
NA	GND	AM25	
NA	GND	AM28	
NA	GND	AM33	
NA	GND	AN1	
NA	GND	AN2	
NA	GND	AN5	
NA	GND	AN10	
NA	GND	AN14	
NA	GND	AN16	
NA	GND	AN20	
NA	GND	AN22	
NA	GND	AN27	
NA	GND	AN33	

Notes:

1. V_{REF} or I/O option only in the XCV2000E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV1600E & 2000E; otherwise, I/O option only.
3. V_{REF} or I/O option only in the XCV1000E, 1600E, & 2000E; otherwise, I/O option only.
4. V_{REF} or I/O option only in the XCV600E, 1000E, 1600E, & 2000E; otherwise, I/O option only.

Table 15: **BG560 Differential Pin Pair Summary XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
171	7	J33	M29	√	-
172	7	K31	L30	√	VREF
173	7	H33	L29	4	-
174	7	H32	J31	18	VREF
175	7	H31	K29	14	-
176	7	G32	J30	20	VREF
177	7	G31	J29	√	VREF
178	7	E32	E33	15	-
179	7	F31	H29	14	-
180	7	E31	D32	15	VREF
181	7	C33	G29	14	-
182	7	D31	F30	14	VREF

Notes:
1. AO in the XCV1600E.
2. AO in the XCV2000E.
3. AO in the XCV1600E, 2000E.
4. AO in the XCV1000E, 1600E.
5. AO in the XCV1000E, 2000E.
6. AO in the XCV1000E.
7. AO in the XCV1000E, 1600E, 2000E.
8. AO in the XCV600E, 1600E.
9. AO in the XCV400E, 600E, 1600E.
10. AO in the XCV400E, 600E, 1000E, 2000E.
11. AO in the XCV400E, 600E, 1000E.
12. AO in the XCV400E, 1000E, 2000E.
13. AO in the XCV400E, 600E, 1000E, 1600E.
14. AO in the XCV400E, 1000E, 1600E.
15. AO in the XCV600E, 1000E, 2000E.
16. AO in the XCV600E, 2000E.
17. AO in the XCV400E, 600E, 1600E, 2000E.
18. AO in the XCV600E, 1000E, 1600E, 2000E.
19. AO in the XCV400E, 600E, 2000E.
20. AO in the XCV400E, 1000E.

FG256 Fine-Pitch Ball Grid Array Packages

XCV50E, XCV100E, XCV200E, and XCV300E devices in FG256 fine-pitch Ball Grid Array packages have footprint compatibility. Pins labeled I0_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 16, see Table 17 for Differential Pair information.

Table 16: **FG256 Package — XCV50E, XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
0	GCK3	B8
0	IO	B3
0	IO	E7
0	IO	D8
0	IO_L0N_Y	C5
0	IO_VREF_L0P_Y	A3[2]
0	IO_L1N_YY	D5
0	IO_L1P_YY	E6
0	IO_VREF_L2N_YY	B4
0	IO_L2P_YY	A4
0	IO_L3N_Y	D6
0	IO_L3P_Y	B5
0	IO_VREF_L4N_YY	C6[1]
0	IO_L4P_YY	A5
0	IO_L5N_YY	B6
0	IO_L5P_YY	C7
0	IO_L6N_Y	D7
0	IO_L6P_Y	C8
0	IO_VREF_L7N_Y	B7
0	IO_L7P_Y	A6
0	IO_LVDS_DLL_L8N	A7
1	GCK2	C9
1	IO	B10
1	IO_LVDS_DLL_L8P	A8
1	IO_L9N_Y	D9
1	IO_L9P_Y	A9
1	IO_L10N_Y	E10
1	IO_VREF_L10P_Y	B9

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
5	IO_L76N_Y	W11
5	IO_L77P_YY	V11
5	IO_VREF_L77N_YY	Y10
5	IO_L78P_YY	AB10
5	IO_L78N_YY	W10
5	IO_L79P_Y	V10
5	IO_L79N_Y	Y9
5	IO_L80P_Y	AB9
5	IO_L80N_Y	W9
5	IO_L81P_YY	V9
5	IO_L81N_YY	AA8
5	IO_L82P_YY	Y8
5	IO_VREF_L82N_YY	W8
5	IO_L83P_Y	W7
5	IO_L83N_Y	AA7
5	IO_L84P_Y	AB6
5	IO_L84N_Y	AA6
5	IO_L85P_YY	AB5
5	IO_VREF_L85N_YY	AA5
5	IO_L86P_YY	Y7
5	IO_L86N_YY	W6
5	IO_L87P_YY	AA4
5	IO_VREF_L87N_YY	Y6
5	IO_L88P_YY	V7
5	IO_L88N_YY	AB3
6	IO	M2[1]
6	IO	M5
6	IO	P4
6	IO	R3[1]
6	IO	T2
6	IO	T4
6	IO	U3[1]
6	IO	W2
6	IO	AA1[1]
6	IO_L89N_YY	W3
6	IO_L89P_YY	Y2

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
6	IO_L90N_YY	V4
6	IO_L90P_YY	V3
6	IO_VREF_L91N_YY	Y1
6	IO_L91P_YY	U4
6	IO_L92N_YY	V2
6	IO_L92P_YY	W1
6	IO_VREF_L93N_YY	T3
6	IO_L93P_YY	U2
6	IO_L94N_Y	T5
6	IO_L94P_Y	V1
6	IO_L95N_Y	R5
6	IO_L95P_Y	U1
6	IO_VREF_L96N_Y	R4
6	IO_L96P_Y	T1
6	IO_L97N_YY	R2
6	IO_L97P_YY	P3
6	IO_L98N_YY	P5
6	IO_L98P_YY	R1
6	IO_L99N_YY	P2
6	IO_L99P_YY	N5
6	IO_L100N_Y	P1
6	IO_L100P_Y	N4
6	IO_L101N	N3
6	IO_VREF_L101P	N2
6	IO_L102N_Y	N1
6	IO_L102P_Y	M4
6	IO_L103N_YY	M3
6	IO_L103P_YY	M6
6	IO	M1
7	IO	B1
7	IO	C2[1]
7	IO	D1[1]
7	IO	E4
7	IO	F4
7	IO	G2[1]
7	IO	G4

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
3	IO_L97N	AA2
3	IO_L98P_YY	AC5
3	IO_L98N_YY	AB1
3	IO_D4_L99P_YY	AD3
3	IO_VREF_L99N_YY	AC1
3	IO_L100P_Y	AD1
3	IO_L100N_Y	AD4
3	IO_L101P	AD2
3	IO_L101N	AE3
3	IO_L102P_YY	AE1
3	IO_L102N_YY	AE4
3	IO_L103P_Y	AE2
3	IO_VREF_L103N_Y	AF3[1]
3	IO_L104P	AF4
3	IO_L104N	AF1
3	IO_L105P	AG3
3	IO_L105N	AF2
3	IO_L106P_Y	AG4
3	IO_L106N_Y	AG1
3	IO_L107P_YY	AH3
3	IO_D5_L107N_YY	AG2
3	IO_D6_L108P_YY	AH1
3	IO_VREF_L108N_YY	AJ2
3	IO_L109P	AH2
3	IO_L109N	AJ3
3	IO_L110P_YY	AJ1
3	IO_L110N_YY	AJ4
3	IO_L111P_YY	AK1
3	IO_VREF_L111N_YY	AK3
3	IO_L112P	AK2
3	IO_L112N	AK4
3	IO_L113P	AL1
3	IO_VREF_L113N	AL2[3]
3	IO_L114P_YY	AM1
3	IO_L114N_YY	AL3
3	IO_L115P_YY	AM2
3	IO_VREF_L115N_YY	AL4
3	IO_L116P_Y	AM3
3	IO_L116N_Y	AN1
3	IO_L117P	AM4
3	IO_L117N	AP1
3	IO_L118P_YY	AN2
3	IO_L118N_YY	AP2
3	IO_L119P_Y	AN3
3	IO_VREF_L119N_Y	AR1
3	IO_L120P	AN4
3	IO_L120N	AT1
3	IO_L121P	AR2
3	IO_VREF_L121N	AP4[1]
3	IO_L122P_Y	AT2
3	IO_L122N_Y	AR3
3	IO_D7_L123P_YY	AR4
3	IO_INIT_L123N_YY	AU2
4	GCK0	AW19
4	IO	AV3
4	IO_L124P_YY	AU4
4	IO_L124N_YY	AV5
4	IO_L125P_Y	AT6
4	IO_L125N_Y	AV4
4	IO_VREF_L126P_Y	AU6[1]
4	IO_L126N_Y	AW4
4	IO_L127P_YY	AT7
4	IO_L127N_YY	AW5
4	IO_VREF_L128P_YY	AU7
4	IO_L128N_YY	AV6
4	IO_L129P_Y	AT8
4	IO_L129N_Y	AW6
4	IO_L130P_Y	AU8
4	IO_L130N_Y	AV7
4	IO_L131P_YY	AT9
4	IO_L131N_YY	AW7

FG680 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 23: **FG680 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
GCLK LVDS					
3	0	A20	C22	NA	IO_DLL_L29N
2	1	D21	A19	NA	IO_DLL_L29P
1	5	AU22	AT22	NA	IO_DLL_L155N
0	4	AW19	AT21	NA	IO_DLL_L155P
IO LVDS Total Pairs: 247, Asynchronous Output Pairs: 111					
0	0	A36	C35	5	-
1	0	B35	D34	5	VREF
2	0	A35	C34	√	-
3	0	B34	D33	√	VREF
4	0	A34	C33	3	-
5	0	B33	D32	3	-
6	0	D31	C32	√	-
7	0	C31	A33	√	VREF
8	0	B31	B32	5	-
9	0	D30	A32	5	VREF
10	0	C30	A31	√	-
11	0	D29	B30	√	VREF
12	0	C29	A30	2	-
13	0	B29	A29	2	-
14	0	A28	B28	√	VREF
15	0	B27	C28	√	-
16	0	A27	D27	5	-
17	0	B26	C27	5	-

Table 23: **FG680 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
18	0	C26	D26	√	-
19	0	D25	A26	√	VREF
20	0	C25	B25	3	-
21	0	D24	A25	3	-
22	0	B23	A24	√	-
23	0	A23	C24	√	VREF
24	0	B22	B24	5	-
25	0	A22	E23	5	-
26	0	B21	D23	√	-
27	0	A21	C23	√	VREF
28	0	B20	E22	2	-
29	1	A19	C22	NA	IO_LVDS_DLL
30	1	B19	C21	2	VREF
31	1	A18	C19	2	-
32	1	B18	D19	√	VREF
33	1	A17	C18	√	-
34	1	B17	D18	5	-
35	1	A16	E18	5	-
36	1	D17	C17	√	VREF
37	1	E17	B16	√	-
38	1	C16	A15	3	-
39	1	D16	B15	3	-
40	1	B14	A14	√	VREF
41	1	A13	C15	√	-
42	1	B13	D15	5	-
43	1	A12	C14	5	-
44	1	C13	D14	√	-
45	1	D13	B12	√	VREF
46	1	C12	A11	2	-
47	1	C11	B11	2	-
48	1	D11	A10	√	VREF
49	1	C10	B10	√	-
50	1	D10	A9	5	VREF
51	1	C9	B9	5	-

Table 23: **FG680 Differential Pin Pair Summary**
XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
188	6	AP39	AP38	4	-
189	6	AN38	AN36	6	VREF
190	6	AN39	AN37	√	-
191	6	AM38	AM36	4	-
192	6	AL36	AM37	6	-
193	6	AL37	AM39	√	VREF
194	6	AK36	AL38	√	-
195	6	AK37	AL39	7	VREF
196	6	AJ36	AK38	4	-
197	6	AJ37	AK39	√	VREF
198	6	AH37	AJ38	√	-
199	6	AH38	AJ39	4	-
200	6	AG38	AH39	√	VREF
201	6	AG39	AG36	√	-
202	6	AF39	AG37	6	-
203	6	AE38	AF36	4	-
204	6	AF38	AF37	4	-
205	6	AE36	AE39	6	VREF
206	6	AE37	AD38	√	-
207	6	AD36	AD39	4	-
208	6	AC39	AC38	6	-
209	6	AB38	AD37	√	VREF
210	6	AB39	AC35	√	-
211	6	AA38	AC36	7	-
212	6	AA39	AC37	4	-
213	6	Y38	AB35	√	VREF
214	6	Y39	AB36	√	-
215	6	AA36	AB37	4	VREF
216	7	W38	AA37	√	-
217	7	V39	W37	4	VREF
218	7	U39	W36	√	-
219	7	U38	V38	√	VREF
220	7	T39	V37	4	-
221	7	T38	V36	7	-

Table 23: **FG680 Differential Pin Pair Summary**
XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
222	7	R39	V35	√	-
223	7	U36	U37	√	VREF
224	7	U35	R38	6	-
225	7	T37	P39	4	-
226	7	T36	P38	√	-
227	7	N38	N39	6	VREF
228	7	M39	R37	4	-
229	7	M38	R36	4	-
230	7	L39	P37	6	-
231	7	N37	P36	√	-
232	7	N36	L38	√	VREF
233	7	M37	K39	4	-
234	7	L37	K38	√	-
235	7	L36	J39	√	VREF
236	7	K37	J38	4	-
237	7	K36	H39	√	VREF
238	7	J37	H38	√	-
239	7	G38	G39	√	VREF
240	7	F39	J36	6	-
241	7	F38	H37	4	-
242	7	E39	H36	√	-
243	7	E38	G37	6	VREF
244	7	D39	G36	4	-
245	7	F36	D38	4	VREF
246	7	E37	D37	6	-

Notes:
1. AO in the XCV1000E, 1600E, 2000E.
2. AO in the XCV600E, 1000E, 1600E.
3. AO in the XCV600E, 1000E.
4. AO in the XCV1000E, 1600E.
5. AO in the XCV1000E, 2000E.
6. AO in the XCV600E, 1000E, 2000E.
7. AO in the XCV1000E.
8. AO in the XCV2000E.

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
7	IO_L275N_YY	G3
7	IO_L275P_YY	E1
7	IO_L276N_YY	H6
7	IO_L276P_YY	E2
7	IO_L277N	E4
7	IO_VREF_L277P	K9
7	IO_L278N_YY	J8
7	IO_L278P_YY	F4
7	IO_L279N_Y	D1[3]
7	IO_L279P_Y	H7[4]
7	IO_L280N_YY	G6
7	IO_VREF_L280P_YY	C2[1]
7	IO_L281N	D2
7	IO_L281P	F5
7	IO_L282N_YY	D3[4]
7	IO_L282P_YY	K10[3]
2	CCLK	F26
3	DONE	AJ28
NA	DXN	AJ3
NA	DXP	AH4
NA	M0	AF4
NA	M1	AC7
NA	M2	AK3
NA	PROGRAM	AG28
NA	TCK	B3
NA	TDI	H22
2	TDO	D26
NA	TMS	C1
NA	VCCINT	L11
NA	VCCINT	L12
NA	VCCINT	L19
NA	VCCINT	L20
NA	VCCINT	M11
NA	VCCINT	M12
NA	VCCINT	M19

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
NA	VCCINT	M20
NA	VCCINT	N13
NA	VCCINT	N14
NA	VCCINT	N15
NA	VCCINT	N16
NA	VCCINT	N17
NA	VCCINT	N18
NA	VCCINT	P13
NA	VCCINT	P18
NA	VCCINT	R13
NA	VCCINT	R18
NA	VCCINT	T13
NA	VCCINT	T18
NA	VCCINT	U13
NA	VCCINT	U18
NA	VCCINT	V13
NA	VCCINT	V14
NA	VCCINT	V15
NA	VCCINT	V16
NA	VCCINT	V17
NA	VCCINT	V18
NA	VCCINT	W11
NA	VCCINT	W12
NA	VCCINT	W19
NA	VCCINT	W20
NA	VCCINT	Y11
NA	VCCINT	Y12
NA	VCCINT	Y19
NA	VCCINT	Y20
NA	VCCO_0	B6
NA	VCCO_0	M15
NA	VCCO_0	M14
NA	VCCO_0	L15
NA	VCCO_0	L14
NA	VCCO_0	H14
NA	VCCO_0	M13

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
32	0	B14	E14	3200 2600 2000 1600 1000	-
33	0	D14	G15	3200 2600 2000 1600 1000	VREF
34	0	D15	J16	3200 1600	-
35	0	B15	F15	3200 2000 1000	-
36	0	E15	A15	3200 2000 1000	-
37	0	A16	G16	3200 2600	-
38	0	J17	F16	3200 2600 2000 1600 1000	-
39	0	B16	C16	3200 2600 2000 1600 1000	VREF
40	0	A17	H17	2600 1600 1000	-
41	0	B17	G17	2600 1600 1000	VREF
42	1	J18	C17	None	IO_LVDS_DLL
43	1	C18	G18	2600 1600 1000	VREF
44	1	F18	H18	2600 1600 1000	-
45	1	A19	B19	3200 2600 2000 1600 1000	VREF
46	1	C19	K19	3200 2600 2000 1600 1000	-
47	1	E19	F19	3200 2600	-
48	1	J19	G19	3200 2000 1000	-
49	1	G20	A20	3200 2000 1000	-
50	1	F20	B20	3200 1600	-
51	1	E20	D20	3200 2600 2000 1600 1000	VREF

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
52	1	A21	H20	3200 2600 2000 1600 1000	-
53	1	J20	E21	3200	-
54	1	K20	D21	3200 2600 1000	-
55	1	H21	B21	3200 2600 1000	-
56	1	F21	G21	2000 1600	-
57	1	B22	A22	3200 2600 2000 1600 1000	VREF
58	1	C22	J21	3200 2600 2000 1600 1000	-
59	1	G22	D22	3200 2600 1000	-
60	1	A23	K21	3200 2000 1000	-
61	1	B23	F22	3200 2000 1000	-
62	1	H22	C23	3200 1600 1000	-
63	1	K22	D23	3200 2600 2000 1600 1000	-
64	1	J22	A24	3200 2600 2000 1600 1000	VREF
65	1	D24	H23	2600 1600 1000	-
66	1	E24	A25	2600 1600 1000	-
67	1	C25	A26	3200 2600 2000 1600 1000	VREF
68	1	B26	F24	3200 2600 2000 1600 1000	-
69	1	F25	K23	3200 2600	-
70	1	H24	C26	3200 2000 1000	VREF

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
311	7	P2	R8	2600 2000 1000	-
312	7	N1	R9	3200 2600 2000	-
313	7	R10	P4	3200 2600 1600 1000	-
314	7	N2	P8	3200 2600 2000 1600 1000	-
315	7	P7	P6	3200 2600 2000 1600	-
316	7	N4	M1	2600 2000 1000	VREF
317	7	N3	N6	3200 1600 1000	-
318	7	M2	P9	2600 1600	-
319	7	M3	N7	3200 2600 1600 1000	-
320	7	M4	P10	2000 1000	-
321	7	N8	L1	3200 2600 2000	-
322	7	N9	L2	3200 2600 2000 1600 1000	-
323	7	K1	M7	2000 1600 1000	VREF
324	7	L4	M8	3200 1600 1000	-
325	7	L5	J1	3200 2600 2000 1600 1000	-
326	7	K3	J2	3200 2600 2000 1600 1000	VREF
327	7	J3	L7	3200 2600 1600 1000	-
328	7	H2	M9	3200 2600 1600	-
329	7	K6	J4	2600 1000	VREF
330	7	G2	L8	3200 2600 2000 1600 1000	-

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
331	7	K7	H3	2000 1600	-
332	7	J5	G3	3200 2600 2000 1600 1000	VREF
333	7	H5	L9	2600 2000 1000	-
334	7	H4	J6	3200 2600 2000	-
335	7	K8	G4	3200 2600 1600 1000	-
336	7	F2	J7	3200 2600 2000 1600 1000	-
337	7	L10	F3	3200 2600 2000 1600	-
338	7	H6	E1	2600 2000 1000	VREF
339	7	E2	G5	3200 2600 1600 1000	-
340	7	D1	K9	2600 1600	-
341	7	J8	E3	3200 2600 1600 1000	VREF
342	7	D2	E4	2600 2000 1000	-
343	7	D3	F4	3200 2600 2000	-