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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	600
Number of Logic Elements/Cells	2700
Total RAM Bits	81920
Number of I/O	196
Number of Gates	128236
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	352-LBGA Exposed Pad, Metal
Supplier Device Package	352-MBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv100e-7bg352i

the internal storage elements to begin changing state in response to the logic and the user clock.

The relative timing of these events can be changed. In addition, the GTS, GSR, and GWE events can be made depen-

Readback

The configuration data stored in the Virtex-E configuration memory can be readback for verification. Along with the configuration data it is possible to readback the contents all flip-flops/latches, LUT RAMs, and block RAMs. This capa-

Design Considerations

This section contains more detailed design information on the following features.

- Delay-Locked Loop . . . see [page 19](#)
- BlockRAM . . . see [page 24](#)
- SelectI/O . . . see [page 31](#)

Using DLLs

The Virtex-E FPGA series provides up to eight fully digital dedicated on-chip Delay-Locked Loop (DLL) circuits which provide zero propagation delay, low clock skew between output clock signals distributed throughout the device, and advanced clock domain control. These dedicated DLLs can be used to implement several circuits which improve and simplify system level design.

Introduction

As FPGAs grow in size, quality on-chip clock distribution becomes increasingly important. Clock skew and clock delay impact device performance and the task of managing clock skew and clock delay with conventional clock trees becomes more difficult in large devices. The Virtex-E series of devices resolve this potential problem by providing up to eight fully digital dedicated on-chip DLL circuits, which provide zero propagation delay and low clock skew between output clock signals distributed throughout the device.

Each DLL can drive up to two global clock routing networks within the device. The global clock distribution network minimizes clock skews due to loading differences. By monitoring a sample of the DLL output clock, the DLL can compensate for the delay on the routing network, effectively eliminating the delay from the external input port to the individual clock loads within the device.

In addition to providing zero delay with respect to a user source clock, the DLL can provide multiple phases of the source clock. The DLL can also act as a clock doubler or it can divide the user source clock by up to 16.

Clock multiplication gives the designer a number of design alternatives. For instance, a 50 MHz source clock doubled by the DLL can drive an FPGA design operating at 100 MHz. This technique can simplify board design because the clock path on the board no longer distributes such a

dent on the DONE pins of multiple devices all going High, forcing the devices to start synchronously. The sequence can also be paused at any stage until lock has been achieved on any or all DLLs.

bility is used for real-time debugging. For more detailed information, see application note XAPP138 “Virtex FPGA Series Configuration and Readback”.

high-speed signal. A multiplied clock also provides designers the option of time-domain-multiplexing, using one circuit twice per clock cycle, consuming less area than two copies of the same circuit. Two DLLs in can be connected in series to increase the effective clock multiplication factor to four.

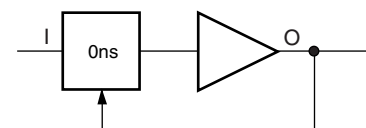
The DLL can also act as a clock mirror. By driving the DLL output off-chip and then back in again, the DLL can be used to deskew a board level clock between multiple devices.

In order to guarantee the system clock establishes prior to the device “waking up,” the DLL can delay the completion of the device configuration process until after the DLL achieves lock.

By taking advantage of the DLL to remove on-chip clock delay, the designer can greatly simplify and improve system level design involving high-fanout, high-performance clocks.

Library DLL Symbols

Figure 21 shows the simplified Xilinx library DLL macro symbol, BUFGDLL. This macro delivers a quick and efficient way to provide a system clock with zero propagation delay throughout the device. **Figure 22** and **Figure 23** show the two library DLL primitives. These symbols provide access to the complete set of DLL features when implementing more complex applications.



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Figure 21: Simplified DLL Macro Symbol BUFGDLL

Because any single DLL can access only two BUFGs at most, any additional output clock signals must be routed from the DLL in this example on the high speed backbone routing.

The dll_2x files in the [xapp132.zip](#) file show the VHDL and Verilog implementation of this circuit.

Virtex-E 4x Clock

Two DLLs located in the same half-edge (top-left, top-right, bottom-right, bottom-left) can be connected together, without using a BUFG between the CLKDLLs, to generate a 4x clock as shown in [Figure 30](#). Virtex-E devices, like the Virtex devices, have four clock networks that are available for internal deskewing of the clock. Each of the eight DLLs have access to two of the four clock networks. Although all the DLLs can be used for internal deskewing, the presence of two GCLKBUFs on the top and two on the bottom indicate that only two of the four DLLs on the top (and two of the four DLLs on the bottom) can be used for this purpose.

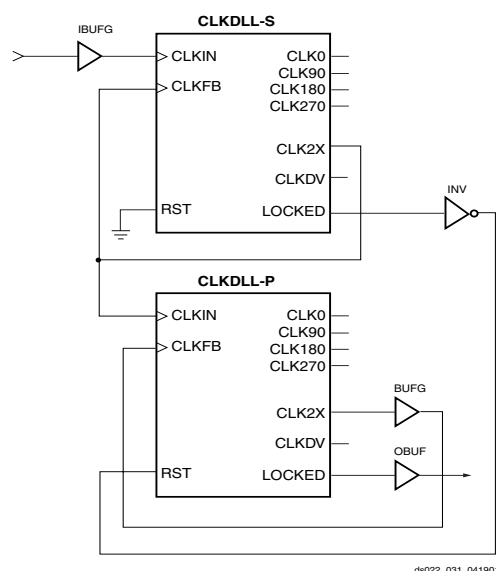


Figure 30: DLL Generation of 4x Clock in Virtex-E Devices

The dll_4xe files in the xapp132.zip file show the DLL implementation in Verilog for Virtex-E devices. These files can be found at:

<ftp://ftp.xilinx.com/pub/applications/xapp/xapp132.zip>

Using Block SelectRAM+ Features

The Virtex FPGA Series provides dedicated blocks of on-chip, true dual-read/write port synchronous RAM, with 4096 memory cells. Each port of the block SelectRAM+ memory can be independently configured as a read/write port, a read port, a write port, and can be configured to a specific data width. The block SelectRAM+ memory offers

new capabilities allowing the FPGA designer to simplify designs.

Operating Modes

Virtex-E block SelectRAM+ memory supports two operating modes:

- Read Through
- Write Back

Read Through (one clock edge)

The read address is registered on the read port clock edge and data appears on the output after the RAM access time. Some memories might place the latch/register at the outputs, depending on whether a faster clock-to-out versus set-up time is desired. This is generally considered to be an inferior solution, since it changes the read operation to an asynchronous function with the possibility of missing an address/control line transition during the generation of the read pulse clock.

Write Back (one clock edge)

The write address is registered on the write port clock edge and the data input is written to the memory and mirrored on the output.

Block SelectRAM+ Characteristics

- All inputs are registered with the port clock and have a set-up to clock timing specification.
- All outputs have a read through or write back function depending on the state of the port WE pin. The outputs relative to the port clock are available after the clock-to-out timing specification.
- The block SelectRAMs are true SRAM memories and do not have a combinatorial path from the address to the output. The LUT SelectRAM+ cells in the CLBs are still available with this function.
- The ports are completely independent from each other (*i.e.*, clocking, control, address, read/write function, and data width) without arbitration.
- A write operation requires only one clock edge.
- A read operation requires only one clock edge.

The output ports are latched with a self timed circuit to guarantee a glitch free read. The state of the output port does not change until the port executes another read or write operation.

Library Primitives

Figure 31 and Figure 32 show the two generic library block SelectRAM+ primitives. Table 14 describes all of the available primitives for synthesis and simulation.

Fundamentals

Modern bus applications, pioneered by the largest and most influential companies in the digital electronics industry, are commonly introduced with a new I/O standard tailored specifically to the needs of that application. The bus I/O standards provide specifications to other vendors who create products designed to interface with these applications. Each standard often has its own specifications for current, voltage, I/O buffering, and termination techniques.

The ability to provide the flexibility and time-to-market advantages of programmable logic is increasingly dependent on the capability of the programmable logic device to support an ever increasing variety of I/O standards

The SelectI/O resources feature highly configurable input and output buffers which provide support for a wide variety of I/O standards. As shown in [Table 18](#), each buffer type can support a variety of voltage requirements.

Table 18: Virtex-E Supported I/O Standards

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Board Termination Voltage (V_{TT})
LVTTL	3.3	3.3	N/A	N/A
LVC MOS2	2.5	2.5	N/A	N/A
LVC MOS18	1.8	1.8	N/A	N/A
SSTL3 I & II	3.3	N/A	1.50	1.50
SSTL2 I & II	2.5	N/A	1.25	1.25
GTL	N/A	N/A	0.80	1.20
GTL+	N/A	N/A	1.0	1.50
HSTL I	1.5	N/A	0.75	0.75
HSTL III & IV	1.5	N/A	0.90	1.50
CTT	3.3	N/A	1.50	1.50
AGP-2X	3.3	N/A	1.32	N/A
PCI33_3	3.3	3.3	N/A	N/A
PCI66_3	3.3	3.3	N/A	N/A
BLVDS & LVDS	2.5	N/A	N/A	N/A
LVPECL	3.3	N/A	N/A	N/A

Overview of Supported I/O Standards

This section provides a brief overview of the I/O standards supported by all Virtex-E devices.

While most I/O standards specify a range of allowed voltages, this document records typical voltage values only. Detailed information on each specification can be found on the Electronic Industry Alliance Jedec website at:

<http://www.jedec.org>

LVTTL — Low-Voltage TTL

The Low-Voltage TTL, or LVTTL standard is a general purpose EIA/JESDSA standard for 3.3V applications that uses an LVTTL input buffer and a Push-Pull output buffer. This standard requires a 3.3V output source voltage (V_{CCO}), but does not require the use of a reference voltage (V_{REF}) or a termination voltage (V_{TT}).

LVC MOS2 — Low-Voltage CMOS for 2.5 Volts

The Low-Voltage CMOS for 2.5 Volts or lower, or LVC MOS2 standard is an extension of the LVC MOS standard (JESD 8-5) used for general purpose 2.5V applications. This standard requires a 2.5V output source voltage (V_{CCO}), but does not require the use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}).

LVC MOS18 — 1.8 V Low Voltage CMOS

This standard is an extension of the LVC MOS standard. It is used in general purpose 1.8 V applications. The use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}) is not required.

PCI — Peripheral Component Interface

The Peripheral Component Interface, or PCI standard specifies support for both 33 MHz and 66 MHz PCI bus applications. It uses a LVTTL input buffer and a Push-Pull output buffer. This standard does not require the use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}), however, it does require a 3.3V output source voltage (V_{CCO}).

GTL — Gunning Transceiver Logic Terminated

The Gunning Transceiver Logic, or GTL standard is a high-speed bus standard (JESD8.3) invented by Xerox. Xilinx has implemented the terminated variation for this standard. This standard requires a differential amplifier input buffer and an Open Drain output buffer.

GTL+ — Gunning Transceiver Logic Plus

The Gunning Transceiver Logic Plus, or GTL+ standard is a high-speed bus standard (JESD8.3) first used by the Pentium Pro processor.

HSTL — High-Speed Transceiver Logic

The High-Speed Transceiver Logic, or HSTL standard is a general purpose high-speed, 1.5V bus standard sponsored by IBM (EIA/JESD 8-6). This standard has four variations or classes. SelectI/O devices support Class I, III, and IV. This

represents a combination of the LVTTTL IBUFG and BUFG symbols, such that the output of the BUFGP can connect directly to the clock pins throughout the design.

Unlike previous architectures, the Virtex-E BUFGP symbol can only be placed in a global clock pad location. The LOC property can specify a location for the BUFGP.

OBUF

An OBUF must drive outputs through an external output port. The generic output buffer (OBUF) symbol appears in [Figure 40](#).

The extension to the base name defines which I/O standard the OBUF uses. With no extension specified for the generic OBUF symbol, the assumed standard is slew rate limited LVTTTL with 12 mA drive strength.

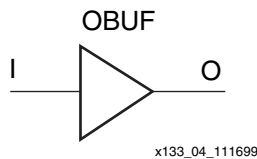


Figure 40: Virtex-E Output Buffer (OBUF) Symbol

The LVTTTL OBUF additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTTL output buffers have selectable drive strengths.

The format for LVTTTL OBUF symbol names is as follows:

OBUF_<slew_rate>_<drive_strength>

where <slew_rate> is either F (Fast) or S (Slow), and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

The following list details variations of the OBUF symbol.

- OBUF
- OBUF_S_2
- OBUF_S_4
- OBUF_S_6
- OBUF_S_8
- OBUF_S_12
- OBUF_S_16
- OBUF_S_24
- OBUF_F_2
- OBUF_F_4
- OBUF_F_6
- OBUF_F_8
- OBUF_F_12
- OBUF_F_16
- OBUF_F_24
- OBUF_LVCMOS2
- OBUF_PCI33_3

- OBUF_PCI66_3
- OBUF_GTL
- OBUF_GTLP
- OBUF_HSTL_I
- OBUF_HSTL_III
- OBUF_HSTL_IV
- OBUF_SSTL3_I
- OBUF_SSTL3_II
- OBUF_SSTL2_I
- OBUF_SSTL2_II
- OBUF_CTT
- OBUF_AGP
- OBUF_LVCMOS18
- OBUF_LVDS
- OBUF_LVPECL

The Virtex-E series supports eight banks for the HQ and PQ packages. The CS packages support four V_{CCO} banks.

OBUF placement restrictions require that within a given V_{CCO} bank each OBUF share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within any V_{CCO} bank. [Table 20](#) summarizes the Virtex-E output compatibility requirements. The LOC property can specify a location for the OBUF.

Table 20: Output Standards Compatibility Requirements

Rule 1	Only outputs with standards that share compatible V_{CCO} can be used within the same bank.
Rule 2	There are no placement restrictions for outputs with standards that do not require a V_{CCO} .
V_{CCO}	Compatible Standards
3.3	LVTTTL, SSTL3_I, SSTL3_II, CTT, AGP, GTL, GTL+, PCI33_3, PCI66_3
2.5	SSTL2_I, SSTL2_II, LVCMOS2, GTL, GTL+
1.5	HSTL_I, HSTL_III, HSTL_IV, GTL, GTL+

OBUFT

The generic 3-state output buffer OBUFT (see [Figure 41](#)) typically implements 3-state outputs or bidirectional I/O.

The extension to the base name defines which I/O standard OBUFT uses. With no extension specified for the generic OBUFT symbol, the assumed standard is slew rate limited LVTTTL with 12 mA drive strength.

The LVTTTL OBUFT additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

Table 21: Guidelines for Max Number of Simultaneously Switching Outputs per Power/Ground Pair (Continued)

Standard	Package		
	BGA, CS, FGA	HQ	PQ, TQ
HSTL Class I	18	13	9
HSTL Class III	9	7	5
HSTL Class IV	5	4	3
SSTL2 Class I	15	11	8
SSTL2 Class II	10	7	5
SSTL3 Class I	11	8	6
SSTL3 Class II	7	5	4
CTT	14	10	7
AGP	9	7	5

Note: This analysis assumes a 35 pF load for each output.

Table 22: Virtex-E Equivalent Power/Ground Pairs

Pkg/Part	XCV100E	XCV200E	XCV300E	XCV400E	XCV600E	XCV1000E	XCV1600E	XCV2000E
CS144	12	12						
PQ240	20	20	20	20				
HQ240					20	20		
BG352	20	32	32					
BG432			32	40	40			
BG560				40	40	56	58	60
FG256 ⁽¹⁾	20	24	24					
FG456		40	40					
FG676				54	56			
FG680 ⁽²⁾					46	56	56	56
FG860						58	60	64
FG900					56	58		60
FG1156						96	104	120

Notes:

1. Virtex-E devices in FG256 packages have more V_{CCO} than Virtex series devices.
2. FG680 numbers are preliminary.

Virtex-E Pin Definitions

Pin Name	Dedicated Pin	Direction	Description
GCK0, GCK1, GCK2, GCK3	Yes	Input	Clock input pins that connect to Global Clock Buffers.
M0, M1, M2	Yes	Input	Mode pins are used to specify the configuration mode.
CCLK	Yes	Input or Output	The configuration Clock I/O pin: it is an input for SelectMAP and slave-serial modes, and output in master-serial mode. After configuration, it is input only, logic level = Don't Care.
PROGRAM	Yes	Input	Initiates a configuration sequence when asserted Low.
DONE	Yes	Bidirectional	Indicates that configuration loading is complete, and that the start-up sequence is in progress. The output can be open drain.
INIT	No	Bidirectional (Open-drain)	When Low, indicates that the configuration memory is being cleared. The pin becomes a user I/O after configuration.
BUSY/DOUT	No	Output	In SelectMAP mode, BUSY controls the rate at which configuration data is loaded. The pin becomes a user I/O after configuration unless the SelectMAP port is retained. In bit-serial modes, DOUT provides preamble and configuration data to downstream devices in a daisy-chain. The pin becomes a user I/O after configuration.
D0/DIN, D1, D2, D3, D4, D5, D6, D7	No	Input or Output	In SelectMAP mode, D0-7 are configuration data pins. These pins become user I/Os after configuration unless the SelectMAP port is retained. In bit-serial modes, DIN is the single data input. This pin becomes a user I/O after configuration.
WRITE	No	Input	In SelectMAP mode, the active-low Write Enable signal. The pin becomes a user I/O after configuration unless the SelectMAP port is retained.
CS	No	Input	In SelectMAP mode, the active-low Chip Select signal. The pin becomes a user I/O after configuration unless the SelectMAP port is retained.
TDI, TDO, TMS, TCK	Yes	Mixed	Boundary-scan Test-Access-Port pins, as defined in IEEE1149.1.
DXN, DXP	Yes	N/A	Temperature-sensing diode pins. (Anode: DXP, cathode: DXN)
V _{CCINT}	Yes	Input	Power-supply pins for the internal core logic.
V _{CCO}	Yes	Input	Power-supply pins for the output drivers (subject to banking rules)
V _{REF}	No	Input	Input threshold voltage pins. Become user I/Os when an external threshold voltage is not needed (subject to banking rules).
GND	Yes	Input	Ground

Table 4: CS144 — XCV50E, XCV100E, XCV200E

Bank	Pin Description	Pin #
1	VCCO	A13
1	VCCO	D7
2	VCCO	B12
3	VCCO	G11
3	VCCO	M13
4	VCCO	N13
5	VCCO	N1
5	VCCO	N7
6	VCCO	M2
7	VCCO	B2
7	VCCO	G2
NA	GND	A1
NA	GND	B9
NA	GND	B11
NA	GND	C7
NA	GND	D5
NA	GND	E4
NA	GND	E11
NA	GND	F1
NA	GND	G10
NA	GND	J1
NA	GND	J12
NA	GND	L3
NA	GND	L5
NA	GND	L7
NA	GND	L9
NA	GND	N12

Notes:

1. V_{REF} or I/O option only in the XCV200E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV100E, 200E; otherwise, I/O option only.

CS144 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A $\checkmark$ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 5: CS144 Differential Pin Pair Summary
XCV50E, XCV100E, XCV200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	K7	N8	NA	IO_DLL_L18P
1	5	M7	M6	NA	IO_DLL_L18N
2	1	A7	B7	NA	IO_DLL_L2P
3	0	A6	C6	NA	IO_DLL_L2N
IO LVDS					
Total Pairs: 30, Asynchronous Output Pairs: 18					
0	0	A4	B4	$\checkmark$	VREF
1	0	A5	B5	$\checkmark$	-
2	1	B7	C6	NA	IO_LVDS_DLL
3	1	D8	C8	$\checkmark$	-
4	1	D9	C9	$\checkmark$	VREF
5	1	D10	C10	$\checkmark$	CS, WRITE
6	2	C11	C12	$\checkmark$	DIN, D0
7	2	D13	E10	1	D1, VREF
8	2	E12	E13	$\checkmark$	D2
9	2	F10	F11	1	D3, VREF
10	3	F13	G13	NA	-
11	3	H12	H11	1	D4, VREF
12	3	H10	J13	$\checkmark$	D5
13	3	J11	J10	1	D6, VREF
14	3	K10	L13	$\checkmark$	INIT
15	4	L11	M11	$\checkmark$	-
16	4	N10	K9	$\checkmark$	VREF
17	4	N9	K8	$\checkmark$	-

Table 6: PQ240 — XCV50E, XCV100E, XCV200E, XCV300E, XCV400E

Pin #	Pin Description	Bank
P173	IO_L16N_Y	2
P171	IO_VREF_L17P_Y	2
P170	IO_L17N_Y	2
P169	IO	2
P168 ¹	IO_VREF_L18P_Y	2
P167	IO_D1_L18N_Y	2
P163	IO_D2_L19P_YY	2
P162	IO_L19N_YY	2
P161	IO	2
P160	IO_L20P_Y	2
P159	IO_L20N_Y	2
P157	IO_VREF_L21P_Y	2
P156	IO_D3_L21N_Y	2
P155	IO_L22P_Y	2
P154 ³	IO_VREF_L22N_Y	2
P153	IO_L23P_YY	2
P152	IO_L23N_YY	2
P149	IO	3
P147 ³	IO_VREF	3
P145	IO_D4_L24P_Y	3
P144	IO_VREF_L24N_Y	3
P142	IO_L25P_Y	3
P141	IO_L25N_Y	3
P140	IO	3
P139	IO_L26P_YY	3
P138	IO_D5_L26N_YY	3
P134	IO_D6_L27P_Y	3
P133 ¹	IO_VREF_L27N_Y	3
P132	IO	3
P131	IO_L28P_Y	3
P130	IO_VREF_L28N_Y	3
P128	IO_L29P_Y	3
P127	IO_L29N_Y	3
P126 ²	IO_VREF_L30P_Y	3

Table 6: PQ240 — XCV50E, XCV100E, XCV200E, XCV300E, XCV400E

Pin #	Pin Description	Bank
P125	IO_L30N_Y	3
P124	IO_D7_L31P_YY	3
P123	IO_INIT_L31N_YY	3
P118	IO_L32P_YY	4
P117	IO_L32N_YY	4
P115 ²	IO_VREF	4
P114	IO_L33P_YY	4
P113	IO_L33N_YY	4
P111	IO_VREF_L34P_YY	4
P110	IO_L34N_YY	4
P109	IO	4
P108 ¹	IO_VREF_L35P_YY	4
P107	IO_L35N_YY	4
P103	IO_L36P_YY	4
P102	IO_L36N_YY	4
P101	IO	4
P100	IO_L37P_Y	4
P99	IO_L37N_Y	4
P97	IO_VREF_L38P_Y	4
P96	IO_L38N_Y	4
P95	IO_L39P_Y	4
P94 ³	IO_VREF_L39N_Y	4
P93	IO_LVDS_DLL_L40P	4
P92	GCK0	4
P89	GCK1	5
P87	IO_LVDS_DLL_L40N	5
P86 ³	IO_VREF	5
P84	IO_VREF_L41P_Y	5
P82	IO_L41N_Y	5
P81	IO	5
P80	IO	5
P79	IO_L42P_YY	5
P78	IO_L42N_YY	5

Table 6: PQ240 — XCV50E, XCV100E, XCV200E, XCV300E, XCV400E

Pin #	Pin Description	Bank
P74	IO_L43P_YY	5
P73 ¹	IO_VREF_L43N_YY	5
P72	IO	5
P71	IO_L44P_YY	5
P70	IO_VREF_L44N_YY	5
P68	IO_L45P_YY	5
P67	IO_L45N_YY	5
P66 ²	IO_VREF_L46P_Y	5
P65	IO_L46N_Y	5
P64	IO_L47P_YY	5
P63	IO_L47N_YY	5
P57	IO_L48N_YY	6
P56	IO_L48P_YY	6
P54 ²	IO_VREF	6
P53	IO_L49N_Y	6
P52	IO_L49P_Y	6
P50	IO_VREF_L50N_Y	6
P49	IO_L50P_Y	6
P48	IO	6
P47 ¹	IO_VREF_L51N_Y	6
P46	IO_L51P_Y	6
P42	IO_L52N_YY	6
P41	IO_L52P_YY	6
P40	IO	6
P39	IO_L53N_Y	6
P38	IO_L53P_Y	6
P36	IO_VREF_L54N_Y	6
P35	IO_L54P_Y	6
P34	IO_L55N_Y	6
P33 ³	IO_VREF_L55P_Y	6
P31	IO	6
P28	IO_L56N_YY	7
P27	IO_L56P_YY	7

Table 6: PQ240 — XCV50E, XCV100E, XCV200E, XCV300E, XCV400E

Pin #	Pin Description	Bank
P26 ³	IO_VREF	7
P24	IO_L57N_Y	7
P23	IO_VREF_L57P_Y	7
P21	IO_L58N_Y	7
P20	IO_L58P_Y	7
P19	IO	7
P18	IO_L59N_YY	7
P17	IO_L59P_YY	7
P13	IO_L60N_Y	7
P12 ¹	IO_VREF_L60P_Y	7
P11	IO	7
P10	IO_L61N_Y	7
P9	IO_VREF_L61P_Y	7
P7	IO_L62N_Y	7
P6	IO_L62P_Y	7
P5 ²	IO_VREF_L63N_Y	7
P4	IO_L63P_Y	7
P3	IO	7
P179	CCLK	2
P120	DONE	3
P60	M0	NA
P58	M1	NA
P62	M2	NA
P122	PROGRAM	NA
P183	TDI	NA
P239	TCK	NA
P181	TDO	2
P2	TMS	NA
P225	VCCINT	NA
P214	VCCINT	NA
P198	VCCINT	NA
P164	VCCINT	NA
P148	VCCINT	NA

Table 13: BG432 Differential Pin Pair Summary
XCV300E, XCV400E, XC600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
48	2	N1	P4	√	D3
49	2	P3	P2	4	-
50	2	R3	R4	1	VREF
51	2	R1	T3	√	-
52	3	U4	U2	1	VREF
53	3	U1	V3	4	-
54	3	V4	V2	√	VREF
55	3	W3	W4	1	-
56	3	Y1	Y3	1	-
57	3	Y4	Y2	4	-
58	3	AA3	AB1	√	D5
59	3	AB3	AB4	√	VREF
60	3	AD1	AC3	1	VREF
61	3	AC4	AD2	4	-
62	3	AD3	AD4	√	VREF
63	3	AF2	AE3	1	-
64	3	AE4	AG1	5	-
65	3	AG2	AF3	1	VREF
66	3	AF4	AH1	4	-
67	3	AH2	AG3	3	-
68	3	AG4	AJ2	√	INIT
69	4	AJ4	AK3	√	-
70	4	AH5	AK4	1	-
71	4	AJ5	AH6	√	-
72	4	AL4	AK5	√	VREF
73	4	AJ6	AH7	2	-
74	4	AL5	AK6	√	-
75	4	AJ7	AL6	√	VREF
76	4	AH9	AJ8	1	-
77	4	AK8	AJ9	1	VREF
78	4	AL8	AK9	√	VREF
79	4	AK10	AL10	√	-

Table 13: BG432 Differential Pin Pair Summary
XCV300E, XCV400E, XC600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
80	4	AH12	AK11	√	-
81	4	AJ12	AK12	√	-
82	4	AH13	AJ13	√	-
83	4	AL13	AK14	√	VREF
84	4	AH14	AJ14	1	-
85	4	AK15	AJ15	1	VREF
86	5	AH15	AL17	NA	IO_LVDS_DLL
87	5	AK17	AJ17	1	VREF
88	5	AH17	AK18	1	-
89	5	AL19	AJ18	√	VREF
90	5	AH18	AL20	√	-
91	5	AK20	AH19	√	-
92	5	AJ20	AK21	√	-
93	5	AJ21	AL22	√	-
94	5	AJ22	AK23	√	VREF
95	5	AH22	AL24	1	VREF
96	5	AK24	AH23	1	-
97	5	AK25	AJ25	√	VREF
98	5	AL26	AK26	√	-
99	5	AH25	AL27	2	-
100	5	AJ26	AK27	√	VREF
101	5	AH26	AL28	√	-
102	5	AJ27	AK28	1	-
103	6	AH30	AJ30	√	-
104	6	AH31	AG28	3	-
105	6	AG30	AG29	4	-
106	6	AG31	AF28	1	VREF
107	6	AF30	AF29	5	-
108	6	AF31	AE28	1	-
109	6	AD28	AE30	√	VREF
110	6	AD31	AD30	4	-
111	6	AC29	AC28	1	VREF

Table 19: FG456 Differential Pin Pair Summary
XCV200E, XCV300E

Pair	Bank	P Pin	N Pin	AO	Other Functions
88	5	V7	AB3	√	-
89	6	Y2	W3	√	-
90	6	V3	V4	√	-
91	6	U4	Y1	√	VREF
92	6	W1	V2	√	-
93	6	U2	T3	√	VREF
94	6	V1	T5	2	-
95	6	U1	R5	1	-
96	6	T1	R4	2	VREF
97	6	P3	R2	√	-
98	6	R1	P5	√	-
99	6	N5	P2	√	-
100	6	N4	P1	2	-
101	6	N2	N3	1	VREF
102	6	M4	N1	2	-
103	6	M6	M3	√	-
104	7	L4	L3	√	-
105	7	L1	L5	√	-
106	7	K2	L6	2	-
107	7	K3	K4	2	VREF
108	7	K5	K1	√	-
109	7	J2	J3	√	-
110	7	H1	J5	√	-
111	7	H3	H2	√	-
112	7	H4	G1	2	VREF
113	7	F2	F1	2	-
114	7	G3	H5	√	-
115	7	E2	E1	√	VREF
116	7	G5	F3	√	-
117	7	D2	E3	√	VREF
118	7	C1	F5	√	-

Notes:

1. AO in the XCV200E.
2. AO in the XCV300E.

FG676 Fine-Pitch Ball Grid Array Package

XCV400E and XCV600E devices in the FG676 fine-pitch Ball Grid Array package have footprint compatibility. Pins labeled IO_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF} it can be used as general I/O. Immediately following Table 20, see Table 21 for Differential Pair information.

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
0	GCK3	E13
0	IO	A6
0	IO	A9 ¹
0	IO	A10 ¹
0	IO	B3
0	IO	B4 ¹
0	IO	B12 ¹
0	IO	C6
0	IO	C8
0	IO	D5
0	IO	D13 ¹
0	IO	G13
0	IO_L0N_Y	C4
0	IO_L0P_Y	F7
0	IO_L1N_YY	G8
0	IO_L1P_YY	C5
0	IO_VREF_L2N_YY	D6
0	IO_L2P_YY	E7
0	IO_L3N	A4
0	IO_L3P	F8
0	IO_L4N	B5
0	IO_L4P	D7
0	IO_VREF_L5N_YY	E8
0	IO_L5P_YY	G9
0	IO_L6N_YY	A5
0	IO_L6P_YY	F9
0	IO_L7N_Y	D8
0	IO_L7P_Y	C7
0	IO_VREF_L8N_Y	B7 ²
0	IO_L8P_Y	E9

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
NA	GND	D20
NA	GND	D12
NA	GND	C39
NA	GND	C37
NA	GND	C3
NA	GND	C20
NA	GND	C1
NA	GND	B39
NA	GND	B38
NA	GND	B2
NA	GND	B1
NA	GND	AW39
NA	GND	AW38
NA	GND	AW37
NA	GND	AW3
NA	GND	AW2
NA	GND	AW1
NA	GND	AV39
NA	GND	AV38
NA	GND	AV2
NA	GND	AV1
NA	GND	AU39
NA	GND	AU37
NA	GND	AU3
NA	GND	AU20
NA	GND	AU1
NA	GND	AT4
NA	GND	AT36
NA	GND	AT28
NA	GND	AT20
NA	GND	AT12
NA	GND	AR5
NA	GND	AR35
NA	GND	AR28
NA	GND	AR21
NA	GND	AR20

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
NA	GND	AR19
NA	GND	AR12
NA	GND	AH5
NA	GND	AH4
NA	GND	AH36
NA	GND	AH35
NA	GND	AA5
NA	GND	AA35
NA	GND	A39
NA	GND	A38
NA	GND	A37
NA	GND	A3
NA	GND	A2
NA	GND	A1

Notes:

1. V_{REF} or I/O option only in the XCV1000E, 1600E, 2000E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV1600E, 2000E; otherwise, I/O option only.
3. V_{REF} or I/O option only in the XCV2000E; otherwise, I/O option only.

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
NA	GND	C42
NA	GND	C41
NA	GND	C40
NA	GND	C3
NA	GND	C2
NA	GND	C1
NA	GND	BB41
NA	GND	BB40
NA	GND	BB4
NA	GND	BB39
NA	GND	BB3
NA	GND	BB2
NA	GND	BA42
NA	GND	BA41
NA	GND	BA40
NA	GND	BA3
NA	GND	BA2
NA	GND	BA1
NA	GND	B42
NA	GND	B41
NA	GND	B40
NA	GND	B3
NA	GND	B2
NA	GND	B1
NA	GND	AY42
NA	GND	AY41
NA	GND	AY40
NA	GND	AY3
NA	GND	AY2
NA	GND	AY1
NA	GND	AW42
NA	GND	AW4
NA	GND	AW39
NA	GND	AW1
NA	GND	AV5
NA	GND	AV38
NA	GND	AV30

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
NA	GND	AV22
NA	GND	AV21
NA	GND	AV13
NA	GND	AU6
NA	GND	AU37
NA	GND	AU30
NA	GND	AU22
NA	GND	AU21
NA	GND	AU13
NA	GND	AK6
NA	GND	AK5
NA	GND	AK38
NA	GND	AK37
NA	GND	AB6
NA	GND	AB5
NA	GND	AB38
NA	GND	AB37
NA	GND	AA6
NA	GND	AA5
NA	GND	AA38
NA	GND	AA37
NA	GND	A41
NA	GND	A40
NA	GND	A4
NA	GND	A39
NA	GND	A3
NA	GND	A2

Notes:

1. V_{REF} or I/O option only in the XCV1600E, 2000E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV2000E; otherwise, I/O option only.

FG860 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A $\checkmark$ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 25: FG860 Differential Pin Pair Summary
XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
3	0	C22	A22	NA	IO_DLL_L34N
2	1	B22	D22	NA	IO_DLL_L34P
1	5	AY22	AW21	NA	IO_DLL_L176N
0	4	BA22	AW20	NA	IO_DLL_L176P
IO LVDS					
Total Pairs: 281, Asynchronous Output Pairs: 111					
0	0	D38	A38	2	-
1	0	E37	B37	1	-
2	0	C39	A37	1	VREF
3	0	C38	B36	1	-
4	0	B35	A36	$\checkmark$	-
5	0	D37	A35	$\checkmark$	VREF
6	0	A34	C37	5	-
7	0	B33	E36	5	-
8	0	C32	A33	$\checkmark$	-
9	0	B32	C36	$\checkmark$	VREF
10	0	D35	A32	1	-
11	0	C35	C31	1	VREF
12	0	A31	E34	$\checkmark$	-
13	0	C30	D34	$\checkmark$	VREF
14	0	E33	B30	2	-
15	0	D33	A30	2	-
16	0	B29	C33	$\checkmark$	VREF
17	0	A29	E32	$\checkmark$	-

Table 25: FG860 Differential Pin Pair Summary
XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
18	0	C28	D32	2	-
19	0	B28	E31	1	-
20	0	A28	D31	1	-
21	0	C27	D30	5	-
22	0	B27	E29	$\checkmark$	-
23	0	A27	D29	$\checkmark$	VREF
24	0	D28	C26	5	-
25	0	F27	B26	5	-
26	0	C25	E27	$\checkmark$	-
27	0	B25	D27	$\checkmark$	VREF
28	0	D26	A25	1	-
29	0	E25	A24	1	-
30	0	B24	D25	$\checkmark$	-
31	0	A23	E24	$\checkmark$	VREF
32	0	E23	C23	2	-
33	0	D23	B23	2	VREF
34	1	D22	A22	NA	IO_LVDS_DLL
35	1	B21	D21	2	VREF
36	1	A21	D20	2	-
37	1	D19	C20	$\checkmark$	VREF
38	1	E19	B20	$\checkmark$	-
39	1	A19	D18	1	-
40	1	C19	E18	1	-
41	1	E17	B19	$\checkmark$	VREF
42	1	D16	A18	$\checkmark$	-
43	1	B18	E16	5	-
44	1	A17	F16	5	-
45	1	E15	C17	$\checkmark$	VREF
46	1	D14	B17	$\checkmark$	-
47	1	E14	A16	5	-
48	1	D13	C16	1	-
49	1	D12	B16	1	-
50	1	E12	A15	2	-
51	1	C11	C15	$\checkmark$	-

Table 25: FG860 Differential Pin Pair Summary
XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
256	7	T38	T41	√	-
257	7	T42	R39	1	VREF
258	7	R38	R42	2	-
259	7	P39	R40	4	-
260	7	P38	R41	2	-
261	7	N39	P42	1	-
262	7	M39	P40	3	-
263	7	M38	P41	√	-
264	7	L39	N42	√	VREF
265	7	N41	L38	2	-
266	7	M42	K40	√	-
267	7	K38	M40	√	VREF
268	7	J40	M41	2	-
269	7	L40	J39	5	VREF
270	7	L41	J38	√	-
271	7	H39	K42	√	VREF
272	7	H38	K41	1	-
273	7	G40	J41	2	-
274	7	G39	H42	√	-
275	7	G42	G38	1	VREF
276	7	F40	G41	2	-
277	7	F41	F42	4	-
278	7	E42	F39	2	VREF
279	7	E41	E40	1	-
280	7	D41	E39	3	-

Notes:

1. AO in the XCV1000E, 2000E.
2. AO in the XCV1000E, 1600E.
3. AO in the XCV2000E.
4. AO in the XCV1600E.
5. AO in the XCV1000E.

FG900 Fine-Pitch Ball Grid Array Package

XCV600E, XCV1000E, and XCV1600E devices in the FG900 fine-pitch Ball Grid Array package have footprint compatibility. Pins labeled IO_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF} , it can be used as general I/O. Immediately following Table 26, see Table 27 for Differential Pair information.

Table 26: FG900 — XCV600E, XCV1000E, XCV1600E

Bank	Pin Description	Pin #
0	GCK3	C15
0	IO	A7 ⁴
0	IO	A13 ⁴
0	IO	C5 ⁴
0	IO	C6 ⁴
0	IO	C14 ⁴
0	IO	D8 ⁵
0	IO	D10
0	IO	D13 ⁴
0	IO	E6
0	IO	E9 ⁵
0	IO	E14 ⁵
0	IO	F9 ⁴
0	IO	F14 ⁵
0	IO	G15
0	IO	K11 ⁵
0	IO	K12
0	IO	L13 ⁴
0	IO_L0N_YY	C4 ⁴
0	IO_L0P_YY	F7 ³
0	IO_L1N_Y	D5
0	IO_L1P_Y	G8
0	IO_VREF_L2N_Y	A3 ¹
0	IO_L2P_Y	H9
0	IO_L3N_Y	B4 ⁴
0	IO_L3P_Y	J10 ⁴
0	IO_L4N_YY	A4
0	IO_L4P_YY	D6
0	IO_VREF_L5N_YY	E7
0	IO_L5P_YY	B5

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
1	IO_L66P_Y	E24
1	IO_L67N_YY	A26
1	IO_VREF_L67P_YY	C25
1	IO_L68N_YY	F24
1	IO_L68P_YY	B26
1	IO_L69N	K23 ⁵
1	IO_L69P	F25 ⁴
1	IO_L70N_Y	C26
1	IO_VREF_L70P_Y	H24 ²
1	IO_L71N_Y	G24
1	IO_L71P_Y	A27
1	IO_L72N	B27 ⁵
1	IO_L72P	G25 ⁴
1	IO_L73N_YY	E26
1	IO_VREF_L73P_YY	C27
1	IO_L74N_YY	J24
1	IO_L74P_YY	B28
1	IO_L75N	K24 ⁵
1	IO_L75P	H25 ⁴
1	IO_L76N_Y	D27
1	IO_L76P_Y	F26
1	IO_L77N_Y	G26
1	IO_L77P_Y	C28
1	IO_L78N_YY	E27 ⁵
1	IO_L78P_YY	J25 ⁴
1	IO_L79N_YY	A30
1	IO_VREF_L79P_YY	H26
1	IO_L80N_YY	G27
1	IO_L80P_YY	B29
1	IO_L81N_Y	F27
1	IO_L81P_Y	C29
1	IO_L82N_Y	E28
1	IO_VREF_L82P_Y	F28
1	IO_L83N_Y	L25

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
1	IO_L83P_Y	B30
1	IO_L84N	B31
1	IO_L84P	E29
1	IO_WRITE_L85N_YY	A31
1	IO_CS_L85P_YY	D30
2	IO	F31 ³
2	IO	J32
2	IO	K27 ³
2	IO	K31 ³
2	IO	L28 ³
2	IO	L30 ³
2	IO	M32 ³
2	IO	N26
2	IO	N28 ³
2	IO	P25 ³
2	IO	U26 ³
2	IO	U30
2	IO	U32 ³
2	IO	U34
2	IO_D2	M30
2	IO_DOUT_BUSY_L86P_YY	D32
2	IO_DIN_D0_L86N_YY	J27
2	IO_L87P_Y	E31
2	IO_L87N_Y	F30
2	IO_L88P_Y	G29
2	IO_L88N_Y	F32
2	IO_VREF_L89P_Y	E32
2	IO_L89N_Y	G30
2	IO_L90P	M25
2	IO_L90N	G31
2	IO_L91P_Y	L26
2	IO_L91N_Y	D33
2	IO_VREF_L92P_Y	D34

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
5	IO_L239P_Y	AP9
5	IO_L239N_Y	AK11
5	IO_L240P_YY	AL11
5	IO_VREF_L240N_YY	AL10
5	IO_L241P_YY	AE13
5	IO_L241N_YY	AM9
5	IO_L242P	AF12 ⁵
5	IO_L242N	AP8 ⁴
5	IO_L243P_Y	AL9
5	IO_VREF_L243N_Y	AH11 ²
5	IO_L244P_Y	AF11
5	IO_L244N_Y	AN8
5	IO_L245P_Y	AM8 ⁵
5	IO_L245N_Y	AG11 ⁴
5	IO_L246P_YY	AL8
5	IO_VREF_L246N_YY	AK9
5	IO_L247P_YY	AH10
5	IO_L247N_YY	AN7
5	IO_L248P	AE12 ⁵
5	IO_L248N	AJ9 ⁴
5	IO_L249P_Y	AM7
5	IO_L249N_Y	AL7
5	IO_L250P_Y	AG10
5	IO_L250N_Y	AN6
5	IO_L251P_YY	AK8 ⁵
5	IO_L251N_YY	AH9 ⁴
5	IO_L252P_YY	AP5
5	IO_VREF_L252N_YY	AJ8
5	IO_L253P_YY	AE11
5	IO_L253N_YY	AN5
5	IO_L254P_Y	AF10
5	IO_L254N_Y	AM6
5	IO_L255P_Y	AL6
5	IO_VREF_L255N_Y	AG9

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
5	IO_L256P_Y	AH8
5	IO_L256N_Y	AP4
5	IO_L257P_Y	AN4
5	IO_L257N_Y	AJ7
5	IO_L258P_YY	AM5
5	IO_L258N_YY	AK6
6	IO	T1
6	IO	V2
6	IO	V3
6	IO	V5 ³
6	IO	V8 ³
6	IO	AA10 ³
6	IO	AB5 ³
6	IO	AB7 ³
6	IO	AB9 ³
6	IO	AD7 ³
6	IO	AD8 ³
6	IO	AE2
6	IO	AE4
6	IO	AJ4 ³
6	IO	AH5 ³
6	IO_L259N_YY	AH6
6	IO_L259P_YY	AF8
6	IO_L260N_Y	AE9
6	IO_L260P_Y	AK3
6	IO_L261N_Y	AD10
6	IO_L261P_Y	AL2
6	IO_VREF_L262N_Y	AL1
6	IO_L262P_Y	AH4
6	IO_L263N	AG6
6	IO_L263P	AK1
6	IO_L264N_Y	AF7
6	IO_L264P_Y	AK2

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
NA	VCCO_2	T23
NA	VCCO_2	T24
NA	VCCO_2	R23
NA	VCCO_2	R24
NA	VCCO_2	P23
NA	VCCO_2	P24
NA	VCCO_2	P32
NA	VCCO_2	N23
NA	VCCO_3	V23
NA	VCCO_3	V24
NA	VCCO_3	Y23
NA	VCCO_3	Y24
NA	VCCO_3	W23
NA	VCCO_3	W24
NA	VCCO_3	AJ34
NA	VCCO_3	AE30
NA	VCCO_3	AC24
NA	VCCO_3	AB23
NA	VCCO_3	AB24
NA	VCCO_3	AA23
NA	VCCO_3	AA24
NA	VCCO_3	AA32
NA	VCCO_4	AD18
NA	VCCO_4	AC18
NA	VCCO_4	AC19
NA	VCCO_4	AC20
NA	VCCO_4	AC21
NA	VCCO_4	AC22
NA	VCCO_4	AP29
NA	VCCO_4	AM21
NA	VCCO_4	AK25
NA	VCCO_4	AD19
NA	VCCO_4	AD20
NA	VCCO_4	AD21

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
NA	VCCO_4	AD22
NA	VCCO_4	AD23
NA	VCCO_5	AC17
NA	VCCO_5	AD17
NA	VCCO_5	AC13
NA	VCCO_5	AC14
NA	VCCO_5	AC15
NA	VCCO_5	AC16
NA	VCCO_5	AP6
NA	VCCO_5	AM14
NA	VCCO_5	AK10
NA	VCCO_5	AD12
NA	VCCO_5	AD13
NA	VCCO_5	AD14
NA	VCCO_5	AD15
NA	VCCO_5	AD16
NA	VCCO_6	V11
NA	VCCO_6	V12
NA	VCCO_6	Y11
NA	VCCO_6	Y12
NA	VCCO_6	W11
NA	VCCO_6	W12
NA	VCCO_6	AJ1
NA	VCCO_6	AE5
NA	VCCO_6	AC11
NA	VCCO_6	AB11
NA	VCCO_6	AB12
NA	VCCO_6	AA3
NA	VCCO_6	AA11
NA	VCCO_6	AA12
NA	VCCO_7	U11
NA	VCCO_7	U12
NA	VCCO_7	N12
NA	VCCO_7	M11

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
111	2	M31	R26	2600 1600	-
112	2	N30	P28	3200 1600 1000	-
113	2	N29	N33	2600 2000 1000	VREF
114	2	T25	N34	3200 2600 2000 1600	-
115	2	P34	R27	3200 2600 2000 1600 1000	-
116	2	P29	P31	3200 2600 1600 1000	-
117	2	P33	T26	3200 2600 2000	-
118	2	R34	R28	2600 2000 1000	-
119	2	N31	N32	2000 1600 1000	D3
120	2	P30	R33	2000 1600	-
121	2	R29	T34	3200 2600 2000 1600 1000	-
122	2	R30	T30	1000	-
123	2	T28	R31	3200 1600	-
124	2	T29	U27	3200 2600 1600 1000	-
125	2	T31	T33	2000 1600 1000	VREF
126	2	U28	T32	2000 1600 1000	-
127	2	U29	U33	3200 2600 1600 1000	VREF
128	2	V33	U31	3200 2600 2000 1600 1000	-
129	3	V26	V30	3200 2600 1600 1000	VREF
130	3	W34	V28	2000 1600 1000	-
131	3	W32	W30	2000 1600 1000	VREF

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
132	3	V29	Y34	3200 2600 1600 1000	-
133	3	W29	Y33	3200 1600	-
134	3	W26	W28	1000	-
135	3	Y31	Y30	3200 2600 2000 1600 1000	-
136	3	AA34	W31	2000 1600	-
137	3	AA33	Y29	2000 1600 1000	VREF
138	3	W25	AB34	2600 2000 1000	-
139	3	Y28	AB33	3200 2600 2000	-
140	3	AA30	Y26	3200 2600 1600 1000	-
141	3	Y27	AA31	3200 2600 2000 1600 1000	-
142	3	AA27	AA29	3200 2600 2000 1600	-
143	3	AB32	AB29	2600 2000 1000	VREF
144	3	AA28	AC34	3200 1600 1000	-
145	3	Y25	AD34	2600 1600	-
146	3	AB30	AC33	3200 2600 1600 1000	-
147	3	AA26	AC32	2000 1000	-
148	3	AD33	AB28	3200 2600 2000	-
149	3	AE34	AB27	3200 2600 2000 1600 1000	D5
150	3	AE33	AC30	2000 1600 1000	VREF
151	3	AA25	AE32	3200 1600 1000	-
152	3	AE31	AD29	3200 2600 2000 1600 1000	-

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
231	5	AH14	AP12	3200 2600 2000 1600 1000	-
232	5	AJ14	AL14	3200 2600 1000	-
233	5	AF13	AN12	3200 2000 1000	-
234	5	AF14	AP11	3200 2000 1000	-
235	5	AN11	AH13	3200 1600 1000	-
236	5	AM12	AL12	3200 2600 2000 1600 1000	-
237	5	AJ13	AP10	3200 2600 2000 1600 1000	VREF
238	5	AK12	AM10	2600 1600 1000	-
239	5	AP9	AK11	2600 1600 1000	-
240	5	AL11	AL10	3200 2600 2000 1600 1000	VREF
241	5	AE13	AM9	3200 2600 2000 1600 1000	-
242	5	AF12	AP8	3200 2600	-
243	5	AL9	AH11	3200 2000 1000	VREF
244	5	AF11	AN8	3200 2000 1000	-
245	5	AM8	AG11	3200 1600	-
246	5	AL8	AK9	3200 2600 2000 1600 1000	VREF
247	5	AH10	AN7	3200 2600 2000 1600 1000	-
248	5	AE12	AJ9	3200 2600	-
249	5	AM7	AL7	3200 1000	-
250	5	AG10	AN6	3200 1000	-

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
251	5	AK8	AH9	2000 1600	-
252	5	AP5	AJ8	3200 2600 2000 1600 1000	VREF
253	5	AE11	AN5	3200 2600 2000 1600 1000	-
254	5	AF10	AM6	3200 2600 1000	-
255	5	AL6	AG9	3200 2000 1000	VREF
256	5	AH8	AP4	3200 2000 1000	-
257	5	AN4	AJ7	3200 1600 1000	-
258	5	AM5	AK6	3200 2600 2000 1600 1000	-
259	6	AF8	AH6	3200 2600 2000 1600 1000	-
260	6	AK3	AE9	3200 2600 2000	-
261	6	AL2	AD10	2600 2000 1000	-
262	6	AH4	AL1	3200 2600 1600 1000	VREF
263	6	AK1	AG6	2600 1600	-
264	6	AK2	AF7	3200 2600 1600 1000	-
265	6	AG5	AJ3	2600 2000 1000	VREF
266	6	AJ2	AD9	3200 2600 2000 1600	-
267	6	AH2	AC10	3200 2600 2000 1600 1000	-
268	6	AF5	AH3	3200 2600 1600 1000	-
269	6	AG3	AE8	3200 2600 2000	-