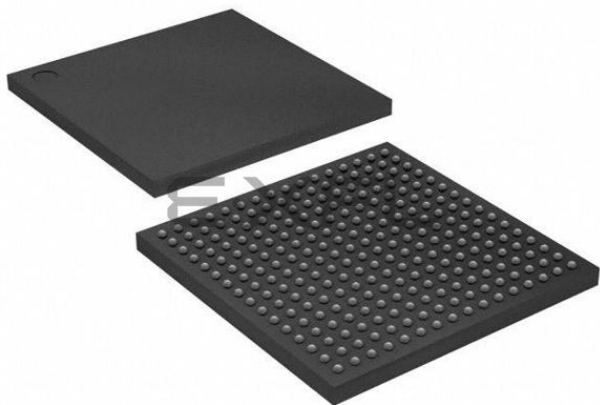




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	600
Number of Logic Elements/Cells	2700
Total RAM Bits	81920
Number of I/O	176
Number of Gates	128236
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv100e-7fg256c

the internal storage elements to begin changing state in response to the logic and the user clock.

The relative timing of these events can be changed. In addition, the GTS, GSR, and GWE events can be made depen-

Readback

The configuration data stored in the Virtex-E configuration memory can be readback for verification. Along with the configuration data it is possible to readback the contents all flip-flops/latches, LUT RAMs, and block RAMs. This capa-

Design Considerations

This section contains more detailed design information on the following features.

- Delay-Locked Loop . . . see [page 19](#)
- BlockRAM . . . see [page 24](#)
- SelectI/O . . . see [page 31](#)

Using DLLs

The Virtex-E FPGA series provides up to eight fully digital dedicated on-chip Delay-Locked Loop (DLL) circuits which provide zero propagation delay, low clock skew between output clock signals distributed throughout the device, and advanced clock domain control. These dedicated DLLs can be used to implement several circuits which improve and simplify system level design.

Introduction

As FPGAs grow in size, quality on-chip clock distribution becomes increasingly important. Clock skew and clock delay impact device performance and the task of managing clock skew and clock delay with conventional clock trees becomes more difficult in large devices. The Virtex-E series of devices resolve this potential problem by providing up to eight fully digital dedicated on-chip DLL circuits, which provide zero propagation delay and low clock skew between output clock signals distributed throughout the device.

Each DLL can drive up to two global clock routing networks within the device. The global clock distribution network minimizes clock skews due to loading differences. By monitoring a sample of the DLL output clock, the DLL can compensate for the delay on the routing network, effectively eliminating the delay from the external input port to the individual clock loads within the device.

In addition to providing zero delay with respect to a user source clock, the DLL can provide multiple phases of the source clock. The DLL can also act as a clock doubler or it can divide the user source clock by up to 16.

Clock multiplication gives the designer a number of design alternatives. For instance, a 50 MHz source clock doubled by the DLL can drive an FPGA design operating at 100 MHz. This technique can simplify board design because the clock path on the board no longer distributes such a

dent on the DONE pins of multiple devices all going High, forcing the devices to start synchronously. The sequence can also be paused at any stage until lock has been achieved on any or all DLLs.

bility is used for real-time debugging. For more detailed information, see application note XAPP138 "Virtex FPGA Series Configuration and Readback".

high-speed signal. A multiplied clock also provides designers the option of time-domain-multiplexing, using one circuit twice per clock cycle, consuming less area than two copies of the same circuit. Two DLLs in can be connected in series to increase the effective clock multiplication factor to four.

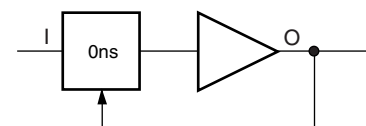
The DLL can also act as a clock mirror. By driving the DLL output off-chip and then back in again, the DLL can be used to deskew a board level clock between multiple devices.

In order to guarantee the system clock establishes prior to the device "waking up," the DLL can delay the completion of the device configuration process until after the DLL achieves lock.

By taking advantage of the DLL to remove on-chip clock delay, the designer can greatly simplify and improve system level design involving high-fanout, high-performance clocks.

Library DLL Symbols

Figure 21 shows the simplified Xilinx library DLL macro symbol, BUFGDLL. This macro delivers a quick and efficient way to provide a system clock with zero propagation delay throughout the device. **Figure 22** and **Figure 23** show the two library DLL primitives. These symbols provide access to the complete set of DLL features when implementing more complex applications.



ds022_25_121099

Figure 21: Simplified DLL Macro Symbol BUFGDLL

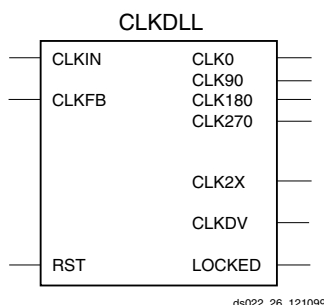


Figure 22: Standard DLL Symbol CLKDLL

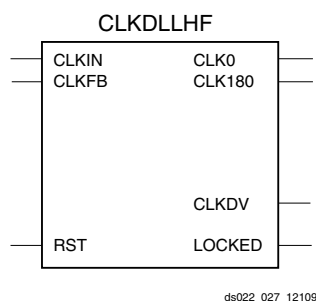


Figure 23: High Frequency DLL Symbol CLKDLLHF

BUFGDLL Pin Descriptions

Use the BUFGDLL macro as the simplest way to provide zero propagation delay for a high-fanout on-chip clock from an external input. This macro uses the IBUFG, CLKDLL and BUFG primitives to implement the most basic DLL application as shown in Figure 24.

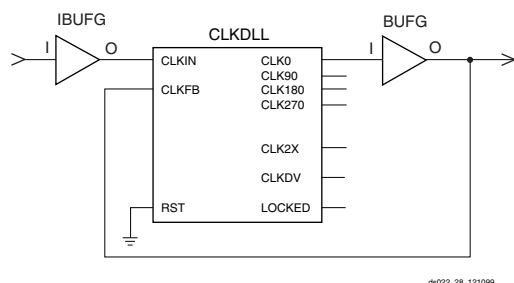


Figure 24: BUFGDLL Schematic

This symbol does not provide access to the advanced clock domain controls or to the clock multiplication or clock division features of the DLL. This symbol also does not provide access to the RST, or LOCKED pins of the DLL. For access to these features, a designer must use the library DLL primitives described in the following sections.

Source Clock Input — I

The I pin provides the user source clock, the clock signal on which the DLL operates, to the BUFGDLL. For the BUFGDLL macro the source clock frequency must fall in the low frequency range as specified in the data sheet. The BUF-

GDLL requires an external signal source clock. Therefore, only an external input port can source the signal that drives the BUFGDLL I pin.

Clock Output — O

The clock output pin O represents a delay-compensated version of the source clock (I) signal. This signal, sourced by a global clock buffer BUFG symbol, takes advantage of the dedicated global clock routing resources of the device.

The output clock has a 50-50 duty cycle unless you deactivate the duty cycle correction property.

CLKDLL Primitive Pin Descriptions

The library CLKDLL primitives provide access to the complete set of DLL features needed when implementing more complex applications with the DLL.

Source Clock Input — CLKIN

The CLKIN pin provides the user source clock (the clock signal on which the DLL operates) to the DLL. The CLKIN frequency must fall in the ranges specified in the data sheet. A global clock buffer (BUFG) driven from another CLKDLL, one of the global clock input buffers (IBUFG), or an IO_LVDS_DLL pin on the same edge of the device (top or bottom) must source this clock signal. There are four IO_LVDS_DLL input pins that can be used as inputs to the DLLs. This makes a total of eight usable input pins for DLLs in the Virtex-E family.

Feedback Clock Input — CLKFB

The DLL requires a reference or feedback signal to provide the delay-compensated output. Connect only the CLK0 or CLK2X DLL outputs to the feedback clock input (CLKFB) pin to provide the necessary feedback to the DLL. The feedback clock input can also be provided through one of the following pins.

IBUFG - Global Clock Input Pad

IO_LVDS_DLL - the pin adjacent to IBUFG

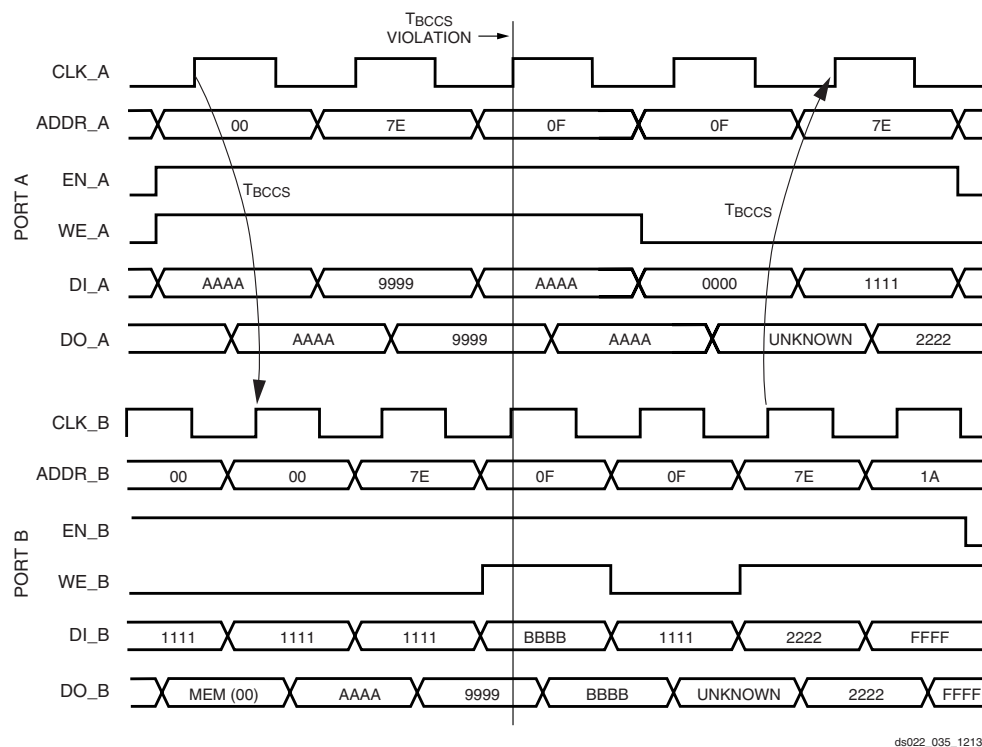
If an IBUFG sources the CLKFB pin, the following special rules apply.

1. An external input port must source the signal that drives the IBUFG I pin.
2. The CLK2X output must feedback to the device if both the CLK0 and CLK2X outputs are driving off chip devices.
3. That signal must directly drive only OBUFs and nothing else.

These rules enable the software determine which DLL clock output sources the CLKFB pin.

Reset Input — RST

When the reset pin RST activates the LOCKED signal deactivates within four source clock cycles. The RST pin, active High, must either connect to a dynamic signal or tied to



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Figure 34: Timing Diagram for a True Dual-port Read/Write Block SelectRAM+ Memory

At the third rising edge of CLKA, the T_{BCCS} parameter is violated with two writes to memory location 0x0F. The DOA and DOB buses reflect the contents of the DIA and DIB buses, but the stored value at 0x0F is invalid.

At the fourth rising edge of CLKA, a read operation is performed at memory location 0x0F and invalid data is present on the DOA bus. Port B also executes a read operation to memory location 0x0F and also reads invalid data.

At the fifth rising edge of CLKA a read operation is performed that does not violate the T_{BCCS} parameter to the previous write of 0x7E by Port B. The DOA bus reflects the recently written value by Port B.

Initialization

The block SelectRAM+ memory can initialize during the device configuration sequence. The 16 initialization properties of 64 hex values each (a total of 4096 bits) set the initialization of each RAM. These properties appear in Table 17. Any initialization properties not explicitly set configure as zeros. Partial initialization strings pad with zeros. Initialization strings greater than 64 hex values generate an error. The RAMs can be simulated with the initialization values using generics in VHDL simulators and parameters in Verilog simulators.

Initialization in VHDL and Synopsys

The block SelectRAM+ structures can be initialized in VHDL for both simulation and synthesis for inclusion in the EDIF output file. The simulation of the VHDL code uses a generic to pass the initialization. Synopsys FPGA compiler does not

presently support generics. The initialization values instead attach as attributes to the RAM by a built-in Synopsys `dc_script`. The `translate_off` statement stops synthesis translation of the generic statements. The following code illustrates a module that employs these techniques.

Table 17: RAM Initialization Properties

Property	Memory Cells
INIT_00	255 to 0
INIT_01	511 to 256
INIT_02	767 to 512
INIT_03	1023 to 768
INIT_04	1279 to 1024
INIT_05	1535 to 1280
INIT_06	1791 to 1536
INIT_07	2047 to 1792
INIT_08	2303 to 2048
INIT_09	2559 to 2304
INIT_0a	2815 to 2560
INIT_0b	3071 to 2816
INIT_0c	3327 to 3072
INIT_0d	3583 to 3328
INIT_0e	3839 to 3584
INIT_0f	4095 to 3840

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply. This is the time required to reach the nominal power supply voltage of the device¹ from 0V. The fastest ramp rate is 0V to nominal voltage in 2 ms, and the slowest allowed ramp rate is 0V to nominal voltage in 50 ms. For more details on power supply requirements, see XAPP158 on www.xilinx.com.

Product (Commercial Grade)	Description ⁽²⁾	Current Requirement ⁽³⁾
XCV50E - XCV600E	Minimum required current supply	500 mA
XCV812E - XCV2000E	Minimum required current supply	1 A
XCV2600E - XCV3200E	Minimum required current supply	1.2 A
Virtex-E Family, Industrial Grade	Minimum required current supply	2 A

Notes:

1. Ramp rate used for this specification is from 0 - 1.8 V DC. Peak current occurs on or near the internal power-on reset threshold and lasts for less than 3 ms.
2. Devices are guaranteed to initialize properly with the minimum current available from the power supply as noted above.
3. Larger currents might result if ramp rates are forced to be faster.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTL ⁽¹⁾	- 0.5	0.8	2.0	3.6	0.4	2.4	24	- 24
LVC MOS2	- 0.5	0.7	1.7	2.7	0.4	1.9	12	- 12
LVC MOS18	- 0.5	35% V_{CCO}	65% V_{CCO}	1.95	0.4	$V_{CCO} - 0.4$	8	- 8
PCI, 3.3 V	- 0.5	30% V_{CCO}	50% V_{CCO}	$V_{CCO} + 0.5$	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
GTL	- 0.5	$V_{REF} - 0.05$	$V_{REF} + 0.05$	3.6	0.4	n/a	40	n/a
GTL+	- 0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.6	n/a	36	n/a
HSTL I ⁽³⁾	- 0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	8	- 8
HSTL III	- 0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	24	- 8
HSTL IV	- 0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	48	- 8
SSTL3 I	- 0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.6$	$V_{REF} + 0.6$	8	- 8
SSTL3 II	- 0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.8$	$V_{REF} + 0.8$	16	- 16
SSTL2 I	- 0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.61$	$V_{REF} + 0.61$	7.6	- 7.6
SSTL2 II	- 0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.80$	$V_{REF} + 0.80$	15.2	- 15.2

IOB Output Switching Characteristics, Figure 1

Output delays terminating at a pad are specified for LVTTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 10.

		Speed Grade ⁽¹⁾				Units
Description ⁽²⁾	Symbol	Min	-8	-7	-6	
Propagation Delays						
O input to Pad	T _{ILOOP}	1.04	2.5	2.7	2.9	ns, max
O input to Pad via transparent latch	T _{IOOLP}	1.24	2.9	3.1	3.4	ns, max
3-State Delays						
T input to Pad high-impedance (Note 2)	T _{IOTHZ}	0.73	1.5	1.7	1.9	ns, max
T input to valid data on Pad	T _{IOTON}	1.13	2.7	2.9	3.1	ns, max
T input to Pad high-impedance via transparent latch (Note 2)	T _{IOTLPHZ}	0.86	1.8	2.0	2.2	ns, max
T input to valid data on Pad via transparent latch	T _{IOTLPON}	1.26	3.0	3.2	3.4	ns, max
GTS to Pad high impedance (Note 2)	T _{GTS}	1.94	4.1	4.6	4.9	ns, max
Sequential Delays						
Clock CLK						
Minimum Pulse Width, High	T _{CH}	0.56	1.2	1.3	1.4	ns, min
Minimum Pulse Width, Low	T _{CL}	0.56	1.2	1.3	1.4	ns, min
Clock CLK to Pad	T _{IOCKP}	0.97	2.4	2.8	2.9	ns, max
Clock CLK to Pad high-impedance (synchronous) (Note 2)	T _{IOCKHZ}	0.77	1.6	2.0	2.2	ns, max
Clock CLK to valid data on Pad (synchronous)	T _{IOCKON}	1.17	2.8	3.2	3.4	ns, max
Setup and Hold Times before/after Clock CLK						
O input	T _{IOOCK} / T _{IOCKO}	0.43 / 0	0.9 / 0	1.0 / 0	1.1 / 0	ns, min
OCE input	T _{IOOCECK} / T _{IOCKOCE}	0.28 / 0	0.55 / 0.01	0.7 / 0	0.7 / 0	ns, min
SR input (OFF)	T _{IOSRCKO} / T _{IOCKOSR}	0.40 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
3-State Setup Times, T input	T _{IOTCK} / T _{IOCKT}	0.26 / 0	0.51 / 0	0.6 / 0	0.7 / 0	ns, min
3-State Setup Times, TCE input	T _{IOTCECK} / T _{IOCKTCE}	0.30 / 0	0.6 / 0	0.7 / 0	0.8 / 0	ns, min
3-State Setup Times, SR input (TFF)	T _{IOSRCKT} / T _{IOCKTSR}	0.38 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
Set/Reset Delays						
SR input to Pad (asynchronous)	T _{IOSRP}	1.30	3.1	3.3	3.5	ns, max
SR input to Pad high-impedance (asynchronous) (Note 2)	T _{IOSRHZ}	1.08	2.2	2.4	2.7	ns, max
SR input to valid data on Pad (asynchronous)	T _{IOSRON}	1.48	3.4	3.7	3.9	ns, max
GSR to Pad	T _{IOGSRQ}	3.88	7.6	8.5	9.7	ns, max

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. 3-state turn-off delays should not be adjusted.

Virtex-E Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *with* DLL

Description ⁽¹⁾	Symbol	Device	Speed Grade ^(2, 3)				Units
			Min	-8	-7	-6	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, <i>with</i> DLL. For data <i>output</i> with different standards, adjust the delays with the values shown in IOB Output Switching Characteristics Standard Adjustments , page 10.	T _{ICKOFDLL}	XCV50E	1.0	3.1	3.1	3.1	ns
		XCV100E	1.0	3.1	3.1	3.1	ns
		XCV200E	1.0	3.1	3.1	3.1	ns
		XCV300E	1.0	3.1	3.1	3.1	ns
		XCV400E	1.0	3.1	3.1	3.1	ns
		XCV600E	1.0	3.1	3.1	3.1	ns
		XCV1000E	1.0	3.1	3.1	3.1	ns
		XCV1600E	1.0	3.1	3.1	3.1	ns
		XCV2000E	1.0	3.1	3.1	3.1	ns
		XCV2600E	1.0	3.1	3.1	3.1	ns
		XCV3200E	1.0	3.1	3.1	3.1	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For other I/O standards and different loads, see [Table 3](#) and [Table 4](#).
3. DLL output jitter is already included in the timing calculation.

Date	Version	Revision
07/23/01	2.2	- Under Absolute Maximum Ratings, changed (T_{SOL}) to 220 °C. - Changes made to SSTL symbol names in IOB Input Switching Characteristics Standard Adjustments table.
07/26/01	2.3	Removed T_{SOL} parameter and added footnote to Absolute Maximum Ratings table.
9/18/01	2.4	Reworded power supplies footnote to Absolute Maximum Ratings table.
10/25/01	2.5	- Updated the speed grade designations used in data sheets, and added Table 1, which shows the current speed grade designation for each device. - Added XCV2600E and XCV3200E values to DC Characteristics Over Recommended Operating Conditions and Power-On Power Supply Requirements tables.
11/09/01	2.6	Updated the Power-On Power Supply Requirements table.
02/01/02	2.7	Updated footnotes to the DC Input and Output Levels and DLL Clock Tolerance, Jitter, and Phase Information tables.
07/17/02	2.8	- Data sheet designation upgraded from Preliminary to Production. - Removed mention of MIL-M-38510/605 specification. - Added link to XAPP158 from the Power-On Power Supply Requirements section.
09/10/02	2.9	- Revised V_{IN} in Absolute Maximum Ratings table. - Added Clock CLK switching characteristics to Table 2, “IOB Input Switching Characteristics,” on page 6 and IOB Output Switching Characteristics, Figure 1.
12/22/02	2.9.1	- Added footnote regarding V_{IN} PCI compliance to Absolute Maximum Ratings table. - The fastest ramp rate is 0V to nominal voltage in 2 ms
03/14/03	2.9.2	Under Power-On Power Supply Requirements, the fastest ramp rate is no longer a "suggested" rate.

Virtex-E Data Sheet

The Virtex-E Data Sheet contains the following modules:

- DS022-1, Virtex-E 1.8V FPGAs:
[Introduction and Ordering Information \(Module 1\)](#)
- DS022-2, Virtex-E 1.8V FPGAs:
[Functional Description \(Module 2\)](#)
- DS022-3, Virtex-E 1.8V FPGAs:
DC and Switching Characteristics (Module 3)
- DS022-4, Virtex-E 1.8V FPGAs:
[Pinout Tables \(Module 4\)](#)

CS144 Chip-Scale Package

XCV50E, XCV100E, XCV200E, XCV300E and XCV400E devices in CS144 Chip-scale packages have footprint compatibility. In the CS144 package, bank pairs that share a side are internally interconnected, permitting four choices for V_{CCO} . See [Table 3](#).

Table 3: I/O Bank Pairs and Shared V_{CCO} Pins

Paired Banks	Shared V_{CCO} Pins
Banks 0 & 1	A2, A13, D7
Banks 2 & 3	B12, G11, M13
Banks 4 & 5	N1, N7, N13
Banks 6 & 7	B2, G2, M2

Pins labeled IO_VREF can be used as either in all parts unless device-dependent, as indicated in the footnotes. If the pin is not used as V_{REF} , it can be used as general I/O. Immediately following [Table 4](#), see [Table 5](#) is Differential Pair information.

Table 4: CS144 — XCV50E, XCV100E, XCV200E

Bank	Pin Description	Pin #
0	GCK3	A6
0	IO	B3
0	IO_VREF_L0N_YY	B4 ²
0	IO_L0P_YY	A4
0	IO_L1N_YY	B5
0	IO_L1P_YY	A5
0	IO_LVDS_DLL_L2N	C6
0	IO_VREF	A3 ¹
0	IO_VREF	C4
0	IO_VREF	D6
1	GCK2	A7
1	IO	A8
1	IO_LVDS_DLL_L2P	B7
1	IO_L3N_YY	C8
1	IO_L3P_YY	D8
1	IO_L4N_YY	C9
1	IO_VREF_L4P_YY	D9 ²
1	IO_WRITE_L5N_YY	C10
1	IO_CS_L5P_YY	D10

Table 4: CS144 — XCV50E, XCV100E, XCV200E

Bank	Pin Description	Pin #
1	IO_VREF	A10
1	IO_VREF	B8
1	IO_VREF	B10 ¹
2	IO	D12
2	IO	F12
2	IO_DOUT_BUSY_L6P_YY	C11
2	IO_DIN_D0_L6N_YY	C12
2	IO_D1_L7N	E10
2	IO_VREF_L7P	D13 ²
2	IO_L8N_YY	E13
2	IO_D2_L8P_YY	E12
2	IO_D3_L9N	F11
2	IO_VREF_L9P	F10
2	IO_L10P	F13
2	IO_VREF	C13 ¹
2	IO_VREF	D11
3	IO	H13
3	IO	K13
3	IO_L10N	G13
3	IO_VREF_L11N	H11
3	IO_D4_L11P	H12
3	IO_D5_L12N_YY	J13
3	IO_L12P_YY	H10
3	IO_VREF_L13N	J10 ²
3	IO_D6_L13P	J11
3	IO_INIT_L14N_YY	L13
3	IO_D7_L14P_YY	K10
3	IO_VREF	K11 ¹
3	IO_VREF	K12
4	GCK0	K7
4	IO	M8
4	IO	M10

BG352 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A check (✓) in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock

Table 11: BG352 Differential Pin Pair Summary
XCV100E, XCV200E, XCV300E

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	AE13	AC13	NA	IO LVDS 55
1	5	AF14	AD14	NA	IO LVDS 55
2	1	B14	A13	NA	IO LVDS 9
3	0	D14	A15	NA	IO LVDS 9
IO LVDS					
Total Outputs: 87, Asynchronous Output Pairs: 43					
0	0	B23	D21	✓	VREF_0
1	0	D20	A23	✓	-
2	0	B22	C21	✓	VREF_0
3	0	A21	B20	2	-
4	0	B19	C19	✓	VREF_0
5	0	C18	D17	✓	-
6	0	A18	C17	2	-
7	0	C16	B17	✓	-
8	0	D15	A16	✓	VREF_0
9	1	A13	A15	✓	GCLK LVDS 3/2
10	1	A12	C13	2	-
11	1	C12	B12	✓	VREF_1
12	1	B11	A11	✓	-
13	1	D11	C11	2	-
14	1	C10	B9	✓	-
15	1	C9	B8	✓	VREF_1
16	1	A7	D9	1	-
17	1	B6	A6	✓	VREF_1
18	1	A4	C7	✓	-

Table 11: BG352 Differential Pin Pair Summary
XCV100E, XCV200E, XCV300E

Pair	Bank	P Pin	N Pin	AO	Other Functions
19	1	D6	C6	✓	VREF_1
20	1	C4	D5	✓	CS
21	2	E4	D3	✓	DIN_D0
22	2	D2	C1	✓	VREF_2
23	2	G4	F3	✓	-
24	2	E2	F2	✓	VREF_2
25	2	F1	J4	2	-
26	2	H2	G1	✓	D1
27	2	J3	J2	✓	D2
28	2	J1	L4	1	-
29	2	L3	L2	✓	-
30	2	M4	M3	✓	D3
31	2	M2	M1	2	-
32	2	N4	N2	✓	-
33	3	R1	R2	2	-
34	3	R3	R4	✓	VREF_3
35	3	T2	U2	✓	-
36	3	T4	V1	1	-
37	3	U3	U4	✓	D5
38	3	V3	V4	✓	VREF_3
39	3	Y1	Y2	1	-
40	3	AA2	Y3	✓	VREF_3
41	3	AC1	AB2	✓	-
42	3	AA4	AC2	✓	VREF_3
43	3	AC3	AD2	✓	INIT
44	4	AC5	AD4	✓	-
45	4	AE4	AF3	✓	VREF_4
46	4	AC7	AD6	✓	-
47	4	AE5	AE6	✓	VREF_4
48	4	AF6	AC9	2	-
49	4	AE8	AF7	✓	VREF_4
50	4	AD9	AE9	✓	-
51	4	AF9	AC11	2	-
52	4	AD11	AE11	✓	-
53	4	AC12	AD12	✓	VREF_4
54	4	AE12	AF12	2	-

Table 15: BG560 Differential Pin Pair Summary
XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
47	2	F4	C1	14	-
48	2	G5	E3	15	VREF
49	2	D2	G4	16	-
50	2	H5	E2	15	-
51	2	H4	G3	√	VREF
52	2	J5	F1	17	VREF
53	2	J4	H3	14	-
54	2	K5	H2	18	VREF
55	2	J3	K4	19	-
56	2	L5	K3	√	D1
57	2	L4	K2	√	D2
58	2	M5	L3	17	-
59	2	L1	M4	14	-
60	2	N5	M2	15	VREF
61	2	N4	N3	16	-
62	2	N2	P5	15	-
63	2	P4	P3	√	D3
64	2	P2	R5	17	-
65	2	R4	R3	14	-
66	2	R1	T4	18	VREF
67	2	T5	T3	19	VREF
68	2	T2	U3	√	-
69	3	U1	U2	19	VREF
70	3	V2	V4	18	VREF
71	3	V5	V3	14	-
72	3	W1	W3	17	-
73	3	W4	W5	√	VREF
74	3	Y3	Y4	15	-
75	3	AA1	Y5	16	-
76	3	AA3	AA4	15	VREF
77	3	AB3	AA5	14	-

Table 15: BG560 Differential Pin Pair Summary
XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
78	3	AC1	AB4	17	-
79	3	AC3	AB5	√	D5
80	3	AC4	AD3	√	VREF
81	3	AE1	AC5	4	-
82	3	AD4	AF1	18	VREF
83	3	AF2	AD5	14	-
84	3	AG2	AE4	20	VREF
85	3	AH1	AE5	√	VREF
86	3	AF4	AJ1	15	-
87	3	AJ2	AF5	14	-
88	3	AG4	AK2	15	VREF
89	3	AJ3	AG5	14	-
90	3	AL1	AH4	14	VREF
91	3	AJ4	AH5	√	INIT
92	4	AL4	AJ6	√	-
93	4	AK5	AN3	8	VREF
94	4	AL5	AJ7	√	-
95	4	AM4	AM5	√	VREF
96	4	AK7	AL6	3	-
97	4	AM6	AN6	√	-
98	4	AL7	AJ9	√	VREF
99	4	AN7	AL8	9	VREF
100	4	AM8	AJ10	7	-
101	4	AL9	AM9	7	VREF
102	4	AK10	AN9	2	-
103	4	AL10	AM10	√	VREF
104	4	AL11	AJ12	√	-
105	4	AN11	AK12	8	-
106	4	AL12	AM12	√	-
107	4	AK13	AL13	√	VREF
108	4	AM13	AN13	3	-

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
1	IO	C5
1	IO_LVDS_DLL_L29P	A19
1	IO_L30N_Y	C21
1	IO_VREF_L30P_Y	B19 ²
1	IO_L31N_Y	C19
1	IO_L31P_Y	A18
1	IO_L32N_YY	D19
1	IO_VREF_L32P_YY	B18
1	IO_L33N_YY	C18
1	IO_L33P_YY	A17
1	IO_L34N_Y	D18
1	IO_L34P_Y	B17
1	IO_L35N_Y	E18
1	IO_L35P_Y	A16
1	IO_L36N_YY	C17
1	IO_VREF_L36P_YY	D17
1	IO_L37N_YY	B16
1	IO_L37P_YY	E17
1	IO_L38N_Y	A15
1	IO_L38P_Y	C16
1	IO_L39N_Y	B15
1	IO_L39P_Y	D16
1	IO_L40N_YY	A14
1	IO_VREF_L40P_YY	B14 ¹
1	IO_L41N_YY	C15
1	IO_L41P_YY	A13
1	IO_L42N_Y	D15
1	IO_L42P_Y	B13
1	IO_L43N_Y	C14
1	IO_L43P_Y	A12
1	IO_L44N_YY	D14
1	IO_L44P_YY	C13
1	IO_L45N_YY	B12
1	IO_VREF_L45P_YY	D13
1	IO_L46N_Y	A11
1	IO_L46P_Y	C12

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
1	IO_L47N_Y	B11
1	IO_L47P_Y	C11
1	IO_L48N_YY	A10
1	IO_VREF_L48P_YY	D11
1	IO_L49N_YY	B10
1	IO_L49P_YY	C10
1	IO_L50N_Y	A9
1	IO_VREF_L50P_Y	D10 ³
1	IO_L51N_Y	B9
1	IO_L51P_Y	C9
1	IO_L52N_YY	A8
1	IO_VREF_L52P_YY	B8
1	IO_L53N_YY	D9
1	IO_L53P_YY	A7
1	IO_L54N_Y	C8
1	IO_L54P_Y	B7
1	IO_L55N_Y	D8
1	IO_L55P_Y	A6
1	IO_L56N_YY	C7
1	IO_VREF_L56P_YY	B6
1	IO_L57N_YY	D7
1	IO_L57P_YY	A5
1	IO_L58N_Y	C6
1	IO_VREF_L58P_Y	B5 ¹
1	IO_L59N_Y	D6
1	IO_L59P_Y	A4
1	IO_WRITE_L60N_YY	B4
1	IO_CS_L60P_YY	D5
2	IO	D1
2	IO	F4
2	IO_DOUT_BUSY_L61P_YY	E3
2	IO_DIN_D0_L61N_YY	C2
2	IO_L62P_Y	D3
2	IO_L62N_Y	F3
2	IO_VREF_L63P	D2 ¹

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
6	IO_VREF_L200N_YY	AH39
6	IO_L200P_YY	AG38
6	IO_L201N_YY	AG36
6	IO_L201P_YY	AG39
6	IO_L202N_Y	AG37
6	IO_L202P_Y	AF39
6	IO_L203N	AF36
6	IO_L203P	AE38
6	IO_L204N	AF37
6	IO_L204P	AF38
6	IO_VREF_L205N_Y	AE39 ¹
6	IO_L205P_Y	AE36
6	IO_L206N_YY	AD38
6	IO_L206P_YY	AE37
6	IO_L207N	AD39
6	IO_L207P	AD36
6	IO_L208N_Y	AC38
6	IO_L208P_Y	AC39
6	IO_VREF_L209N_YY	AD37
6	IO_L209P_YY	AB38
6	IO_L210N_YY	AC35
6	IO_L210P_YY	AB39
6	IO_L211N	AC36
6	IO_L211P	AA38
6	IO_L212N	AC37
6	IO_L212P	AA39
6	IO_VREF_L213N_YY	AB35
6	IO_L213P_YY	Y38
6	IO_L214N_YY	AB36
6	IO_L214P_YY	Y39
6	IO_VREF_L215N	AB37 ²
6	IO_L215P	AA36
7	IO	C38
7	IO	B37
7	IO	F37

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
7	IO_L216N_YY	AA37
7	IO_L216P_YY	W38
7	IO_L217N	W37
7	IO_VREF_L217P	V39 ²
7	IO_L218N_YY	W36
7	IO_L218P_YY	U39
7	IO_L219N_YY	V38
7	IO_VREF_L219P_YY	U38
7	IO_L220N	V37
7	IO_L220P	T39
7	IO_L221N	V36
7	IO_L221P	T38
7	IO_L222N_YY	V35
7	IO_L222P_YY	R39
7	IO_L223N_YY	U37
7	IO_VREF_L223P_YY	U36
7	IO_L224N_Y	R38
7	IO_L224P_Y	U35
7	IO_L225N	P39
7	IO_L225P	T37
7	IO_L226N_YY	P38
7	IO_L226P_YY	T36
7	IO_L227N_Y	N39
7	IO_VREF_L227P_Y	N38 ¹
7	IO_L228N	R37
7	IO_L228P	M39
7	IO_L229N	R36
7	IO_L229P	M38
7	IO_L230N_Y	P37
7	IO_L230P_Y	L39
7	IO_L231N_YY	P36
7	IO_L231P_YY	N37
7	IO_L232N_YY	L38
7	IO_VREF_L232P_YY	N36
7	IO_L233N	K39
7	IO_L233P	M37

Table 25: FG860 Differential Pin Pair Summary
XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
188	5	AY27	AV28	√	-
189	5	BA27	AW29	5	-
190	5	BB28	AV29	1	-
191	5	AY28	AW30	1	-
192	5	BA28	AW31	2	-
193	5	BB29	AV31	√	-
194	5	AY29	AY32	√	VREF
195	5	AW32	BB30	2	-
196	5	AV32	AY30	2	-
197	5	BA30	AW33	√	VREF
198	5	BB31	AV33	√	-
199	5	AY34	BA31	1	VREF
200	5	AW34	BB32	1	-
201	5	BA32	AY35	√	VREF
202	5	BB33	AW35	√	-
203	5	AV35	BB34	5	-
204	5	AY36	BA34	5	-
205	5	BB35	AV36	√	VREF
206	5	BA35	AY37	√	-
207	5	BB36	BA36	5	-
208	5	AW37	BB37	1	VREF
209	5	BA37	AY38	1	-
210	5	BB38	AY39	2	-
211	6	AV42	AV41	√	-
212	6	AU41	AW40	3	-
213	6	AU42	AV39	1	-
214	6	AU38	AT41	2	VREF
215	6	AV40	AT42	4	-
216	6	AU39	AR41	2	-
217	6	AU40	AR42	1	VREF
218	6	AP42	AT38	√	-
219	6	AT39	AN41	2	-
220	6	AM40	AT40	1	-
221	6	AM41	AR38	√	VREF

Table 25: FG860 Differential Pin Pair Summary
XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
222	6	AR40	AM42	√	-
223	6	AP38	AL40	5	VREF
224	6	AL42	AP39	2	-
225	6	AK40	AP40	√	VREF
226	6	AN39	AK41	√	-
227	6	AN40	AK42	2	-
228	6	AJ41	AM38	√	VREF
229	6	AM39	AJ42	√	-
230	6	AH41	AH40	3	-
231	6	AH42	AL38	1	-
232	6	AG41	AL39	2	-
233	6	AG40	AK39	4	-
234	6	AG42	AJ38	2	-
235	6	AJ39	AF42	1	VREF
236	6	AH38	AF41	√	-
237	6	AH39	AE42	2	-
238	6	AE41	AG38	1	-
239	6	AD42	AG39	√	VREF
240	6	AF39	AD40	√	-
241	6	AE38	AD41	5	-
242	6	AC40	AE39	2	-
243	6	AC41	AD38	√	VREF
244	6	AC38	AB42	√	-
245	6	AC39	AB40	2	VREF
246	7	AB39	AA41	√	-
247	7	AA39	Y41	2	VREF
248	7	Y39	Y40	√	-
249	7	W41	Y38	√	VREF
250	7	W39	W40	2	-
251	7	V41	W38	5	-
252	7	V40	V39	√	-
253	7	U39	V42	√	VREF
254	7	U38	U41	1	-
255	7	T39	U42	2	-

Table 26: FG900 — XCV600E, XCV1000E, XCV1600E

Bank	Pin Description	Pin #
7	IO	E3
7	IO	F1 ⁴
7	IO	G1 ⁵
7	IO	G4 ⁵
7	IO	H3 ⁵
7	IO	J1 ⁴
7	IO	J3 ⁴
7	IO	J4 ⁴
7	IO	J6 ⁴
7	IO	L10 ⁴
7	IO	N2 ⁴
7	IO	N8 ⁴
7	IO	N10 ⁴
7	IO	P3 ⁵
7	IO	P9 ⁴
7	IO	R1 ⁵
7	IO	T3 ⁴
7	IO_L247P	R10
7	IO_L248N_YY	R5 ³
7	IO_L248P_YY	R6 ⁴
7	IO_L249N_YY	R8
7	IO_VREF_L249P_YY	R4 ²
7	IO_L250N_YY	R7
7	IO_L250P_YY	R3
7	IO_L251N_YY	P10
7	IO_VREF_L251P_YY	P6
7	IO_L252N_YY	P5
7	IO_L252P_YY	P2
7	IO_L253N	P7
7	IO_L253P	P4
7	IO_L254N_YY	N4
7	IO_L254P_YY	R2
7	IO_L255N_YY	N7
7	IO_VREF_L255P_YY	P1
7	IO_L256N	M6

Table 26: FG900 — XCV600E, XCV1000E, XCV1600E

Bank	Pin Description	Pin #
7	IO_L256P	N6
7	IO_L257N_YY	N5
7	IO_L257P_YY	N1
7	IO_L258N_YY	M4
7	IO_L258P_YY	M5
7	IO_L259N	M2
7	IO_VREF_L259P	M1 ¹
7	IO_L260N_YY	L4
7	IO_L260P_YY	L2
7	IO_L261N_Y	M7 ⁴
7	IO_L261P_Y	L5 ⁴
7	IO_L262N_YY	L1
7	IO_L262P_YY	M8
7	IO_L263N	K2
7	IO_L263P	M9
7	IO_L264N	L3 ⁴
7	IO_L264P	M10 ⁴
7	IO_L265N_YY	K5
7	IO_L265P_YY	K1
7	IO_L266N_YY	L6
7	IO_VREF_L266P_YY	K3
7	IO_L267N_YY	L7
7	IO_L267P_YY	K4
7	IO_L268N_YY	L8
7	IO_L268P_YY	J5
7	IO_L269N_YY	K6
7	IO_VREF_L269P_YY	H4
7	IO_L270N_YY	H1
7	IO_L270P_YY	K7
7	IO_L271N	J7
7	IO_L271P	J2
7	IO_L272N_YY	H5
7	IO_L272P_YY	G2
7	IO_L273N_YY	L9
7	IO_VREF_L273P_YY	G5
7	IO_L274N	F3
7	IO_L274P	K8

Table 27: FG900 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
256	7	N6	M6	1	-
257	7	N1	N5	4	-
258	7	M5	M4	√	-
259	7	M1	M2	1	VREF
260	7	L2	L4	4	-
261	7	L5	M7	3	-
262	7	M8	L1	4	-
263	7	M9	K2	1	-
264	7	M10	L3	NA	-
265	7	K1	K5	√	-
266	7	K3	L6	√	VREF
267	7	K4	L7	4	-
268	7	J5	L8	4	-
269	7	H4	K6	4	VREF
270	7	K7	H1	4	-
271	7	J2	J7	2	-
272	7	G2	H5	√	-
273	7	G5	L9	√	VREF
274	7	K8	F3	1	-
275	7	E1	G3	4	-
276	7	E2	H6	√	-
277	7	K9	E4	1	VREF
278	7	F4	J8	4	-
279	7	H7	D1	3	-
280	7	C2	G6	4	VREF
281	7	F5	D2	1	-
282	7	K10	D3	4	-

Notes:

1. AO in the XCV600E, 1000E.
2. AO in the XCV1000E.
3. AO in the XCV1600E.
4. AO in the XCV1000E, XCV1600E.

FG1156 Fine-Pitch Ball Grid Array Package

XCV1000E, XCV1600E, XCV2000E, XCV2600E, and XCV3200E devices in the FG1156 fine-pitch Ball Grid Array package have footprint compatibility. Pins labeled IO_VREF can be used as either V_{REF} or general I/O, unless indicated in the footnotes. If the pin is not used as V_{REF} , it can be used as general I/O. Immediately following Table 28, see Table 29 for Differential Pair information.

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
0	GCK3	E17
0	IO	B4
0	IO	B9
0	IO	B10
0	IO	D9 ³
0	IO	D16
0	IO	E7 ³
0	IO	E11 ³
0	IO	E13 ³
0	IO	E16 ³
0	IO	F17 ³
0	IO	J12 ³
0	IO	J13 ³
0	IO	J14 ³
0	IO	K11 ³
0	IO_L0N_Y	F7
0	IO_L0P_Y	H9
0	IO_L1N_Y	C5
0	IO_L1P_Y	J10
0	IO_VREF_L2N_Y	E6
0	IO_L2P_Y	D6
0	IO_L3N_Y	A4
0	IO_L3P_Y	G8
0	IO_L4N_YY	C6
0	IO_L4P_YY	J11
0	IO_VREF_L5N_YY	G9
0	IO_L5P_YY	F8
0	IO_L6N_YY	A5 ⁴

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
4	IO_L178N_YY	AL28
4	IO_L179P_YY	AE24 ⁴
4	IO_L179N_YY	AN28 ⁵
4	IO_L180P_Y	AJ27
4	IO_L180N_Y	AH26
4	IO_L181P_Y	AG25
4	IO_L181N_Y	AK27
4	IO_L182P	AM28 ⁴
4	IO_L182N	AF24 ⁵
4	IO_L183P_YY	AJ26
4	IO_L183N_YY	AP27
4	IO_VREF_L184P_YY	AK26
4	IO_L184N_YY	AN27
4	IO_L185P	AE23 ⁴
4	IO_L185N	AM27 ⁵
4	IO_L186P_Y	AL26
4	IO_L186N_Y	AP26
4	IO_VREF_L187P_Y	AN26 ²
4	IO_L187N_Y	AJ25
4	IO_L188P	AG24 ⁴
4	IO_L188N	AP25 ⁵
4	IO_L189P_YY	AF23
4	IO_L189N_YY	AM26
4	IO_VREF_L190P_YY	AJ24
4	IO_L190N_YY	AN25
4	IO_L191P_Y	AE22
4	IO_L191N_Y	AM25
4	IO_L192P_Y	AK24
4	IO_L192N_Y	AH23
4	IO_VREF_L193P_YY	AF22
4	IO_L193N_YY	AP24
4	IO_L194P_YY	AL24
4	IO_L194N_YY	AK23
4	IO_L195P_Y	AG22

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
4	IO_L195N_Y	AN23
4	IO_L196P_Y	AP23
4	IO_L196N_Y	AM23
4	IO_L197P_Y	AH22
4	IO_L197N_Y	AP22
4	IO_L198P_Y	AL23
4	IO_L198N_Y	AF21
4	IO_L199P_YY	AL22
4	IO_L199N_YY	AJ22
4	IO_VREF_L200P_YY	AK22
4	IO_L200N_YY	AM22
4	IO_L201P_YY	AG21 ⁴
4	IO_L201N_YY	AJ21 ⁵
4	IO_L202P_Y	AP21
4	IO_L202N_Y	AE20
4	IO_L203P_Y	AH21
4	IO_L203N_Y	AL21
4	IO_L204P	AN21 ⁴
4	IO_L204N	AF20 ⁵
4	IO_L205P_YY	AK21
4	IO_L205N_YY	AP20
4	IO_VREF_L206P_YY	AE19
4	IO_L206N_YY	AN20
4	IO_L207P_Y	AG20 ⁴
4	IO_L207N_Y	AL20 ⁵
4	IO_L208P_Y	AH20
4	IO_L208N_Y	AK20
4	IO_L209P_Y	AN19
4	IO_L209N_Y	AJ20
4	IO_L210P	AF19 ⁴
4	IO_L210N	AP19 ⁵
4	IO_L211P_YY	AM19
4	IO_L211N_YY	AH19
4	IO_VREF_L212P_YY	AJ19

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
7	IO_L324P_Y	L4
7	IO_L325N_YY	J1
7	IO_L325P_YY	L5
7	IO_L326N_YY	J2
7	IO_VREF_L326P_YY	K3
7	IO_L327N_Y	L7
7	IO_L327P_Y	J3
7	IO_L328N_Y	M9 ⁵
7	IO_L328P_Y	H2 ⁴
7	IO_L329N_Y	J4
7	IO_VREF_L329P_Y	K6 ²
7	IO_L330N_YY	L8
7	IO_L330P_YY	G2
7	IO_L331N_YY	H3 ⁵
7	IO_L331P_YY	K7 ⁴
7	IO_L332N_YY	G3
7	IO_VREF_L332P_YY	J5
7	IO_L333N_Y	L9
7	IO_L333P_Y	H5
7	IO_L334N_Y	J6 ⁵
7	IO_L334P_Y	H4 ⁴
7	IO_L335N_Y	G4
7	IO_L335P_Y	K8
7	IO_L336N_YY	J7
7	IO_L336P_YY	F2
7	IO_L337N_YY	F3 ⁵
7	IO_L337P_YY	L10 ⁴
7	IO_L338N_Y	E1
7	IO_VREF_L338P_Y_Y	H6
7	IO_L339N_Y	G5
7	IO_L339P_Y	E2
7	IO_L340N	K9
7	IO_L340P	D1
7	IO_L341N_Y	E3

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
7	IO_VREF_L341P_Y	J8
7	IO_L342N_Y	E4
7	IO_L342P_Y	D2
7	IO_L343N_Y	F4
7	IO_L343P_Y	D3
2	CCLK	C31
3	DONE	AM31
NA	DXN	AJ5
NA	DXP	AL5
NA	M0	AK4
NA	M1	AG7
NA	M2	AL3
NA	PROGRAM	AG28
NA	TCK	D5
NA	TDI	C30
2	TDO	K26
NA	TMS	C4
NA	VCCINT	K10
NA	VCCINT	K17
NA	VCCINT	K18
NA	VCCINT	K25
NA	VCCINT	L11
NA	VCCINT	L24
NA	VCCINT	M12
NA	VCCINT	M23
NA	VCCINT	N13
NA	VCCINT	N14
NA	VCCINT	N15
NA	VCCINT	N16
NA	VCCINT	N19
NA	VCCINT	N20
NA	VCCINT	N21

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
153	3	AD31	AF33	3200 2600 2000 1600 1000	VREF
154	3	AC28	AF31	3200 2600 1600 1000	-
155	3	AC27	AF32	3200 2600 1600	-
156	3	AE29	AD28	2600 1000	VREF
157	3	AD30	AG32	3200 2600 2000 1600 1000	-
158	3	AC26	AH33	2000 1600	-
159	3	AD26	AF30	3200 2600 2000 1600 1000	VREF
160	3	AC25	AH32	2600 2000 1000	-
161	3	AE28	AL34	3200 2600 2000	-
162	3	AG30	AD27	3200 2600 1600 1000	-
163	3	AF29	AK34	3200 2600 2000 1600 1000	-
164	3	AD25	AE27	3200 2600 2000 1600	-
165	3	AJ33	AH31	2600 2000 1000	VREF
166	3	AE26	AL33	3200 2600 1600 1000	-
167	3	AF28	AL32	2600 1600	-
168	3	AJ31	AF27	3200 2600 1600 1000	VREF
169	3	AG29	AJ32	2600 2000 1000	-
170	3	AK33	AH30	3200 2600 2000	-
171	3	AK32	AK31	3200 2600 2000 1600 1000	INIT

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
172	4	AP31	AK29	3200 2600 2000 1600 1000	-
173	4	AP30	AN31	3200 1600 1000	-
174	4	AH27	AN30	3200 2000 1000	-
175	4	AM30	AK28	3200 2000 1000	VREF
176	4	AG26	AN29	3200 2600 1000	-
177	4	AF25	AM29	3200 2600 2000 1600 1000	-
178	4	AL29	AL28	3200 2600 2000 1600 1000	VREF
179	4	AE24	AN28	2000 1600	-
180	4	AJ27	AH26	3200 1000	-
181	4	AG25	AK27	3200 1000	-
182	4	AM28	AF24	3200 2600	-
183	4	AJ26	AP27	3200 2600 2000 1600 1000	-
184	4	AK26	AN27	3200 2600 2000 1600 1000	VREF
185	4	AE23	AM27	3200 1600	-
186	4	AL26	AP26	3200 2000 1000	-
187	4	AN26	AJ25	3200 2000 1000	VREF
188	4	AG24	AP25	3200 2600	-
189	4	AF23	AM26	3200 2600 2000 1600 1000	-
190	4	AJ24	AN25	3200 2600 2000 1600 1000	VREF
191	4	AE22	AM25	2600 1600 1000	-

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
192	4	AK24	AH23	2600 1600 1000	-
193	4	AF22	AP24	3200 2600 2000 1600 1000	VREF
194	4	AL24	AK23	3200 2600 2000 1600 1000	-
195	4	AG22	AN23	3200 1600 1000	-
196	4	AP23	AM23	3200 2000 1000	-
197	4	AH22	AP22	3200 2000 1000	-
198	4	AL23	AF21	3200 2600 1000	-
199	4	AL22	AJ22	3200 2600 2000 1600 1000	-
200	4	AK22	AM22	3200 2600 2000 1600 1000	VREF
201	4	AG21	AJ21	2000 1600	-
202	4	AP21	AE20	3200 2600 1000	-
203	4	AH21	AL21	3200 2600 1000	-
204	4	AN21	AF20	3200	-
205	4	AK21	AP20	3200 2600 2000 1600 1000	-
206	4	AE19	AN20	3200 2600 2000 1600 1000	VREF
207	4	AG20	AL20	3200 1600	-
208	4	AH20	AK20	3200 2000 1000	-
209	4	AN19	AJ20	3200 2000 1000	-
210	4	AF19	AP19	3200 2600	-

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
211	4	AM19	AH19	3200 2600 2000 1600 1000	-
212	4	AJ19	AP18	3200 2600 2000 1600 1000	VREF
213	4	AF18	AP17	2600 1600 1000	-
214	4	AJ18	AL18	2600 1600 1000	VREF
215	5	AM18	AL17	None	IO_LVDS_DLL
216	5	AH17	AM17	2600 1600 1000	VREF
217	5	AJ17	AG17	2600 1600 1000	-
218	5	AP16	AL16	3200 2600 2000 1600 1000	VREF
219	5	AJ16	AM16	3200 2600 2000 1600 1000	-
220	5	AK16	AP15	3200 2600	-
221	5	AL15	AH16	3200 2000 1000	-
222	5	AN15	AF16	3200 2000 1000	-
223	5	AP14	AE16	3200 1600	-
224	5	AK15	AJ15	3200 2600 2000 1600 1000	VREF
225	5	AH15	AN14	3200 2600 2000 1600 1000	-
226	5	AK14	AG15	3200	-
227	5	AM13	AF15	3200 2600 1000	-
228	5	AG14	AP13	3200 2600 1000	-
229	5	AE14	AE15	2000 1600	-
230	5	AN13	AG13	3200 2600 2000 1600 1000	VREF