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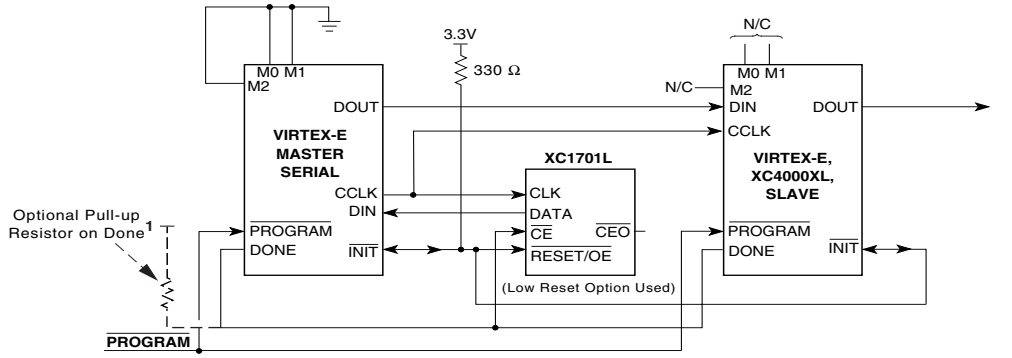
Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	600
Number of Logic Elements/Cells	2700
Total RAM Bits	81920
Number of I/O	158
Number of Gates	128236
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	240-BFQFP
Supplier Device Package	240-PQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv100e-7pq240c



Note 1: If none of the Virtex FPGAs have been selected to drive DONE, an external pull-up resistor of 330 Ω should be added to the common DONE line. (For Spartan-XL devices, add a 4.7K Ω pull-up resistor.) This pull-up is not needed if the DriveDONE attribute is set. If used, DriveDONE should be selected only for the last device in the configuration chain.

XCVE_ds_013_050103

Figure 13: **Master/Slave Serial Mode Circuit Diagram**

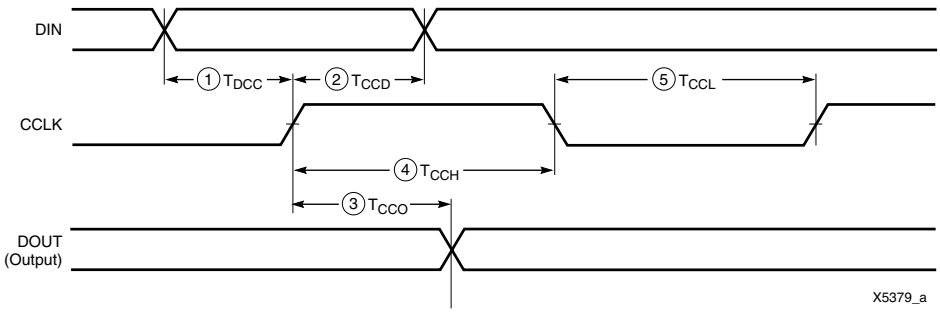


Figure 14: **Slave-Serial Mode Programming Switching Characteristics**

Master-Serial Mode

In master-serial mode, the CCLK output of the FPGA drives a Xilinx Serial PROM that feeds bit-serial data to the DIN input. The FPGA accepts this data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge. The maximum capacity for a single LOUT/DOUT write is 2^{20}-1 (1,048,575) 32-bit words, or 33,554,4000 bits.

The interface is identical to slave-serial except that an internal oscillator is used to generate the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK, which always starts at a slow default frequency. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration. Switching to a lower frequency is prohibited.

The CCLK frequency is set using the ConfigRate option in the bitstream generation software. The maximum CCLK frequency that can be selected is 60 MHz. When selecting a CCLK frequency, ensure that the serial PROM and any daisy-chained FPGAs are fast enough to support the clock rate.

On power-up, the CCLK frequency is approximately 2.5 MHz. This frequency is used until the ConfigRate bits have been loaded when the frequency changes to the selected ConfigRate. Unless a different frequency is specified in the design, the default ConfigRate is 4 MHz.

In a full master/slave system (Figure 13), the left-most device operates in master-serial mode. The remaining devices operate in slave-serial mode. The SPROM $\overline{\text{RESET}}$ pin is driven by $\overline{\text{INIT}}$, and the $\overline{\text{CE}}$ input is driven by DONE. There is the potential for contention on the DONE pin, depending on the start-up sequence options chosen.

The sequence of operations necessary to configure a Virtex-E FPGA serially appears in Figure 15.

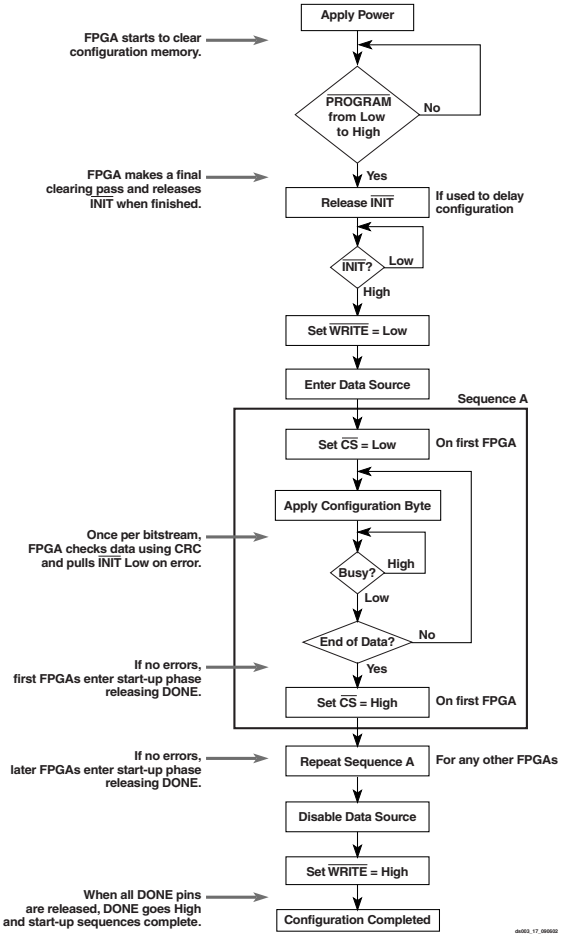


Figure 18: **SelectMAP Flowchart for Write Operations**

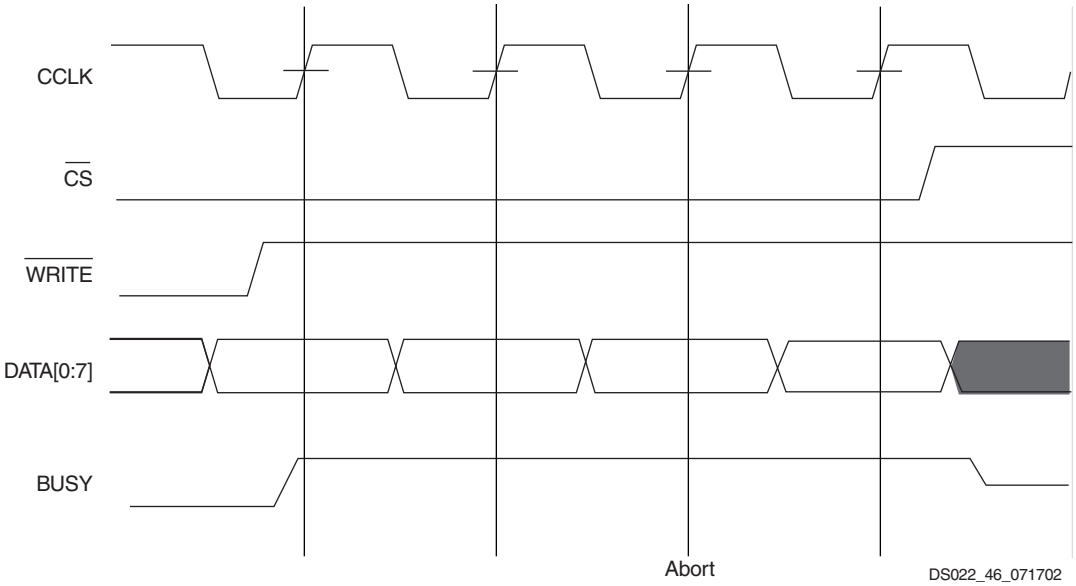


Figure 19: **SelectMAP Write Abort Waveforms**

Boundary Scan Mode

In the Boundary Scan mode, configuration is done through the IEEE 1149.1 Test Access Port. Note that the PROGRAM pin must be pulled High prior to reconfiguration. A Low on the PROGRAM pin resets the TAP controller and no JTAG operations can be performed.

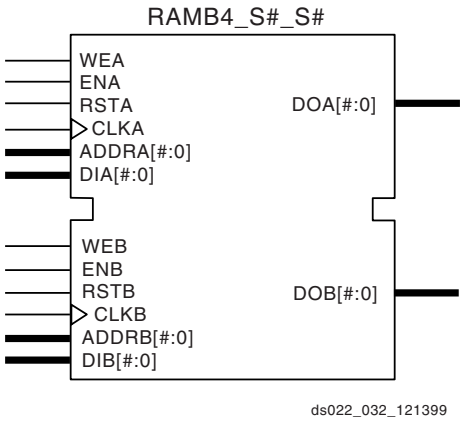


Figure 31: **Dual-Port Block SelectRAM+ Memory**

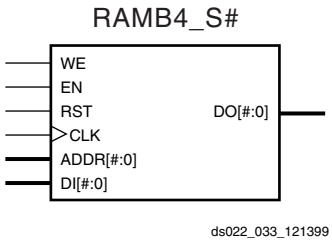


Figure 32: **Single-Port Block SelectRAM+ Memory**

Table 14: **Available Library Primitives**

Primitive	Port A Width	Port B Width
RAMB4_S1	1	N/A
RAMB4_S1_S1		1
RAMB4_S1_S2		2
RAMB4_S1_S4		4
RAMB4_S1_S8		8
RAMB4_S1_S16		16
RAMB4_S2	2	N/A
RAMB4_S2_S2		2
RAMB4_S2_S4		4
RAMB4_S2_S8		8
RAMB4_S2_S16		16
RAMB4_S4	4	N/A
RAMB4_S4_S4		4
RAMB4_S4_S8		8
RAMB4_S4_S16		16
RAMB4_S8	8	N/A
RAMB4_S8_S8		8
RAMB4_S8_S16		16
RAMB4_S16	16	N/A
RAMB4_S16_S16		16

Port Signals

Each block SelectRAM+ port operates independently of the others while accessing the same set of 4096 memory cells.

Table 15 describes the depth and width aspect ratios for the block SelectRAM+ memory.

Table 15: **Block SelectRAM+ Port Aspect Ratios**

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

Clock—CLK[A|B]

Each port is fully synchronous with independent clock pins. All port input pins have setup time referenced to the port CLK pin. The data output bus has a clock-to-out time referenced to the CLK pin.

Enable—EN[A|B]

The enable pin affects the read, write and reset functionality of the port. Ports with an inactive enable pin keep the output pins in the previous state and do not write data to the memory cells.

Write Enable—WE[A|B]

Activating the write enable pin allows the port to write to the memory cells. When active, the contents of the data input bus are written to the RAM at the address pointed to by the address bus, and the new data also reflects on the data out bus. When inactive, a read operation occurs and the contents of the memory cells referenced by the address bus reflect on the data out bus.

Reset—RST[A|B]

The reset pin forces the data output bus latches to zero synchronously. This does not affect the memory cells of the RAM and does not disturb a write operation on the other port.

Address Bus—ADDR[A|B]<#:0>

The address bus selects the memory cells for read or write. The width of the port determines the required width of this bus as shown in Table 15.

Data In Bus—DI[A|B]<#:0>

The data in bus provides the new data value to be written into the RAM. This bus and the port have the same width, as shown in Table 15.

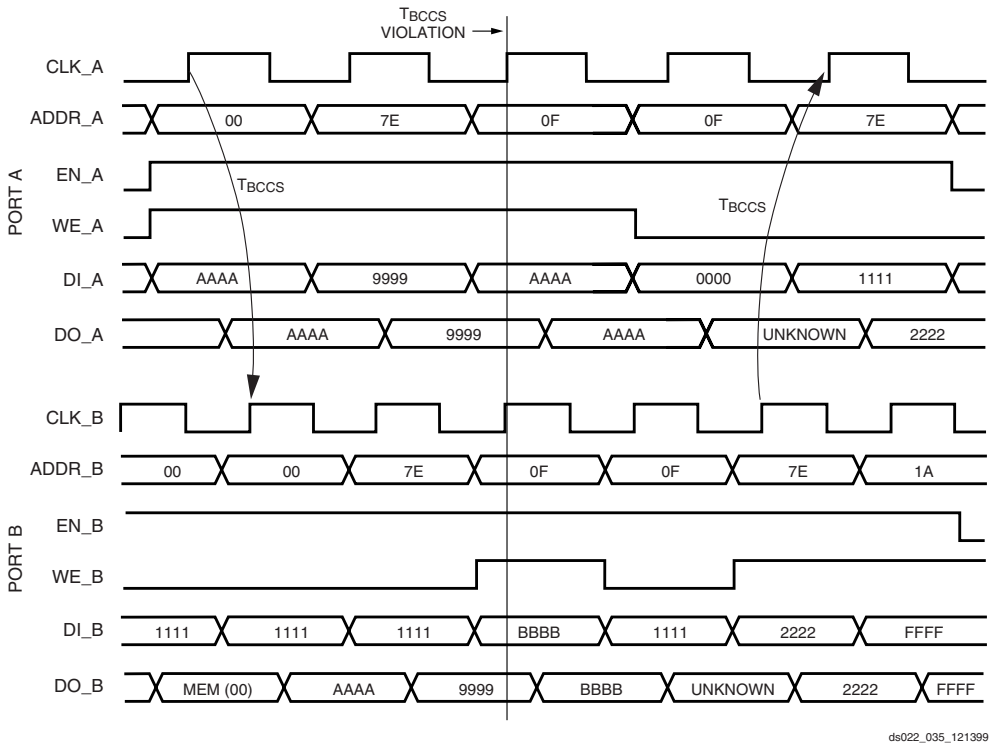


Figure 34: **Timing Diagram for a True Dual-port Read/Write Block SelectRAM+ Memory**

At the third rising edge of CLKA, the T_{BCCS} parameter is violated with two writes to memory location 0x0F. The DOA and DOB buses reflect the contents of the DIA and DIB buses, but the stored value at 0x0F is invalid.

At the fourth rising edge of CLKA, a read operation is performed at memory location 0x0F and invalid data is present on the DOA bus. Port B also executes a read operation to memory location 0x0F and also reads invalid data.

At the fifth rising edge of CLKA a read operation is performed that does not violate the T_{BCCS} parameter to the previous write of 0x7E by Port B. THe DOA bus reflects the recently written value by Port B.

Initialization

The block SelectRAM+ memory can initialize during the device configuration sequence. The 16 initialization properties of 64 hex values each (a total of 4096 bits) set the initialization of each RAM. These properties appear in Table 17. Any initialization properties not explicitly set configure as zeros. Partial initialization strings pad with zeros. Initialization strings greater than 64 hex values generate an error. The RAMs can be simulated with the initialization values using generics in VHDL simulators and parameters in Verilog simulators.

Initialization in VHDL and Synopsys

The block SelectRAM+ structures can be initialized in VHDL for both simulation and synthesis for inclusion in the EDIF output file. The simulation of the VHDL code uses a generic to pass the initialization. Synopsys FPGA compiler does not presently support generics. The initialization values instead attach as attributes to the RAM by a built-in Synopsys dc_script. The translate_off statement stops synthesis translation of the generic statements. The following code illustrates a module that employs these techniques.

Table 17: **RAM Initialization Properties**

Property	Memory Cells
INIT_00	255 to 0
INIT_01	511 to 256
INIT_02	767 to 512
INIT_03	1023 to 768
INIT_04	1279 to 1024
INIT_05	1535 to 1280
INIT_06	1791 to 2047
INIT_07	2047 to 1792
INIT_08	2303 to 2048
INIT_09	2559 to 2304
INIT_0a	2815 to 2560
INIT_0b	3071 to 2816
INIT_0c	3327 to 3072
INIT_0d	3583 to 3328
INIT_0e	3839 to 3584
INIT_0f	4095 to 3840

LVTTL 3-state output buffers have selectable drive strengths.

The format for LVTTL OBUFT symbol names is as follows:

OBUFT_<slew_rate>_<drive_strength>

where <slew_rate> is either F (Fast) or S (Slow), and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

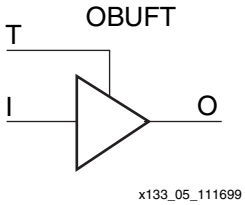


Figure 41: **3-State Output Buffer Symbol (OBUFT)**

The following list details variations of the OBUFT symbol.

- OBUFT
- OBUFT_S_2
- OBUFT_S_4
- OBUFT_S_6
- OBUFT_S_8
- OBUFT_S_12
- OBUFT_S_16
- OBUFT_S_24
- OBUFT_F_2
- OBUFT_F_4
- OBUFT_F_6
- OBUFT_F_8
- OBUFT_F_12
- OBUFT_F_16
- OBUFT_F_24
- OBUFT_LVCMOS2
- OBUFT_PCI33_3
- OBUFT_PCI66_3
- OBUFT_GTL
- OBUFT_GTLP
- OBUFT_HSTL_I
- OBUFT_HSTL_III
- OBUFT_HSTL_IV
- OBUFT_SSTL3_I
- OBUFT_SSTL3_II
- OBUFT_SSTL2_I
- OBUFT_SSTL2_II
- OBUFT_CTT
- OBUFT_AGP
- OBUFT_LVCMOS18
- OBUFT_LVDS
- OBUFT_LVPECL

The Virtex-E series supports eight banks for the HQ and PQ packages. The CS package supports four V_{CCO} banks.

The SelectI/O OBUFT placement restrictions require that within a given V_{CCO} bank each OBUFT share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within the same V_{CCO} bank.

The LOC property can specify a location for the OBUFT.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak “keeper” circuit. Control this feature by adding the appropriate symbol to the output net of the OBUFT (PULLUP, PULLDOWN, or KEEPER).

The weak “keeper” circuit requires the input buffer within the IOB to sample the I/O signal. So, OBUFTs programmed for an I/O standard that requires a V_{REF} have automatic placement of a V_{REF} in the bank with an OBUFT configured with a weak “keeper” circuit. This restriction does not affect most circuit design as applications using an OBUFT configured with a weak “keeper” typically implement a bidirectional I/O. In this case the IBUF (and the corresponding V_{REF}) are explicitly placed.

The LOC property can specify a location for the OBUFT.

IOBUF

Use the IOBUF symbol for bidirectional signals that require both an input buffer and a 3-state output buffer with an active high 3-state pin. The generic input/output buffer IOBUF appears in Figure 42.

The extension to the base name defines which I/O standard the IOBUF uses. With no extension specified for the generic IOBUF symbol, the assumed standard is LVTTL input buffer and slew rate limited LVTTL with 12 mA drive strength for the output buffer.

The LVTTL IOBUF additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL bidirectional buffers have selectable output drive strengths.

The format for LVTTL IOBUF symbol names is as follows:

IOBUF_<slew_rate>_<drive_strength>

where <slew_rate> is either F (Fast) or S (Slow), and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

SSTL2_II

A sample circuit illustrating a valid termination technique for SSTL2_II appears in Figure 52. DC voltage specifications appear in Table 31.

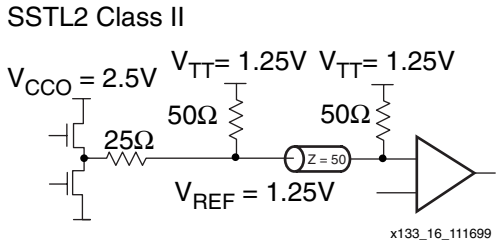


Figure 52: **Terminated SSTL2 Class II**

Table 31: **SSTL2_II Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
$V_{REF} = 0.5 \times V_{CCO}$	1.15	1.25	1.35
$V_{TT} = V_{REF} + N^{(1)}$	1.11	1.25	1.39
$V_{IH} = V_{REF} + 0.18$	1.33	1.43	3.0(2)
$V_{IL} = V_{REF} - 0.18$	–0.3(3)	1.07	1.17
$V_{OH} = V_{REF} + 0.8$	1.95	-	-
$V_{OL} = V_{REF} - 0.8$	-	-	0.55
I_{OH} at V_{OH} (mA)	–15.2	-	-
I_{OL} at V_{OL} (mA)	15.2	-	-

Notes:
1. N must be greater than or equal to -0.04 and less than or equal to 0.04.
2. V_{IH} maximum is V_{CCO} + 0.3.
3. V_{IL} minimum does not conform to the formula.

CTT

A sample circuit illustrating a valid termination technique for CTT appear in Figure 53. DC voltage specifications appear in Table 32.

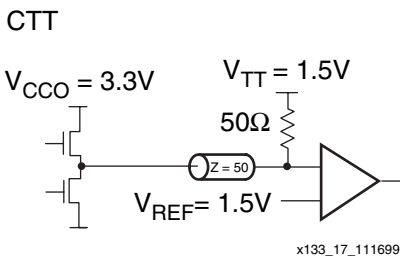


Figure 53: **Terminated CTT**

Table 32: **CTT Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	2.05(1)	3.3	3.6
V_{REF}	1.35	1.5	1.65
V_{TT}	1.35	1.5	1.65
$V_{IH} = V_{REF} + 0.2$	1.55	1.7	-
$V_{IL} = V_{REF} - 0.2$	-	1.3	1.45
$V_{OH} = V_{REF} + 0.4$	1.75	1.9	-
$V_{OL}= V_{REF} - 0.4$	-	1.1	1.25
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL} at V_{OL} (mA)	8	-	-

Notes:
1. Timing delays are calculated based on V_{CCO} min of 3.0V.

PCI33_3 & PCI66_3

PCI33_3 or PCI66_3 require no termination. DC voltage specifications appear in Table 33.

Table 33: **PCI33_3 and PCI66_3 Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
V_{REF}	-	-	-
V_{TT}	-	-	-
$V_{IH} = 0.5 \times V_{CCO}$	1.5	1.65	V_{CCO} + 0.5
$V_{IL} = 0.3 \times V_{CCO}$	–0.5	0.99	1.08
$V_{OH} = 0.9 \times V_{CCO}$	2.7	-	-
$V_{OL}= 0.1 \times V_{CCO}$	-	-	0.36
I_{OH} at V_{OH} (mA)	Note 1	-	-
I_{OL} at V_{OL} (mA)	Note 1	-	-

Notes:
1. Tested according to the relevant specification.

LVTTL

LVTTL requires no termination. DC voltage specifications appears in Table 34.

Table 34: **LVTTL Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
V_{REF}	-	-	-
V_{TT}	-	-	-
V_{IH}	2.0	-	3.6
V_{IL}	–0.5	-	0.8
V_{OH}	2.4	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–24	-	-
I_{OL} at V_{OL} (mA)	24	-	-

Notes:
1. Note: V_{OL} and V_{OH} for lower drive currents sample tested.

LVCMOS2

LVCMOS2 requires no termination. DC voltage specifications appear in Table 35.

Table 35: **LVCMOS2 Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
V_{REF}	-	-	-
V_{TT}	-	-	-
V_{IH}	1.7	-	3.6
V_{IL}	–0.5	-	0.7
V_{OH}	1.9	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–12	-	-
I_{OL} at V_{OL} (mA)	12	-	-

LVCMOS18

LVCMOS18 does not require termination. Table 36 lists DC voltage specifications.

Table 36: **LVCMOS18 Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	1.70	1.80	1.90
V_{REF}	-	-	-
V_{TT}	-	-	-
V_{IH}	0.65 x V_{CCO}	-	1.95
V_{IL}	– 0.5	-	0.2 x V_{CCO}
V_{OH}	V_{CCO} – 0.4	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL} at V_{OL} (mA)	8	-	-

AGP-2X

The specification for the AGP-2X standard does not document a recommended termination technique. DC voltage specifications appear in Table 37.

Table 37: **AGP-2X Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = N \times V_{CCO}$ (1)	1.17	1.32	1.48
V_{TT}	-	-	-
$V_{IH} = V_{REF} + 0.2$	1.37	1.52	-
$V_{IL} = V_{REF} – 0.2$	-	1.12	1.28
$V_{OH} = 0.9 \times V_{CCO}$	2.7	3.0	-
$V_{OL} = 0.1 \times V_{CCO}$	-	0.33	0.36
I_{OH} at V_{OH} (mA)	Note 2	-	-
I_{OL} at V_{OL} (mA)	Note 2	-	-

Notes:
1. N must be greater than or equal to 0.39 and less than or equal to 0.41.
2. Tested according to the relevant specification.

Date	Version	Revision
9/20/00	1.7	• Min values added to **Virtex-E Electrical Characteristics** tables. • XCV2600E and XCV3200E numbers added to **Virtex-E Electrical Characteristics** tables (Module 3). • Corrected user I/O count for XCV100E device in Table 1 (Module 1). • Changed several pins to “No Connect in the XCV100E“ and removed duplicate V_{CCINT} pins in Table ~ (Module 4). • Changed pin J10 to “No connect in XCV600E” in Table 74 (Module 4). • Changed pin J30 to “VREF option only in the XCV600E” in Table 74 (Module 4). • Corrected pair 18 in Table 75 (Module 4) to be “AO in the XCV1000E, XCV1600E“.
11/20/00	1.8	• Upgraded speed grade -8 numbers in **Virtex-E Electrical Characteristics** tables to Preliminary. • Updated minimums in Table 13 and added notes to Table 14. • Added to note 2 to **Absolute Maximum Ratings**. • Changed speed grade -8 numbers for $T_{SHCKO32}$, T_{REG}, T_{BCCS}, and T_{ICKOF}. • Changed all minimum hold times to –0.4 under **Global Clock Set-Up and Hold for LVTTL Standard, with DLL**. • Revised maximum T_{DLLPW} in -6 speed grade for **DLL Timing Parameters**. • Changed GCLK0 to BA22 for FG860 package in Table 46.
2/12/01	1.9	• Revised footnote for Table 14. • Added numbers to **Virtex-E Electrical Characteristics** tables for XCV1000E and XCV2000E devices. • Updated Table 27 and Table 78 to include values for XCV400E and XCV600E devices. • Revised Table 62 to include pinout information for the XCV400E and XCV600E devices in the BG560 package. • Updated footnotes 1 and 2 for Table 76 to include XCV2600E and XCV3200E devices.
4/02/01	2.0	• Updated numerous values in **Virtex-E Switching Characteristics** tables. • Converted data sheet to modularized format. See the **Virtex-E Data Sheet** section.
4/19/01	2.1	• Modified Figure 30 "DLL Generation of 4x Clock in Virtex-E Devices."
07/23/01	2.2	• Made minor edits to text under **Configuration**. • Added CLB column locations for XCV2600E anbd XCV3200E devices in Table 3.
11/09/01	2.3	• Added warning under **Configuration** section that attempting to load an incorrect bitstream causes configuration to fail and can damage the device.
07/17/02	2.4	• Data sheet designation upgraded from Preliminary to Production.
09/10/02	2.5	• Added clarification to the **Input/Output Block**, **Configuration**, **Boundary Scan Mode**, and **Block SelectRAM** sections. Revised Figure 18, Table 11, and Table 36.
11/19/02	2.6	• Added clarification in the **Boundary Scan** section. • Removed last sentence regarding deactivation of duty-cycle correction in **Duty Cycle Correction Property** section.
06/15/04	2.6.1	• Updated clickable web addresses.
01/12/06	2.7	• Updated the **Slave-Serial Mode** and the **Master-Serial Mode** sections.
01/16/06	2.8	• Made minor updates to Table 8.

Virtex-E Electrical Characteristics

Definition of Terms

Electrical and switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance: These speed files are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These speed files are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production: These speed files are released once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. Contact the factory for design considerations requiring more detailed information.

Table 1 correlates the current status of each Virtex-E device with a corresponding speed file designation.

Table 1: **Virtex-E Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XCV50E			–8, –7, –6
XCV100E			–8, –7, –6
XCV200E			–8, –7, –6
XCV300E			–8, –7, –6
XCV400E			–8, –7, –6
XCV600E			–8, –7, –6
XCV1000E			–8, –7, –6
XCV1600E			–8, –7, –6
XCV2000E			–8, –7, –6
XCV2600E			–8, –7, –6
XCV3200E			–8, –7, –6

All specifications are subject to change without notice.

DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Device	Min	Max	Units
V_{DRINT}	Data Retention V_{CCINT} Voltage (below which configuration data might be lost)		All	1.5		V
V_{DRIO}	Data Retention V_{CCO} Voltage (below which configuration data might be lost)		All	1.2		V
I_{CCINTQ}	Quiescent V_{CCINT} supply current (Note 1)		XCV50E		200	mA
			XCV100E		200	mA
			XCV200E		300	mA
			XCV300E		300	mA
			XCV400E		300	mA
			XCV600E		400	mA
			XCV1000E		500	mA
			XCV1600E		500	mA
			XCV2000E		500	mA
			XCV2600E		500	mA
			XCV3200E		500	mA
I_{CCOQ}	Quiescent V_{CCO} supply current (Note 1)		XCV50E		2	mA
			XCV100E		2	mA
			XCV200E		2	mA
			XCV300E		2	mA
			XCV400E		2	mA
			XCV600E		2	mA
			XCV1000E		2	mA
			XCV1600E		2	mA
			XCV2000E		2	mA
			XCV2600E		2	mA
			XCV3200E		2	mA
I_L	Input or output leakage current		All	–10	+10	µA
C_{IN}	Input capacitance (sample tested)	BGA, PQ, HQ, packages	All		8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0 V, V_{CCO} = 3.3 V (sample tested)		All	Note 2	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 3.6 V (sample tested)			Note 2	0.25	mA

Notes:
1. With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating.
2. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.

CLB Distributed RAM Switching Characteristics

Description	Symbol	Speed Grade(1)				Units
		Min	-8	-7	-6	
Sequential Delays						
Clock CLK to X/Y outputs (WE active) 16 x 1 mode	$T_{SHCKO16}$	0.67	1.38	1.5	1.7	ns, max
Clock CLK to X/Y outputs (WE active) 32 x 1 mode	$T_{SHCKO32}$	0.84	1.66	1.9	2.1	ns, max
Shift-Register Mode Clock CLK to X/Y outputs	T_{REG}	1.25	2.39	2.9	3.2	ns, max
Setup and Hold Times before/after Clock CLK						
F/G address inputs	T_{AS}/T_{AH}	0.19 / 0	0.38 / 0	0.42 / 0	0.47 / 0	ns, min
BX/BY data inputs (DIN)	T_{DS}/T_{DH}	0.44 / 0	0.87 / 0	0.97 / 0	1.09 / 0	ns, min
SR input (WE)	T_{WS}/T_{WH}	0.29 / 0	0.57 / 0	0.7 / 0	0.8 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T_{WPH}	0.96	1.9	2.1	2.4	ns, min
Minimum Pulse Width, Low	T_{WPL}	0.96	1.9	2.1	2.4	ns, min
Minimum clock period to meet address write cycle time	T_{WC}	1.92	3.8	4.2	4.8	ns, min
Shift-Register Mode						
Minimum Pulse Width, High	T_{SRPH}	1.0	1.9	2.1	2.4	ns, min
Minimum Pulse Width, Low	T_{SRPL}	1.0	1.9	2.1	2.4	ns, min

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

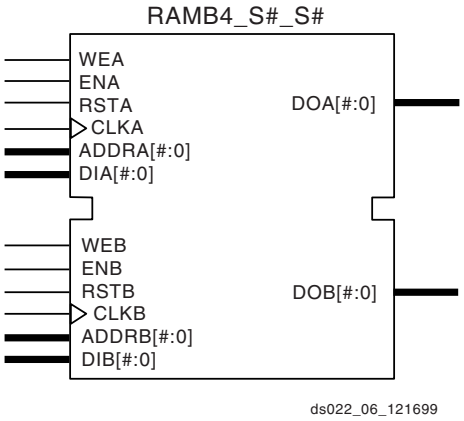


Figure 3: **Dual-Port Block SelectRAM**

DLL Clock Tolerance, Jitter, and Phase Information

All DLL output jitter and phase specifications determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers.

			CLKDLLHF		CLKDLL		
Description	**Symbol**	**F_{CLKIN}**	**Min**	**Max**	**Min**	**Max**	**Units**
Input Clock Period Tolerance	T_{IPTOL}		-	1.0	-	1.0	ns
Input Clock Jitter Tolerance (Cycle to Cycle)	T_{IJITCC}		-	± 150	-	± 300	ps
Time Required for DLL to Acquire Lock(6)	T_{LOCK}	> 60 MHz	-	20	-	20	µs
		50 - 60 MHz	-	-	-	25	µs
		40 - 50 MHz	-	-	-	50	µs
		30 - 40 MHz	-	-	-	90	µs
		25 - 30 MHz	-	-	-	120	µs
Output Jitter (cycle-to-cycle) for any DLL Clock Output(1)	T_{OJITCC}			± 60		± 60	ps
Phase Offset between CLKIN and CLKO(2)	T_{PHIO}			± 100		± 100	ps
Phase Offset between Clock Outputs on the DLL(3)	T_{PHOO}			± 140		± 140	ps
Maximum Phase Difference between CLKIN and CLKO(4)	T_{PHIOM}			± 160		± 160	ps
Maximum Phase Difference between Clock Outputs on the DLL(5)	T_{PHOOM}			± 200		± 200	ps

Notes:

1. **Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock and is based on a maximum tap delay resolution, *excluding* input clock jitter.
2. **Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* Output Jitter and input clock jitter.
3. **Phase Offset between Clock Outputs on the DLL** is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* Output Jitter and input clock jitter.
4. **Maximum Phase Difference between CLKIN an CLKO** is the sum of Output Jitter and Phase Offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).
5. **Maximum Phase DIfference between Clock Outputs on the DLL** is the sum of Output JItter and Phase Offset between any DLL clock outputs, or the greatest difference between any two DLL output rising edges sue to DLL alone (*excluding* input clock jitter).
6. Add 30% to the value for industrial grade parts.

Table 4: **CS144 — XCV50E, XCV100E, XCV200E**

Bank	Pin Description	Pin #
1	VCCO	A13
1	VCCO	D7
2	VCCO	B12
3	VCCO	G11
3	VCCO	M13
4	VCCO	N13
5	VCCO	N1
5	VCCO	N7
6	VCCO	M2
7	VCCO	B2
7	VCCO	G2
NA	GND	A1
NA	GND	B9
NA	GND	B11
NA	GND	C7
NA	GND	D5
NA	GND	E4
NA	GND	E11
NA	GND	F1
NA	GND	G10
NA	GND	J1
NA	GND	J12
NA	GND	L3
NA	GND	L5
NA	GND	L7
NA	GND	L9
NA	GND	N12

Notes:
1. V_{REF} or I/O option only in the XCV200E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV100E, 200E; otherwise, I/O option only.

CS144 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 5: **CS144 Differential Pin Pair Summary XCV50E, XCV100E, XCV200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	K7	N8	NA	IO_DLL_L18P
1	5	M7	M6	NA	IO_DLL_L18N
2	1	A7	B7	NA	IO_DLL_L2P
3	0	A6	C6	NA	IO_DLL_L2N
IO LVDS Total Pairs: 30, Asynchronous Output Pairs: 18					
0	0	A4	B4	√	VREF
1	0	A5	B5	√	-
2	1	B7	C6	NA	IO_LVDS_DLL
3	1	D8	C8	√	-
4	1	D9	C9	√	VREF
5	1	D10	C10	√	CS, WRITE
6	2	C11	C12	√	DIN, D0
7	2	D13	E10	1	D1, VREF
8	2	E12	E13	√	D2
9	2	F10	F11	1	D3, VREF
10	3	F13	G13	NA	-
11	3	H12	H11	1	D4, VREF
12	3	H10	J13	√	D5
13	3	J11	J10	1	D6, VREF
14	3	K10	L13	√	INIT
15	4	L11	M11	√	-
16	4	N10	K9	√	VREF
17	4	N9	K8	√	-

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P210	GCK2	1
P209	IO_LVDS_DLL_L6P	1
P208	IO_VREF	1
P207	VCCO	1
P206	IO_L7N_Y	1
P205	IO_VREF_L7P_Y	1
P204	GND	NA
P203	IO_L8N_Y	1
P202	IO_L8P_Y	1
P201[1]	IO_VREF	1
P200	IO_L9N_YY	1
P199	IO_L9P_YY	1
P198	VCCINT	NA
P197	VCCO	1
P196	GND	NA
P195	IO_L10N_YY	1
P194	IO_VREF_L10P_YY	1
P193	IO_VREF	1
P192	IO_L11N_YY	1
P191	IO_VREF_L11P_YY	1
P190	GND	NA
P189	IO_L12N_YY	1
P188	IO_L12P_YY	1
P187	IO_VREF_L13N	1
P186	IO_L13P	1
P185	IO_WRITE_L14N_YY	1
P184	IO_CS_L14P_YY	1
P183	TDI	NA
P182	GND	NA
P181	TDO	2
P180	VCCO	1
P179	CCLK	2
P178	IO_DOUT_BUSY_L15P_YY	2
P177	IO_DIN_D0_L15N_YY	2
P176	VCCO	2
P175	IO_VREF	2

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P174	IO_L16P_Y	2
P173	IO_L16N_Y	2
P172	GND	NA
P171	IO_VREF_L17P_Y	2
P170	IO_L17N_Y	2
P169	IO_VREF	2
P168	IO_VREF_L18P_Y	2
P167	IO_D1_L18N_Y	2
P166	GND	NA
P165	VCCO	2
P164	VCCINT	NA
P163	IO_D2_L19P_YY	2
P162	IO_L19N_YY	2
P161[1]	IO_VREF	2
P160	IO_L20P_Y	2
P159	IO_L20N_Y	2
P158	GND	NA
P157	IO_VREF_L21P_Y	2
P156	IO_D3_L21N_Y	2
P155	IO_L22P_Y	2
P154	IO_VREF_L22N_Y	2
P153	IO_L23P_YY	2
P152	IO_L23N_YY	2
P151	GND	NA
P150	VCCO	2
P149	IO	3
P148	VCCINT	NA
P147	IO_VREF	3
P146	VCCO	3
P145	IO_D4_L24P_Y	3
P144	IO_VREF_L24N_Y	3
P143	GND	NA
P142	IO_L25P_Y	3
P141	IO_L25N_Y	3
P140[1]	IO_VREF	3
P139	IO_L26P_YY	3

Table 15: **BG560 Differential Pin Pair Summary XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
109	4	AJ14	AK14	√	-
110	4	AM14	AN15	√	VREF
111	4	AJ15	AK15	1	-
112	4	AL15	AM16	7	-
113	4	AL16	AJ16	7	VREF
114	4	AK16	AN17	2	VREF
115	5	AM17	AM18	NA	IO_LVDS_DLL
116	5	AK18	AJ18	7	VREF
117	5	AN19	AL19	7	-
118	5	AK19	AM20	9	-
119	5	AJ19	AL20	√	VREF
120	5	AN21	AL21	√	-
121	5	AJ20	AM22	3	-
122	5	AK21	AN23	√	VREF
123	5	AJ21	AM23	√	-
124	5	AK22	AM24	8	-
125	5	AL23	AJ22	√	-
126	5	AK23	AL24	√	VREF
127	5	AN26	AJ23	13	-
128	5	AK24	AM26	7	VREF
129	5	AM27	AJ24	7	-
130	5	AL26	AK25	5	VREF
131	5	AN29	AJ25	√	VREF
132	5	AK26	AM29	√	-
133	5	AM30	AJ26	11	-
134	5	AK27	AL29	√	VREF
135	5	AN31	AJ27	√	-
136	5	AM31	AK28	12	VREF
137	6	AJ30	AH29	√	-
138	6	AH30	AK31	17	VREF
139	6	AJ31	AG29	14	-

Table 15: **BG560 Differential Pin Pair Summary XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
140	6	AG30	AK32	15	VREF
141	6	AF29	AH31	16	-
142	6	AF30	AH32	15	-
143	6	AH33	AE29	√	VREF
144	6	AE30	AG33	17	VREF
145	6	AF32	AD29	14	-
146	6	AD30	AE31	18	VREF
147	6	AC29	AE32	19	-
148	6	AC30	AD31	√	VREF
149	6	AC31	AB29	√	-
150	6	AB30	AC33	17	-
151	6	AA29	AB31	14	-
152	6	AA31	AA30	15	VREF
153	6	Y29	AA32	16	-
154	6	Y30	AA33	15	-
155	6	W29	Y32	√	VREF
156	6	W31	W30	17	-
157	6	V30	W33	14	-
158	6	V31	V29	18	VREF
159	6	U33	V32	19	VREF
160	7	U32	U31	√	-
161	7	T30	T32	19	VREF
162	7	T31	T29	18	VREF
163	7	R31	R33	14	-
164	7	R29	R30	17	-
165	7	P31	P32	√	VREF
166	7	P29	P30	15	-
167	7	N31	M32	16	-
168	7	L33	N30	15	VREF
169	7	L32	M31	14	-
170	7	L31	M30	17	-

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
4	IO_L98N_YY	AB19
4	IO_L99P_YY	AC20
4	IO_L99N_YY	AA18
4	IO_L100P_Y	AC19
4	IO_L100N_Y	AD20
4	IO_VREF_L101P_Y	AF20[2]
4	IO_L101N_Y	AB18
4	IO_L102P	AD19
4	IO_L102N	Y17
4	IO_L103P	AE19
4	IO_VREF_L103N	AD18
4	IO_L104P_YY	AF19
4	IO_L104N_YY	AA17
4	IO_L105P_Y	AC17
4	IO_L105N_Y	AB17
4	IO_L106P_YY	Y16
4	IO_L106N_YY	AE17
4	IO_L107P_YY	AF17
4	IO_L107N_YY	AA16
4	IO_L108P	AD17
4	IO_L108N	AB16
4	IO_L109P_YY	AC16
4	IO_L109N_YY	AD16
4	IO_VREF_L110P_YY	AC15
4	IO_L110N_YY	Y15
4	IO_L111P_YY	AD15
4	IO_L111N_YY	AA15
4	IO_L112P_Y	W14
4	IO_L112N_Y	AB15
4	IO_VREF_L113P_Y	AF15
4	IO_L113N_Y	Y14
4	IO_L114P	AD14
4	IO_L114N	AB14
4	IO_LVDS_DLL_L115P	AC14
5	GCK1	AB13
5	IO	Y13[1]

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
5	IO	AD7
5	IO	AD13
5	IO	AE4
5	IO	AE7
5	IO	AE12[1]
5	IO	AF3[1]
5	IO	AF5
5	IO	AF10[1]
5	IO	AF11[1]
5	IO_LVDS_DLL_L115N	AF13
5	IO_L116P_Y	AA13
5	IO_VREF_L116N_Y	AF12
5	IO_L117P_Y	AC13
5	IO_L117N_Y	W13
5	IO_L118P_YY	AA12
5	IO_L118N_YY	AD12
5	IO_L119P_YY	AC12
5	IO_VREF_L119N_YY	AB12
5	IO_L120P_YY	AD11
5	IO_L120N_YY	Y12
5	IO_L121P	AB11
5	IO_L121N	AD10
5	IO_L122P_YY	AC11
5	IO_L122N_YY	AE10
5	IO_L123P_YY	AC10
5	IO_L123N_YY	AA11
5	IO_L124P_Y	Y11
5	IO_L124N_Y	AD9
5	IO_L125P_YY	AB10
5	IO_L125N_YY	AF9
5	IO_L126P_YY	AD8
5	IO_VREF_L126N_YY	AA10
5	IO_L127P_YY	AE8
5	IO_L127N_YY	Y10
5	IO_L128P_Y	AC9
5	IO_VREF_L128N_Y	AF8[2]
5	IO_L129P_Y	AF7

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
0	VCCO	E34
0	VCCO	E33
0	VCCO	E30
0	VCCO	E29
0	VCCO	E27
0	VCCO	E26
1	VCCO	E10
1	VCCO	E11
1	VCCO	E13
1	VCCO	E14
1	VCCO	E6
1	VCCO	E7
2	VCCO	P5
2	VCCO	N5
2	VCCO	L5
2	VCCO	K5
2	VCCO	G5
2	VCCO	F5
3	VCCO	AP5
3	VCCO	AN5
3	VCCO	AK5
3	VCCO	AJ5
3	VCCO	AG5
3	VCCO	AF5
4	VCCO	AR10
4	VCCO	AR11
4	VCCO	AR13
4	VCCO	AR14
4	VCCO	AR6
4	VCCO	AR7
5	VCCO	AR34
5	VCCO	AR33
5	VCCO	AR30
5	VCCO	AR29
5	VCCO	AR27
5	VCCO	AR26
6	VCCO	AP35
6	VCCO	AN35
6	VCCO	AK35
6	VCCO	AJ35
6	VCCO	AG35
6	VCCO	AF35
7	VCCO	P35
7	VCCO	N35
7	VCCO	L35
7	VCCO	K35
7	VCCO	G35
7	VCCO	F35
NA	GND	Y5
NA	GND	Y4
NA	GND	Y37
NA	GND	Y36
NA	GND	Y35
NA	GND	Y3
NA	GND	W5
NA	GND	W35
NA	GND	M5
NA	GND	M4
NA	GND	M36
NA	GND	M35
NA	GND	E5
NA	GND	E35
NA	GND	E28
NA	GND	E21
NA	GND	E20
NA	GND	E19
NA	GND	E12
NA	GND	D4
NA	GND	D36
NA	GND	D28

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
3	IO_L117N_Y	AJ5
3	IO_L118P	AG2
3	IO_L118N	AK4
3	IO_L119P_Y	AG3
3	IO_L119N_Y	AL4
3	IO_L120P_Y	AH1
3	IO_L120N_Y	AL5
3	IO_L121P_Y	AH2
3	IO_L121N_Y	AM4
3	IO_L122P_YY	AH3
3	IO_D5_L122N_YY	AM5
3	IO_D6_L123P_YY	AJ1
3	IO_VREF_L123N_YY	AN3
3	IO_L124P_Y	AN4
3	IO_L124N_Y	AJ3
3	IO_L125P_YY	AN5
3	IO_L125N_YY	AK1
3	IO_L126P_YY	AK2
3	IO_VREF_L126N_YY	AP4
3	IO_L127P_Y	AK3
3	IO_L127N_Y	AP5
3	IO_L128P_Y	AR3
3	IO_VREF_L128N_Y	AL2[2]
3	IO_L129P_YY	AR4
3	IO_L129N_YY	AL3
3	IO_L130P_YY	AM1
3	IO_VREF_L130N_YY	AT3
3	IO_L131P_Y	AM2
3	IO_L131N_Y	AT4
3	IO_L132P_Y	AT5
3	IO_L132N_Y	AN1
3	IO_L133P_YY	AU3
3	IO_L133N_YY	AN2
3	IO_L134P_Y	AP1
3	IO_VREF_L134N_Y	AP2
3	IO_L135P_Y	AR1
3	IO_L135N_Y	AV3

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
3	IO_L136P	AR2
3	IO_L136N	AT1
3	IO_L137P_Y	AV4
3	IO_VREF_L137N_Y	AT2
3	IO_L138P_Y	AU1
3	IO_L138N_Y	AU5
3	IO_L139P_Y	AU2
3	IO_L139N_Y	AW3
3	IO_D7_L140P_YY	AV1
3	IO_INIT_L140N_YY	AW5
4	GCK0	BA22
4	IO	AV17
4	IO	AY11
4	IO	AY12
4	IO	AY13
4	IO	AY14
4	IO	BA8
4	IO	BA17
4	IO	BA19
4	IO	BA20
4	IO	BA21
4	IO	BB9
4	IO	BB18
4	IO_L141P_YY	AV6
4	IO_L141N_YY	BA4
4	IO_L142P_Y	AY4
4	IO_L142N_Y	BA5
4	IO_L143P_Y	AW6
4	IO_L143N_Y	BB5
4	IO_VREF_L144P_Y	BA6
4	IO_L144N_Y	AY5
4	IO_L145P_Y	BB6
4	IO_L145N_Y	AY6
4	IO_L146P_YY	BA7
4	IO_L146N_YY	AV7
4	IO_VREF_L147P_YY	BB7

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
5	IO_L239P_Y	AP9
5	IO_L239N_Y	AK11
5	IO_L240P_YY	AL11
5	IO_VREF_L240N_YY	AL10
5	IO_L241P_YY	AE13
5	IO_L241N_YY	AM9
5	IO_L242P	AF12[5]
5	IO_L242N	AP8[4]
5	IO_L243P_Y	AL9
5	IO_VREF_L243N_Y	AH11[2]
5	IO_L244P_Y	AF11
5	IO_L244N_Y	AN8
5	IO_L245P_Y	AM8[5]
5	IO_L245N_Y	AG11[4]
5	IO_L246P_YY	AL8
5	IO_VREF_L246N_YY	AK9
5	IO_L247P_YY	AH10
5	IO_L247N_YY	AN7
5	IO_L248P	AE12[5]
5	IO_L248N	AJ9[4]
5	IO_L249P_Y	AM7
5	IO_L249N_Y	AL7
5	IO_L250P_Y	AG10
5	IO_L250N_Y	AN6
5	IO_L251P_YY	AK8[5]
5	IO_L251N_YY	AH9[4]
5	IO_L252P_YY	AP5
5	IO_VREF_L252N_YY	AJ8
5	IO_L253P_YY	AE11
5	IO_L253N_YY	AN5
5	IO_L254P_Y	AF10
5	IO_L254N_Y	AM6
5	IO_L255P_Y	AL6
5	IO_VREF_L255N_Y	AG9

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
5	IO_L256P_Y	AH8
5	IO_L256N_Y	AP4
5	IO_L257P_Y	AN4
5	IO_L257N_Y	AJ7
5	IO_L258P_YY	AM5
5	IO_L258N_YY	AK6
6	IO	T1
6	IO	V2
6	IO	V3
6	IO	V5[3]
6	IO	V8[3]
6	IO	AA10[3]
6	IO	AB5[3]
6	IO	AB7[3]
6	IO	AB9[3]
6	IO	AD7[3]
6	IO	AD8[3]
6	IO	AE2
6	IO	AE4
6	IO	AJ4[3]
6	IO	AH5[3]
6	IO_L259N_YY	AH6
6	IO_L259P_YY	AF8
6	IO_L260N_Y	AE9
6	IO_L260P_Y	AK3
6	IO_L261N_Y	AD10
6	IO_L261P_Y	AL2
6	IO_VREF_L262N_Y	AL1
6	IO_L262P_Y	AH4
6	IO_L263N	AG6
6	IO_L263P	AK1
6	IO_L264N_Y	AF7
6	IO_L264P_Y	AK2

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
231	5	AH14	AP12	3200 2600 2000 1600 1000	-
232	5	AJ14	AL14	3200 2600 1000	-
233	5	AF13	AN12	3200 2000 1000	-
234	5	AF14	AP11	3200 2000 1000	-
235	5	AN11	AH13	3200 1600 1000	-
236	5	AM12	AL12	3200 2600 2000 1600 1000	-
237	5	AJ13	AP10	3200 2600 2000 1600 1000	VREF
238	5	AK12	AM10	2600 1600 1000	-
239	5	AP9	AK11	2600 1600 1000	-
240	5	AL11	AL10	3200 2600 2000 1600 1000	VREF
241	5	AE13	AM9	3200 2600 2000 1600 1000	-
242	5	AF12	AP8	3200 2600	-
243	5	AL9	AH11	3200 2000 1000	VREF
244	5	AF11	AN8	3200 2000 1000	-
245	5	AM8	AG11	3200 1600	-
246	5	AL8	AK9	3200 2600 2000 1600 1000	VREF
247	5	AH10	AN7	3200 2600 2000 1600 1000	-
248	5	AE12	AJ9	3200 2600	-
249	5	AM7	AL7	3200 1000	-
250	5	AG10	AN6	3200 1000	-

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
251	5	AK8	AH9	2000 1600	-
252	5	AP5	AJ8	3200 2600 2000 1600 1000	VREF
253	5	AE11	AN5	3200 2600 2000 1600 1000	-
254	5	AF10	AM6	3200 2600 1000	-
255	5	AL6	AG9	3200 2000 1000	VREF
256	5	AH8	AP4	3200 2000 1000	-
257	5	AN4	AJ7	3200 1600 1000	-
258	5	AM5	AK6	3200 2600 2000 1600 1000	-
259	6	AF8	AH6	3200 2600 2000 1600 1000	-
260	6	AK3	AE9	3200 2600 2000	-
261	6	AL2	AD10	2600 2000 1000	-
262	6	AH4	AL1	3200 2600 1600 1000	VREF
263	6	AK1	AG6	2600 1600	-
264	6	AK2	AF7	3200 2600 1600 1000	-
265	6	AG5	AJ3	2600 2000 1000	VREF
266	6	AJ2	AD9	3200 2600 2000 1600	-
267	6	AH2	AC10	3200 2600 2000 1600 1000	-
268	6	AF5	AH3	3200 2600 1600 1000	-
269	6	AG3	AE8	3200 2600 2000	-