AMD Xilinx - XCV100E-8FG256C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	600
Number of Logic Elements/Cells	2700
Total RAM Bits	81920
Number of I/O	176
Number of Gates	128236
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv100e-8fg256c

forces a storage element into the initialization state specified for it in the configuration. BY forces it into the opposite state. Alternatively, these signals can be configured to operate asynchronously. All of the control signals are independently invertible, and are shared by the two flip-flops within the slice.

Additional Logic

The F5 multiplexer in each slice combines the function generator outputs. This combination provides either a function generator that can implement any 5-input function, a 4:1 multiplexer, or selected functions of up to nine inputs.

Similarly, the F6 multiplexer combines the outputs of all four function generators in the CLB by selecting one of the F5-multiplexer outputs. This permits the implementation of any 6-input function, an 8:1 multiplexer, or selected functions of up to 19 inputs.

Each CLB has four direct feedthrough paths, two per slice. These paths provide extra data input lines or additional local routing that does not consume logic resources.

Arithmetic Logic

Dedicated carry logic provides fast arithmetic carry capability for high-speed arithmetic functions. The Virtex-E CLB supports two separate carry chains, one per Slice. The height of the carry chains is two bits per CLB.

The arithmetic logic includes an XOR gate that allows a 2-bit full adder to be implemented within a slice. In addition, a dedicated AND gate improves the efficiency of multiplier implementation. The dedicated carry path can also be used to cascade function generators for implementing wide logic functions.

BUFTs

Each Virtex-E CLB contains two 3-state drivers (BUFTs) that can drive on-chip buses. See **Dedicated Routing**. Each Virtex-E BUFT has an independent 3-state control pin and an independent input pin.

Block SelectRAM

Virtex-E FPGAs incorporate large block SelectRAM memories. These complement the Distributed SelectRAM memories that provide shallow RAM structures implemented in CLBs.

Block SelectRAM memory blocks are organized in columns, starting at the left (column 0) and right outside edges and inserted every 12 CLB columns (see notes for smaller devices). Each memory block is four CLBs high, and each memory column extends the full height of the chip, immediately adjacent (to the right, except for column 0) of the CLB column locations indicated in Table 3.

Table 3: **CLB/Block RAM Column Locations**

XCV Device /Col.	0	12	24	36	48	60	72	84	96	108	120	138	156
50E	Columns 0, 6, 18, & 24												
100E	Columns 0, 12, 18, & 30												
200E	Columns 0, 12, 30, & 42												
300E	√	√		√	√								
400E	√	√			√	√							
600E	√	√	√		√	√	√						
1000E	√	√	√				√	√	√				
1600E	√	√	√	√			√	√	√	√			
2000E	√	√	√	√				√	√	√	√		
2600E	√	√	√	√					√	√	√	√	
3200E	√	√	√	√						√	√	√	√

Table 4 shows the amount of block SelectRAM memory that is available in each Virtex-E device.

Table 4: **Virtex-E Block SelectRAM Amounts**

Virtex-E Device	# of Blocks	Block SelectRAM Bits
XCV50E	16	65,536
XCV100E	20	81,920
XCV200E	28	114,688
XCV300E	32	131,072
XCV400E	40	163,840
XCV600E	72	294,912
XCV1000E	96	393,216
XCV1600E	144	589,824
XCV2000E	160	655,360
XCV2600E	184	753,664
XCV3200E	208	851,968

As illustrated in Figure 6, each block SelectRAM cell is a fully synchronous dual-ported (True Dual Port) 4096-bit RAM with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.

For in-circuit debugging, an optional download and readback cable is available. This cable connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can single-step the logic, readback the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.

Configuration

Virtex-E devices are configured by loading configuration data into the internal configuration memory. Note that attempting to load an incorrect bitstream causes configuration to fail and can damage the device.

Some of the pins used for configuration are dedicated pins, while others can be re-used as general purpose inputs and outputs once configuration is complete.

The following are dedicated pins:

- Mode pins (M2, M1, M0)
- Configuration clock pin (CCLK)
- $\overline{\text{PROGRAM}}$ pin
- DONE pin
- Boundary Scan pins (TDI, TDO, TMS, TCK)

Depending on the configuration mode chosen, CCLK can be an output generated by the FPGA, or can be generated externally and provided to the FPGA as an input. The $\overline{\text{PROGRAM}}$ pin must be pulled High prior to reconfiguration.

Note that some configuration pins can act as outputs. For correct operation, these pins require a V_{CCO} of 3.3 V or 2.5 V. At 3.3 V the pins operate as LVTTL, and at 2.5 V they operate as LVCMOS. All affected pins fall in banks 2 or 3. The configuration pins needed for SelectMap (CS, Write) are located in bank 1.

Configuration Modes

Virtex-E supports the following four configuration modes.

- Slave-serial mode
- Master-serial mode
- SelectMAP mode
- Boundary Scan mode (JTAG)

The Configuration mode pins (M2, M1, M0) select among these configuration modes with the option in each case of having the IOB pins either pulled up or left floating prior to configuration. The selection codes are listed in Table 8.

Configuration through the Boundary Scan port is always available, independent of the mode selection. Selecting the Boundary Scan mode simply turns off the other modes. The three mode pins have internal pull-up resistors, and default to a logic High if left unconnected. However, it is recommended to drive the configuration mode pins externally.

Table 8: **Configuration Codes**

Configuration Mode	M2[1]	M1	M0	CCLK Direction	Data Width	Serial D_{out}	Configuration Pull-ups[1]
Master-serial mode	0	0	0	Out	1	Yes	No
Boundary Scan mode	1	0	1	N/A	1	No	No
SelectMAP mode	1	1	0	In	8	No	No
Slave-serial mode	1	1	1	In	1	Yes	No
Master-serial mode	1	0	0	Out	1	Yes	Yes
Boundary Scan mode	0	0	1	N/A	1	No	Yes
SelectMAP mode	0	1	0	In	8	No	Yes
Slave-serial mode	0	1	1	In	1	Yes	Yes

Notes:
1. M2 is sampled continuously from power up until the end of the configuration. Toggling M2 while INIT is being held externally Low can cause the configuration pull-up settings to change.

Configuration through the TAP uses the CFG_IN instruction. This instruction allows data input on TDI to be converted into data packets for the internal configuration bus.

The following steps are required to configure the FPGA through the Boundary Scan port (when using TCK as a start-up clock).

1. Load the CFG_IN instruction into the Boundary Scan instruction register (IR).
2. Enter the Shift-DR (SDR) state.
3. Shift a configuration bitstream into TDI.
4. Return to Run-Test-Idle (RTI).
5. Load the JSTART instruction into IR.
6. Enter the SDR state.
7. Clock TCK through the startup sequence.
8. Return to RTI.

Configuration and readback via the TAP is always available. The Boundary Scan mode is selected by a <101> or <001> on the mode pins (M2, M1, M0). For details on TAP characteristics, refer to XAPP139.

Configuration Sequence

The configuration of Virtex-E devices is a three-phase process. First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user, as described below. The configuration process can also be initiated by asserting $\overline{\text{PROGRAM}}$. The end of the memory-clearing phase is signalled by $\overline{\text{INIT}}$ going High, and the completion of the entire process is signalled by DONE going High.

The power-up timing of configuration signals is shown in Figure 20.

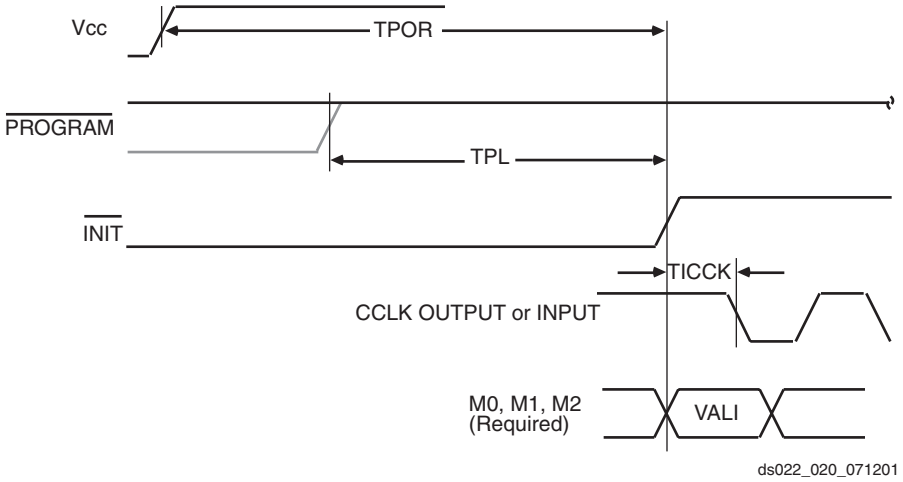

Figure 20: **Power-Up Timing Configuration Signals**

The corresponding timing characteristics are listed in Table 12.

Table 12: **Power-up Timing Characteristics**

Description	Symbol	Value	Units
Power-on Reset[1]	T_{POR}	2.0	ms, max
Program Latency	T_{PL}	100.0	µs, max
CCLK (output) Delay	T_{ICCK}	0.5	µs, min
		4.0	µs, max
Program Pulse Width	$T_{PROGRAM}$	300	ns, min

Notes:
1. T_{POR} delay is the initialization time required after V_{CCINT} and V_{CCO} in Bank 2 reach the recommended operating voltage.

Delaying Configuration

$\overline{\text{INIT}}$ can be held Low using an open-drain driver. An open-drain is required since $\overline{\text{INIT}}$ is a bidirectional open-drain pin that is held Low by the FPGA while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

Start-Up Sequence

The default Start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary.

One CCLK cycle later, the Global Set/Reset (GSR) and Global Write Enable (GWE) signals are released. This permits

Initialization in Verilog and Synopsys

The block SelectRAM+ structures can be initialized in Verilog for both simulation and synthesis for inclusion in the EDIF output file. The simulation of the Verilog code uses a defparam to pass the initialization. The Synopsys FPGA compiler does not presently support defparam. The initialization values instead attach as attributes to the RAM by a built-in Synopsys dc_script. The translate_off statement stops synthesis translation of the defparam statements. The following code illustrates a module that employs these techniques.

Design Examples

Creating a 32-bit Single-Port RAM

The true dual-read/write port functionality of the block SelectRAM+ memory allows a single port, 128 deep by 32-bit wide RAM to be created using a single block SelectRAM+ cell as shown in Figure 35.

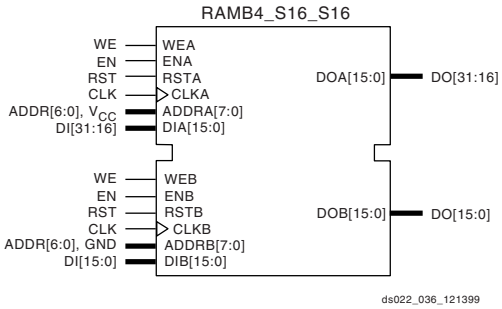

Figure 35: **Single Port 128 x 32 RAM**

Interleaving the memory space, setting the LSB of the address bus of Port A to 1 (V_{CC}), and the LSB of the address bus of Port B to 0 (GND), allows a 32-bit wide single port RAM to be created.

Creating Two Single-Port RAMs

The true dual-read/write port functionality of the block SelectRAM+ memory allows a single RAM to be split into two single port memories of 2K bits each as shown in Figure 36.

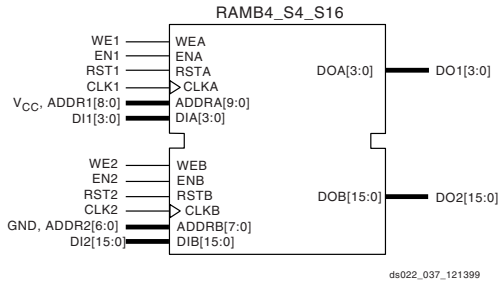

Figure 36: **512 x 4 RAM and 128 x 16 RAM**

In this example, a 512K x 4 RAM (Port A) and a 128 x 16 RAM (Port B) are created out of a single block SelectRAM+. The address space for the RAM is split by fixing the MSB of Port A to 1 (V_{CC}) for the upper 2K bits and the MSB of Port B to 0 (GND) for the lower 2K bits.

Block Memory Generation

The CoreGen program generates memory structures using the block SelectRAM+ features. This program outputs VHDL or Verilog simulation code templates and an EDIF file for inclusion in a design.

IOB Flip-Flop/Latch Property

The Virtex-E series I/O Block (IOB) includes an optional register on the input path, an optional register on the output path, and an optional register on the 3-state control pin. The design implementation software automatically takes advantage of these registers when the following option for the Map program is specified.

map –pr b <filename>

Alternatively, the IOB = TRUE property can be placed on a register to force the mapper to place the register in an IOB.

Location Constraints

Specify the location of each SelectI/O symbol with the location constraint LOC attached to the SelectI/O symbol. The external port identifier indicates the value of the location constrain. The format of the port identifier depends on the package chosen for the specific design.

The LOC properties use the following form:

LOC=A42

LOC=P37

Output Slew Rate Property

As mentioned above, a variety of symbol names provide the option of choosing the desired slew rate for the output buffers. In the case of the LVTTL output buffers (OBUF, OBUFT, and IOBUF), slew rate control can be alternatively programed with the SLEW= property. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals. The SLEW= property has one of the two following values.

SLEW=SLOW

SLEW=FAST

Output Drive Strength Property

The desired output drive strength can be additionally specified by choosing the appropriate library symbol. The Xilinx library also provides an alternative method for specifying this feature. For the LVTTL output buffers (OBUF, OBUFT, and IOBUF, the desired drive strength can be specified with the DRIVE= property. This property could have one of the following seven values.

DRIVE=2
DRIVE=4
DRIVE=6
DRIVE=8
DRIVE=12 (Default)
DRIVE=16
DRIVE=24

Design Considerations

Reference Voltage (V_{REF}) Pins

Low-voltage I/O standards with a differential amplifier input buffer require an input reference voltage (V_{REF}). Provide the V_{REF} as an external signal to the device.

The voltage reference signal is “banked” within the device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 38 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

Within each V_{REF} bank, any input buffers that require a V_{REF} signal must be of the same type. Output buffers of any type and input buffers can be placed without requiring a reference voltage within the same V_{REF} bank.

Output Drive Source Voltage (V_{CCO}) Pins

Many of the low voltage I/O standards supported by SelectI/O devices require a different output drive source voltage (V_{CCO}). As a result each device can often have to support multiple output drive source voltages.

The Virtex-E series supports eight banks for the HQ and PQ packages. The CS package supports four V_{CCO} banks.

Output buffers within a given V_{CCO} bank must share the same output drive source voltage. Input buffers for LVTTL, LVCMOS2, LVCMOS18, PCI33_3, and PCI 66_3 use the V_{CCO} voltage for Input V_{CCO} voltage.

Transmission Line Effects

The delay of an electrical signal along a wire is dominated by the rise and fall times when the signal travels a short distance. Transmission line delays vary with inductance and capacitance, but a well-designed board can experience delays of approximately 180 ps per inch.

Transmission line effects, or reflections, typically start at 1.5" for fast (1.5 ns) rise and fall times. Poor (or non-existent) termination or changes in the transmission line impedance cause these reflections and can cause additional delay in longer traces. As system speeds continue to increase, the effect of I/O delays can become a limiting factor and therefore transmission line termination becomes increasingly more important.

Termination Techniques

A variety of termination techniques reduce the impact of transmission line effects.

The following are output termination techniques:

- None
- Series
- Parallel (Shunt)
- Series and Parallel (Series-Shunt)

Virtex-E Data Sheet

The Virtex-E Data Sheet contains the following modules:

- DS022-1, Virtex-E 1.8V FPGAs:
  Introduction and Ordering Information (Module 1)
- DS022-2, Virtex-E 1.8V FPGAs:
  Functional Description (Module 2)
- DS022-3, Virtex-E 1.8V FPGAs:
  DC and Switching Characteristics (Module 3)
- DS022-4, Virtex-E 1.8V FPGAs:
  Pinout Tables (Module 4)

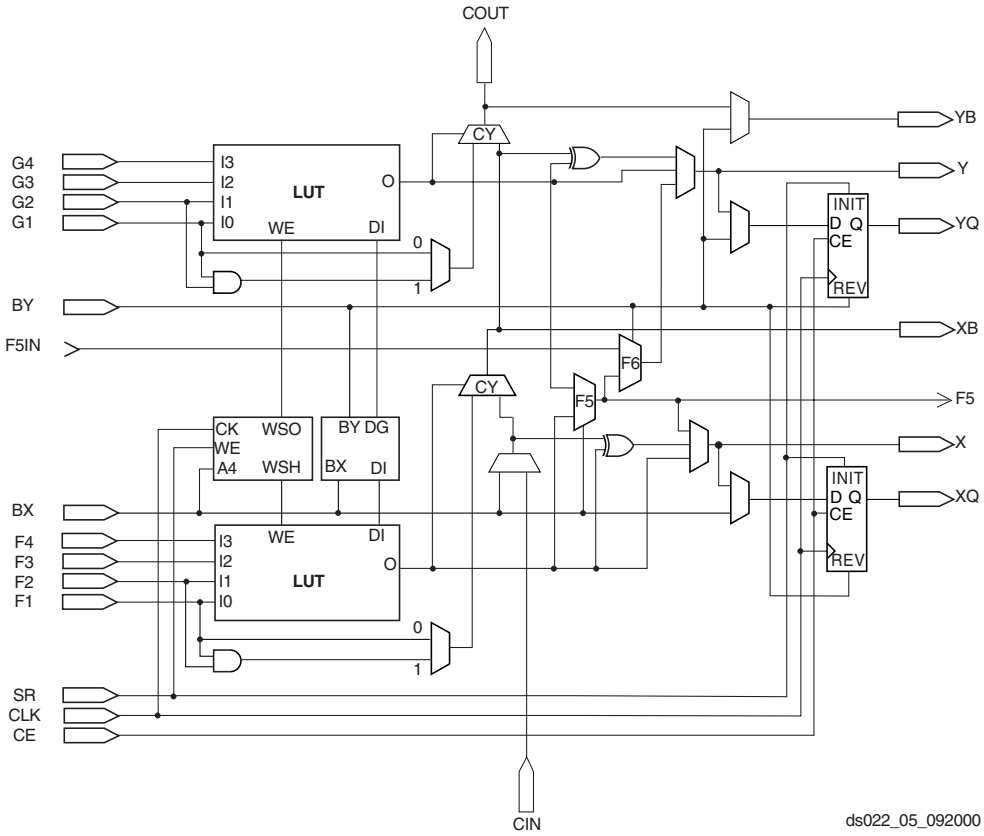

Figure 2: **Detailed View of Virtex-E Slice**

BG352 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A check (√) in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock

Table 11: **BG352 Differential Pin Pair Summary XCV100E, XCV200E, XCV300E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	AE13	AC13	NA	IO LVDS 55
1	5	AF14	AD14	NA	IO LVDS 55
2	1	B14	A13	NA	IO LVDS 9
3	0	D14	A15	NA	IO LVDS 9
IO LVDS Total Outputs: 87, Asynchronous Output Pairs: 43					
0	0	B23	D21	√	VREF_0
1	0	D20	A23	√	-
2	0	B22	C21	√	VREF_0
3	0	A21	B20	2	-
4	0	B19	C19	√	VREF_0
5	0	C18	D17	√	-
6	0	A18	C17	2	-
7	0	C16	B17	√	-
8	0	D15	A16	√	VREF_0
9	1	A13	A15	√	GCLK LVDS 3/2
10	1	A12	C13	2	-
11	1	C12	B12	√	VREF_1
12	1	B11	A11	√	-
13	1	D11	C11	2	-
14	1	C10	B9	√	-
15	1	C9	B8	√	VREF_1
16	1	A7	D9	1	-
17	1	B6	A6	√	VREF_1
18	1	A4	C7	√	-

Table 11: **BG352 Differential Pin Pair Summary XCV100E, XCV200E, XCV300E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
19	1	D6	C6	√	VREF_1
20	1	C4	D5	√	CS
21	2	E4	D3	√	DIN_D0
22	2	D2	C1	√	VREF_2
23	2	G4	F3	√	-
24	2	E2	F2	√	VREF_2
25	2	F1	J4	2	-
26	2	H2	G1	√	D1
27	2	J3	J2	√	D2
28	2	J1	L4	1	-
29	2	L3	L2	√	-
30	2	M4	M3	√	D3
31	2	M2	M1	2	-
32	2	N4	N2	√	-
33	3	R1	R2	2	-
34	3	R3	R4	√	VREF_3
35	3	T2	U2	√	-
36	3	T4	V1	1	-
37	3	U3	U4	√	D5
38	3	V3	V4	√	VREF_3
39	3	Y1	Y2	1	-
40	3	AA2	Y3	√	VREF_3
41	3	AC1	AB2	√	-
42	3	AA4	AC2	√	VREF_3
43	3	AC3	AD2	√	INIT
44	4	AC5	AD4	√	-
45	4	AE4	AF3	√	VREF_4
46	4	AC7	AD6	√	-
47	4	AE5	AE6	√	VREF_4
48	4	AF6	AC9	2	-
49	4	AE8	AF7	√	VREF_4
50	4	AD9	AE9	√	-
51	4	AF9	AC11	2	-
52	4	AD11	AE11	√	-
53	4	AC12	AD12	√	VREF_4
54	4	AE12	AF12	2	-

Table 12: **BG432 — XCV300E, XCV400E, XCV600E**

Bank	Pin Description	Pin #
0	IO_L12N_YY	A20
0	IO_L12P_YY	D19
0	IO_VREF_L13N_YY	B19
0	IO_L13P_YY	A19
0	IO_L14N_Y	B18
0	IO_L14P_Y	D18
0	IO_VREF_L15N_Y	C18[2]
0	IO_L15P_Y	B17
0	IO_LVDS_DLL_L16N	C17
1	GCK2	A16
1	IO	A12
1	IO	B9
1	IO	B11
1	IO	C16
1	IO	D9
1	IO_LVDS_DLL_L16P	B16
1	IO_L17N_Y	A15
1	IO_VREF_L17P_Y	B15[2]
1	IO_L18N_Y	C15
1	IO_L18P_Y	D15
1	IO_L19N_YY	B14
1	IO_VREF_L19P_YY	A13
1	IO_L20N_YY	B13
1	IO_L20P_YY	D14
1	IO_L21N_YY	C13
1	IO_L21P_YY	B12
1	IO_L22N_YY	D13
1	IO_L22P_YY	C12
1	IO_L23N_YY	D12
1	IO_L23P_YY	C11
1	IO_L24N_YY	B10
1	IO_VREF_L24P_YY	C10
1	IO_L25N_Y	C9
1	IO_VREF_L25P_Y	D10[1]
1	IO_L26N_Y	A8

Table 12: **BG432 — XCV300E, XCV400E, XCV600E**

Bank	Pin Description	Pin #
1	IO_L26P_Y	B8
1	IO_L27N_YY	C8
1	IO_VREF_L27P_YY	B7
1	IO_L28N_YY	D8
1	IO_L28P_YY	A6
1	IO_L29N_Y	B6
1	IO_L29P_Y	D7
1	IO_L30N_YY	A5
1	IO_VREF_L30P_YY	C6
1	IO_L31N_YY	B5
1	IO_L31P_YY	D6
1	IO_L32N_Y	A4
1	IO_L32P_Y	C5
1	IO_WRITE_L33N_YY	B4
1	IO_CS_L33P_YY	D5
2	IO	H4
2	IO	J3
2	IO	L3
2	IO	M1
2	IO	R2
2	IO_DOUT_BUSY_L34P_YY	D3
2	IO_DIN_D0_L34N_YY	C2
2	IO_L35P	D2
2	IO_L35N	E4
2	IO_L36P_Y	D1
2	IO_L36N_Y	E3
2	IO_VREF_L37P_Y	E2
2	IO_L37N_Y	F4
2	IO_L38P	E1
2	IO_L38N	F3
2	IO_L39P_Y	F2
2	IO_L39N_Y	G4
2	IO_VREF_L40P_YY	G3
2	IO_L40N_YY	G2
2	IO_L41P_Y	H3

Table 15: **BG560 Differential Pin Pair Summary XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
171	7	J33	M29	√	-
172	7	K31	L30	√	VREF
173	7	H33	L29	4	-
174	7	H32	J31	18	VREF
175	7	H31	K29	14	-
176	7	G32	J30	20	VREF
177	7	G31	J29	√	VREF
178	7	E32	E33	15	-
179	7	F31	H29	14	-
180	7	E31	D32	15	VREF
181	7	C33	G29	14	-
182	7	D31	F30	14	VREF

Notes:
1. AO in the XCV1600E.
2. AO in the XCV2000E.
3. AO in the XCV1600E, 2000E.
4. AO in the XCV1000E, 1600E.
5. AO in the XCV1000E, 2000E.
6. AO in the XCV1000E.
7. AO in the XCV1000E, 1600E, 2000E.
8. AO in the XCV600E, 1600E.
9. AO in the XCV400E, 600E, 1600E.
10. AO in the XCV400E, 600E, 1000E, 2000E.
11. AO in the XCV400E, 600E, 1000E.
12. AO in the XCV400E, 1000E, 2000E.
13. AO in the XCV400E, 600E, 1000E, 1600E.
14. AO in the XCV400E, 1000E, 1600E.
15. AO in the XCV600E, 1000E, 2000E.
16. AO in the XCV600E, 2000E.
17. AO in the XCV400E, 600E, 1600E, 2000E.
18. AO in the XCV600E, 1000E, 1600E, 2000E.
19. AO in the XCV400E, 600E, 2000E.
20. AO in the XCV400E, 1000E.

FG256 Fine-Pitch Ball Grid Array Packages

XCV50E, XCV100E, XCV200E, and XCV300E devices in FG256 fine-pitch Ball Grid Array packages have footprint compatibility. Pins labeled I0_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 16, see Table 17 for Differential Pair information.

Table 16: **FG256 Package — XCV50E, XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
0	GCK3	B8
0	IO	B3
0	IO	E7
0	IO	D8
0	IO_L0N_Y	C5
0	IO_VREF_L0P_Y	A3[2]
0	IO_L1N_YY	D5
0	IO_L1P_YY	E6
0	IO_VREF_L2N_YY	B4
0	IO_L2P_YY	A4
0	IO_L3N_Y	D6
0	IO_L3P_Y	B5
0	IO_VREF_L4N_YY	C6[1]
0	IO_L4P_YY	A5
0	IO_L5N_YY	B6
0	IO_L5P_YY	C7
0	IO_L6N_Y	D7
0	IO_L6P_Y	C8
0	IO_VREF_L7N_Y	B7
0	IO_L7P_Y	A6
0	IO_LVDS_DLL_L8N	A7
1	GCK2	C9
1	IO	B10
1	IO_LVDS_DLL_L8P	A8
1	IO_L9N_Y	D9
1	IO_L9P_Y	A9
1	IO_L10N_Y	E10
1	IO_VREF_L10P_Y	B9

Table 16: **FG256 Package — XCV50E, XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
NA	GND	K11
NA	GND	K10
NA	GND	K9
NA	GND	K8
NA	GND	K7
NA	GND	K6
NA	GND	J10
NA	GND	J9
NA	GND	J8
NA	GND	J7
NA	GND	H10
NA	GND	H9
NA	GND	H8
NA	GND	H7
NA	GND	G11
NA	GND	G10
NA	GND	G9
NA	GND	G8
NA	GND	G7
NA	GND	G6
NA	GND	F11
NA	GND	F10
NA	GND	F7
NA	GND	F6
NA	GND	B15
NA	GND	B2
NA	GND	A16
NA	GND	A1

Notes:
1. V_{REF} or I/O option only in the XCV100E, 200E, 300E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV200E, 300E; otherwise, I/O option only.

FG256 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 17: **FG256 Differential Pin Pair Summary XCV50E, XCV100E, XCV200E, XCV300E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	N8	N9	NA	IO_DLL_L52P
1	5	R8	T8	NA	IO_DLL_L52N
2	1	C9	A8	NA	IO_DLL_L8P
3	0	B8	A7	NA	IO_DLL_L8N
IO LVDS Total Pairs: 83, Asynchronous Outputs: 35					
0	0	A3	C5	7	VREF
1	0	E6	D5	√	-
2	0	A4	B4	√	VREF
3	0	B5	D6	2	-
4	0	A5	C6	√	VREF
5	0	C7	B6	√	-
6	0	C8	D7	1	-
7	0	A6	B7	1	VREF
8	1	A8	A7	NA	IO_LVDS_DLL
9	1	A9	D9	2	-
10	1	B9	E10	1	VREF
11	1	D10	A10	1	-
12	1	A11	C10	√	-
13	1	E11	B11	√	VREF
14	1	D11	A12	2	-
15	1	C11	A13	√	VREF
16	1	D12	B12	√	-
17	1	C12	A14	7	VREF
18	1	B13	C13	√	CS

Table 17: **FG256 Differential Pin Pair Summary XCV50E, XCV100E, XCV200E, XCV300E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
19	2	C15	D14	√	DIN, D0
20	2	B16	E13	6	VREF
21	2	C16	E14	√	-
22	2	F13	E15	1	VREF
23	2	F12	D16	5	-
24	2	F14	E16	3	D1
25	2	F15	G13	√	D2
26	2	F16	G12	6	-
27	2	G15	G14	√	-
28	2	H13	G16	3	D3
29	2	J13	H15	4	-
30	2	H14	H16	√	-
31	3	K15	J14	4	-
32	3	J16	K16	3	VREF
33	3	K12	L15	√	-
34	3	K13	L16	6	-
35	3	K14	M16	√	D5
36	3	N16	L13	3	VREF
37	3	P16	L12	5	-
38	3	M15	L14	1	VREF
39	3	M14	R16	√	-
40	3	M13	T15	6	VREF
41	3	N14	N15	√	INIT
42	4	T14	P13	√	-
43	4	P12	R13	7	VREF
44	4	N12	T13	√	-
45	4	T12	P11	√	VREF
46	4	R12	N11	2	-
47	4	T11	M11	√	VREF
48	4	R11	T10	√	-
49	4	R10	M10	1	-
50	4	P9	T9	1	VREF
51	4	N10	R9	1	-
52	5	N9	T8	NA	IO_LVDS_DLL
53	5	R7	P8	1	VREF
54	5	P7	T6	1	-

Table 17: **FG256 Differential Pin Pair Summary XCV50E, XCV100E, XCV200E, XCV300E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
55	5	M7	R6	√	-
56	5	P6	R5	√	VREF
57	5	N6	T5	2	-
58	5	M6	T4	√	VREF
59	5	T3	P5	√	-
60	5	T2	N5	7	VREF
61	6	R1	M3	√	-
62	6	N2	M4	6	VREF
63	6	P1	L5	√	-
64	6	L3	N1	1	VREF
65	6	L4	M2	5	-
66	6	K4	M1	3	VREF
67	6	L1	L2	√	-
68	6	K1	K3	6	-
69	6	K5	K2	√	-
70	6	J1	J3	3	VREF
71	6	H1	J4	4	-
72	7	H4	G1	√	-
73	7	H2	G5	4	-
74	7	H3	G4	3	VREF
75	7	F5	G2	√	-
76	7	F1	F4	6	-
77	7	F2	G3	√	-
78	7	D1	E1	3	VREF
79	7	E2	E4	5	-
80	7	C1	F3	1	VREF
81	7	E3	D2	√	-
82	7	A2	B1	6	VREF

Notes:
1. AO in the XCV50E, 200E, 300E.
2. AO in the XCV50E, 200E.
3. AO in the XCV50E, 300E.
4. AO in the XCV100E, 200E.
5. AO in the XCV200E.
6. AO in the XCV100E.
7. AO in the XCV50E.

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
7	IO	J1
7	IO	J4
7	IO	L2[1]
7	IO_L104N_YY	L3
7	IO_L104P_YY	L4
7	IO_L105N_YY	L5
7	IO_L105P_YY	L1
7	IO_L106N_Y	L6
7	IO_L106P_Y	K2
7	IO_L107N_Y	K4
7	IO_VREF_L107P_Y	K3
7	IO_L108N_YY	K1
7	IO_L108P_YY	K5
7	IO_L109N_YY	J3
7	IO_L109P_YY	J2
7	IO_L110N_YY	J5
7	IO_L110P_YY	H1
7	IO_L111N_YY	H2
7	IO_L111P_YY	H3
7	IO_L112N_Y	G1
7	IO_VREF_L112P_Y	H4
7	IO_L113N_Y	F1
7	IO_L113P_Y	F2
7	IO_L114N_YY	H5
7	IO_L114P_YY	G3
7	IO_L115N_YY	E1
7	IO_VREF_L115P_YY	E2
7	IO_L116N_YY	F3
7	IO_L116P_YY	G5
7	IO_L117N_YY	E3
7	IO_VREF_L117P_YY	D2
7	IO_L118N_YY	F5
7	IO_L118P_YY	C1
2	CCLK	B22
3	DONE	Y19
NA	DXN	Y5

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
NA	DXP	V6
NA	M0	AB2
NA	M1	U5
NA	M2	Y4
NA	PROGRAM	W20
NA	TCK	C4
NA	TDI	B20
2	TDO	A21
NA	TMS	D3
NA	NC	W19
NA	NC	W4
NA	NC	D19
NA	NC	D4
NA	VCCINT	E5
NA	VCCINT	E18
NA	VCCINT	F6
NA	VCCINT	F17
NA	VCCINT	G7
NA	VCCINT	G8
NA	VCCINT	G9
NA	VCCINT	G14
NA	VCCINT	G15
NA	VCCINT	H7
NA	VCCINT	G16
NA	VCCINT	H16
NA	VCCINT	J7
NA	VCCINT	J16
NA	VCCINT	P7
NA	VCCINT	P16
NA	VCCINT	R7
NA	VCCINT	R16
NA	VCCINT	T7
NA	VCCINT	T8
NA	VCCINT	T9
NA	VCCINT	T14

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
NA	GND	D20
NA	GND	D12
NA	GND	C39
NA	GND	C37
NA	GND	C3
NA	GND	C20
NA	GND	C1
NA	GND	B39
NA	GND	B38
NA	GND	B2
NA	GND	B1
NA	GND	AW39
NA	GND	AW38
NA	GND	AW37
NA	GND	AW3
NA	GND	AW2
NA	GND	AW1
NA	GND	AV39
NA	GND	AV38
NA	GND	AV2
NA	GND	AV1
NA	GND	AU39
NA	GND	AU37
NA	GND	AU3
NA	GND	AU20
NA	GND	AU1
NA	GND	AT4
NA	GND	AT36
NA	GND	AT28
NA	GND	AT20
NA	GND	AT12
NA	GND	AR5
NA	GND	AR35
NA	GND	AR28
NA	GND	AR21
NA	GND	AR20

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
NA	GND	AR19
NA	GND	AR12
NA	GND	AH5
NA	GND	AH4
NA	GND	AH36
NA	GND	AH35
NA	GND	AA5
NA	GND	AA35
NA	GND	A39
NA	GND	A38
NA	GND	A37
NA	GND	A3
NA	GND	A2
NA	GND	A1

Notes:
1. V_{REF} or I/O option only in the XCV1000E, 1600E, 2000E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV1600E, 2000E; otherwise, I/O option only.
3. V_{REF} or I/O option only in the XCV2000E; otherwise, I/O option only.

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
7	IO_L275N_Y	G38
7	IO_VREF_L275P_Y	G42
7	IO_L276N_Y	G41
7	IO_L276P_Y	F40
7	IO_L277N	F42
7	IO_L277P	F41
7	IO_L278N_Y	F39
7	IO_VREF_L278P_Y	E42
7	IO_L279N_Y	E40
7	IO_L279P_Y	E41
7	IO_L280N_Y	E39
7	IO_L280P_Y	D41
2	CCLK	B4
3	DONE	AW2
NA	DXN	BA38
NA	DXP	AW38
NA	M0	AW41
NA	M1	AV37
NA	M2	BA39
NA	PROGRAM	AV2
NA	TCK	B38
NA	TDI	B5
2	TDO	D5
NA	TMS	B39
NA	VCCINT	F9
NA	VCCINT	F10
NA	VCCINT	F17
NA	VCCINT	F18
NA	VCCINT	F25
NA	VCCINT	F26
NA	VCCINT	F33
NA	VCCINT	F34
NA	VCCINT	J6
NA	VCCINT	J37
NA	VCCINT	K6

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
NA	VCCINT	K37
NA	VCCINT	T6
NA	VCCINT	T37
NA	VCCINT	U6
NA	VCCINT	U37
NA	VCCINT	V6
NA	VCCINT	V37
NA	VCCINT	AE6
NA	VCCINT	AE37
NA	VCCINT	AF6
NA	VCCINT	AF37
NA	VCCINT	AG6
NA	VCCINT	AG37
NA	VCCINT	AN6
NA	VCCINT	AN37
NA	VCCINT	AP6
NA	VCCINT	AP37
NA	VCCINT	AU9
NA	VCCINT	AU10
NA	VCCINT	AU17
NA	VCCINT	AU18
NA	VCCINT	AU25
NA	VCCINT	AU26
NA	VCCINT	AU33
NA	VCCINT	AU34
NA	VCCO_0	F23
NA	VCCO_0	F24
NA	VCCO_0	F28
NA	VCCO_0	F29
NA	VCCO_0	F31
NA	VCCO_0	F32
NA	VCCO_0	F35
NA	VCCO_0	F36
NA	VCCO_1	F11
NA	VCCO_1	F12
NA	VCCO_1	F14

FG860 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 25: **FG860 Differential Pin Pair Summary XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
3	0	C22	A22	NA	IO_DLL_L34N
2	1	B22	D22	NA	IO_DLL_L34P
1	5	AY22	AW21	NA	IO_DLL_L176N
0	4	BA22	AW20	NA	IO_DLL_L176P
IO LVDS Total Pairs: 281, Asynchronous Output Pairs: 111					
0	0	D38	A38	2	-
1	0	E37	B37	1	-
2	0	C39	A37	1	VREF
3	0	C38	B36	1	-
4	0	B35	A36	√	-
5	0	D37	A35	√	VREF
6	0	A34	C37	5	-
7	0	B33	E36	5	-
8	0	C32	A33	√	-
9	0	B32	C36	√	VREF
10	0	D35	A32	1	-
11	0	C35	C31	1	VREF
12	0	A31	E34	√	-
13	0	C30	D34	√	VREF
14	0	E33	B30	2	-
15	0	D33	A30	2	-
16	0	B29	C33	√	VREF
17	0	A29	E32	√	-

Table 25: **FG860 Differential Pin Pair Summary XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
18	0	C28	D32	2	-
19	0	B28	E31	1	-
20	0	A28	D31	1	-
21	0	C27	D30	5	-
22	0	B27	E29	√	-
23	0	A27	D29	√	VREF
24	0	D28	C26	5	-
25	0	F27	B26	5	-
26	0	C25	E27	√	-
27	0	B25	D27	√	VREF
28	0	D26	A25	1	-
29	0	E25	A24	1	-
30	0	B24	D25	√	-
31	0	A23	E24	√	VREF
32	0	E23	C23	2	-
33	0	D23	B23	2	VREF
34	1	D22	A22	NA	IO_LVDS_DLL
35	1	B21	D21	2	VREF
36	1	A21	D20	2	-
37	1	D19	C20	√	VREF
38	1	E19	B20	√	-
39	1	A19	D18	1	-
40	1	C19	E18	1	-
41	1	E17	B19	√	VREF
42	1	D16	A18	√	-
43	1	B18	E16	5	-
44	1	A17	F16	5	-
45	1	E15	C17	√	VREF
46	1	D14	B17	√	-
47	1	E14	A16	5	-
48	1	D13	C16	1	-
49	1	D12	B16	1	-
50	1	E12	A15	2	-
51	1	C11	C15	√	-

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
NA	VCCO_0	C12
NA	VCCO_1	B25
NA	VCCO_1	C19
NA	VCCO_1	M18
NA	VCCO_1	M17
NA	VCCO_1	L17
NA	VCCO_1	H17
NA	VCCO_1	L16
NA	VCCO_1	M16
NA	VCCO_2	F29
NA	VCCO_2	M28
NA	VCCO_2	P23
NA	VCCO_2	R20
NA	VCCO_2	P20
NA	VCCO_2	R19
NA	VCCO_2	N19
NA	VCCO_2	P19
NA	VCCO_3	AE29
NA	VCCO_3	W28
NA	VCCO_3	U23
NA	VCCO_3	U20
NA	VCCO_3	T20
NA	VCCO_3	V19
NA	VCCO_3	T19
NA	VCCO_3	U19
NA	VCCO_4	AJ25
NA	VCCO_4	AH19
NA	VCCO_4	W18
NA	VCCO_4	AC17
NA	VCCO_4	Y17
NA	VCCO_4	W17
NA	VCCO_4	W16
NA	VCCO_4	Y16
NA	VCCO_5	AJ6
NA	VCCO_5	Y15
NA	VCCO_5	W15
NA	VCCO_5	AC14

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
NA	VCCO_5	Y14
NA	VCCO_5	W14
NA	VCCO_5	W13
NA	VCCO_5	AH12
NA	VCCO_6	AE2
NA	VCCO_6	V12
NA	VCCO_6	U12
NA	VCCO_6	T12
NA	VCCO_6	U11
NA	VCCO_6	T11
NA	VCCO_6	U8
NA	VCCO_6	W3
NA	VCCO_7	F2
NA	VCCO_7	R12
NA	VCCO_7	P12
NA	VCCO_7	N12
NA	VCCO_7	R11
NA	VCCO_7	P11
NA	VCCO_7	P8
NA	VCCO_7	M3
NA	GND	Y18
NA	GND	AH7
NA	GND	AK30
NA	GND	AJ30
NA	GND	B30
NA	GND	A30
NA	GND	AK29
NA	GND	AJ29
NA	GND	AC29
NA	GND	H29
NA	GND	B29
NA	GND	A29
NA	GND	AH28
NA	GND	V28
NA	GND	N28
NA	GND	C28

Table 27: **FG900 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
188	5	AA12	AJ12	√	VREF
189	5	AB12	AE11	√	-
190	5	AK12	Y13	2	-
191	5	AG11	AF11	2	-
192	5	AH11	AJ11	2	-
193	5	AE12	AG10	4	-
194	5	AD12	AK11	√	-
195	5	AJ10	AC12	√	VREF
196	5	AK10	AD11	4	-
197	5	AJ9	AE9	4	-
198	5	AH10	AF9	√	VREF
199	5	AH9	AK9	√	-
200	5	AF8	AB11	2	-
201	5	AC11	AG8	2	-
202	5	AK8	AF7	√	VREF
203	5	AG7	AK7	√	-
204	5	AJ7	AD10	1	-
205	5	AH6	AC10	1	-
206	5	AD9	AG6	√	VREF
207	5	AB10	AJ5	√	-
208	5	AD8	AK5	2	-
209	5	AC9	AJ4	2	VREF
210	5	AG5	AK4	2	-
211	5	AH5	AG3	4	-
212	6	AC6	AF3	√	-
213	6	AG2	AH2	NA	-
214	6	AE4	AB9	1	-
215	6	AH1	AE3	4	VREF
216	6	AD6	AB8	3	-
217	6	AA10	AG1	4	-
218	6	AD4	AA9	1	VREF
219	6	AD2	AD5	√	-
220	6	AF2	AD3	4	-
221	6	AA7	AA8	1	-

Table 27: **FG900 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
222	6	Y9	AF1	√	VREF
223	6	AC4	AB6	√	-
224	6	W8	AE1	2	-
225	6	AB4	Y8	4	-
226	6	W9	AB3	4	VREF
227	6	W10	AA5	4	-
228	6	V10	AB1	4	-
229	6	AC1	Y7	4	VREF
230	6	AA3	V11	NA	-
231	6	U10	AA2	4	-
232	6	AA6	W7	1	-
233	6	Y4	Y6	4	-
234	6	V7	AA1	3	-
235	6	Y2	Y3	4	-
236	6	W5	Y5	1	VREF
237	6	W6	W4	√	-
238	6	W2	V6	4	-
239	6	V4	U9	1	-
240	6	T8	AB2	√	VREF
241	6	W1	U5	√	-
242	6	T9	Y1	2	-
243	6	U3	T7	4	-
244	6	V2	T5	4	VREF
245	6	T6	R9	4	-
246	6	U2	T4	4	VREF
247	7	R10	T1	NA	
248	7	R6	R5	4	-
249	7	R4	R8	4	VREF
250	7	R3	R7	4	-
251	7	P6	P10	4	VREF
252	7	P2	P5	4	-
253	7	P4	P7	2	-
254	7	R2	N4	√	-
255	7	P1	N7	√	VREF

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
2	IO_L126N_YY	T32
2	IO_VREF_L127P_Y	U29[1]
2	IO_L127N_Y	U33
2	IO_L128P_YY	V33
2	IO_L128N_YY	U31
3	IO	V27[3]
3	IO	V31
3	IO	V32[3]
3	IO	W33
3	IO	AB25[3]
3	IO	AB26[3]
3	IO	AB31[3]
3	IO	AC31[3]
3	IO	AF34
3	IO	AG31[3]
3	IO	AG33[3]
3	IO	AG34
3	IO	AH29[3]
3	IO	AJ30[3]
3	IO_L129P_Y	V26
3	IO_VREF_L129N_Y	V30[1]
3	IO_L130P_YY	W34
3	IO_L130N_YY	V28
3	IO_L131P_YY	W32
3	IO_VREF_L131N_YY	W30
3	IO_L132P_Y	V29
3	IO_L132N_Y	Y34
3	IO_L133P	W29[5]
3	IO_L133N	Y33[4]
3	IO_L134P_Y	W26
3	IO_L134N_Y	W28
3	IO_L135P_YY	Y31
3	IO_L135N_YY	Y30

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
3	IO_L136P_YY	AA34[5]
3	IO_L136N_YY	W31[4]
3	IO_D4_L137P_YY	AA33
3	IO_VREF_L137N_YY	Y29
3	IO_L138P_Y	W25
3	IO_L138N_Y	AB34
3	IO_L139P_Y	Y28[5]
3	IO_L139N_Y	AB33[4]
3	IO_L140P_Y	AA30
3	IO_L140N_Y	Y26
3	IO_L141P_YY	Y27
3	IO_L141N_YY	AA31
3	IO_L142P_YY	AA27[5]
3	IO_L142N_YY	AA29[4]
3	IO_L143P_Y	AB32
3	IO_VREF_L143N_Y	AB29
3	IO_L144P_Y	AA28
3	IO_L144N_Y	AC34
3	IO_L145P	Y25
3	IO_L145N	AD34
3	IO_L146P_Y	AB30
3	IO_L146N_Y	AC33
3	IO_L147P_Y	AA26
3	IO_L147N_Y	AC32
3	IO_L148P_Y	AD33
3	IO_L148N_Y	AB28
3	IO_L149P_YY	AE34
3	IO_D5_L149N_YY	AB27
3	IO_D6_L150P_YY	AE33
3	IO_VREF_L150N_YY	AC30
3	IO_L151P_Y	AA25
3	IO_L151N_Y	AE32
3	IO_L152P_YY	AE31
3	IO_L152N_YY	AD29

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
5	IO_L239P_Y	AP9
5	IO_L239N_Y	AK11
5	IO_L240P_YY	AL11
5	IO_VREF_L240N_YY	AL10
5	IO_L241P_YY	AE13
5	IO_L241N_YY	AM9
5	IO_L242P	AF12[5]
5	IO_L242N	AP8[4]
5	IO_L243P_Y	AL9
5	IO_VREF_L243N_Y	AH11[2]
5	IO_L244P_Y	AF11
5	IO_L244N_Y	AN8
5	IO_L245P_Y	AM8[5]
5	IO_L245N_Y	AG11[4]
5	IO_L246P_YY	AL8
5	IO_VREF_L246N_YY	AK9
5	IO_L247P_YY	AH10
5	IO_L247N_YY	AN7
5	IO_L248P	AE12[5]
5	IO_L248N	AJ9[4]
5	IO_L249P_Y	AM7
5	IO_L249N_Y	AL7
5	IO_L250P_Y	AG10
5	IO_L250N_Y	AN6
5	IO_L251P_YY	AK8[5]
5	IO_L251N_YY	AH9[4]
5	IO_L252P_YY	AP5
5	IO_VREF_L252N_YY	AJ8
5	IO_L253P_YY	AE11
5	IO_L253N_YY	AN5
5	IO_L254P_Y	AF10
5	IO_L254N_Y	AM6
5	IO_L255P_Y	AL6
5	IO_VREF_L255N_Y	AG9

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
5	IO_L256P_Y	AH8
5	IO_L256N_Y	AP4
5	IO_L257P_Y	AN4
5	IO_L257N_Y	AJ7
5	IO_L258P_YY	AM5
5	IO_L258N_YY	AK6
6	IO	T1
6	IO	V2
6	IO	V3
6	IO	V5[3]
6	IO	V8[3]
6	IO	AA10[3]
6	IO	AB5[3]
6	IO	AB7[3]
6	IO	AB9[3]
6	IO	AD7[3]
6	IO	AD8[3]
6	IO	AE2
6	IO	AE4
6	IO	AJ4[3]
6	IO	AH5[3]
6	IO_L259N_YY	AH6
6	IO_L259P_YY	AF8
6	IO_L260N_Y	AE9
6	IO_L260P_Y	AK3
6	IO_L261N_Y	AD10
6	IO_L261P_Y	AL2
6	IO_VREF_L262N_Y	AL1
6	IO_L262P_Y	AH4
6	IO_L263N	AG6
6	IO_L263P	AK1
6	IO_L264N_Y	AF7
6	IO_L264P_Y	AK2