AMD Xilinx - XCV1600E-6FG680I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	7776
Number of Logic Elements/Cells	34992
Total RAM Bits	589824
Number of I/O	512
Number of Gates	2188742
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	680-LBGA Exposed Pad
Supplier Device Package	680-FTEBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv1600e-6fg680i

Table 1: **Supported I/O Standards**

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Board Termination Voltage (V_{TT})
LVTTL	3.3	3.3	N/A	N/A
LVCMOS2	2.5	2.5	N/A	N/A
LVCMOS18	1.8	1.8	N/A	N/A
SSTL3 I & II	3.3	N/A	1.50	1.50
SSTL2 I & II	2.5	N/A	1.25	1.25
GTL	N/A	N/A	0.80	1.20
GTL+	N/A	N/A	1.0	1.50
HSTL I	1.5	N/A	0.75	0.75
HSTL III & IV	1.5	N/A	0.90	1.50
CTT	3.3	N/A	1.50	1.50
AGP-2X	3.3	N/A	1.32	N/A
PCI33_3	3.3	3.3	N/A	N/A
PCI66_3	3.3	3.3	N/A	N/A
BLVDS & LVDS	2.5	N/A	N/A	N/A
LVPECL	3.3	N/A	N/A	N/A

In addition to the CLK and CE control signals, the three flip-flops share a Set/Reset (SR). For each flip-flop, this signal can be independently configured as a synchronous Set, a synchronous Reset, an asynchronous Preset, or an asynchronous Clear.

The output buffer and all of the IOB control signals have independent polarity controls.

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. After configuration, clamping diodes are connected to V_{CCO} with the exception of LVCMOS18, LVCMOS25, GTL, GTL+, LVDS, and LVPECL.

Optional pull-up, pull-down and weak-keeper circuits are attached to each pad. Prior to configuration all outputs not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive, but I/Os can optionally be pulled up.

The activation of pull-up resistors prior to configuration is controlled on a global basis by the configuration mode pins. If the pull-up resistors are not activated, all the pins are in a high-impedance state. Consequently, external pull-up or pull-down resistors must be provided on pins required to be at a well-defined logic level prior to configuration.

All Virtex-E IOBs support IEEE 1149.1-compatible Boundary Scan testing.

Input Path

The Virtex-E IOB input path routes the input signal directly to internal logic and/ or through an optional input flip-flop.

An optional delay element at the D-input of this flip-flop eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the FPGA, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signalling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF}. The need to supply V_{REF} imposes constraints on which standards can be used in close proximity to each other. See **I/O Banking**.

There are optional pull-up and pull-down resistors at each user I/O input for use after configuration. Their value is in the range 50 – 100 kΩ.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output signal can be routed to the buffer directly from the internal logic or through an optional IOB output flip-flop.

The 3-state control of the output can also be routed directly from the internal logic or through a flip-flip that provides synchronous enable and disable.

Each output driver can be individually programmed for a wide range of low-voltage signalling standards. Each output buffer can source up to 24 mA and sink up to 48 mA. Drive strength and slew rate controls minimize bus transients.

In most signalling standards, the output High voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in close proximity to each other. See **I/O Banking**.

An optional weak-keeper circuit is connected to each output. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low to match the input signal. If the pin is connected to a multiple-source signal, the weak keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way eliminates bus chatter.

Since the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate V_{REF} voltage must be provided if the signalling standard requires one. The provision of this voltage must comply with the I/O banking rules.

I/O Banking

Some of the I/O standards described above require V_{CCO} and/or V_{REF} voltages. These voltages are externally supplied and connected to device pins that serve groups of IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Data Registers

The primary data register is the Boundary Scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out, and 3-State Control. Non-IOB pins have appropriate partial bit population if input-only or output-only. Each EXTEST CAPTURED-OR state captures all In, Out, and 3-state pins.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream Boundary Scan device.

The FPGA supports up to two additional internal scan chains that can be specified using the BSCAN macro. The macro provides two user pins (SEL1 and SEL2) which are decodes of the USER1 and USER2 instructions respectively. For these instructions, two corresponding pins (T DO1 and TDO2) allow user scan data to be shifted out of TDO.

Likewise, there are individual clock pins (DRCK1 and DRCK2) for each user register. There is a common input pin (TDI) and shared output pins that represent the state of the TAP controller (RESET, SHIFT, and UPDATE).

Bit Sequence

The order within each IOB is: In, Out, 3-State. The input-only pins contribute only the In bit to the Boundary Scan I/O data register, while the output-only pins contributes all three bits.

From a cavity-up view of the chip (as shown in EPIC), starting in the upper right chip corner, the Boundary Scan data-register bits are ordered as shown in Figure 12.

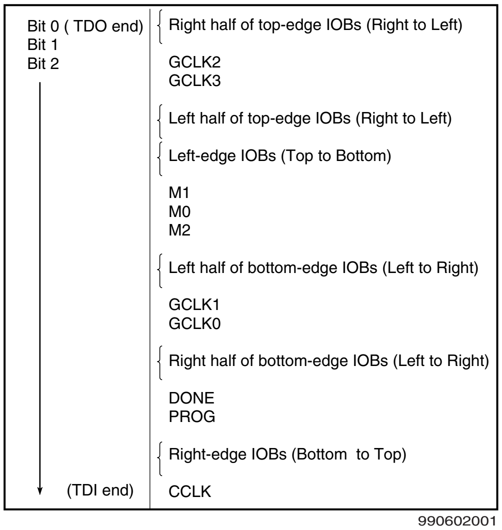

Figure 12: **Boundary Scan Bit Sequence**

BSDL (Boundary Scan Description Language) files for Virtex-E Series devices are available on the Xilinx web site in the File Download area.

Identification Registers

The IDCODE register is supported. By using the IDCODE, the device connected to the JTAG port can be determined.

The IDCODE register has the following binary format:

vvvv:ffff:fffa:aaaa:aaaa:cccc:cccc:ccc1

where

v = the die version number

f = the family code (05 for Virtex-E family)

a = the number of CLB rows (ranges from 16 for

XCV50E to 104 for XCV3200E)

c = the company code (49h for Xilinx)

The USERCODE register is supported. By using the USERCODE, a user-programmable identification code can be loaded and shifted out for examination. The identification code (see Table 7) is embedded in the bitstream during bitstream generation and is valid only after configuration.

Table 7: **IDCODEs Assigned to Virtex-E FPGAs**

FPGA	IDCODE
XCV50E	v0A10093h
XCV100E	v0A14093h
XCV200E	v0A1C093h
XCV300E	v0A20093h
XCV400E	v0A28093h
XCV600E	v0A30093h
XCV1000E	v0A40093h
XCV1600E	v0A48093h
XCV2000E	v0A50093h
XCV2600E	v0A5C093h
XCV3200E	v0A68093h

Note:

Attempting to load an incorrect bitstream causes configuration to fail and can damage the device.

Including Boundary Scan in a Design

Since the Boundary Scan pins are dedicated, no special element needs to be added to the design unless an internal data register (USER1 or USER2) is desired.

If an internal data register is used, insert the Boundary Scan symbol and connect the necessary pins as appropriate.

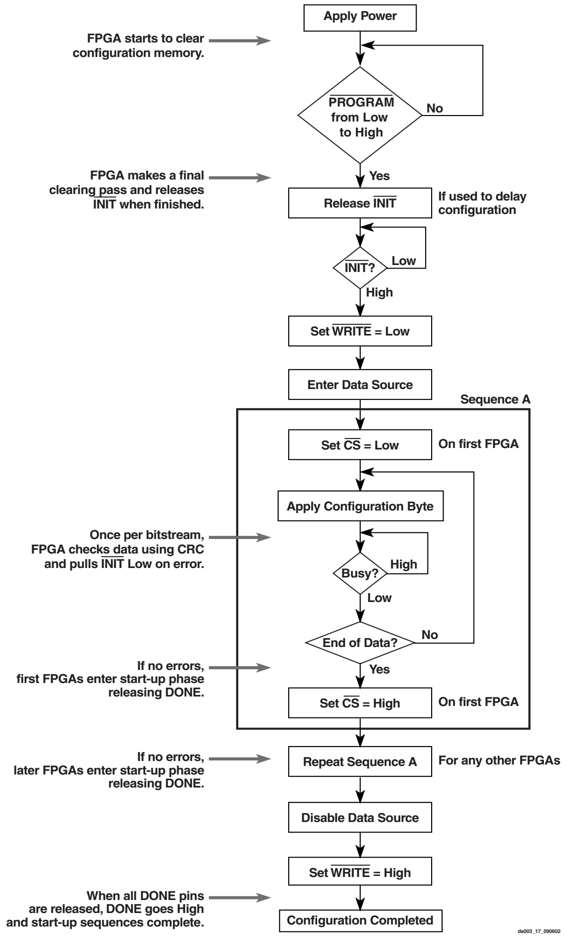

Figure 18: **SelectMAP Flowchart for Write Operations**

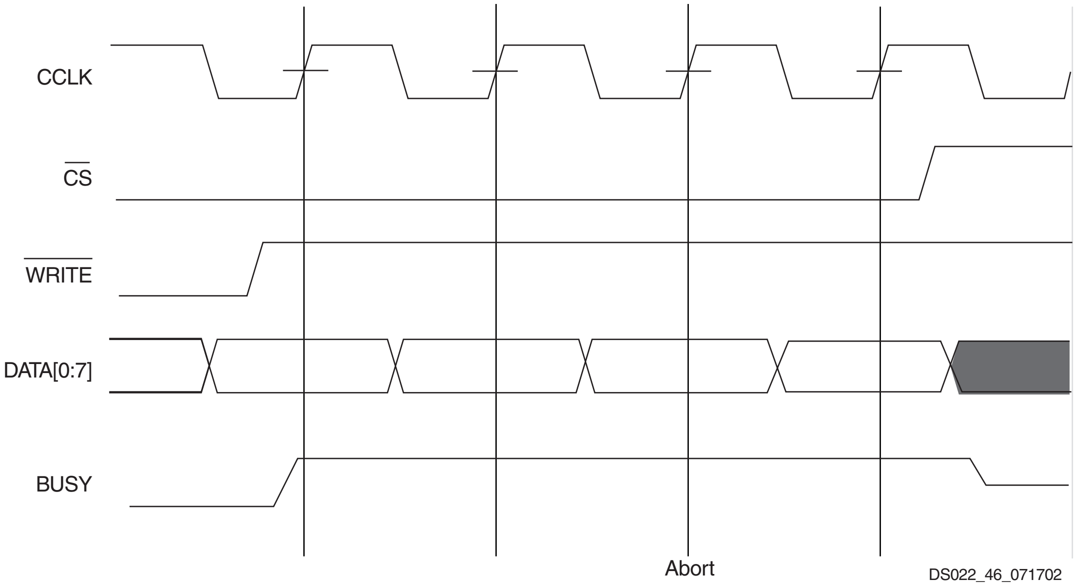

Figure 19: **SelectMAP Write Abort Waveforms**

Boundary Scan Mode

In the Boundary Scan mode, configuration is done through the IEEE 1149.1 Test Access Port. Note that the PROGRAM pin must be pulled High prior to reconfiguration. A Low on the PROGRAM pin resets the TAP controller and no JTAG operations can be performed.

SSTL3_I

A sample circuit illustrating a valid termination technique for SSTL3_I appears in Figure 49. DC voltage specifications appear in Table 28.

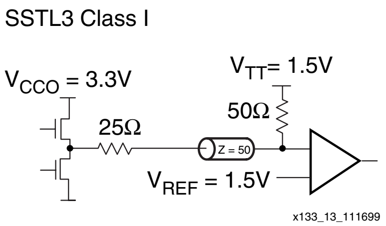

Figure 49: **Terminated SSTL3 Class I**

Table 28: **SSTL3_I Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	**3.0**	**3.3**	**3.6**
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} = V_{REF} + 0.2$	1.5	1.7	3.9(1)
$V_{IL} = V_{REF} - 0.2$	–0.3(2)	1.3	1.5
$V_{OH} = V_{REF} + 0.6$	1.9	-	-
$V_{OL} = V_{REF} - 0.6$	-	-	1.1
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL}at V_{OL} (mA)	8	-	-

Notes:

1. V_{IH} maximum is V_{CCO} + 0.3
2. V_{IL} minimum does not conform to the formula

SSTL3_II

A sample circuit illustrating a valid termination technique for SSTL3_II appears in Figure 50. DC voltage specifications appear in Table 29.

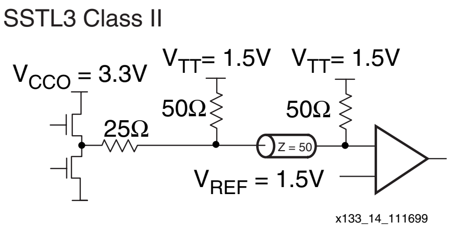

Figure 50: **Terminated SSTL3 Class II**

Table 29: **SSTL3_II Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} = V_{REF} + 0.2$	1.5	1.7	3.9(1)
$V_{IL}= V_{REF} - 0.2$	–0.3(2)	1.3	1.5
$V_{OH} = V_{REF} + 0.8$	2.1	-	-
$V_{OL}= V_{REF} - 0.8$	-	-	0.9
I_{OH} at V_{OH} (mA)	–16	-	-
I_{OL}at V_{OL} (mA)	16	-	-

Notes:

1. V_{IH} maximum is V_{CCO} + 0.3
2. V_{IL} minimum does not conform to the formula

SSTL2_I

A sample circuit illustrating a valid termination technique for SSTL2_I appears in Figure 51. DC voltage specifications appear in Table 30.

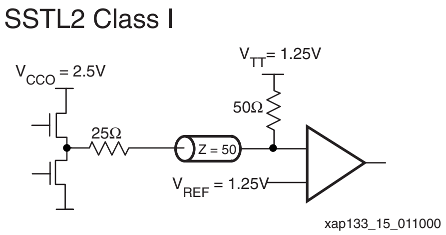

Figure 51: **Terminated SSTL2 Class I**

Table 30: **SSTL2_I Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
$V_{REF} = 0.5 \times V_{CCO}$	1.15	1.25	1.35
$V_{TT} = V_{REF} + N$(1)	1.11	1.25	1.39
$V_{IH} = V_{REF} + 0.18$	1.33	1.43	3.0(2)
$V_{IL} = V_{REF} - 0.18$	–0.3(3)	1.07	1.17
$V_{OH} = V_{REF} + 0.61$	1.76	-	-
$V_{OL}= V_{REF} - 0.61$	-	-	0.74
I_{OH} at V_{OH} (mA)	–7.6	-	-
I_{OL}at V_{OL} (mA)	7.6	-	-

Notes:

1. N must be greater than or equal to -0.04 and less than or equal to 0.04.
2. V_{IH} maximum is V_{CCO} + 0.3.
3. V_{IL} minimum does not conform to the formula.

Termination Resistor Packs

Resistor packs are available with the values and the configuration required for LVDS and LVPECL termination from Bourns, Inc., as listed in Table. For pricing and availability, please contact Bourns directly at http://www.bourns.com.

Table 40: **Bourns LVDS/LVPECL Resistor Packs**

Part Number	I/O Standard	Term. for:	Pairs/ Pack	Pins
CAT16–LV2F6	LVDS	Driver	2	8
CAT16–LV4F12	LVDS	Driver	4	16
CAT16–PC2F6	LVPECL	Driver	2	8
CAT16–PC4F12	LVPECL	Driver	4	16
CAT16–PT2F2	LVDS/LVPECL	Receiver	2	8
CAT16–PT4F4	LVDS/LVPECL	Receiver	4	16

LVDS Design Guide

The SelectI/O library elements have been expanded for Virtex-E devices to include new LVDS variants. At this time all of the cells might not be included in the Synthesis libraries. The 2.1i-Service Pack 2 update for Alliance and Foundation software includes these cells in the VHDL and Verilog libraries. It is necessary to combine these cells to create the P-side (positive) and N-side (negative) as described in the input, output, 3-state and bidirectional sections.

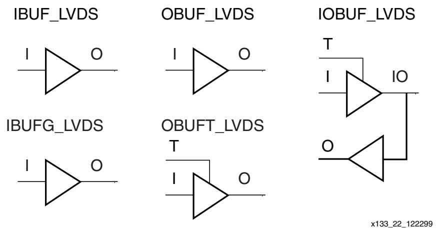

Figure 58: **LVDS elements**

Creating LVDS Global Clock Input Buffers

Global clock input buffers can be combined with adjacent IOBs to form LVDS clock input buffers. P-side is the GCLKPAD location; N-side is the adjacent IO_LVDS_DLL site.

Table 41: **Global Clock Input Buffer Pair Locations**

Pkg	GCLK 3		GCLK 2		GCLK 1		GCLK 0	
	P	N	P	N	P	N	P	N
CS144	A6	C6	A7	B7	M7	M6	K7	N8
PQ240	P213	P215	P210	P209	P89	P87	P92	P93
HQ240	P213	P215	P210	P209	P89	P87	P92	P93
BG352	D14	A15	B14	A13	AF14	AD14	AE13	AC13
BG432	D17	C17	A16	B16	AK16	AL17	AL16	AH15
BG560	A17	C18	D17	E17	AJ17	AM18	AL17	AM17
FG256	B8	A7	C9	A8	R8	T8	N8	N9
FG456	C11	B11	A11	D11	YII	AA11	W12	U12
FG676	E13	B13	C13	F14	AB13	AF13	AA14	AC14
FG680	A20	C22	D21	A19	AU22	AT22	AW19	AT21
FG860	C22	A22	B22	D22	AY22	AW21	BA22	AW20
FG900	C15	A15	E15	E16	AK16	AH16	AJ16	AF16
FG1156	E17	C17	D17	J18	AI19	AL17	AH18	AM18

HDL Instantiation

Only one global clock input buffer is required to be instantiated in the design and placed on the correct GCLKPAD location. The N-side of the buffer is reserved and no other IOB is allowed to be placed on this location.

In the physical device, a configuration option is enabled that routes the pad wire to the differential input buffer located in the GCLKIOB. The output of this buffer then drives the output of the GCLKIOB cell. In EPIC it appears that the second buffer is unused. Any attempt to use this location for another purpose leads to a DRC error in the software.

VHDL Instantiation

```
gclk0_p : IBUFG_LVDS port map
(I=>clk_external, O=>clk_internal);
```

Verilog Instantiation

```
IBUFG_LVDS gclk0_p (.I(clk_external),
.O(clk_internal));
```

Location constraints

All LVDS buffers must be explicitly placed on a device. For the global clock input buffers this can be done with the following constraint in the .ucf or .ncf file.

```
NET clk_external LOC = GCLKPAD3;
```

GCLKPAD3 can also be replaced with the package pin name such as D17 for the BG432 package.

DC Characteristics

Absolute Maximum Ratings

Symbol	Description[1]			Units
V_{CCINT}	Internal Supply voltage relative to GND		–0.5 to 2.0	V
V_{CCO}	Supply voltage relative to GND		–0.5 to 4.0	V
V_{REF}	Input Reference Voltage		–0.5 to 4.0	V
V_{IN} (3)	Input voltage relative to GND		–0.5 to V_{CCO} +0.5	V
V_{TS}	Voltage applied to 3-state output		–0.5 to 4.0	V
V_{CC}	Longest Supply Voltage Rise Time from 0 V - 1.71 V		50	ms
T_{STG}	Storage temperature (ambient)		–65 to +150	°C
T_J	Junction temperature (2)	Plastic packages	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time can affect device reliability.
2. For soldering guidelines and thermal considerations, see the device packaging information on www.xilinx.com.
3. Inputs configured as PCI are fully PCI compliant. This statement takes precedence over any specification that would imply that the device is not PCI compliant.

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CCINT}	Internal Supply voltage relative to GND, T_J = 0 °C to +85 °C	Commercial	1.8 – 5%	1.8 + 5%	V
	Internal Supply voltage relative to GND, T_J = –40 °C to +100 °C	Industrial	1.8 – 5%	1.8 + 5%	V
V_{CCO}	Supply voltage relative to GND, T_J = 0 °C to +85 °C	Commercial	1.2	3.6	V
	Supply voltage relative to GND, T_J = –40 °C to +100 °C	Industrial	1.2	3.6	V
T_{IN}	Input signal transition time			250	ns

DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Device	Min	Max	Units
V_{DRINT}	Data Retention V_{CCINT} Voltage (below which configuration data might be lost)		All	1.5		V
V_{DRIO}	Data Retention V_{CCO} Voltage (below which configuration data might be lost)		All	1.2		V
I_{CCINTQ}	Quiescent V_{CCINT} supply current (Note 1)		XCV50E		200	mA
			XCV100E		200	mA
			XCV200E		300	mA
			XCV300E		300	mA
			XCV400E		300	mA
			XCV600E		400	mA
			XCV1000E		500	mA
			XCV1600E		500	mA
			XCV2000E		500	mA
			XCV2600E		500	mA
			XCV3200E		500	mA
I_{CCOQ}	Quiescent V_{CCO} supply current (Note 1)		XCV50E		2	mA
			XCV100E		2	mA
			XCV200E		2	mA
			XCV300E		2	mA
			XCV400E		2	mA
			XCV600E		2	mA
			XCV1000E		2	mA
			XCV1600E		2	mA
			XCV2000E		2	mA
			XCV2600E		2	mA
			XCV3200E		2	mA
I_L	Input or output leakage current		All	–10	+10	µA
C_{IN}	Input capacitance (sample tested)	BGA, PQ, HQ, packages	All		8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0 V, V_{CCO} = 3.3 V (sample tested)		All	Note 2	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 3.6 V (sample tested)			Note 2	0.25	mA

Notes:

1. With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating.
2. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.

IOB Output Switching Characteristics Standard Adjustments

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

			Speed Grade				
Description	**Symbol**	**Standard**	**Min**	**-8**	**-7**	**-6**	**Units**
Output Delay Adjustments							
Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl)	T_{OLVTTL_S2}	LVTTL, Slow, 2 mA	4.2	+14.7	+14.7	+14.7	ns
	T_{OLVTTL_S4}	4 mA	2.5	+7.5	+7.5	+7.5	ns
	T_{OLVTTL_S6}	6 mA	1.8	+4.8	+4.8	+4.8	ns
	T_{OLVTTL_S8}	8 mA	1.2	+3.0	+3.0	+3.0	ns
	T_{OLVTTL_S12}	12 mA	1.0	+1.9	+1.9	+1.9	ns
	T_{OLVTTL_S16}	16 mA	0.9	+1.7	+1.7	+1.7	ns
	T_{OLVTTL_S24}	24 mA	0.8	+1.3	+1.3	+1.3	ns
	T_{OLVTTL_F2}	LVTTL, Fast, 2 mA	1.9	+13.1	+13.1	+13.1	ns
	T_{OLVTTL_F4}	4 mA	0.7	+5.3	+5.3	+5.3	ns
	T_{OLVTTL_F6}	6 mA	0.20	+3.1	+3.1	+3.1	ns
	T_{OLVTTL_F8}	8 mA	0.10	+1.0	+1.0	+1.0	ns
	T_{OLVTTL_F12}	12 mA	0.0	0.0	0.0	0.0	ns
	T_{OLVTTL_F16}	16 mA	–0.10	–0.05	–0.05	–0.05	ns
	T_{OLVTTL_F24}	24 mA	–0.10	–0.20	–0.20	–0.20	ns
	$T_{OLVCMOS\_2}$	LVCMOS2	0.10	+0.09	+0.09	+0.09	ns
	$T_{OLVCMOS\_18}$	LVCMOS18	0.10	+0.7	+0.7	+0.7	ns
	T_{OLVDS}	LVDS	–0.39	–1.2	–1.2	–1.2	ns
	$T_{OLVPECL}$	LVPECL	–0.20	–0.41	–0.41	–0.41	ns
	T_{OPCI33_3}	PCI, 33 MHz, 3.3 V	0.50	+2.3	+2.3	+2.3	ns
	T_{OPCI66_3}	PCI, 66 MHz, 3.3 V	0.10	–0.41	–0.41	–0.41	ns
	T_{OGTL}	GTL	0.6	+0.49	+0.49	+0.49	ns
	T_{OGTLP}	GTL+	0.7	+0.8	+0.8	+0.8	ns
	T_{OHSTL_I}	HSTL I	0.10	–0.51	–0.51	–0.51	ns
	T_{OHSTL_III}	HSTL III	–0.10	–0.91	–0.91	–0.91	ns
	T_{OHSTL_IV}	HSTL IV	–0.20	–1.01	–1.01	–1.01	ns
	T_{OSSTL2_I}	SSTL2 I	–0.10	–0.51	–0.51	–0.51	ns
	T_{OSSTL2_II}	SSTL2 II	–0.20	–0.91	–0.91	–0.91	ns
	T_{OSSTL3_I}	SSTL3 I	–0.20	–0.51	–0.51	–0.51	ns
	T_{OSSTL3_II}	SSTL3 II	–0.30	–1.01	–1.01	–1.01	ns
	T_{OCTT}	CTT	0.0	–0.61	–0.61	–0.61	ns
	T_{OAGP}	AGP	–0.1	–0.91	–0.91	–0.91	ns

CLB Distributed RAM Switching Characteristics

		Speed Grade[1]				
Description	**Symbol**	**Min**	**-8**	**-7**	**-6**	**Units**
Sequential Delays						
Clock CLK to X/Y outputs (WE active) 16 x 1 mode	$T_{SHCKO16}$	0.67	1.38	1.5	1.7	ns, max
Clock CLK to X/Y outputs (WE active) 32 x 1 mode	$T_{SHCKO32}$	0.84	1.66	1.9	2.1	ns, max
Shift-Register Mode Clock CLK to X/Y outputs	T_{REG}	1.25	2.39	2.9	3.2	ns, max
Setup and Hold Times before/after Clock CLK						
F/G address inputs	T_{AS}/T_{AH}	0.19 / 0	0.38 / 0	0.42 / 0	0.47 / 0	ns, min
BX/BY data inputs (DIN)	T_{DS}/T_{DH}	0.44 / 0	0.87 / 0	0.97 / 0	1.09 / 0	ns, min
SR input (WE)	T_{WS}/T_{WH}	0.29 / 0	0.57 / 0	0.7 / 0	0.8 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T_{WPH}	0.96	1.9	2.1	2.4	ns, min
Minimum Pulse Width, Low	T_{WPL}	0.96	1.9	2.1	2.4	ns, min
Minimum clock period to meet address write cycle time	T_{WC}	1.92	3.8	4.2	4.8	ns, min
Shift-Register Mode						
Minimum Pulse Width, High	T_{SRPH}	1.0	1.9	2.1	2.4	ns, min
Minimum Pulse Width, Low	T_{SRPL}	1.0	1.9	2.1	2.4	ns, min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

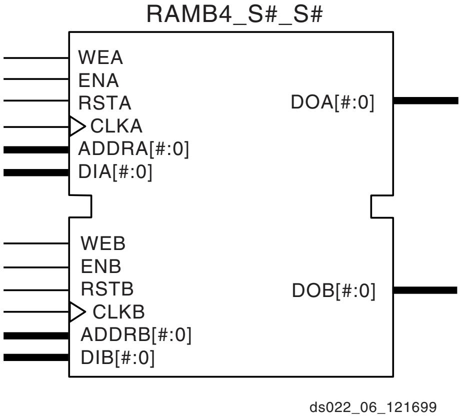

Figure 3: **Dual-Port Block SelectRAM**

Block RAM Switching Characteristics

		Speed Grade[1]				
Description	**Symbol**	**Min**	**-8**	**-7**	**-6**	**Units**
Sequential Delays						
Clock CLK to DOUT output	T_{BCKO}	0.63	2.46	3.1	3.5	ns, max
Setup and Hold Times before Clock CLK						
ADDR inputs	T_{BACK}/T_{BCKA}	0.42 / 0	0.9 / 0	1.0 / 0	1.1 / 0	ns, min
DIN inputs	T_{BDCK}/T_{BCKD}	0.42 / 0	0.9 / 0	1.0 / 0	1.1 / 0	ns, min
EN input	T_{BECK}/T_{BCKE}	0.97 / 0	2.0 / 0	2.2 / 0	2.5 / 0	ns, min
RST input	T_{BRCK}/T_{BCKR}	0.9 / 0	1.8 / 0	2.1 / 0	2.3 / 0	ns, min
WEN input	T_{BWCK}/T_{BCKW}	0.86 / 0	1.7 / 0	2.0 / 0	2.2 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T_{BPWH}	0.6	1.2	1.35	1.5	ns, min
Minimum Pulse Width, Low	T_{BPWL}	0.6	1.2	1.35	1.5	ns, min
CLKA -> CLKB setup time for different ports	T_{BCCS}	1.2	2.4	2.7	3.0	ns, min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

TBUF Switching Characteristics

		Speed Grade				
Description	**Symbol**	**Min**	**-8**	**-7**	**-6**	**Units**
Combinatorial Delays						
IN input to OUT output	T_{IO}	0.0	0.0	0.0	0 .0	ns, max
TRI input to OUT output high-impedance	T_{OFF}	0.05	0.092	0.10	0.11	ns, max
TRI input to valid data on OUT output	T_{ON}	0.05	0.092	0.10	0.11	ns, max

JTAG Test Access Port Switching Characteristics

Description	Symbol	Value	Units
TMS and TDI Setup times before TCK	T_{TAPTK}	4.0	ns, min
TMS and TDI Hold times after TCK	T_{TCKTAP}	2.0	ns, min
Output delay from clock TCK to output TDO	T_{TCKTDO}	11.0	ns, max
Maximum TCK clock frequency	F_{TCK}	33	MHz, max

Table 6: **PQ240 — XCV50E, XCV100E, XCV200E, XCV300E, XCV400E**

Pin #	Pin Description	Bank
P173	IO_L16N_Y	2
P171	IO_VREF_L17P_Y	2
P170	IO_L17N_Y	2
P169	IO	2
P168[1]	IO_VREF_L18P_Y	2
P167	IO_D1_L18N_Y	2
P163	IO_D2_L19P_YY	2
P162	IO_L19N_YY	2
P161	IO	2
P160	IO_L20P_Y	2
P159	IO_L20N_Y	2
P157	IO_VREF_L21P_Y	2
P156	IO_D3_L21N_Y	2
P155	IO_L22P_Y	2
P154[3]	IO_VREF_L22N_Y	2
P153	IO_L23P_YY	2
P152	IO_L23N_YY	2
P149	IO	3
P147[3]	IO_VREF	3
P145	IO_D4_L24P_Y	3
P144	IO_VREF_L24N_Y	3
P142	IO_L25P_Y	3
P141	IO_L25N_Y	3
P140	IO	3
P139	IO_L26P_YY	3
P138	IO_D5_L26N_YY	3
P134	IO_D6_L27P_Y	3
P133[1]	IO_VREF_L27N_Y	3
P132	IO	3
P131	IO_L28P_Y	3
P130	IO_VREF_L28N_Y	3
P128	IO_L29P_Y	3
P127	IO_L29N_Y	3
P126[2]	IO_VREF_L30P_Y	3
P125	IO_L30N_Y	3
P124	IO_D7_L31P_YY	3
P123	IO_INIT_L31N_YY	3
P118	IO_L32P_YY	4
P117	IO_L32N_YY	4
P115[2]	IO_VREF	4
P114	IO_L33P_YY	4
P113	IO_L33N_YY	4
P111	IO_VREF_L34P_YY	4
P110	IO_L34N_YY	4
P109	IO	4
P108[1]	IO_VREF_L35P_YY	4
P107	IO_L35N_YY	4
P103	IO_L36P_YY	4
P102	IO_L36N_YY	4
P101	IO	4
P100	IO_L37P_Y	4
P99	IO_L37N_Y	4
P97	IO_VREF_L38P_Y	4
P96	IO_L38N_Y	4
P95	IO_L39P_Y	4
P94[3]	IO_VREF_L39N_Y	4
P93	IO_LVDS_DLL_L40P	4
P92	GCK0	4
P89	GCK1	5
P87	IO_LVDS_DLL_L40N	5
P86[3]	IO_VREF	5
P84	IO_VREF_L41P_Y	5
P82	IO_L41N_Y	5
P81	IO	5
P80	IO	5
P79	IO_L42P_YY	5
P78	IO_L42N_YY	5

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P138	IO_D5_L26N_YY	3
P137	VCCINT	NA
P136	VCCO	3
P135	GND	NA
P134	IO_D6_L27P_Y	3
P133	IO_VREF_L27N_Y	3
P132	IO_VREF	3
P131	IO_L28P_Y	3
P130	IO_VREF_L28N_Y	3
P129	GND	NA
P128	IO_L29P_Y	3
P127	IO_L29N_Y	3
P126	IO_VREF_L30P_Y	3
P125	IO_L30N_Y	3
P124	IO_D7_L31P_YY	3
P123	IO_INIT_L31N_YY	3
P122	PROGRAM	NA
P121	VCCO	3
P120	DONE	3
P119	GND	NA
P118	IO_L32P_YY	4
P117	IO_L32N_YY	4
P116	VCCO	4
P115	IO_VREF	4
P114	IO_L33P_YY	4
P113	IO_L33N_YY	4
P112	GND	NA
P111	IO_VREF_L34P_YY	4
P110	IO_L34N_YY	4
P109	IO_VREF	4
P108	IO_VREF_L35P_YY	4
P107	IO_L35N_YY	4
P106	GND	NA
P105	VCCO	4
P104	VCCINT	NA
P103	IO_L36P_YY	4

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P102	IO_L36N_YY	4
P101[1]	IO_VREF	4
P100	IO_L37P_Y	4
P99	IO_L37N_Y	4
P98	GND	NA
P97	IO_VREF_L38P_Y	4
P96	IO_L38N_Y	4
P95	IO_L39P	4
P94	IO_VREF_L39N	4
P93	IO_LVDS_DLL_L40P	4
P92	GCK0	4
P91	GND	NA
P90	VCCO	4
P89	GCK1	5
P88	VCCINT	NA
P87	IO_LVDS_DLL_L40N	5
P86	IO_VREF	5
P85	VCCO	5
P84	IO_VREF_L41P	5
P83	GND	NA
P82	IO_L41N	5
P81	IO	5
P80[1]	IO_VREF	5
P79	IO_L42P_YY	5
P78	IO_L42N_YY	5
P77	VCCINT	NA
P76	VCCO	5
P75	GND	NA
P74	IO_L43P_YY	5
P73	IO_VREF_L43N_YY	5
P72	IO_VREF	5
P71	IO_L44P_YY	5
P70	IO_VREF_L44N_YY	5
P69	GND	NA
P68	IO_L45P_YY	5
P67	IO_L45N_YY	5

Table 10: **BG352 — XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
4	IO_VREF_4_L53P_Y	AC12
4	IO_L53N_Y	AD12
4	IO_L54P	AE12
4	IO_L54N	AF12
4	IO	AD13[1]
4	IO_LVDS_DLL_L55P	AC13
4	GCK0	AE13
5	GCK1	AF14
5	IO_LVDS_DLL_L55N	AD14
5	IO	AF15[1]
5	IO	AE15
5	IO_L56P_Y	AD15
5	IO_VREF_5_L56N_Y	AC15
5	IO_L57P_Y	AE16
5	IO_L57N_Y	AE17
5	IO	AD16[1]
5	IO_L58P	AC16
5	IO_L58N	AF18
5	IO	AE18[1]
5	IO_L59P_YY	AD17
5	IO_L59N_YY	AC17
5	IO_L60P_YY	AD18
5	IO_VREF_5_L60N_YY	AC18
5	IO_L61P _Y	AF20
5	IO_L61N _Y	AE20
5	IO	AD19
5	IO	AC19[1]
5	IO	AF21[1]
5	IO_L62P_YY	AE21
5	IO_VREF_5_L62N_YY	AD20
5	IO_L63P_YY	AF23
5	IO_L63N_YY	AE22
5	IO	AD21[1]
5	IO_L64P_YY	AC21
5	IO_VREF_5_L64N_YY	AE23[2]
5	IO	AD22
5	IO	AF24[1]
5	IO	AC22[1]
6	IO_L65N_YY	AC24
6	IO_L65P_YY	AD25
6	IO	AB24[1]
6	IO	AA23[1]
6	IO	AC25
6	IO_VREF_6_L66N_YY	AD26[2]
6	IO_L66P_YY	AC26
6	IO	Y23[1]
6	IO_L67N_YY	AA24
6	IO_L67P_YY	AB25
6	IO_VREF_6_L68N_Y	AA25
6	IO_L68P_Y	Y24
6	IO	Y25[1]
6	IO	AA26[1]
6	IO_L69N	V23
6	IO_L69P	W24
6	IO	W25
6	IO_VREF_6_L70N _Y	Y26
6	IO_L70P _Y	U23
6	IO_L71N_YY	V25
6	IO_L71P_YY	U24
6	IO	V26[1]
6	IO_L72N	T23
6	IO_L72P	U25
6	IO	T24[1]
6	IO_L73N_YY	T25
6	IO_L73P_YY	T26
6	IO_VREF_6_L74N _Y	R24

BG352 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A check (√) in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock

Table 11: **BG352 Differential Pin Pair Summary XCV100E, XCV200E, XCV300E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	AE13	AC13	NA	IO LVDS 55
1	5	AF14	AD14	NA	IO LVDS 55
2	1	B14	A13	NA	IO LVDS 9
3	0	D14	A15	NA	IO LVDS 9
IO LVDS Total Outputs: 87, Asynchronous Output Pairs: 43					
0	0	B23	D21	√	VREF_0
1	0	D20	A23	√	-
2	0	B22	C21	√	VREF_0
3	0	A21	B20	2	-
4	0	B19	C19	√	VREF_0
5	0	C18	D17	√	-
6	0	A18	C17	2	-
7	0	C16	B17	√	-
8	0	D15	A16	√	VREF_0
9	1	A13	A15	√	GCLK LVDS 3/2
10	1	A12	C13	2	-
11	1	C12	B12	√	VREF_1
12	1	B11	A11	√	-
13	1	D11	C11	2	-
14	1	C10	B9	√	-
15	1	C9	B8	√	VREF_1
16	1	A7	D9	1	-
17	1	B6	A6	√	VREF_1
18	1	A4	C7	√	-
19	1	D6	C6	√	VREF_1
20	1	C4	D5	√	CS
21	2	E4	D3	√	DIN_D0
22	2	D2	C1	√	VREF_2
23	2	G4	F3	√	-
24	2	E2	F2	√	VREF_2
25	2	F1	J4	2	-
26	2	H2	G1	√	D1
27	2	J3	J2	√	D2
28	2	J1	L4	1	-
29	2	L3	L2	√	-
30	2	M4	M3	√	D3
31	2	M2	M1	2	-
32	2	N4	N2	√	-
33	3	R1	R2	2	-
34	3	R3	R4	√	VREF_3
35	3	T2	U2	√	-
36	3	T4	V1	1	-
37	3	U3	U4	√	D5
38	3	V3	V4	√	VREF_3
39	3	Y1	Y2	1	-
40	3	AA2	Y3	√	VREF_3
41	3	AC1	AB2	√	-
42	3	AA4	AC2	√	VREF_3
43	3	AC3	AD2	√	INIT
44	4	AC5	AD4	√	-
45	4	AE4	AF3	√	VREF_4
46	4	AC7	AD6	√	-
47	4	AE5	AE6	√	VREF_4
48	4	AF6	AC9	2	-
49	4	AE8	AF7	√	VREF_4
50	4	AD9	AE9	√	-
51	4	AF9	AC11	2	-
52	4	AD11	AE11	√	-
53	4	AC12	AD12	√	VREF_4
54	4	AE12	AF12	2	-

Table 12: **BG432 — XCV300E, XCV400E, XCV600E**

Bank	Pin Description	Pin #
2	IO_L41N_Y	H2
2	IO_VREF_L42P_Y	H1[1]
2	IO_L42N_Y	J4
2	IO_VREF_L43P_YY	J2
2	IO_D1_L43N_YY	K4
2	IO_D2_L44P_YY	K2
2	IO_L44N_YY	K1
2	IO_L45P_Y	L2
2	IO_L45N_Y	M4
2	IO_L46P_Y	M3
2	IO_L46N_Y	M2
2	IO_L47P_Y	N4
2	IO_L47N_Y	N3
2	IO_VREF_L48P_YY	N1
2	IO_D3_L48N_YY	P4
2	IO_L49P_Y	P3
2	IO_L49N_Y	P2
2	IO_VREF_L50P_Y	R3[2]
2	IO_L50N_Y	R4
2	IO_L51P_YY	R1
2	IO_L51N_YY	T3
3	IO	AA2
3	IO	AC2
3	IO	AE2
3	IO	U3
3	IO	W1
3	IO_L52P_Y	U4
3	IO_VREF_L52N_Y	U2[2]
3	IO_L53P_Y	U1
3	IO_L53N_Y	V3
3	IO_D4_L54P_YY	V4
3	IO_VREF_L54N_YY	V2
3	IO_L55P_Y	W3
3	IO_L55N_Y	W4
3	IO_L56P_Y	Y1
3	IO_L56N_Y	Y3
3	IO_L57P_Y	Y4
3	IO_L57N_Y	Y2
3	IO_L58P_YY	AA3
3	IO_D5_L58N_YY	AB1
3	IO_D6_L59P_YY	AB3
3	IO_VREF_L59N_YY	AB4
3	IO_L60P_Y	AD1
3	IO_VREF_L60N_Y	AC3[1]
3	IO_L61P_Y	AC4
3	IO_L61N_Y	AD2
3	IO_L62P_YY	AD3
3	IO_VREF_L62N_YY	AD4
3	IO_L63P_Y	AF2
3	IO_L63N_Y	AE3
3	IO_L64P	AE4
3	IO_L64N	AG1
3	IO_L65P_Y	AG2
3	IO_VREF_L65N_Y	AF3
3	IO_L66P_Y	AF4
3	IO_L66N_Y	AH1
3	IO_L67P	AH2
3	IO_L67N	AG3
3	IO_D7_L68P_YY	AG4
3	IO_INIT_L68N_YY	AJ2
3	IO	T2
4	GCK0	AL16
4	IO	AH10
4	IO	AJ11
4	IO	AK7
4	IO	AL12
4	IO	AL15
4	IO_L69P_YY	AJ4
4	IO_L69N_YY	AK3
4	IO_L70P_Y	AH5

Table 12: **BG432 — XCV300E, XCV400E, XCV600E**

Bank	Pin Description	Pin #
6	IO	AA30
6	IO	AC30
6	IO	AD29
6	IO	U31
6	IO	W28
6	IO_L103N_YY	AJ30
6	IO_L103P_YY	AH30
6	IO_L104N	AG28
6	IO_L104P	AH31
6	IO_L105N_Y	AG29
6	IO_L105P_Y	AG30
6	IO_VREF_L106N_Y	AF28
6	IO_L106P_Y	AG31
6	IO_L107N	AF29
6	IO_L107P	AF30
6	IO_L108N_Y	AE28
6	IO_L108P_Y	AF31
6	IO_VREF_L109N_YY	AE30
6	IO_L109P_YY	AD28
6	IO_L110N_Y	AD30
6	IO_L110P_Y	AD31
6	IO_VREF_L111N_Y	AC28[1]
6	IO_L111P_Y	AC29
6	IO_VREF_L112N_YY	AB28
6	IO_L112P_YY	AB29
6	IO_L113N_YY	AB31
6	IO_L113P_YY	AA29
6	IO_L114N_Y	Y28
6	IO_L114P_Y	Y29
6	IO_L115N_Y	Y30
6	IO_L115P_Y	Y31
6	IO_L116N_Y	W29
6	IO_L116P_Y	W30
6	IO_VREF_L117N_YY	V28
6	IO_L117P_YY	V29
6	IO_L118N_Y	V30
6	IO_L118P_Y	U29
6	IO_VREF_L119N_Y	U28[2]
6	IO_L119P_Y	U30
6	IO	T30
7	IO	C30
7	IO	H29
7	IO	H31
7	IO	L29
7	IO	M31
7	IO	R28
7	IO_L120N_YY	T31
7	IO_L120P_YY	R29
7	IO_L121N_Y	R30
7	IO_VREF_L121P_Y	R31[2]
7	IO_L122N_Y	P29
7	IO_L122P_Y	P28
7	IO_L123N_YY	P30
7	IO_VREF_L123P_YY	N30
7	IO_L124N_Y	N28
7	IO_L124P_Y	N31
7	IO_L125N_Y	M29
7	IO_L125P_Y	M28
7	IO_L126N_Y	M30
7	IO_L126P_Y	L30
7	IO_L127N_YY	K31
7	IO_L127P_YY	K30
7	IO_L128N_YY	K28
7	IO_VREF_L128P_YY	J30
7	IO_L129N_Y	J29
7	IO_VREF_L129P_Y	J28[1]
7	IO_L130N_Y	H30
7	IO_L130P_Y	G30
7	IO_L131N_YY	H28
7	IO_VREF_L131P_YY	F31
7	IO_L132N_Y	G29

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
3	IO_L50N_YY	P19
3	IO_L51P_YY	P18
3	IO_D5_L51N_YY	R21
3	IO_D6_L52P_Y	T22
3	IO_VREF_L52N_Y	R19
3	IO_L53P_Y	U22
3	IO_L53N_Y	R18
3	IO_L54P_YY	T21
3	IO_L54N_YY	V22
3	IO_L55P_YY	T20
3	IO_VREF_L55N_YY	U21
3	IO_L56P_YY	W22
3	IO_L56N_YY	T18
3	IO_L57P_YY	U19
3	IO_VREF_L57N_YY	U20
3	IO_L58P_YY	W21
3	IO_L58N_YY	AA22
3	IO_D7_L59P_YY	Y21
3	IO_INIT_L59N_YY	V19
3	IO	M22
4	GCK0	W12
4	IO	W14
4	IO	Y13
4	IO	Y17
4	IO	AA16[1]
4	IO	AA19
4	IO	AB12[1]
4	IO	AB17
4	IO	AB21[1]
4	IO_L60P_YY	W18
4	IO_L60N_YY	AA20
4	IO_L61P	Y18
4	IO_L61N	V17
4	IO_VREF_L62P_YY	AB20
4	IO_L62N_YY	W17
4	IO_L63P	AA18

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
4	IO_L63N	V16
4	IO_VREF_L64P_YY	AB19
4	IO_L64N_YY	AB18
4	IO_L65P_Y	W16
4	IO_L65N_Y	AA17
4	IO_L66P_Y	Y16
4	IO_L66N_Y	V15
4	IO_VREF_L67P_YY	AB16
4	IO_L67N_YY	Y15
4	IO_L68P_YY	AA15
4	IO_L68N_YY	AB15
4	IO_L69P_Y	W15
4	IO_L69N_Y	Y14
4	IO_L70P_Y	V14
4	IO_L70N_Y	AA14
4	IO_L71P	AB14
4	IO_L71N	V13
4	IO_VREF_L72P_YY	AA13
4	IO_L72N_YY	AB13
4	IO_L73P_Y	W13
4	IO_L73N_Y	AA12
4	IO_L74P_Y	Y12
4	IO_L74N_Y	V12
4	IO_LVDS_DLL_L75P	U12
5	IO	U11[1]
5	IO	V8
5	IO	W5
5	IO	AA3[1]
5	IO	AA9
5	IO	AA10
5	IO	AB4
5	IO	AB7[1]
5	IO	AB8
5	GCK1	Y11
5	IO_LVDS_DLL_L75N	AA11
5	IO_L76P_Y	AB11

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
NA	GND	D20
NA	GND	D12
NA	GND	C39
NA	GND	C37
NA	GND	C3
NA	GND	C20
NA	GND	C1
NA	GND	B39
NA	GND	B38
NA	GND	B2
NA	GND	B1
NA	GND	AW39
NA	GND	AW38
NA	GND	AW37
NA	GND	AW3
NA	GND	AW2
NA	GND	AW1
NA	GND	AV39
NA	GND	AV38
NA	GND	AV2
NA	GND	AV1
NA	GND	AU39
NA	GND	AU37
NA	GND	AU3
NA	GND	AU20
NA	GND	AU1
NA	GND	AT4
NA	GND	AT36
NA	GND	AT28
NA	GND	AT20
NA	GND	AT12
NA	GND	AR5
NA	GND	AR35
NA	GND	AR28
NA	GND	AR21
NA	GND	AR20
NA	GND	AR19
NA	GND	AR12
NA	GND	AH5
NA	GND	AH4
NA	GND	AH36
NA	GND	AH35
NA	GND	AA5
NA	GND	AA35
NA	GND	A39
NA	GND	A38
NA	GND	A37
NA	GND	A3
NA	GND	A2
NA	GND	A1

Notes:

1. V_{REF} or I/O option only in the XCV1000E, 1600E, 2000E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV1600E, 2000E; otherwise, I/O option only.
3. V_{REF} or I/O option only in the XCV2000E; otherwise, I/O option only.

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
2	IO	D29[5]
2	IO	G26[4]
2	IO	H24[4]
2	IO	H25[4]
2	IO	H28[5]
2	IO	J25[4]
2	IO	J27[5]
2	IO	K30[4]
2	IO	M24[4]
2	IO	M25[4]
2	IO	N20
2	IO	N23[4]
2	IO	P26[5]
2	IO	P27[5]
2	IO	P30[4]
2	IO	R30
2	IO_DOUT_BUSY_L70P_YY	J22
2	IO_DIN_D0_L70N_YY	E27
2	IO_L71P	C29[4]
2	IO_L71N	D28[3]
2	IO_L72P_Y	G25
2	IO_L72N_Y	E25
2	IO_VREF_L73P_YY	E28[1]
2	IO_L73N_YY	C30
2	IO_L74P_Y	K22[4]
2	IO_L74N_Y	F27[3]
2	IO_L75P_YY	D30
2	IO_L75N_YY	J23
2	IO_VREF_L76P_Y	L21
2	IO_L76N_Y	F28
2	IO_L77P_YY	G28
2	IO_L77N_YY	E30
2	IO_L78P_YY	G27
2	IO_L78N_YY	E29
2	IO_L79P	K23
2	IO_L79N	H26
2	IO_VREF_L80P_YY	F30
2	IO_L80N_YY	L22
2	IO_L81P_YY	H27
2	IO_L81N_YY	G29
2	IO_L82P	G30
2	IO_L82N	M21
2	IO_L83P_YY	J24
2	IO_L83N_YY	J26
2	IO_VREF_L84P_YY	H30
2	IO_L84N_YY	L23
2	IO_L85P_YY	K26[4]
2	IO_L85N_YY	J28[3]
2	IO_L86P_YY	J29
2	IO_L86N_YY	K24
2	IO_L87P_YY	K27[4]
2	IO_VREF_L87N_YY	J30
2	IO_D1_L88P	M22
2	IO_D2_L88N	K29
2	IO_L89P_YY	K28[3]
2	IO_L89N_YY	L25[4]
2	IO_L90P	N21
2	IO_L90N	K25
2	IO_L91P_YY	L24
2	IO_L91N_YY	L27
2	IO_L92P_Y	L29[4]
2	IO_L92N_Y	M23[4]
2	IO_L93P_YY	L26
2	IO_L93N_YY	L28
2	IO_VREF_L94P	L30[1]
2	IO_L94N	M27
2	IO_L95P_YY	M26
2	IO_L95N_YY	M29
2	IO_L96P_YY	N29
2	IO_L96N_YY	M30
2	IO_L97P	N25
2	IO_L97N	N27
2	IO_VREF_L98P_YY	N30
2	IO_D3_L98N_YY	P21

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
71	1	A27	G24	3200 2000 1000	-
72	1	G25	B27	3200 1600	-
73	1	C27	E26	3200 2600 2000 1600 1000	VREF
74	1	B28	J24	3200 2600 2000 1600 1000	-
75	1	H25	K24	3200 2600	-
76	1	F26	D27	3200 1000	-
77	1	C28	G26	3200 1000	-
78	1	J25	E27	2000 1600	-
79	1	H26	A30	3200 2600 2000 1600 1000	VREF
80	1	B29	G27	3200 2600 2000 1600 1000	-
81	1	C29	F27	3200 2600 1000	-
82	1	F28	E28	3200 2000 1000	VREF
83	1	B30	L25	3200 2000 1000	-
84	1	E29	B31	3200 1600 1000	-
85	1	D30	A31	3200 2600 2000 1600 1000	CS
86	2	D32	J27	3200 2600 2000 1600 1000	DIN, D0
87	2	E31	F30	3200 2600 2000	-
88	2	G29	F32	2600 2000 1000	-
89	2	E32	G30	3200 2600 1600 1000	VREF
90	2	M25	G31	2600 1600	-
91	2	L26	D33	3200 2600 1600 1000	-
92	2	D34	H29	2600 2000 1000	VREF
93	2	J28	E33	3200 2600 2000 1600	-
94	2	H28	H30	3200 2600 2000 1600 1000	-
95	2	H32	K28	3200 2600 1600 1000	-
96	2	L27	F33	3200 2600 2000	-
97	2	M26	E34	2600 2000 1000	-
98	2	H31	G32	3200 2600 2000 1600 1000	VREF
99	2	N25	J31	2000 1600	-
100	2	J30	G33	3200 2600 2000 1600 1000	-
101	2	H34	J29	2600 1000	VREF
102	2	M27	H33	3200 2600 1600	-
103	2	K29	J34	3200 2600 1600 1000	-
104	2	L29	J33	3200 2600 2000 1600 1000	VREF
105	2	M28	K34	3200 2600 2000 1600 1000	-
106	2	N27	L34	3200 1600 1000	-
107	2	K33	P26	2000 1600 1000	D1
108	2	R25	M34	3200 2600 2000	-
109	2	L31	L33	2000 1000	-
110	2	P27	M33	3200 2600 1600 1000	-