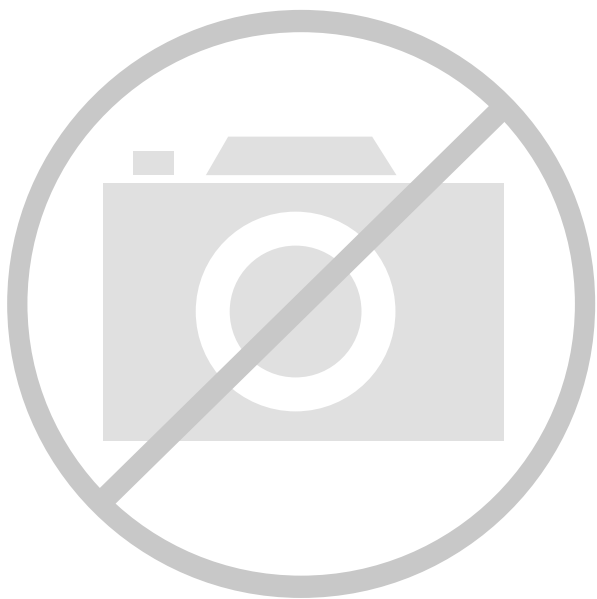




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	7776
Number of Logic Elements/Cells	34992
Total RAM Bits	589824
Number of I/O	660
Number of Gates	2188742
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	860-BGA Exposed Pad
Supplier Device Package	860-FBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv1600e-6fg860c

Data Registers

The primary data register is the Boundary Scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out, and 3-State Control. Non-IOB pins have appropriate partial bit population if input-only or output-only. Each EXTEST CAPTURED-OR state captures all In, Out, and 3-state pins.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream Boundary Scan device.

The FPGA supports up to two additional internal scan chains that can be specified using the BSCAN macro. The macro provides two user pins (SEL1 and SEL2) which are decodes of the USER1 and USER2 instructions respectively. For these instructions, two corresponding pins (TDO1 and TDO2) allow user scan data to be shifted out of TDO.

Likewise, there are individual clock pins (DRCK1 and DRCK2) for each user register. There is a common input pin (TDI) and shared output pins that represent the state of the TAP controller (RESET, SHIFT, and UPDATE).

Bit Sequence

The order within each IOB is: In, Out, 3-State. The input-only pins contribute only the In bit to the Boundary Scan I/O data register, while the output-only pins contribute all three bits.

From a cavity-up view of the chip (as shown in EPIC), starting in the upper right chip corner, the Boundary Scan data-register bits are ordered as shown in Figure 12.

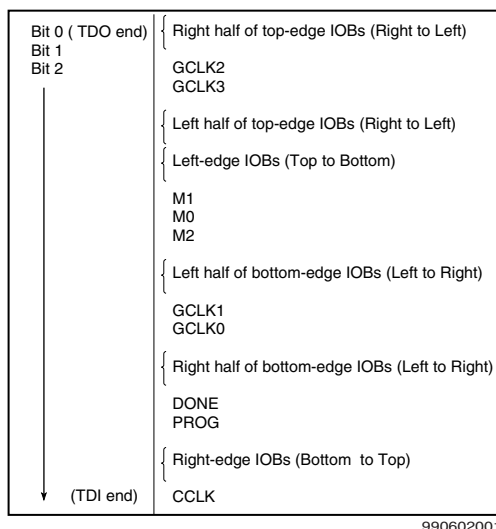


Figure 12: Boundary Scan Bit Sequence

BSDL (Boundary Scan Description Language) files for Virtex-E Series devices are available on the Xilinx web site in the File Download area.

Identification Registers

The IDCODE register is supported. By using the IDCODE, the device connected to the JTAG port can be determined.

The IDCODE register has the following binary format:

vvvv:ffff:ffa:aaaa:aaaa:cccc:cccc:ccc1

where

v = the die version number

f = the family code (05 for Virtex-E family)

a = the number of CLB rows (ranges from 16 for XCV50E to 104 for XCV3200E)

c = the company code (49h for Xilinx)

The USERCODE register is supported. By using the USERCODE, a user-programmable identification code can be loaded and shifted out for examination. The identification code (see Table 7) is embedded in the bitstream during bitstream generation and is valid only after configuration.

Table 7: IDCODEs Assigned to Virtex-E FPGAs

FPGA	IDCODE
XCV50E	v0A10093h
XCV100E	v0A14093h
XCV200E	v0A1C093h
XCV300E	v0A20093h
XCV400E	v0A28093h
XCV600E	v0A30093h
XCV1000E	v0A40093h
XCV1600E	v0A48093h
XCV2000E	v0A50093h
XCV2600E	v0A5C093h
XCV3200E	v0A68093h

Note:

Attempting to load an incorrect bitstream causes configuration to fail and can damage the device.

Including Boundary Scan in a Design

Since the Boundary Scan pins are dedicated, no special element needs to be added to the design unless an internal data register (USER1 or USER2) is desired.

If an internal data register is used, insert the Boundary Scan symbol and connect the necessary pins as appropriate.

indicating that the block SelectRAM+ memory is now disabled. The DO bus retains the last value.

Dual Port Timing

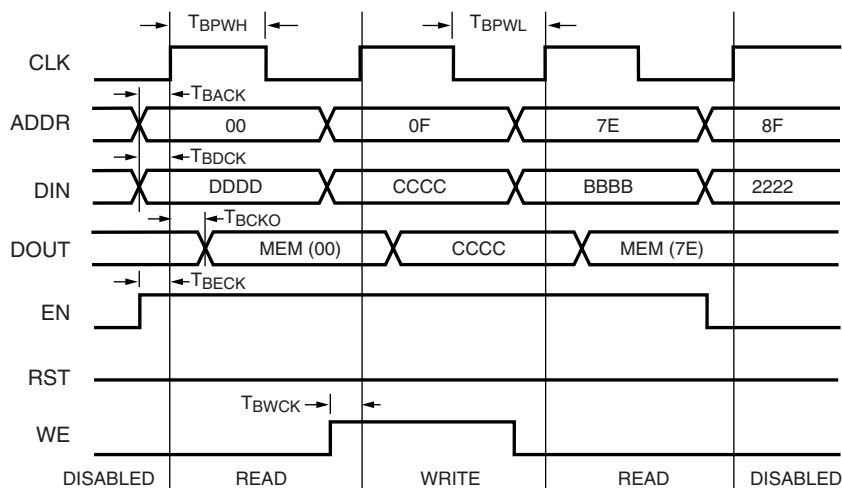
Figure 34 shows a timing diagram for a true dual-port read/write block SelectRAM+ memory. The clock on port A has a longer period than the clock on Port B. The timing parameter T_{BCCS} , (clock-to-clock set-up) is shown on this diagram. The parameter, T_{BCCS} is violated once in the diagram. All other timing parameters are identical to the single port version shown in Figure 33.

T_{BCCS} is only of importance when the address of both ports are the same and at least one port is performing a write operation. When the clock-to-clock set-up parameter is violated for a WRITE-WRITE condition, the contents of the memory at that location are invalid. When the clock-to-clock set-up parameter is violated for a WRITE-READ condition,

the contents of the memory are correct, but the read port has invalid data.

At the first rising edge of the CLKA, memory location 0x00 is to be written with the value 0xAAAA and is mirrored on the DOA bus. The last operation of Port B was a read to the same memory location 0x00. The DOB bus of Port B does not change with the new value on Port A, and retains the last read value. A short time later, Port B executes another read to memory location 0x00, and the DOB bus now reflects the new memory value written by Port A.

At the second rising edge of CLKA, memory location 0x7E is written with the value 0x9999 and is mirrored on the DOA bus. Port B then executes a read operation to the same memory location without violating the T_{BCCS} parameter and the DOB reflects the new memory values written by Port A.



ds022_0343_121399

Figure 33: Timing Diagram for Single Port Block SelectRAM+ Memory

VHDL Initialization Example

```

library IEEE;
use IEEE.std_logic_1164.all;

entity MYMEM is
port (CLK, WE:in std_logic;
ADDR: in std_logic_vector(8 downto 0);
DIN: in std_logic_vector(7 downto 0);
DOUT: out std_logic_vector(7 downto 0));
end MYMEM;

architecture BEHAVE of MYMEM is
signal logic0, logic1: std_logic;

component RAMB4_S8
--synopsys translate_off
generic( INIT_00,INIT_01, INIT_02, INIT_03, INIT_04, INIT_05, INIT_06, INIT_07,
INIT_08, INIT_09, INIT_0a, INIT_0b, INIT_0c, INIT_0d, INIT_0e, INIT_0f : BIT_VECTOR(255
downto 0)
:= X"0000000000000000000000000000000000000000000000000000000000000000");
--synopsys translate_on
port (WE, EN, RST, CLK: in STD_LOGIC;
ADDR: in STD_LOGIC_VECTOR(8 downto 0);
DI: in STD_LOGIC_VECTOR(7 downto 0);
DO: out STD_LOGIC_VECTOR(7 downto 0));
end component;

--synopsys dc_script_begin
--set_attribute ram0 INIT_00
"0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF" -type string
--set_attribute ram0 INIT_01
"FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210" -type string
--synopsys dc_script_end

begin
logic0 <='0';
logic1 <='1';

ram0: RAMB4_S8
--synopsys translate_off
generic map (
INIT_00 => X"0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF",
INIT_01 => X"FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210")
--synopsys translate_on
port map (WE=>WE, EN=>logic1, RST=>logic0, CLK=>CLK,ADDR=>ADDR, DI=>DIN, DO=>DOUT);
end BEHAVE;

```

IOB Flip-Flop/Latch Property

The Virtex-E series I/O Block (IOB) includes an optional register on the input path, an optional register on the output path, and an optional register on the 3-state control pin. The design implementation software automatically takes advantage of these registers when the following option for the Map program is specified.

```
map -pr b <filename>
```

Alternatively, the IOB = TRUE property can be placed on a register to force the mapper to place the register in an IOB.

Location Constraints

Specify the location of each SelectI/O symbol with the location constraint LOC attached to the SelectI/O symbol. The external port identifier indicates the value of the location constrain. The format of the port identifier depends on the package chosen for the specific design.

The LOC properties use the following form:

```
LOC=A42
```

```
LOC=P37
```

Output Slew Rate Property

As mentioned above, a variety of symbol names provide the option of choosing the desired slew rate for the output buffers. In the case of the LVTTTL output buffers (OBUF, OBUFT, and IOBUF), slew rate control can be alternatively programmed with the SLEW= property. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals. The SLEW= property has one of the two following values.

```
SLEW=SLOW
```

```
SLEW=FAST
```

Output Drive Strength Property

The desired output drive strength can be additionally specified by choosing the appropriate library symbol. The Xilinx library also provides an alternative method for specifying this feature. For the LVTTTL output buffers (OBUF, OBUFT, and IOBUF), the desired drive strength can be specified with the DRIVE= property. This property could have one of the following seven values.

```
DRIVE=2
```

```
DRIVE=4
```

```
DRIVE=6
```

```
DRIVE=8
```

```
DRIVE=12 (Default)
```

```
DRIVE=16
```

```
DRIVE=24
```

Design Considerations

Reference Voltage (V_{REF}) Pins

Low-voltage I/O standards with a differential amplifier input buffer require an input reference voltage (V_{REF}). Provide the V_{REF} as an external signal to the device.

The voltage reference signal is “banked” within the device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See [Figure 38](#) for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

Within each V_{REF} bank, any input buffers that require a V_{REF} signal must be of the same type. Output buffers of any type and input buffers can be placed without requiring a reference voltage within the same V_{REF} bank.

Output Drive Source Voltage (V_{CCO}) Pins

Many of the low voltage I/O standards supported by SelectI/O devices require a different output drive source voltage (V_{CCO}). As a result each device can often have to support multiple output drive source voltages.

The Virtex-E series supports eight banks for the HQ and PQ packages. The CS package supports four V_{CCO} banks.

Output buffers within a given V_{CCO} bank must share the same output drive source voltage. Input buffers for LVTTTL, LVCMOS2, LVCMOS18, PCI33_3, and PCI 66_3 use the V_{CCO} voltage for Input V_{CCO} voltage.

Transmission Line Effects

The delay of an electrical signal along a wire is dominated by the rise and fall times when the signal travels a short distance. Transmission line delays vary with inductance and capacitance, but a well-designed board can experience delays of approximately 180 ps per inch.

Transmission line effects, or reflections, typically start at 1.5" for fast (1.5 ns) rise and fall times. Poor (or non-existent) termination or changes in the transmission line impedance cause these reflections and can cause additional delay in longer traces. As system speeds continue to increase, the effect of I/O delays can become a limiting factor and therefore transmission line termination becomes increasingly more important.

Termination Techniques

A variety of termination techniques reduce the impact of transmission line effects.

The following are output termination techniques:

- None
- Series
- Parallel (Shunt)
- Series and Parallel (Series-Shunt)

Virtex-E Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted

Global Clock Set-Up and Hold for LVTTL Standard, *with DLL*

Description ⁽¹⁾	Symbol	Device	Speed Grade ^(2, 3)				Units
			Min	-8	-7	-6	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in IOB Input Switching Characteristics Standard Adjustments , page 8.							
No Delay	T _{PSDLL} /T _{PHDLL}	XCV50E	1.5 / −0.4	1.5 / −0.4	1.6 / −0.4	1.7 / −0.4	ns
Global Clock and IFF, with DLL		XCV100E	1.5 / −0.4	1.5 / −0.4	1.6 / −0.4	1.7 / −0.4	ns
		XCV200E	1.5 / −0.4	1.5 / −0.4	1.6 / −0.4	1.7 / −0.4	ns
		XCV300E	1.5 / −0.4	1.5 / −0.4	1.6 / −0.4	1.7 / −0.4	ns
		XCV400E	1.5 / −0.4	1.5 / −0.4	1.6 / −0.4	1.7 / −0.4	ns
		XCV600E	1.5 / −0.4	1.5 / −0.4	1.6 / −0.4	1.7 / −0.4	ns
		XCV1000E	1.5 / −0.4	1.5 / −0.4	1.6 / −0.4	1.7 / −0.4	ns
		XCV1600E	1.5 / −0.4	1.5 / −0.4	1.6 / −0.4	1.7 / −0.4	ns
		XCV2000E	1.5 / −0.4	1.5 / −0.4	1.6 / −0.4	1.7 / −0.4	ns
		XCV2600E	1.5 / −0.4	1.5 / −0.4	1.6 / −0.4	1.7 / −0.4	ns
XCV3200E	1.5 / −0.4	1.5 / −0.4	1.6 / −0.4	1.7 / −0.4	ns		

Notes:

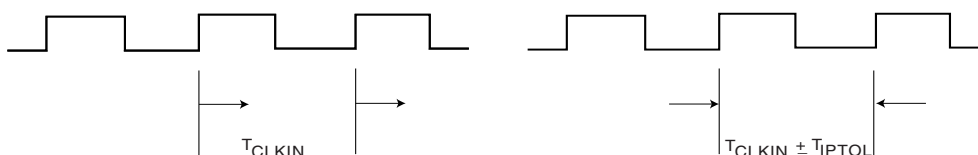
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. DLL output jitter is already included in the timing calculation.

DLL Timing Parameters

All devices are 100 percent functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

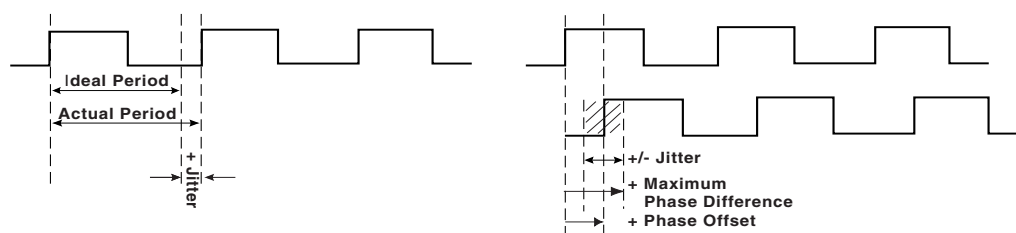
Description	Symbol	F _{CLKIN}	Speed Grade						Units
			-8		-7		-6		
			Min	Max	Min	Max	Min	Max	
Input Clock Frequency (CLKDLLHF)	FCLKINHF		60	350	60	320	60	275	MHz
Input Clock Frequency (CLKDLL)	FCLKINLF		25	160	25	160	25	135	MHz
Input Clock Low/High Pulse Width	T _{DLLPW}	≥2□5 MHz	5.0		5.0		5.0		ns
		≥□50 MHz	3.0		3.0		3.0		ns
		≥100 MHz	2.4		2.4		2.4		ns
		≥□150 MHz	2.0		2.0		2.0		ns
		≥□200 MHz	1.8		1.8		1.8		ns
		≥□250 MHz	1.5		1.5		1.5		ns
		≥□300 MHz	1.3		1.3		NA		ns

Period Tolerance: the allowed input clock period change in nanoseconds.



Output Jitter: the difference between an ideal reference clock edge and the actual design.

Phase Offset and Maximum Phase Difference



ds022_24_091200

Figure 4: DLL Timing Waveforms

Date	Version	Revision
07/23/01	2.2	- Under Absolute Maximum Ratings, changed (T_{SOL}) to 220 °C. - Changes made to SSTL symbol names in IOB Input Switching Characteristics Standard Adjustments table.
07/26/01	2.3	Removed T_{SOL} parameter and added footnote to Absolute Maximum Ratings table.
9/18/01	2.4	Reworded power supplies footnote to Absolute Maximum Ratings table.
10/25/01	2.5	- Updated the speed grade designations used in data sheets, and added Table 1, which shows the current speed grade designation for each device. - Added XCV2600E and XCV3200E values to DC Characteristics Over Recommended Operating Conditions and Power-On Power Supply Requirements tables.
11/09/01	2.6	Updated the Power-On Power Supply Requirements table.
02/01/02	2.7	Updated footnotes to the DC Input and Output Levels and DLL Clock Tolerance, Jitter, and Phase Information tables.
07/17/02	2.8	- Data sheet designation upgraded from Preliminary to Production. - Removed mention of MIL-M-38510/605 specification. - Added link to XAPP158 from the Power-On Power Supply Requirements section.
09/10/02	2.9	- Revised V_{IN} in Absolute Maximum Ratings table. - Added Clock CLK switching characteristics to Table 2, “IOB Input Switching Characteristics,” on page 6 and IOB Output Switching Characteristics, Figure 1.
12/22/02	2.9.1	- Added footnote regarding V_{IN} PCI compliance to Absolute Maximum Ratings table. - The fastest ramp rate is 0V to nominal voltage in 2 ms
03/14/03	2.9.2	Under Power-On Power Supply Requirements, the fastest ramp rate is no longer a "suggested" rate.

Virtex-E Data Sheet

The Virtex-E Data Sheet contains the following modules:

- DS022-1, Virtex-E 1.8V FPGAs:
[Introduction and Ordering Information \(Module 1\)](#)
- DS022-2, Virtex-E 1.8V FPGAs:
[Functional Description \(Module 2\)](#)
- DS022-3, Virtex-E 1.8V FPGAs:
DC and Switching Characteristics (Module 3)
- DS022-4, Virtex-E 1.8V FPGAs:
[Pinout Tables \(Module 4\)](#)

Table 10: BG352 — XCV100E, XCV200E, XCV300E

Bank	Pin Description	Pin #
2	IO_D3_L30N_Y	M3
2	IO_L31P	M2
2	IO_L31N	M1
2	IO	N3 ¹
2	IO_L32P_YY	N4
2	IO_L32N_YY	N2
3	IO	P1
3	IO	P3 ¹
3	IO_L33P	R1
3	IO_L33N	R2
3	IO_D4_L34P_Y	R3
3	IO_VREF_3_L34N_Y	R4
3	IO_L35P_YY	T2
3	IO_L35N_YY	U2
3	IO	T3 ¹
3	IO_L36P	T4
3	IO_L36N	V1
3	IO	V2 ¹
3	IO_L37P_YY	U3
3	IO_D5_L37N_YY	U4
3	IO_D6_L38P_Y	V3
3	IO_VREF_3_L38N_Y	V4
3	IO_L39P_Y	Y1
3	IO_L39N_Y	Y2
3	IO	W3
3	IO	W4 ¹
3	IO	AA1 ¹
3	IO_L40P_Y	AA2
3	IO_VREF_3_L40N_Y	Y3
3	IO_L41P_YY	AC1
3	IO_L41N_YY	AB2
3	IO	AA3 ¹
3	IO_L42P_YY	AA4

Table 10: BG352 — XCV100E, XCV200E, XCV300E

Bank	Pin Description	Pin #
3	IO_VREF_3_L42N_YY	AC2 ²
3	IO	AB3
3	IO	AD1 ¹
3	IO	AB4 ¹
3	IO_D7_L43P_YY	AC3
3	IO_INIT_L43N_YY	AD2
4	IO_L44P_YY	AC5
4	IO_L44N_YY	AD4
4	IO	AE3 ¹
4	IO	AD5 ¹
4	IO	AC6
4	IO_VREF_4_L45P_YY	AE4 ²
4	IO_L45N_YY	AF3
4	IO	AF4 ¹
4	IO_L46P_YY	AC7
4	IO_L46N_YY	AD6
4	IO_VREF_4_L47P_YY	AE5
4	IO_L47N_YY	AE6
4	IO	AD7 ¹
4	IO	AE7 ¹
4	IO_L48P	AF6
4	IO_L48N	AC9
4	IO	AD8
4	IO_VREF_4_L49P_YY	AE8
4	IO_L49N_YY	AF7
4	IO_L50P_YY	AD9
4	IO_L50N_YY	AE9
4	IO	AD10 ¹
4	IO_L51P	AF9
4	IO_L51N	AC11
4	IO	AE10 ¹
4	IO_L52P_Y	AD11
4	IO_L52N_Y	AE11

Table 12: BG432 — XCV300E, XCV400E, XCV600E

Bank	Pin Description	Pin #
7	IO_L132P_Y	G28
7	IO_L133N	E31
7	IO_L133P	E30
7	IO_L134N_Y	F29
7	IO_VREF_L134P_Y	F28
7	IO_L135N_Y	D31
7	IO_L135P_Y	D30
7	IO_L136N	E29
7	IO_L136P	E28
2	CCLK	D4
3	DONE	AH4
NA	DXN	AH27
NA	DXP	AK29
NA	M0	AH28
NA	M1	AH29
NA	M2	AJ28
NA	PROGRAM	AH3
NA	TCK	D28
NA	TDI	B3
2	TDO	C4
NA	TMS	D29
NA	VCCINT	A10
NA	VCCINT	A17
NA	VCCINT	B23
NA	VCCINT	B26
NA	VCCINT	C7
NA	VCCINT	C14
NA	VCCINT	C19
NA	VCCINT	F1
NA	VCCINT	F30
NA	VCCINT	K3
NA	VCCINT	K29
NA	VCCINT	N2
NA	VCCINT	N29

Table 12: BG432 — XCV300E, XCV400E, XCV600E

Bank	Pin Description	Pin #
NA	VCCINT	T1
NA	VCCINT	T29
NA	VCCINT	W2
NA	VCCINT	W31
NA	VCCINT	AB2
NA	VCCINT	AB30
NA	VCCINT	AE29
NA	VCCINT	AF1
NA	VCCINT	AH8
NA	VCCINT	AH24
NA	VCCINT	AJ10
NA	VCCINT	AJ16
NA	VCCINT	AK22
NA	VCCINT	AK13
NA	VCCINT	AK19
0	VCCO	A21
0	VCCO	C29
0	VCCO	D21
1	VCCO	A1
1	VCCO	A11
1	VCCO	D11
2	VCCO	C3
2	VCCO	L4
2	VCCO	L1
3	VCCO	AA1
3	VCCO	AA4
3	VCCO	AJ3
4	VCCO	AH11
4	VCCO	AL1
4	VCCO	AL11
5	VCCO	AH21
5	VCCO	AL21
5	VCCO	AJ29
6	VCCO	AA28
6	VCCO	AA31

Table 14: BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin#	See Note
4	IO_L104N_YY	AJ12	
4	IO_L105P_Y	AN11	
4	IO_L105N_Y	AK12	
4	IO_L106P_YY	AL12	
4	IO_L106N_YY	AM12	
4	IO_VREF_L107P_YY	AK13	3
4	IO_L107N_YY	AL13	
4	IO_L108P_Y	AM13	
4	IO_L108N_Y	AN13	
4	IO_L109P_YY	AJ14	
4	IO_L109N_YY	AK14	
4	IO_VREF_L110P_YY	AM14	
4	IO_L110N_YY	AN15	
4	IO_L111P_Y	AJ15	
4	IO_L111N_Y	AK15	
4	IO_L112P_Y	AL15	
4	IO_L112N_Y	AM16	
4	IO_VREF_L113P_Y	AL16	
4	IO_L113N_Y	AJ16	
4	IO_L114P_Y	AK16	
4	IO_VREF_L114N_Y	AN17	2
4	IO_LVDS_DLL_L115P	AM17	
5	GCK1	AJ17	
5	IO	AL25	
5	IO	AL28	
5	IO	AL30	
5	IO	AN28	
5	IO_LVDS_DLL_L115N	AM18	
5	IO_VREF	AL18	2
5	IO_L116P_Y	AK18	
5	IO_VREF_L116N_Y	AJ18	
5	IO_L117P_Y	AN19	
5	IO_L117N_Y	AL19	
5	IO_L118P_Y	AK19	

Table 14: BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin#	See Note
5	IO_L118N_Y	AM20	
5	IO_L119P_YY	AJ19	
5	IO_VREF_L119N_YY	AL20	
5	IO_L120P_YY	AN21	
5	IO_L120N_YY	AL21	
5	IO_L121P_Y	AJ20	
5	IO_L121N_Y	AM22	
5	IO_L122P_YY	AK21	
5	IO_VREF_L122N_YY	AN23	3
5	IO_L123P_YY	AJ21	
5	IO_L123N_YY	AM23	
5	IO_L124P_Y	AK22	
5	IO_L124N_Y	AM24	
5	IO_L125P_YY	AL23	
5	IO_L125N_YY	AJ22	
5	IO_L126P_YY	AK23	
5	IO_VREF_L126N_YY	AL24	
5	IO_L127P_Y	AN26	
5	IO_L127N_Y	AJ23	
5	IO_L128P_Y	AK24	
5	IO_VREF_L128N_Y	AM26	4
5	IO_L129P_Y	AM27	
5	IO_L129N_Y	AJ24	
5	IO_L130P_Y	AL26	
5	IO_VREF_L130N_Y	AK25	1
5	IO_L131P_YY	AN29	
5	IO_VREF_L131N_YY	AJ25	
5	IO_L132P_YY	AK26	
5	IO_L132N_YY	AM29	
5	IO_L133P_Y	AM30	
5	IO_L133N_Y	AJ26	
5	IO_L134P_YY	AK27	
5	IO_VREF_L134N_YY	AL29	
5	IO_L135P_YY	AN31	
5	IO_L135N_YY	AJ27	

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
3	IO	Y26
3	IO	AB25
3	IO	AC25 ¹
3	IO	AC26
3	IO_L69P_YY	P21
3	IO_L69N_YY	P23
3	IO_L70P_Y	P22
3	IO_VREF_L70N_Y	R25
3	IO_L71P_Y	P19
3	IO_L71N_Y	P20
3	IO_L72P_YY	R21
3	IO_L72N_YY	R22
3	IO_D4_L73P_YY	R24
3	IO_VREF_L73N_YY	R23
3	IO_L74P_Y	T24
3	IO_L74N_Y	R20
3	IO_L75P_Y	T22
3	IO_L75N_Y	U24
3	IO_L76P_Y	T23
3	IO_L76N_Y	U25
3	IO_L77P_Y	T21
3	IO_L77N_Y	U20
3	IO_L78P_YY	U22
3	IO_L78N_YY	V26
3	IO_L79P_YY	T20
3	IO_D5_L79N_YY	U23
3	IO_D6_L80P_YY	V24
3	IO_VREF_L80N_YY	U21
3	IO_L81P_YY	V23
3	IO_L81N_YY	W24
3	IO_L82P_Y	V22
3	IO_VREF_L82N_Y	W26 ²
3	IO_L83P_Y	Y25
3	IO_L83N_Y	V21
3	IO_L84P_YY	V20
3	IO_L84N_YY	AA26
3	IO_L85P_YY	Y24

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
3	IO_VREF_L85N_YY	W23
3	IO_L86P_Y	AA24
3	IO_L86N_Y	Y23
3	IO_L87P_Y	AB26
3	IO_L87N_Y	W21
3	IO_L88P_Y	Y22
3	IO_VREF_L88N_Y	W22
3	IO_L89P_Y	AA23
3	IO_L89N_Y	AB24
3	IO_L90P_YY	W20
3	IO_L90N_YY	AC24
3	IO_D7_L91P_YY	AB23
3	IO_INIT_L91N_YY	Y21
4	GCK0	AA14
4	IO	AC18
4	IO	AE15 ¹
4	IO	AE20
4	IO	AE23
4	IO	AF14 ¹
4	IO	AF16 ¹
4	IO	AF18 ¹
4	IO	AF21
4	IO	AF23 ¹
4	IO_L92P_YY	AC22
4	IO_L92N_YY	AD26
4	IO_L93P_Y	AD23
4	IO_L93N_Y	AA20
4	IO_L94P_YY	Y19
4	IO_L94N_YY	AC21
4	IO_VREF_L95P_YY	AD22
4	IO_L95N_YY	AB20
4	IO_L96P	AE22
4	IO_L96N	Y18
4	IO_L97P	AF22
4	IO_L97N	AA19
4	IO_VREF_L98P_YY	AD21

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
4	IO_L98N_YY	AB19
4	IO_L99P_YY	AC20
4	IO_L99N_YY	AA18
4	IO_L100P_Y	AC19
4	IO_L100N_Y	AD20
4	IO_VREF_L101P_Y	AF20 ²
4	IO_L101N_Y	AB18
4	IO_L102P	AD19
4	IO_L102N	Y17
4	IO_L103P	AE19
4	IO_VREF_L103N	AD18
4	IO_L104P_YY	AF19
4	IO_L104N_YY	AA17
4	IO_L105P_Y	AC17
4	IO_L105N_Y	AB17
4	IO_L106P_YY	Y16
4	IO_L106N_YY	AE17
4	IO_L107P_YY	AF17
4	IO_L107N_YY	AA16
4	IO_L108P	AD17
4	IO_L108N	AB16
4	IO_L109P_YY	AC16
4	IO_L109N_YY	AD16
4	IO_VREF_L110P_YY	AC15
4	IO_L110N_YY	Y15
4	IO_L111P_YY	AD15
4	IO_L111N_YY	AA15
4	IO_L112P_Y	W14
4	IO_L112N_Y	AB15
4	IO_VREF_L113P_Y	AF15
4	IO_L113N_Y	Y14
4	IO_L114P	AD14
4	IO_L114N	AB14
4	IO_LVDS_DLL_L115P	AC14
5	GCK1	AB13
5	IO	Y13 ¹

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
5	IO	AD7
5	IO	AD13
5	IO	AE4
5	IO	AE7
5	IO	AE12 ¹
5	IO	AF3 ¹
5	IO	AF5
5	IO	AF10 ¹
5	IO	AF11 ¹
5	IO_LVDS_DLL_L115N	AF13
5	IO_L116P_Y	AA13
5	IO_VREF_L116N_Y	AF12
5	IO_L117P_Y	AC13
5	IO_L117N_Y	W13
5	IO_L118P_YY	AA12
5	IO_L118N_YY	AD12
5	IO_L119P_YY	AC12
5	IO_VREF_L119N_YY	AB12
5	IO_L120P_YY	AD11
5	IO_L120N_YY	Y12
5	IO_L121P	AB11
5	IO_L121N	AD10
5	IO_L122P_YY	AC11
5	IO_L122N_YY	AE10
5	IO_L123P_YY	AC10
5	IO_L123N_YY	AA11
5	IO_L124P_Y	Y11
5	IO_L124N_Y	AD9
5	IO_L125P_YY	AB10
5	IO_L125N_YY	AF9
5	IO_L126P_YY	AD8
5	IO_VREF_L126N_YY	AA10
5	IO_L127P_YY	AE8
5	IO_L127N_YY	Y10
5	IO_L128P_Y	AC9
5	IO_VREF_L128N_Y	AF8 ²
5	IO_L129P_Y	AF7

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
0	VCCO	H10
1	VCCO	J15
1	VCCO	J14
1	VCCO	H18
1	VCCO	H17
1	VCCO	H16
1	VCCO	H15
2	VCCO	N18
2	VCCO	M19
2	VCCO	M18
2	VCCO	L19
2	VCCO	K19
2	VCCO	J19
3	VCCO	V19
3	VCCO	U19
3	VCCO	T19
3	VCCO	R19
3	VCCO	R18
3	VCCO	P18
4	VCCO	W18
4	VCCO	W17
4	VCCO	W16
4	VCCO	W15
4	VCCO	V15
4	VCCO	V14
5	VCCO	W9
5	VCCO	W12
5	VCCO	W11
5	VCCO	W10
5	VCCO	V13
5	VCCO	V12
6	VCCO	V8
6	VCCO	U8
6	VCCO	T8
6	VCCO	R9
6	VCCO	R8
6	VCCO	P9

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
7	VCCO	N9
7	VCCO	M9
7	VCCO	M8
7	VCCO	L8
7	VCCO	K8
7	VCCO	J8
NA	GND	V25
NA	GND	V2
NA	GND	U17
NA	GND	U16
NA	GND	U15
NA	GND	U14
NA	GND	U13
NA	GND	U12
NA	GND	U11
NA	GND	U10
NA	GND	T17
NA	GND	T16
NA	GND	T15
NA	GND	T14
NA	GND	T13
NA	GND	T12
NA	GND	T11
NA	GND	T10
NA	GND	R17
NA	GND	R16
NA	GND	R15
NA	GND	R14
NA	GND	R13
NA	GND	R12
NA	GND	R11
NA	GND	R10
NA	GND	P25
NA	GND	P17
NA	GND	P16
NA	GND	P15

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
5	IO_L166P_YY	AV26
5	IO_L166N_YY	AW27
5	IO_L167P_Y	AU26
5	IO_L167N_Y	AV27
5	IO_L168P_Y	AT26
5	IO_L168N_Y	AW28
5	IO_L169P_YY	AU27
5	IO_L169N_YY	AV28
5	IO_L170P_YY	AW29
5	IO_VREF_L170N_YY	AT27
5	IO_L171P_Y	AW30
5	IO_L171N_Y	AU28
5	IO_L172P_Y	AV30
5	IO_L172N_Y	AV29
5	IO_L173P_YY	AW31
5	IO_VREF_L173N_YY	AU29
5	IO_L174P_YY	AV31
5	IO_L174N_YY	AT29
5	IO_L175P_Y	AW32
5	IO_VREF_L175N_Y	AU30 ³
5	IO_L176P_Y	AW33
5	IO_L176N_Y	AT30
5	IO_L177P_YY	AV33
5	IO_VREF_L177N_YY	AU31
5	IO_L178P_YY	AT31
5	IO_L178N_YY	AW34
5	IO_L179P_Y	AV32
5	IO_L179N_Y	AV34
5	IO_L180P_Y	AU32
5	IO_L180N_Y	AW35
5	IO_L181P_YY	AT32
5	IO_VREF_L181N_YY	AV35
5	IO_L182P_YY	AU33
5	IO_L182N_YY	AW36
5	IO_L183P_Y	AT33
5	IO_VREF_L183N_Y	AV36 ¹

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
5	IO_L184P_Y	AU34
5	IO_L184N_Y	AU36
6	IO	W39
6	IO	AR37
6	IO	AR39
6	IO_L185N_YY	AR36
6	IO_L185P_YY	AT38
6	IO_L186N_Y	AR38
6	IO_L186P_Y	AP36
6	IO_VREF_L187N	AT39 ¹
6	IO_L187P	AP37
6	IO_L188N	AP38
6	IO_L188P	AP39
6	IO_VREF_L189N_Y	AN36
6	IO_L189P_Y	AN38
6	IO_L190N_YY	AN37
6	IO_L190P_YY	AN39
6	IO_L191N	AM36
6	IO_L191P	AM38
6	IO_L192N_Y	AM37
6	IO_L192P_Y	AL36
6	IO_VREF_L193N_YY	AM39
6	IO_L193P_YY	AL37
6	IO_L194N_YY	AL38
6	IO_L194P_YY	AK36
6	IO_VREF_L195N	AL39 ³
6	IO_L195P	AK37
6	IO_L196N	AK38
6	IO_L196P	AJ36
6	IO_VREF_L197N_YY	AK39
6	IO_L197P_YY	AJ37
6	IO_L198N_YY	AJ38
6	IO_L198P_YY	AH37
6	IO_L199N	AJ39
6	IO_L199P	AH38

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
4	IO_L147N_YY	AW7
4	IO_L148P_Y	AY7
4	IO_L148N_Y	BB8
4	IO_L149P_Y	BA9
4	IO_L149N_Y	AV8
4	IO_L150P_YY	AW8
4	IO_L150N_YY	BA10
4	IO_VREF_L151P_YY	BB10
4	IO_L151N_YY	AY8
4	IO_L152P_Y	AV9
4	IO_L152N_Y	BA11
4	IO_VREF_L153P_Y	BB11 ²
4	IO_L153N_Y	AW9
4	IO_L154P_YY	AY9
4	IO_L154N_YY	BA12
4	IO_VREF_L155P_YY	BB12
4	IO_L155N_YY	AV10
4	IO_L156P_Y	BA13
4	IO_L156N_Y	AW10
4	IO_L157P_Y	BB13
4	IO_L157N_Y	AY10
4	IO_VREF_L158P_YY	AV11
4	IO_L158N_YY	BA14
4	IO_L159P_YY	AW11
4	IO_L159N_YY	BB14
4	IO_L160P_Y	AV12
4	IO_L160N_Y	BA15
4	IO_L161P_Y	AW12
4	IO_L161N_Y	AY15
4	IO_L162P_Y	AW13
4	IO_L162N_Y	BB15
4	IO_L163P_Y	AV14
4	IO_L163N_Y	BA16
4	IO_L164P_YY	AW14
4	IO_L164N_YY	AY16
4	IO_VREF_L165P_YY	BB16
4	IO_L165N_YY	AV15

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
4	IO_L166P_Y	AY17
4	IO_L166N_Y	AW15
4	IO_L167P_Y	BB17
4	IO_L167N_Y	AU16
4	IO_L168P_YY	AV16
4	IO_L168N_YY	AY18
4	IO_VREF_L169P_YY	AW16
4	IO_L169N_YY	BA18
4	IO_L170P_Y	BB19
4	IO_L170N_Y	AW17
4	IO_L171P_Y	AY19
4	IO_L171N_Y	AV18
4	IO_L172P_YY	AW18
4	IO_L172N_YY	BB20
4	IO_VREF_L173P_YY	AY20
4	IO_L173N_YY	AV19
4	IO_L174P_Y	BB21
4	IO_L174N_Y	AW19
4	IO_VREF_L175P_Y	AY21 ¹
4	IO_L175N_Y	AV20
4	IO_LVDS_DLL_L176P	AW20
5	GCK1	AY22
5	IO	AV24
5	IO	AV34
5	IO	AW27
5	IO	AW36
5	IO	AY23
5	IO	AY31
5	IO	AY33
5	IO	BA26
5	IO	BA29
5	IO	BA33
5	IO	BB25
5	IO_LVDS_DLL_L176N	AW21
5	IO_L177P_Y	BB22
5	IO_VREF_L177N_Y	AW22 ¹

FG860 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A $\checkmark$ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 25: FG860 Differential Pin Pair Summary
XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
3	0	C22	A22	NA	IO_DLL_L34N
2	1	B22	D22	NA	IO_DLL_L34P
1	5	AY22	AW21	NA	IO_DLL_L176N
0	4	BA22	AW20	NA	IO_DLL_L176P
IO LVDS					
Total Pairs: 281, Asynchronous Output Pairs: 111					
0	0	D38	A38	2	-
1	0	E37	B37	1	-
2	0	C39	A37	1	VREF
3	0	C38	B36	1	-
4	0	B35	A36	$\checkmark$	-
5	0	D37	A35	$\checkmark$	VREF
6	0	A34	C37	5	-
7	0	B33	E36	5	-
8	0	C32	A33	$\checkmark$	-
9	0	B32	C36	$\checkmark$	VREF
10	0	D35	A32	1	-
11	0	C35	C31	1	VREF
12	0	A31	E34	$\checkmark$	-
13	0	C30	D34	$\checkmark$	VREF
14	0	E33	B30	2	-
15	0	D33	A30	2	-
16	0	B29	C33	$\checkmark$	VREF
17	0	A29	E32	$\checkmark$	-

Table 25: FG860 Differential Pin Pair Summary
XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
18	0	C28	D32	2	-
19	0	B28	E31	1	-
20	0	A28	D31	1	-
21	0	C27	D30	5	-
22	0	B27	E29	$\checkmark$	-
23	0	A27	D29	$\checkmark$	VREF
24	0	D28	C26	5	-
25	0	F27	B26	5	-
26	0	C25	E27	$\checkmark$	-
27	0	B25	D27	$\checkmark$	VREF
28	0	D26	A25	1	-
29	0	E25	A24	1	-
30	0	B24	D25	$\checkmark$	-
31	0	A23	E24	$\checkmark$	VREF
32	0	E23	C23	2	-
33	0	D23	B23	2	VREF
34	1	D22	A22	NA	IO_LVDS_DLL
35	1	B21	D21	2	VREF
36	1	A21	D20	2	-
37	1	D19	C20	$\checkmark$	VREF
38	1	E19	B20	$\checkmark$	-
39	1	A19	D18	1	-
40	1	C19	E18	1	-
41	1	E17	B19	$\checkmark$	VREF
42	1	D16	A18	$\checkmark$	-
43	1	B18	E16	5	-
44	1	A17	F16	5	-
45	1	E15	C17	$\checkmark$	VREF
46	1	D14	B17	$\checkmark$	-
47	1	E14	A16	5	-
48	1	D13	C16	1	-
49	1	D12	B16	1	-
50	1	E12	A15	2	-
51	1	C11	C15	$\checkmark$	-

Table 25: FG860 Differential Pin Pair Summary
XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
120	3	AH1	AL5	1	-
121	3	AH2	AM4	3	-
122	3	AH3	AM5	√	D5
123	3	AJ1	AN3	√	VREF
124	3	AN4	AJ3	2	-
125	3	AN5	AK1	√	-
126	3	AK2	AP4	√	VREF
127	3	AK3	AP5	2	-
128	3	AR3	AL2	5	VREF
129	3	AR4	AL3	√	-
130	3	AM1	AT3	√	VREF
131	3	AM2	AT4	1	-
132	3	AT5	AN1	2	-
133	3	AU3	AN2	√	-
134	3	AP1	AP2	1	VREF
135	3	AR1	AV3	2	-
136	3	AR2	AT1	4	-
137	3	AV4	AT2	2	VREF
138	3	AU1	AU5	1	-
139	3	AU2	AW3	3	-
140	3	AV1	AW5	√	INIT
141	4	AV6	BA4	√	-
142	4	AY4	BA5	2	-
143	4	AW6	BB5	1	-
144	4	BA6	AY5	1	VREF
145	4	BB6	AY6	5	-
146	4	BA7	AV7	√	-
147	4	BB7	AW7	√	VREF
148	4	AY7	BB8	5	-
149	4	BA9	AV8	5	-
150	4	AW8	BA10	√	-
151	4	BB10	AY8	√	VREF
152	4	AV9	BA11	1	-
153	4	BB11	AW9	1	VREF

Table 25: FG860 Differential Pin Pair Summary
XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
154	4	AY9	BA12	√	-
155	4	BB12	AV10	√	VREF
156	4	BA13	AW10	2	-
157	4	BB13	AY10	2	-
158	4	AV11	BA14	√	VREF
159	4	AW11	BB14	√	-
160	4	AV12	BA15	2	-
161	4	AW12	AY15	1	-
162	4	AW13	BB15	1	-
163	4	AV14	BA16	5	-
164	4	AW14	AY16	√	-
165	4	BB16	AV15	√	VREF
166	4	AY17	AW15	5	-
167	4	BB17	AU16	5	-
168	4	AV16	AY18	√	-
169	4	AW16	BA18	√	VREF
170	4	BB19	AW17	1	-
171	4	AY19	AV18	1	-
172	4	AW18	BB20	√	-
173	4	AY20	AV19	√	VREF
174	4	BB21	AW19	2	-
175	4	AY21	AV20	2	VREF
176	5	AW20	AW21	NA	IO_LVDS_DLL
177	5	BB22	AW22	2	VREF
178	5	BB23	AW23	2	-
179	5	AV23	BA23	√	VREF
180	5	AW24	BB24	√	-
181	5	AY24	AW25	1	-
182	5	BA24	AV25	1	-
183	5	AW26	AY25	√	VREF
184	5	AV26	BA25	√	-
185	5	BB26	AV27	5	-
186	5	AY26	AU27	5	-
187	5	AW28	BB27	√	VREF

Table 26: FG900 — XCV600E, XCV1000E, XCV1600E

Bank	Pin Description	Pin #
0	IO_L6N_Y	A5
0	IO_L6P_Y	F8
0	IO_L7N_Y	D7
0	IO_L7P_Y	N11
0	IO_L8N_YY	G9
0	IO_L8P_YY	E8
0	IO_VREF_L9N_YY	A6
0	IO_L9P_YY	J11
0	IO_L10N_Y	C7
0	IO_L10P_Y	B7
0	IO_L11N_Y	C8
0	IO_L11P_Y	H10
0	IO_L12N_YY	G10
0	IO_L12P_YY	F10
0	IO_VREF_L13N_YY	A8
0	IO_L13P_YY	H11
0	IO_L14N	D9 ⁴
0	IO_L14P	C9 ³
0	IO_L15N_YY	B9
0	IO_L15P_YY	J12
0	IO_L16N	E10 ⁴
0	IO_VREF_L16P	A9
0	IO_L17N	G11
0	IO_L17P	B10
0	IO_L18N_YY	H12 ⁴
0	IO_L18P_YY	C10 ⁴
0	IO_L19N_Y	H13
0	IO_L19P_Y	F11
0	IO_L20N_Y	E11
0	IO_L20P_Y	D11
0	IO_L21N_Y	B11 ⁴
0	IO_L21P_Y	G12 ⁴
0	IO_L22N_YY	F12
0	IO_L22P_YY	C11
0	IO_VREF_L23N_YY	A10 ¹
0	IO_L23P_YY	D12
0	IO_L24N_Y	E12

Table 26: FG900 — XCV600E, XCV1000E, XCV1600E

Bank	Pin Description	Pin #
0	IO_L24P_Y	A11
0	IO_L25N_Y	G13
0	IO_L25P_Y	B12
0	IO_L26N_YY	A12
0	IO_L26P_YY	K13
0	IO_VREF_L27N_YY	F13
0	IO_L27P_YY	B13
0	IO_L28N_Y	G14
0	IO_L28P_Y	E13
0	IO_L29N_Y	D14
0	IO_L29P_Y	B14
0	IO_L30N_YY	A14
0	IO_L30P_YY	J14
0	IO_VREF_L31N_YY	K14
0	IO_L31P_YY	J15
0	IO_L32N	B15 ⁴
0	IO_L32P	H15 ³
0	IO_VREF_L33N_YY	F15 ^{2,3}
0	IO_L33P_YY	D15 ⁴
0	IO_LVDS_DLL_L34N	A15
1	GCK2	E15
1	IO	A25 ⁴
1	IO	B17 ⁴
1	IO	B18 ⁴
1	IO	C23 ⁴
1	IO	D16 ⁴
1	IO	D17 ⁵
1	IO	D23 ⁴
1	IO	E19 ⁴
1	IO	E24 ⁵
1	IO	F22 ⁴
1	IO	G17 ⁵
1	IO	G20 ⁴
1	IO	J16 ⁴
1	IO	J17 ⁴
1	IO	J19 ⁵

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
1	IO_L66P_Y	E24
1	IO_L67N_YY	A26
1	IO_VREF_L67P_YY	C25
1	IO_L68N_YY	F24
1	IO_L68P_YY	B26
1	IO_L69N	K23 ⁵
1	IO_L69P	F25 ⁴
1	IO_L70N_Y	C26
1	IO_VREF_L70P_Y	H24 ²
1	IO_L71N_Y	G24
1	IO_L71P_Y	A27
1	IO_L72N	B27 ⁵
1	IO_L72P	G25 ⁴
1	IO_L73N_YY	E26
1	IO_VREF_L73P_YY	C27
1	IO_L74N_YY	J24
1	IO_L74P_YY	B28
1	IO_L75N	K24 ⁵
1	IO_L75P	H25 ⁴
1	IO_L76N_Y	D27
1	IO_L76P_Y	F26
1	IO_L77N_Y	G26
1	IO_L77P_Y	C28
1	IO_L78N_YY	E27 ⁵
1	IO_L78P_YY	J25 ⁴
1	IO_L79N_YY	A30
1	IO_VREF_L79P_YY	H26
1	IO_L80N_YY	G27
1	IO_L80P_YY	B29
1	IO_L81N_Y	F27
1	IO_L81P_Y	C29
1	IO_L82N_Y	E28
1	IO_VREF_L82P_Y	F28
1	IO_L83N_Y	L25

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
1	IO_L83P_Y	B30
1	IO_L84N	B31
1	IO_L84P	E29
1	IO_WRITE_L85N_YY	A31
1	IO_CS_L85P_YY	D30
2	IO	F31 ³
2	IO	J32
2	IO	K27 ³
2	IO	K31 ³
2	IO	L28 ³
2	IO	L30 ³
2	IO	M32 ³
2	IO	N26
2	IO	N28 ³
2	IO	P25 ³
2	IO	U26 ³
2	IO	U30
2	IO	U32 ³
2	IO	U34
2	IO_D2	M30
2	IO_DOUT_BUSY_L86P_YY	D32
2	IO_DIN_D0_L86N_YY	J27
2	IO_L87P_Y	E31
2	IO_L87N_Y	F30
2	IO_L88P_Y	G29
2	IO_L88N_Y	F32
2	IO_VREF_L89P_Y	E32
2	IO_L89N_Y	G30
2	IO_L90P	M25
2	IO_L90N	G31
2	IO_L91P_Y	L26
2	IO_L91N_Y	D33
2	IO_VREF_L92P_Y	D34

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
231	5	AH14	AP12	3200 2600 2000 1600 1000	-
232	5	AJ14	AL14	3200 2600 1000	-
233	5	AF13	AN12	3200 2000 1000	-
234	5	AF14	AP11	3200 2000 1000	-
235	5	AN11	AH13	3200 1600 1000	-
236	5	AM12	AL12	3200 2600 2000 1600 1000	-
237	5	AJ13	AP10	3200 2600 2000 1600 1000	VREF
238	5	AK12	AM10	2600 1600 1000	-
239	5	AP9	AK11	2600 1600 1000	-
240	5	AL11	AL10	3200 2600 2000 1600 1000	VREF
241	5	AE13	AM9	3200 2600 2000 1600 1000	-
242	5	AF12	AP8	3200 2600	-
243	5	AL9	AH11	3200 2000 1000	VREF
244	5	AF11	AN8	3200 2000 1000	-
245	5	AM8	AG11	3200 1600	-
246	5	AL8	AK9	3200 2600 2000 1600 1000	VREF
247	5	AH10	AN7	3200 2600 2000 1600 1000	-
248	5	AE12	AJ9	3200 2600	-
249	5	AM7	AL7	3200 1000	-
250	5	AG10	AN6	3200 1000	-

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
251	5	AK8	AH9	2000 1600	-
252	5	AP5	AJ8	3200 2600 2000 1600 1000	VREF
253	5	AE11	AN5	3200 2600 2000 1600 1000	-
254	5	AF10	AM6	3200 2600 1000	-
255	5	AL6	AG9	3200 2000 1000	VREF
256	5	AH8	AP4	3200 2000 1000	-
257	5	AN4	AJ7	3200 1600 1000	-
258	5	AM5	AK6	3200 2600 2000 1600 1000	-
259	6	AF8	AH6	3200 2600 2000 1600 1000	-
260	6	AK3	AE9	3200 2600 2000	-
261	6	AL2	AD10	2600 2000 1000	-
262	6	AH4	AL1	3200 2600 1600 1000	VREF
263	6	AK1	AG6	2600 1600	-
264	6	AK2	AF7	3200 2600 1600 1000	-
265	6	AG5	AJ3	2600 2000 1000	VREF
266	6	AJ2	AD9	3200 2600 2000 1600	-
267	6	AH2	AC10	3200 2600 2000 1600 1000	-
268	6	AF5	AH3	3200 2600 1600 1000	-
269	6	AG3	AE8	3200 2600 2000	-