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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	7776
Number of Logic Elements/Cells	34992
Total RAM Bits	589824
Number of I/O	404
Number of Gates	2188742
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	560-LBGA Exposed Pad, Metal
Supplier Device Package	560-MBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv1600e-7bg560c

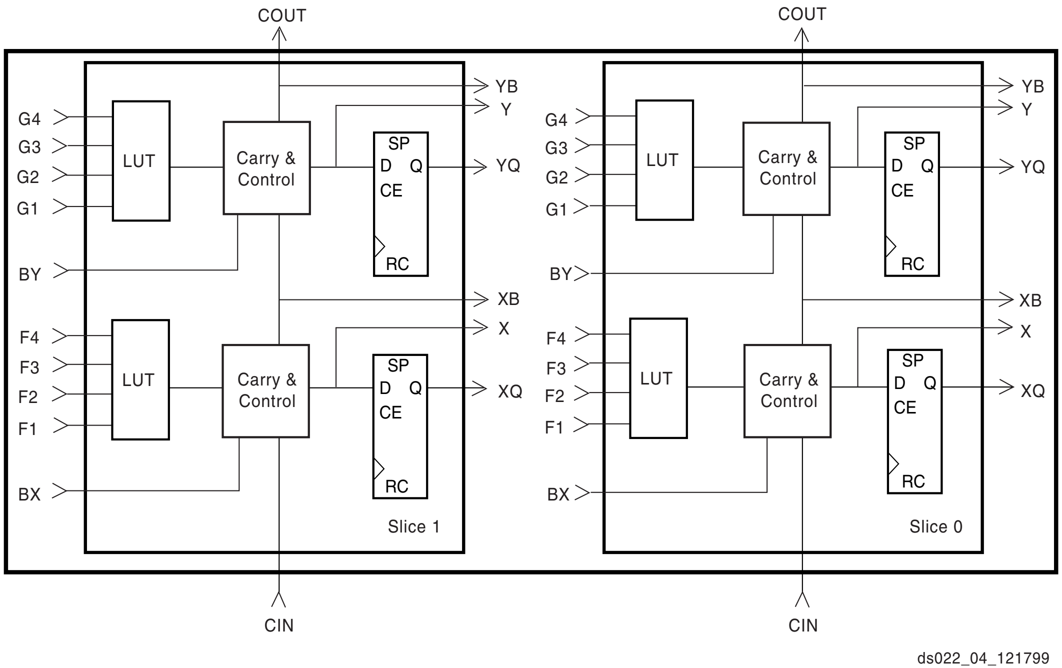

Figure 4: **2-Slice Virtex-E CLB**

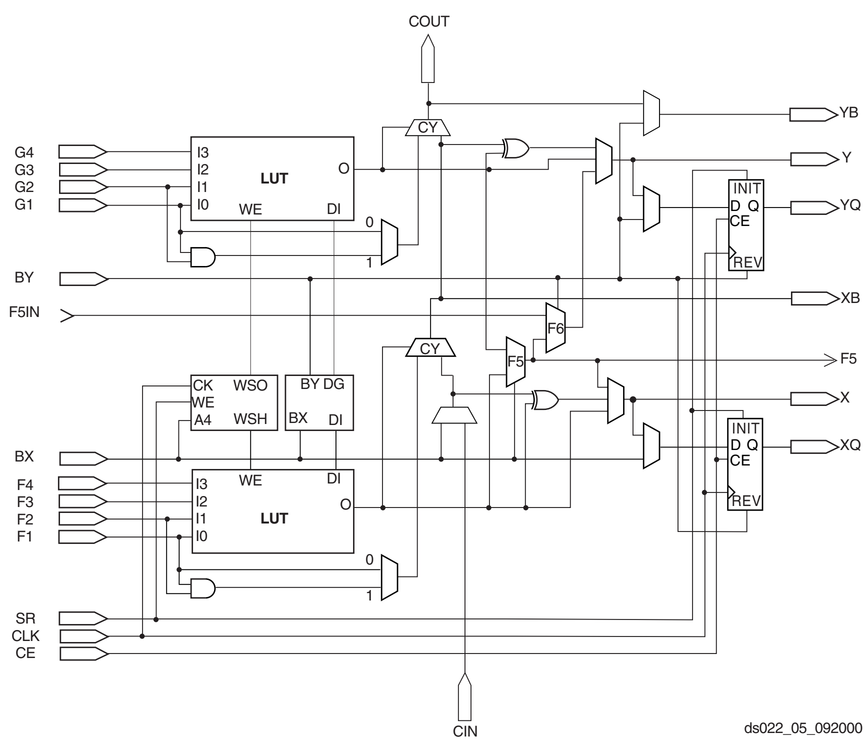

Figure 5: **Detailed View of Virtex-E Slice**

Storage Elements

The storage elements in the Virtex-E slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by the function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each Slice has synchronous set and reset signals (SR and BY). SR

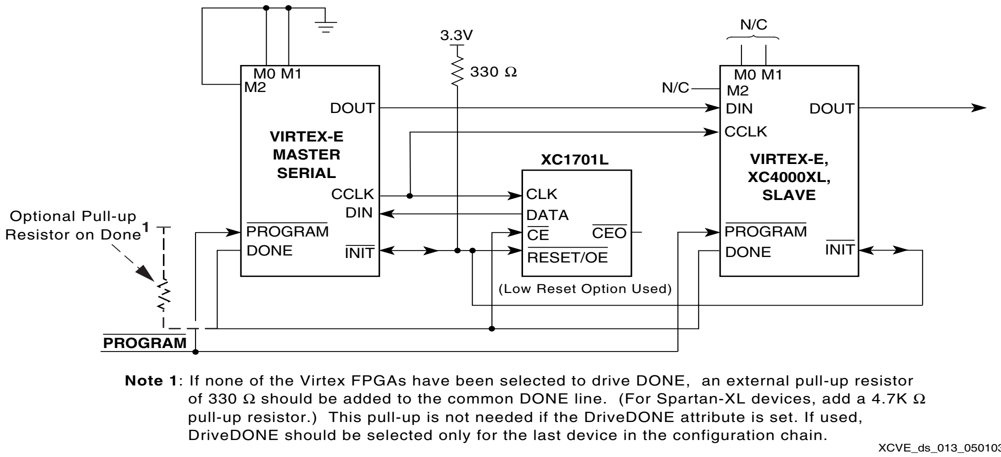

Figure 13: **Master/Slave Serial Mode Circuit Diagram**

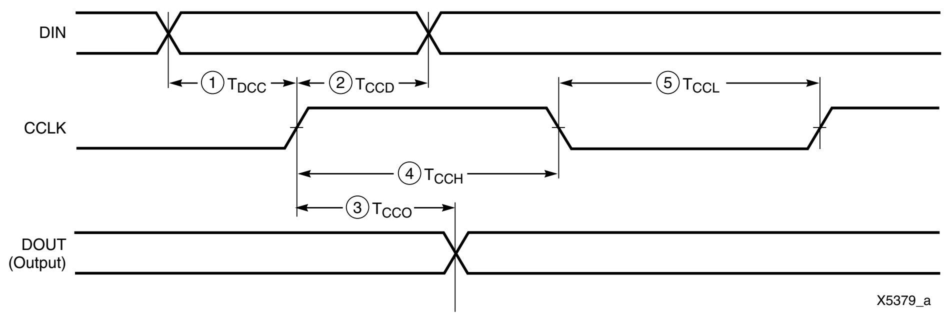

Figure 14: **Slave-Serial Mode Programming Switching Characteristics**

Master-Serial Mode

In master-serial mode, the CCLK output of the FPGA drives a Xilinx Serial PROM that feeds bit-serial data to the DIN input. The FPGA accepts this data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge. The maximum capacity for a single LOUT/DOUT write is 2^{20}-1 (1,048,575) 32-bit words, or 33,554,4000 bits.

The interface is identical to slave-serial except that an internal oscillator is used to generate the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK, which always starts at a slow default frequency. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration. Switching to a lower frequency is prohibited.

The CCLK frequency is set using the ConfigRate option in the bitstream generation software. The maximum CCLK frequency that can be selected is 60 MHz. When selecting a CCLK frequency, ensure that the serial PROM and any daisy-chained FPGAs are fast enough to support the clock rate.

On power-up, the CCLK frequency is approximately 2.5 MHz. This frequency is used until the ConfigRate bits have been loaded when the frequency changes to the selected ConfigRate. Unless a different frequency is specified in the design, the default ConfigRate is 4 MHz.

In a full master/slave system (Figure 13), the left-most device operates in master-serial mode. The remaining devices operate in slave-serial mode. The SPROM $\overline{\text{RESET}}$ pin is driven by $\overline{\text{INIT}}$, and the $\overline{\text{CE}}$ input is driven by DONE. There is the potential for contention on the DONE pin, depending on the start-up sequence options chosen.

The sequence of operations necessary to configure a Virtex-E FPGA serially appears in Figure 15.

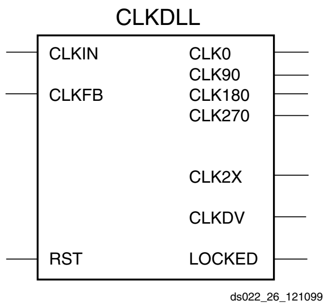

Figure 22: **Standard DLL Symbol CLKDLL**

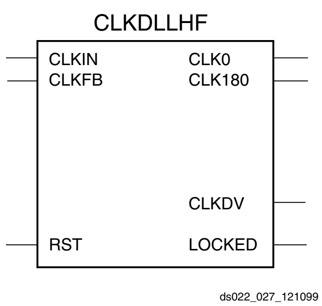

Figure 23: **High Frequency DLL Symbol CLKDLLHF**

BUFGDLL Pin Descriptions

Use the BUFGDLL macro as the simplest way to provide zero propagation delay for a high-fanout on-chip clock from an external input. This macro uses the IBUFG, CLKDLL and BUFG primitives to implement the most basic DLL application as shown in Figure 24.

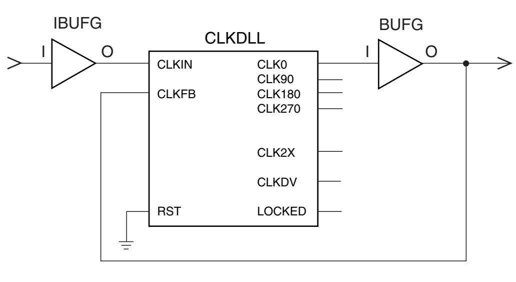

Figure 24: **BUFGDLL Schematic**

This symbol does not provide access to the advanced clock domain controls or to the clock multiplication or clock division features of the DLL. This symbol also does not provide access to the RST, or LOCKED pins of the DLL. For access to these features, a designer must use the library DLL primitives described in the following sections.

Source Clock Input — I

The I pin provides the user source clock, the clock signal on which the DLL operates, to the BUFGDLL. For the BUFGDLL macro the source clock frequency must fall in the low frequency range as specified in the data sheet. The BUFGDLL requires an external signal source clock. Therefore, only an external input port can source the signal that drives the BUFGDLL I pin.

Clock Output — O

The clock output pin O represents a delay-compensated version of the source clock (I) signal. This signal, sourced by a global clock buffer BUFG symbol, takes advantage of the dedicated global clock routing resources of the device.

The output clock has a 50-50 duty cycle unless you deactivate the duty cycle correction property.

CLKDLL Primitive Pin Descriptions

The library CLKDLL primitives provide access to the complete set of DLL features needed when implementing more complex applications with the DLL.

Source Clock Input — CLKIN

The CLKIN pin provides the user source clock (the clock signal on which the DLL operates) to the DLL. The CLKIN frequency must fall in the ranges specified in the data sheet. A global clock buffer (BUFG) driven from another CLKDLL, one of the global clock input buffers (IBUFG), or an IO_LVDS_DLL pin on the same edge of the device (top or bottom) must source this clock signal. There are four IO_LVDS_DLL input pins that can be used as inputs to the DLLs. This makes a total of eight usable input pins for DLLs in the Virtex-E family.

Feedback Clock Input — CLKFB

The DLL requires a reference or feedback signal to provide the delay-compensated output. Connect only the CLK0 or CLK2X DLL outputs to the feedback clock input (CLKFB) pin to provide the necessary feedback to the DLL. The feedback clock input can also be provided through one of the following pins.

IBUFG - Global Clock Input Pad

IO_LVDS_DLL - the pin adjacent to IBUFG

If an IBUFG sources the CLKFB pin, the following special rules apply.

1. An external input port must source the signal that drives the IBUFG I pin.
2. The CLK2X output must feedback to the device if both the CLK0 and CLK2X outputs are driving off chip devices.
3. That signal must directly drive only OBUFs and nothing else.

These rules enable the software determine which DLL clock output sources the CLKFB pin.

Reset Input — RST

When the reset pin RST activates the LOCKED signal deactivates within four source clock cycles. The RST pin, active High, must either connect to a dynamic signal or tied to

SSTL3_I

A sample circuit illustrating a valid termination technique for SSTL3_I appears in Figure 49. DC voltage specifications appear in Table 28.

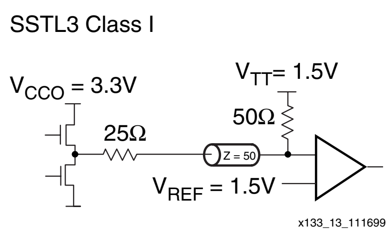

Figure 49: **Terminated SSTL3 Class I**

Table 28: **SSTL3_I Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	**3.0**	**3.3**	**3.6**
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} = V_{REF} + 0.2$	1.5	1.7	3.9(1)
$V_{IL} = V_{REF} – 0.2$	–0.3(2)	1.3	1.5
$V_{OH} = V_{REF} + 0.6$	1.9	-	-
$V_{OL} = V_{REF} – 0.6$	-	-	1.1
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL}at V_{OL} (mA)	8	-	-

Notes:
1. V_{IH} maximum is V_{CCO} + 0.3
2. V_{IL} minimum does not conform to the formula

SSTL3_II

A sample circuit illustrating a valid termination technique for SSTL3_II appears in Figure 50. DC voltage specifications appear in Table 29.

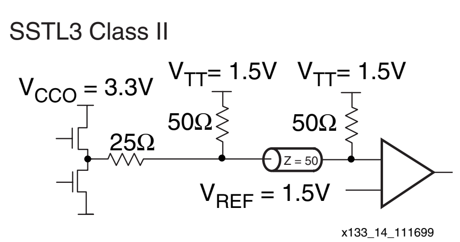

Figure 50: **Terminated SSTL3 Class II**

Table 29: **SSTL3_II Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} = V_{REF} + 0.2$	1.5	1.7	3.9(1)
$V_{IL}= V_{REF} – 0.2$	–0.3(2)	1.3	1.5
$V_{OH} = V_{REF} + 0.8$	2.1	-	-
$V_{OL}= V_{REF} – 0.8$	-	-	0.9
I_{OH} at V_{OH} (mA)	–16	-	-
I_{OL}at V_{OL} (mA)	16	-	-

Notes:
1. V_{IH} maximum is V_{CCO} + 0.3
2. V_{IL} minimum does not conform to the formula

SSTL2_I

A sample circuit illustrating a valid termination technique for SSTL2_I appears in Figure 51. DC voltage specifications appear in Table 30.

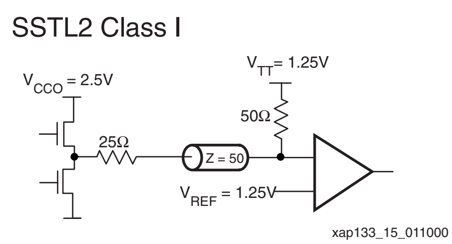

Figure 51: **Terminated SSTL2 Class I**

Table 30: **SSTL2_I Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
$V_{REF} = 0.5 \times V_{CCO}$	1.15	1.25	1.35
$V_{TT} = V_{REF} + N$(1)	1.11	1.25	1.39
$V_{IH} = V_{REF} + 0.18$	1.33	1.43	3.0(2)
$V_{IL} = V_{REF} – 0.18$	–0.3(3)	1.07	1.17
$V_{OH} = V_{REF} + 0.61$	1.76	-	-
$V_{OL}= V_{REF} – 0.61$	-	-	0.74
I_{OH} at V_{OH} (mA)	–7.6	-	-
I_{OL}at V_{OL} (mA)	7.6	-	-

Notes:
1. N must be greater than or equal to -0.04 and less than or equal to 0.04.
2. V_{IH} maximum is V_{CCO} + 0.3.
3. V_{IL} minimum does not conform to the formula.

LVDS

Depending on whether the device is transmitting an LVDS signal or receiving an LVDS signal, there are two different circuits used for LVDS termination. A sample circuit illustrating a valid termination technique for transmitting LVDS signals appears in Figure 54. A sample circuit illustrating a valid termination for receiving LVDS signals appears in Figure 55. Table 38 lists DC voltage specifications. Further information on the specific termination resistor packs shown can be found on Table 40.

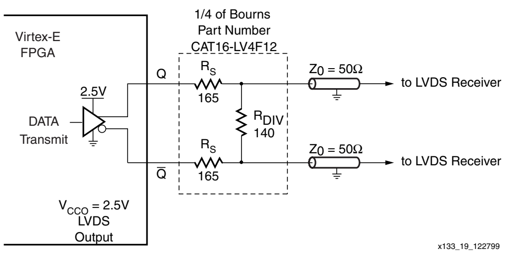

Figure 54: **Transmitting LVDS Signal Circuit**

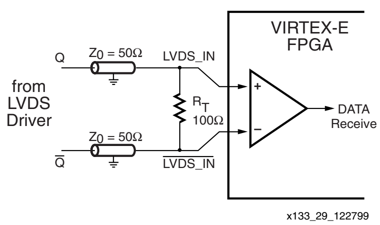

Figure 55: **Receiving LVDS Signal Circuit**

Table 38: **LVDS Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	2.375	2.5	2.625
V_{ICM} (2)	0.2	1.25	2.2
V_{OCM} (1)	1.125	1.25	1.375
V_{IDIFF} (1)	0.1	0.35	-
V_{ODIFF} (1)	0.25	0.35	0.45
V_{OH} (1)	1.25	-	-
V_{OL} (1)	-	-	1.25

Notes:

1. Measured with a 100 Ω resistor across Q and $\overline{Q}$.
2. Measured with a differential input voltage = +/− 350 mV.

LVPECL

Depending on whether the device is transmitting or receiving an LVPECL signal, two different circuits are used for LVPECL termination. A sample circuit illustrating a valid termination technique for transmitting LVPECL signals appears in Figure 56. A sample circuit illustrating a valid termination for receiving LVPECL signals appears in Figure 57. Table 39 lists DC voltage specifications. Further information on the specific termination resistor packs shown can be found on Table 40.

Table 39: **LVPECL Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
V_{REF}	-	-	-
V_{TT}	-	-	-
V_{IH}	1.49	-	2.72
V_{IL}	0.86	-	2.125
V_{OH}	1.8	-	-
V_{OL}	-	-	1.57

Notes:

1. For more detailed information, see **DS022-3**: *Virtex-E 1.8V FPGA DC and Switching Characteristics*, Module 3, LVPECL DC Specifications section.

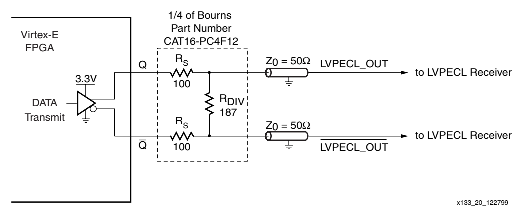

Figure 56: **Transmitting LVPECL Signal Circuit**

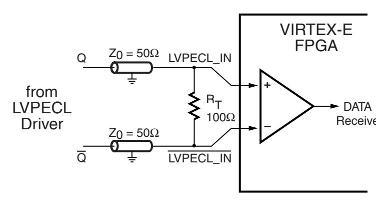

Figure 57: **Receiving LVPECL Signal Circuit**

Virtex-E Data Sheet

The Virtex-E Data Sheet contains the following modules:

- DS022-1, Virtex-E 1.8V FPGAs:
  Introduction and Ordering Information (Module 1)
- DS022-2, Virtex-E 1.8V FPGAs:
  Functional Description (Module 2)
- DS022-3, Virtex-E 1.8V FPGAs:
  DC and Switching Characteristics (Module 3)
- DS022-4, Virtex-E 1.8V FPGAs:
  Pinout Tables (Module 4)

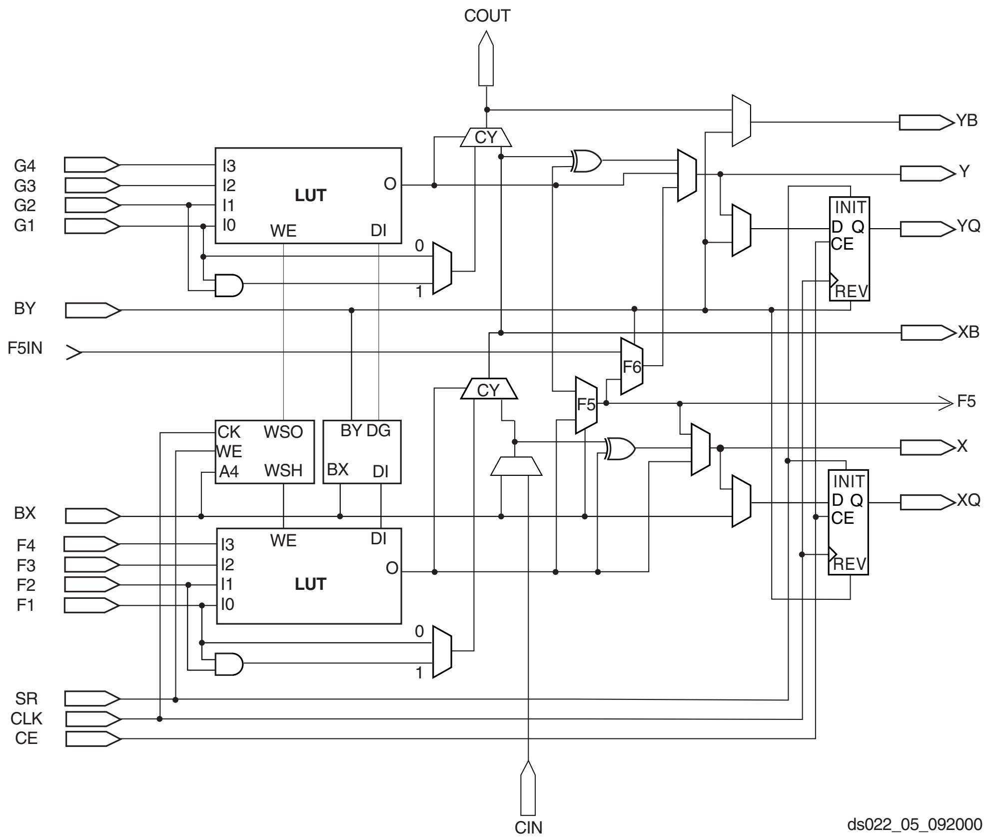

Figure 2: **Detailed View of Virtex-E Slice**

Virtex-E Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *with* DLL

Description(1)	Symbol	Device	Speed Grade(2, 3)				Units
			Min	-8	-7	-6	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *with* DLL. For data *output* with different standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 10.	$T_{ICKOFDLL}$	XCV50E	1.0	3.1	3.1	3.1	ns
		XCV100E	1.0	3.1	3.1	3.1	ns
		XCV200E	1.0	3.1	3.1	3.1	ns
		XCV300E	1.0	3.1	3.1	3.1	ns
		XCV400E	1.0	3.1	3.1	3.1	ns
		XCV600E	1.0	3.1	3.1	3.1	ns
		XCV1000E	1.0	3.1	3.1	3.1	ns
		XCV1600E	1.0	3.1	3.1	3.1	ns
		XCV2000E	1.0	3.1	3.1	3.1	ns
		XCV2600E	1.0	3.1	3.1	3.1	ns
		XCV3200E	1.0	3.1	3.1	3.1	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For other I/O standards and different loads, see Table 3 and Table 4.
3. DLL output jitter is already included in the timing calculation.

CS144 Chip-Scale Package

XCV50E, XCV100E, XCV200E, XCV300E and XCV400E devices in CS144 Chip-scale packages have footprint compatibility. In the CS144 package, bank pairs that share a side are internally interconnected, permitting four choices for V_{CCO}. See Table 3.

Table 3: **I/O Bank Pairs and Shared Vcco Pins**

Paired Banks	Shared V_{CCO} Pins
Banks 0 & 1	A2, A13, D7
Banks 2 & 3	B12, G11, M13
Banks 4 & 5	N1, N7, N13
Banks 6 & 7	B2, G2, M2

Pins labeled I0_VREF can be used as either in all parts unless device-dependent, as indicated in the footnotes. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 4, see Table 5 is Differential Pair information.

Table 4: **CS144 — XCV50E, XCV100E, XCV200E**

Bank	Pin Description	Pin #
0	GCK3	A6
0	IO	B3
0	IO_VREF_L0N_YY	B4[2]
0	IO_L0P_YY	A4
0	IO_L1N_YY	B5
0	IO_L1P_YY	A5
0	IO_LVDS_DLL_L2N	C6
0	IO_VREF	A3[1]
0	IO_VREF	C4
0	IO_VREF	D6
1	GCK2	A7
1	IO	A8
1	IO_LVDS_DLL_L2P	B7
1	IO_L3N_YY	C8
1	IO_L3P_YY	D8
1	IO_L4N_YY	C9
1	IO_VREF_L4P_YY	D9[2]
1	IO_WRITE_L5N_YY	C10
1	IO_CS_L5P_YY	D10

Table 4: **CS144 — XCV50E, XCV100E, XCV200E**

Bank	Pin Description	Pin #
1	IO_VREF	A10
1	IO_VREF	B8
1	IO_VREF	B10[1]
2	IO	D12
2	IO	F12
2	IO_DOUT_BUSY_L6P_YY	C11
2	IO_DIN_D0_L6N_YY	C12
2	IO_D1_L7N	E10
2	IO_VREF_L7P	D13[2]
2	IO_L8N_YY	E13
2	IO_D2_L8P_YY	E12
2	IO_D3_L9N	F11
2	IO_VREF_L9P	F10
2	IO_L10P	F13
2	IO_VREF	C13[1]
2	IO_VREF	D11
3	IO	H13
3	IO	K13
3	IO_L10N	G13
3	IO_VREF_L11N	H11
3	IO_D4_L11P	H12
3	IO_D5_L12N_YY	J13
3	IO_L12P_YY	H10
3	IO_VREF_L13N	J10[2]
3	IO_D6_L13P	J11
3	IO_INIT_L14N_YY	L13
3	IO_D7_L14P_YY	K10
3	IO_VREF	K11[1]
3	IO_VREF	K12
4	GCK0	K7
4	IO	M8
4	IO	M10

Table 12: **BG432 — XCV300E, XCV400E, XCV600E**

Bank	Pin Description	Pin #
6	IO	AA30
6	IO	AC30
6	IO	AD29
6	IO	U31
6	IO	W28
6	IO_L103N_YY	AJ30
6	IO_L103P_YY	AH30
6	IO_L104N	AG28
6	IO_L104P	AH31
6	IO_L105N_Y	AG29
6	IO_L105P_Y	AG30
6	IO_VREF_L106N_Y	AF28
6	IO_L106P_Y	AG31
6	IO_L107N	AF29
6	IO_L107P	AF30
6	IO_L108N_Y	AE28
6	IO_L108P_Y	AF31
6	IO_VREF_L109N_YY	AE30
6	IO_L109P_YY	AD28
6	IO_L110N_Y	AD30
6	IO_L110P_Y	AD31
6	IO_VREF_L111N_Y	AC28[1]
6	IO_L111P_Y	AC29
6	IO_VREF_L112N_YY	AB28
6	IO_L112P_YY	AB29
6	IO_L113N_YY	AB31
6	IO_L113P_YY	AA29
6	IO_L114N_Y	Y28
6	IO_L114P_Y	Y29
6	IO_L115N_Y	Y30
6	IO_L115P_Y	Y31
6	IO_L116N_Y	W29
6	IO_L116P_Y	W30
6	IO_VREF_L117N_YY	V28
6	IO_L117P_YY	V29
6	IO_L118N_Y	V30

Table 12: **BG432 — XCV300E, XCV400E, XCV600E**

Bank	Pin Description	Pin #
6	IO_L118P_Y	U29
6	IO_VREF_L119N_Y	U28[2]
6	IO_L119P_Y	U30
6	IO	T30
7	IO	C30
7	IO	H29
7	IO	H31
7	IO	L29
7	IO	M31
7	IO	R28
7	IO_L120N_YY	T31
7	IO_L120P_YY	R29
7	IO_L121N_Y	R30
7	IO_VREF_L121P_Y	R31[2]
7	IO_L122N_Y	P29
7	IO_L122P_Y	P28
7	IO_L123N_YY	P30
7	IO_VREF_L123P_YY	N30
7	IO_L124N_Y	N28
7	IO_L124P_Y	N31
7	IO_L125N_Y	M29
7	IO_L125P_Y	M28
7	IO_L126N_Y	M30
7	IO_L126P_Y	L30
7	IO_L127N_YY	K31
7	IO_L127P_YY	K30
7	IO_L128N_YY	K28
7	IO_VREF_L128P_YY	J30
7	IO_L129N_Y	J29
7	IO_VREF_L129P_Y	J28[1]
7	IO_L130N_Y	H30
7	IO_L130P_Y	G30
7	IO_L131N_YY	H28
7	IO_VREF_L131P_YY	F31
7	IO_L132N_Y	G29

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
1	IO_L43N_Y	C5	
1	IO_VREF_L43P_Y	E7	3
1	IO_WRITE_L44N_YY	D6	
1	IO_CS_L44P_YY	A2	
2	IO	D3	
2	IO	F3	
2	IO	G1	
2	IO	J2	
2	IO_DOUT_BUSY_L45P_YY	D4	
2	IO_DIN_D0_L45N_YY	E4	
2	IO_L46P_Y	F5	
2	IO_VREF_L46N_Y	B3	3
2	IO_L47P_Y	F4	
2	IO_L47N_Y	C1	
2	IO_VREF_L48P_Y	G5	
2	IO_L48N_Y	E3	
2	IO_L49P_Y	D2	
2	IO_L49N_Y	G4	
2	IO_L50P_Y	H5	
2	IO_L50N_Y	E2	
2	IO_VREF_L51P_YY	H4	
2	IO_L51N_YY	G3	
2	IO_L52P_Y	J5	
2	IO_VREF_L52N_Y	F1	1
2	IO_L53P_Y	J4	
2	IO_L53N_Y	H3	
2	IO_VREF_L54P_Y	K5	4
2	IO_L54N_Y	H2	
2	IO_L55P_Y	J3	
2	IO_L55N_Y	K4	
2	IO_VREF_L56P_YY	L5	
2	IO_D1_L56N_YY	K3	
2	IO_D2_L57P_YY	L4	
2	IO_L57N_YY	K2	

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
2	IO_L58P_Y	M5	
2	IO_L58N_Y	L3	
2	IO_L59P_Y	L1	
2	IO_L59N_Y	M4	
2	IO_VREF_L60P_Y	N5	3
2	IO_L60N_Y	M2	
2	IO_L61P_Y	N4	
2	IO_L61N_Y	N3	
2	IO_L62P_Y	N2	
2	IO_L62N_Y	P5	
2	IO_VREF_L63P_YY	P4	
2	IO_D3_L63N_YY	P3	
2	IO_L64P_Y	P2	
2	IO_L64N_Y	R5	
2	IO_L65P_Y	R4	
2	IO_L65N_Y	R3	
2	IO_VREF_L66P_Y	R1	
2	IO_L66N_Y	T4	
2	IO_L67P_Y	T5	
2	IO_VREF_L67N_Y	T3	2
2	IO_L68P_YY	T2	
2	IO_L68N_YY	U3	
3	IO	AE3	
3	IO	AF3	
3	IO	AH3	
3	IO	AK3	
3	IO_VREF_L69P_Y	U1	2
3	IO_L69N_Y	U2	
3	IO_L70P_Y	V2	
3	IO_VREF_L70N_Y	V4	
3	IO_L71P_Y	V5	
3	IO_L71N_Y	V3	
3	IO_L72P_Y	W1	
3	IO_L72N_Y	W3	

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
7	IO	D2
7	IO	D3
7	IO	E1
7	IO	G1
7	IO	H2
7	IO	J1[1]
7	IO	L1[1]
7	IO	M1[1]
7	IO	N1[1]
7	IO_L160N_YY	N5
7	IO_L160P_YY	N8
7	IO_L161N_YY	N6
7	IO_L161P_YY	N3
7	IO_L162N_Y	N4
7	IO_VREF_L162P_Y	M2
7	IO_L163N_Y	N7
7	IO_L163P_Y	M7
7	IO_L164N_YY	M6
7	IO_L164P_YY	M3
7	IO_L165N_YY	M4
7	IO_VREF_L165P_YY	M5
7	IO_L166N_Y	L3
7	IO_L166P_Y	L7
7	IO_L167N_Y	L6
7	IO_L167P_Y	K2
7	IO_L168N_Y	L4
7	IO_L168P_Y	K1
7	IO_L169N_Y	K3
7	IO_L169P_Y	L5
7	IO_L170N_YY	K5
7	IO_L170P_YY	J3
7	IO_L171N_YY	K4
7	IO_L171P_YY	J4
7	IO_L172N_YY	H3
7	IO_VREF_L172P_YY	K6
7	IO_L173N_YY	K7
7	IO_L173P_YY	G3

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
7	IO_L174N_Y	J5
7	IO_VREF_L174P_Y	H1[2]
7	IO_L175N_Y	G2
7	IO_L175P_Y	J6
7	IO_L176N_YY	J7
7	IO_L176P_YY	F1
7	IO_L177N_YY	H4
7	IO_VREF_L177P_YY	G4
7	IO_L178N_Y	F3
7	IO_L178P_Y	H5
7	IO_L179N_Y	E2
7	IO_L179P_Y	H6
7	IO_L180N_Y	G5
7	IO_VREF_L180P_Y	F4
7	IO_L181N_Y	H7
7	IO_L181P_Y	G6
7	IO_L182N_YY	E3
7	IO_L182P_YY	E4
2	CCLK	D24
3	DONE	AB21
NA	DXN	AB7
NA	DXP	Y8
NA	M0	AD4
NA	M1	W7
NA	M2	AB6
NA	PROGRAM	AA22
NA	TCK	E6
NA	TDI	D22
2	TDO	C23
NA	TMS	F5
NA	NC	T25
NA	NC	T2
NA	NC	P2
NA	NC	N25
NA	NC	L25

Table 21: **FG676 Differential Pin Pair Summary XCV400E, XCV600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
52	2	G24	H22	√	-
53	2	J21	G25	2	-
54	2	G26	J22	1	VREF
55	2	H24	J23	√	-
56	2	J24	K20	√	VREF
57	2	K22	K21	√	D2
58	2	H25	K23	√	-
59	2	L20	J26	2	-
60	2	K25	L22	1	-
61	2	L21	L23	1	-
62	2	M20	L24	1	-
63	2	M23	M22	√	D3
64	2	L26	M21	√	-
65	2	N19	M24	2	-
66	2	M26	N20	1	VREF
67	2	N24	N21	√	-
68	2	N23	N22	√	-
69	3	P21	P23	√	-
70	3	P22	R25	1	VREF
71	3	P19	P20	2	-
72	3	R21	R22	√	-
73	3	R24	R23	√	VREF
74	3	T24	R20	1	-
75	3	T22	U24	1	-
76	3	T23	U25	1	-
77	3	T21	U20	2	-
78	3	U22	V26	√	-
79	3	T20	U23	√	D5
80	3	V24	U21	√	VREF
81	3	V23	W24	√	-
82	3	V22	W26	1	VREF
83	3	Y25	V21	2	-
84	3	V20	AA26	√	-
85	3	Y24	W23	√	VREF

Table 21: **FG676 Differential Pin Pair Summary XCV400E, XCV600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
86	3	AA24	Y23	1	-
87	3	AB26	W21	2	-
88	3	Y22	W22	1	VREF
89	3	AA23	AB24	2	-
90	3	W20	AC24	√	-
91	3	AB23	Y21	√	INIT
92	4	AC22	AD26	√	-
93	4	AD23	AA20	1	-
94	4	Y19	AC21	√	-
95	4	AD22	AB20	√	VREF
96	4	AE22	Y18	NA	-
97	4	AF22	AA19	NA	-
98	4	AD21	AB19	√	VREF
99	4	AC20	AA18	√	-
100	4	AC19	AD20	1	-
101	4	AF20	AB18	1	VREF
102	4	AD19	Y17	NA	-
103	4	AE19	AD18	NA	VREF
104	4	AF19	AA17	√	-
105	4	AC17	AB17	1	-
106	4	Y16	AE17	√	-
107	4	AF17	AA16	√	-
108	4	AD17	AB16	NA	-
109	4	AC16	AD16	√	-
110	4	AC15	Y15	√	VREF
111	4	AD15	AA15	√	-
112	4	W14	AB15	1	-
113	4	AF15	Y14	1	VREF
114	4	AD14	AB14	NA	-
115	5	AC14	AF13	NA	IO_LVDS_DLL
116	5	AA13	AF12	1	VREF
117	5	AC13	W13	1	-
118	5	AA12	AD12	√	-
119	5	AC12	AB12	√	VREF

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
6	IO_VREF_L200N_YY	AH39
6	IO_L200P_YY	AG38
6	IO_L201N_YY	AG36
6	IO_L201P_YY	AG39
6	IO_L202N_Y	AG37
6	IO_L202P_Y	AF39
6	IO_L203N	AF36
6	IO_L203P	AE38
6	IO_L204N	AF37
6	IO_L204P	AF38
6	IO_VREF_L205N_Y	AE39[1]
6	IO_L205P_Y	AE36
6	IO_L206N_YY	AD38
6	IO_L206P_YY	AE37
6	IO_L207N	AD39
6	IO_L207P	AD36
6	IO_L208N_Y	AC38
6	IO_L208P_Y	AC39
6	IO_VREF_L209N_YY	AD37
6	IO_L209P_YY	AB38
6	IO_L210N_YY	AC35
6	IO_L210P_YY	AB39
6	IO_L211N	AC36
6	IO_L211P	AA38
6	IO_L212N	AC37
6	IO_L212P	AA39
6	IO_VREF_L213N_YY	AB35
6	IO_L213P_YY	Y38
6	IO_L214N_YY	AB36
6	IO_L214P_YY	Y39
6	IO_VREF_L215N	AB37[2]
6	IO_L215P	AA36
7	IO	C38
7	IO	B37
7	IO	F37
7	IO_L216N_YY	AA37
7	IO_L216P_YY	W38
7	IO_L217N	W37
7	IO_VREF_L217P	V39[2]
7	IO_L218N_YY	W36
7	IO_L218P_YY	U39
7	IO_L219N_YY	V38
7	IO_VREF_L219P_YY	U38
7	IO_L220N	V37
7	IO_L220P	T39
7	IO_L221N	V36
7	IO_L221P	T38
7	IO_L222N_YY	V35
7	IO_L222P_YY	R39
7	IO_L223N_YY	U37
7	IO_VREF_L223P_YY	U36
7	IO_L224N_Y	R38
7	IO_L224P_Y	U35
7	IO_L225N	P39
7	IO_L225P	T37
7	IO_L226N_YY	P38
7	IO_L226P_YY	T36
7	IO_L227N_Y	N39
7	IO_VREF_L227P_Y	N38[1]
7	IO_L228N	R37
7	IO_L228P	M39
7	IO_L229N	R36
7	IO_L229P	M38
7	IO_L230N_Y	P37
7	IO_L230P_Y	L39
7	IO_L231N_YY	P36
7	IO_L231P_YY	N37
7	IO_L232N_YY	L38
7	IO_VREF_L232P_YY	N36
7	IO_L233N	K39
7	IO_L233P	M37

Table 23: **FG680 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
52	1	B8	A8	√	VREF
53	1	A7	D9	√	-
54	1	B7	C8	3	-
55	1	A6	D8	3	-
56	1	B6	C7	√	VREF
57	1	A5	D7	√	-
58	1	B5	C6	5	VREF
59	1	A4	D6	5	-
60	1	D5	B4	√	CS
61	2	E3	C2	√	DIN, D0
62	2	D3	F3	6	-
63	2	D2	G4	4	VREF
64	2	G3	E2	4	-
65	2	H4	E1	6	VREF
66	2	H3	F2	√	-
67	2	J4	F1	4	-
68	2	J3	G2	6	-
69	2	G1	K4	√	VREF
70	2	H2	K3	√	-
71	2	H1	L4	7	VREF
72	2	J2	L3	4	-
73	2	J1	M3	√	VREF
74	2	K2	N4	√	-
75	2	K1	N3	4	-
76	2	L2	P4	√	D1
77	2	P3	L1	√	D2
78	2	R4	M2	6	-
79	2	R3	M1	4	-
80	2	T4	N2	4	-
81	2	N1	T3	6	VREF
82	2	P2	U5	√	-
83	2	P1	U4	4	-
84	2	R2	U3	6	-
85	2	V5	R1	√	D3

Table 23: **FG680 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
86	2	V4	T2	√	-
87	2	V3	T1	7	-
88	2	W4	U2	4	-
89	2	W3	U1	√	VREF
90	2	AA3	V2	√	-
91	2	AA4	V1	4	VREF
92	2	AB2	W2	√	-
93	3	AB4	W1	4	VREF
94	3	AB5	Y2	√	-
95	3	AC2	Y1	√	VREF
96	3	AC3	AA1	4	-
97	3	AC4	AA2	7	-
98	3	AC5	AB1	√	-
99	3	AD3	AC1	√	VREF
100	3	AD1	AD4	6	-
101	3	AD2	AE3	4	-
102	3	AE1	AE4	√	-
103	3	AE2	AF3	6	VREF
104	3	AF4	AF1	4	-
105	3	AG3	AF2	4	-
106	3	AG4	AG1	6	-
107	3	AH3	AG2	√	D5
108	3	AH1	AJ2	√	VREF
109	3	AH2	AJ3	4	-
110	3	AJ1	AJ4	√	-
111	3	AK1	AK3	√	VREF
112	3	AK2	AK4	4	-
113	3	AL1	AL2	7	VREF
114	3	AM1	AL3	√	-
115	3	AM2	AL4	√	VREF
116	3	AM3	AN1	6	-
117	3	AM4	AP1	4	-
118	3	AN2	AP2	√	-
119	3	AN3	AR1	6	VREF

FG860 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 25: **FG860 Differential Pin Pair Summary XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
3	0	C22	A22	NA	IO_DLL_L34N
2	1	B22	D22	NA	IO_DLL_L34P
1	5	AY22	AW21	NA	IO_DLL_L176N
0	4	BA22	AW20	NA	IO_DLL_L176P
IO LVDS Total Pairs: 281, Asynchronous Output Pairs: 111					
0	0	D38	A38	2	-
1	0	E37	B37	1	-
2	0	C39	A37	1	VREF
3	0	C38	B36	1	-
4	0	B35	A36	√	-
5	0	D37	A35	√	VREF
6	0	A34	C37	5	-
7	0	B33	E36	5	-
8	0	C32	A33	√	-
9	0	B32	C36	√	VREF
10	0	D35	A32	1	-
11	0	C35	C31	1	VREF
12	0	A31	E34	√	-
13	0	C30	D34	√	VREF
14	0	E33	B30	2	-
15	0	D33	A30	2	-
16	0	B29	C33	√	VREF
17	0	A29	E32	√	-

Table 25: **FG860 Differential Pin Pair Summary XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
18	0	C28	D32	2	-
19	0	B28	E31	1	-
20	0	A28	D31	1	-
21	0	C27	D30	5	-
22	0	B27	E29	√	-
23	0	A27	D29	√	VREF
24	0	D28	C26	5	-
25	0	F27	B26	5	-
26	0	C25	E27	√	-
27	0	B25	D27	√	VREF
28	0	D26	A25	1	-
29	0	E25	A24	1	-
30	0	B24	D25	√	-
31	0	A23	E24	√	VREF
32	0	E23	C23	2	-
33	0	D23	B23	2	VREF
34	1	D22	A22	NA	IO_LVDS_DLL
35	1	B21	D21	2	VREF
36	1	A21	D20	2	-
37	1	D19	C20	√	VREF
38	1	E19	B20	√	-
39	1	A19	D18	1	-
40	1	C19	E18	1	-
41	1	E17	B19	√	VREF
42	1	D16	A18	√	-
43	1	B18	E16	5	-
44	1	A17	F16	5	-
45	1	E15	C17	√	VREF
46	1	D14	B17	√	-
47	1	E14	A16	5	-
48	1	D13	C16	1	-
49	1	D12	B16	1	-
50	1	E12	A15	2	-
51	1	C11	C15	√	-

Table 25: **FG860 Differential Pin Pair Summary XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
256	7	T38	T41	√	-
257	7	T42	R39	1	VREF
258	7	R38	R42	2	-
259	7	P39	R40	4	-
260	7	P38	R41	2	-
261	7	N39	P42	1	-
262	7	M39	P40	3	-
263	7	M38	P41	√	-
264	7	L39	N42	√	VREF
265	7	N41	L38	2	-
266	7	M42	K40	√	-
267	7	K38	M40	√	VREF
268	7	J40	M41	2	-
269	7	L40	J39	5	VREF
270	7	L41	J38	√	-
271	7	H39	K42	√	VREF
272	7	H38	K41	1	-
273	7	G40	J41	2	-
274	7	G39	H42	√	-
275	7	G42	G38	1	VREF
276	7	F40	G41	2	-
277	7	F41	F42	4	-
278	7	E42	F39	2	VREF
279	7	E41	E40	1	-
280	7	D41	E39	3	-

Notes:
1. AO in the XCV1000E, 2000E.
2. AO in the XCV1000E, 1600E.
3. AO in the XCV2000E.
4. AO in the XCV1600E.
5. AO in the XCV1000E.

FG900 Fine-Pitch Ball Grid Array Package

XCV600E, XCV1000E, and XCV1600E devices in the FG900 fine-pitch Ball Grid Array package have footprint compatibility. Pins labeled I0_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 26, see Table 27 for Differential Pair information.

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
0	GCK3	C15
0	IO	A7[4]
0	IO	A13[4]
0	IO	C5[4]
0	IO	C6[4]
0	IO	C14[4]
0	IO	D8[5]
0	IO	D10
0	IO	D13[4]
0	IO	E6
0	IO	E9[5]
0	IO	E14[5]
0	IO	F9[4]
0	IO	F14[5]
0	IO	G15
0	IO	K11[5]
0	IO	K12
0	IO	L13[4]
0	IO_L0N_YY	C4[4]
0	IO_L0P_YY	F7[3]
0	IO_L1N_Y	D5
0	IO_L1P_Y	G8
0	IO_VREF_L2N_Y	A3[1]
0	IO_L2P_Y	H9
0	IO_L3N_Y	B4[4]
0	IO_L3P_Y	J10[4]
0	IO_L4N_YY	A4
0	IO_L4P_YY	D6
0	IO_VREF_L5N_YY	E7
0	IO_L5P_YY	B5

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
3	IO_L153P_YY	AD31
3	IO_VREF_L153N_YY	AF33
3	IO_L154P_Y	AC28
3	IO_L154N_Y	AF31
3	IO_L155P_Y	AC27[5]
3	IO_L155N_Y	AF32[4]
3	IO_L156P_Y	AE29
3	IO_VREF_L156N_Y	AD28[2]
3	IO_L157P_YY	AD30
3	IO_L157N_YY	AG32
3	IO_L158P_YY	AC26[5]
3	IO_L158N_YY	AH33[4]
3	IO_L159P_YY	AD26
3	IO_VREF_L159N_YY	AF30
3	IO_L160P_Y	AC25
3	IO_L160N_Y	AH32
3	IO_L161P_Y	AE28[5]
3	IO_L161N_Y	AL34[4]
3	IO_L162P_Y	AG30
3	IO_L162N_Y	AD27
3	IO_L163P_YY	AF29
3	IO_L163N_YY	AK34
3	IO_L164P_YY	AD25[5]
3	IO_L164N_YY	AE27[4]
3	IO_L165P_Y	AJ33
3	IO_VREF_L165N_Y	AH31
3	IO_L166P_Y	AE26
3	IO_L166N_Y	AL33
3	IO_L167P	AF28
3	IO_L167N	AL32
3	IO_L168P_Y	AJ31
3	IO_VREF_L168N_Y	AF27
3	IO_L169P_Y	AG29
3	IO_L169N_Y	AJ32
3	IO_L170P_Y	AK33
3	IO_L170N_Y	AH30
3	IO_D7_L171P_YY	AK32
3	IO_INIT_L171N_YY	AK31
3	IO	V34
4	GCK0	AH18
4	IO	AE21[3]
4	IO	AG18
4	IO	AG23
4	IO	AH24[3]
4	IO	AH25[3]
4	IO	AJ28[3]
4	IO	AK18[3]
4	IO	AK19[3]
4	IO	AL25
4	IO	AL27[3]
4	IO	AL30[3]
4	IO	AN18
4	IO	AN22[3]
4	IO	AN24[3]
4	IO_L172P_YY	AP31
4	IO_L172N_YY	AK29
4	IO_L173P_Y	AP30
4	IO_L173N_Y	AN31
4	IO_L174P_Y	AH27
4	IO_L174N_Y	AN30
4	IO_VREF_L175P_Y	AM30
4	IO_L175N_Y	AK28
4	IO_L176P_Y	AG26
4	IO_L176N_Y	AN29
4	IO_L177P_YY	AF25
4	IO_L177N_YY	AM29
4	IO_VREF_L178P_YY	AL29

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
4	IO_L212N_YY	AP18
4	IO_L213P_Y	AF18
4	IO_L213N_Y	AP17
4	IO_VREF_L214P_Y	AJ18[1]
4	IO_L214N_Y	AL18
4	IO_LVDS_DLL_L215P	AM18
5	GCK1	AL19
5	IO	AF17[3]
5	IO	AG12[3]
5	IO	AH12
5	IO	AJ10[3]
5	IO	AJ11[3]
5	IO	AK7[3]
5	IO	AK13[3]
5	IO	AL13[3]
5	IO	AM4[3]
5	IO	AN9
5	IO	AN10[3]
5	IO	AN16
5	IO	AN17[3]
5	IO_LVDS_DLL_L215N	AL17
5	IO_L216P_Y	AH17
5	IO_VREF_L216N_Y	AM17[1]
5	IO_L217P_Y	AJ17
5	IO_L217N_Y	AG17
5	IO_L218P_YY	AP16
5	IO_VREF_L218N_YY	AL16
5	IO_L219P_YY	AJ16
5	IO_L219N_YY	AM16
5	IO_L220P	AK16[5]
5	IO_L220N	AP15[4]
5	IO_L221P_Y	AL15
5	IO_L221N_Y	AH16
5	IO_L222P_Y	AN15
5	IO_L222N_Y	AF16
5	IO_L223P_Y	AP14[5]
5	IO_L223N_Y	AE16[4]
5	IO_L224P_YY	AK15
5	IO_VREF_L224N_YY	AJ15
5	IO_L225P_YY	AH15
5	IO_L225N_YY	AN14
5	IO_L226P	AK14[5]
5	IO_L226N	AG15[4]
5	IO_L227P_Y	AM13
5	IO_L227N_Y	AF15
5	IO_L228P_Y	AG14
5	IO_L228N_Y	AP13
5	IO_L229P_YY	AE14[5]
5	IO_L229N_YY	AE15[4]
5	IO_L230P_YY	AN13
5	IO_VREF_L230N_YY	AG13
5	IO_L231P_YY	AH14
5	IO_L231N_YY	AP12
5	IO_L232P_Y	AJ14
5	IO_L232N_Y	AL14
5	IO_L233P_Y	AF13
5	IO_L233N_Y	AN12
5	IO_L234P_Y	AF14
5	IO_L234N_Y	AP11
5	IO_L235P_Y	AN11
5	IO_L235N_Y	AH13
5	IO_L236P_YY	AM12
5	IO_L236N_YY	AL12
5	IO_L237P_YY	AJ13
5	IO_VREF_L237N_YY	AP10
5	IO_L238P_Y	AK12
5	IO_L238N_Y	AM10