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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	7776
Number of Logic Elements/Cells	34992
Total RAM Bits	589824
Number of I/O	404
Number of Gates	2188742
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	560-LBGA Exposed Pad, Metal
Supplier Device Package	560-MBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv1600e-7bg560i

Virtex-E Ordering Information

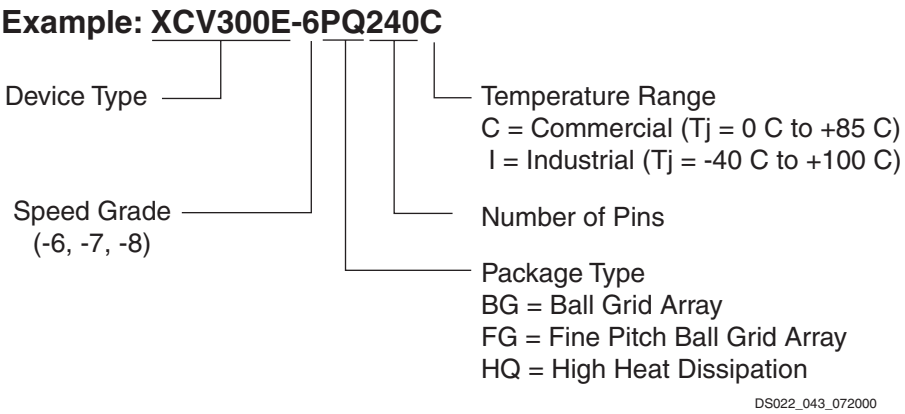

Figure 1: **Ordering Information**

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/7/99	1.0	Initial Xilinx release.
1/10/00	1.1	Re-released with spd.txt v. 1.18, FG860/900/1156 package information, and additional DLL, Select RAM and SelectI/O information.
1/28/00	1.2	Added Delay Measurement Methodology table, updated SelectI/O section, Figures 30, 54, & 55, text explaining Table 5, T_{BYP} values, buffered Hex Line info, p. 8, I/O Timing Measurement notes, notes for Tables 15, 16, and corrected F1156 pinout table footnote references.
2/29/00	1.3	Updated pinout tables, V_{CC} page 20, and corrected Figure 20.
5/23/00	1.4	Correction to table on p. 22.
7/10/00	1.5	• Numerous minor edits. • Data sheet upgraded to Preliminary. • Preview -8 numbers added to **Virtex-E Electrical Characteristics** tables.
8/1/00	1.6	• Reformatted entire document to follow new style guidelines. • Changed speed grade values in tables on pages 35-37.
9/20/00	1.7	• Min values added to **Virtex-E Electrical Characteristics** tables. • XCV2600E and XCV3200E numbers added to **Virtex-E Electrical Characteristics** tables (Module 3). • Corrected user I/O count for XCV100E device in Table 1 (Module 1). • Changed several pins to “No Connect in the XCV100E“ and removed duplicate V_{CCINT} pins in Table ~ (Module 4). • Changed pin J10 to “No connect in XCV600E” in Table 74 (Module 4). • Changed pin J30 to “VREF option only in the XCV600E” in Table 74 (Module 4). • Corrected pair 18 in Table 75 (Module 4) to be “AO in the XCV1000E, XCV1600E“.

Date	Version	Revision
11/20/00	1.8	• Upgraded speed grade -8 numbers in **Virtex-E Electrical Characteristics** tables to Preliminary. • Updated minimums in Table 13 and added notes to Table 14. • Added to note 2 to **Absolute Maximum Ratings**. • Changed speed grade -8 numbers for $T_{SHCKO32}$, T_{REG}, T_{BCCS}, and T_{ICKOF}. • Changed all minimum hold times to –0.4 under **Global Clock Setup and Hold for LVTTL Standard, with DLL**. • Revised maximum T_{DLLPW} in -6 speed grade for **DLL Timing Parameters**. • Changed GCLK0 to BA22 for FG860 package in Table 46.
2/12/01	1.9	• Revised footnote for Table 14. • Added numbers to **Virtex-E Electrical Characteristics** tables for XCV1000E and XCV2000E devices. • Updated Table 27 and Table 78 to include values for XCV400E and XCV600E devices. • Revised Table 62 to include pinout information for the XCV400E and XCV600E devices in the BG560 package. • Updated footnotes 1 and 2 for Table 76 to include XCV2600E and XCV3200E devices.
4/2/01	2.0	• Updated numerous values in **Virtex-E Switching Characteristics** tables. • Converted data sheet to modularized format. See the **Virtex-E Data Sheet** section.
10/25/01	2.1	• Updated the **Virtex-E Device/Package Combinations and Maximum I/O** table to show XCV3200E in the FG1156 package.
11/09/01	2.2	• Minor edits.
07/17/02	2.3	• Data sheet designation upgraded from Preliminary to Production.

Virtex-E Data Sheet

The Virtex-E Data Sheet contains the following modules:

- DS022-1, Virtex-E 1.8V FPGAs:
  Introduction and Ordering Information (Module 1)
- DS022-2, Virtex-E 1.8V FPGAs:
  Functional Description (Module 2)
- DS022-3, Virtex-E 1.8V FPGAs:
  DC and Switching Characteristics (Module 3)
- DS022-4, Virtex-E 1.8V FPGAs:
  Pinout Tables (Module 4)

Architectural Description

Virtex-E Array

The Virtex-E user-programmable gate array, shown in Figure 1, comprises two major configurable elements: configurable logic blocks (CLBs) and input/output blocks (IOBs).

- CLBs provide the functional elements for constructing logic
- IOBs provide the interface between the package pins and the CLBs

CLBs interconnect through a general routing matrix (GRM). The GRM comprises an array of routing switches located at the intersections of horizontal and vertical routing channels. Each CLB nests into a VersaBlock™ that also provides local routing resources to connect the CLB to the GRM.

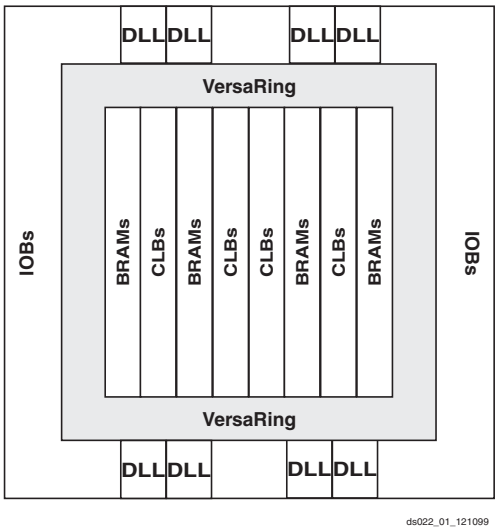

Figure 1: **Virtex-E Architecture Overview**

The VersaRing™ I/O interface provides additional routing resources around the periphery of the device. This routing improves I/O routability and facilitates pin locking.

The Virtex-E architecture also includes the following circuits that connect to the GRM.

- Dedicated block memories of 4096 bits each
- Clock DLLs for clock-distribution delay compensation and clock domain control
- 3-State buffers (BUFTs) associated with each CLB that drive dedicated segmentable horizontal routing resources

Values stored in static memory cells control the configurable logic elements and interconnect resources. These values load into the memory cells on power-up, and can reload if necessary to change the function of the device.

Input/Output Block

The Virtex-E IOB, Figure 2, features SelectI/O+ inputs and outputs that support a wide variety of I/O signalling standards, see Table 1.

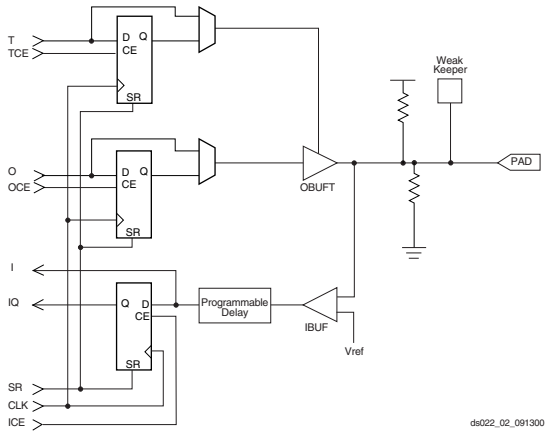

Figure 2: **Virtex-E Input/Output Block (IOB)**

The three IOB storage elements function either as edge-triggered D-type flip-flops or as level-sensitive latches. Each IOB has a clock signal (CLK) shared by the three flip-flops and independent clock enable signals for each flip-flop.

standard requires a Differential Amplifier input buffer and a Push-Pull output buffer.

SSTL3 — Stub Series Terminated Logic for 3.3V

The Stub Series Terminated Logic for 3.3V, or SSTL3 standard is a general purpose 3.3V memory bus standard also sponsored by Hitachi and IBM (JESD8-8). This standard has two classes, I and II. SelectI/O devices support both classes for the SSTL3 standard. This standard requires a Differential Amplifier input buffer and an Push-Pull output buffer.

SSTL2 — Stub Series Terminated Logic for 2.5V

The Stub Series Terminated Logic for 2.5V, or SSTL2 standard is a general purpose 2.5V memory bus standard sponsored by Hitachi and IBM (JESD8-9). This standard has two classes, I and II. SelectI/O devices support both classes for the SSTL2 standard. This standard requires a Differential Amplifier input buffer and an Push-Pull output buffer.

CTT — Center Tap Terminated

The Center Tap Terminated, or CTT standard is a 3.3V memory bus standard sponsored by Fujitsu (JESD8-4). This standard requires a Differential Amplifier input buffer and a Push-Pull output buffer.

AGP-2X — Advanced Graphics Port

The Intel AGP standard is a 3.3V Advanced Graphics Port-2X bus standard used with the Pentium II processor for graphics applications. This standard requires a Push-Pull output buffer and a Differential Amplifier input buffer.

LVDS — Low Voltage Differential Signal

LVDS is a differential I/O standard. It requires that one data bit is carried through two signal lines. As with all differential signaling standards, LVDS has an inherent noise immunity over single-ended I/O standards. The voltage swing between two signal lines is approximately 350mV. The use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}) is not required. LVDS requires the use of two pins per input or output. LVDS requires external resistor termination.

BLVDS — Bus LVDS

This standard allows for bidirectional LVDS communication between two or more devices. The external resistor termination is different than the one for standard LVDS.

LVPECL — Low Voltage Positive Emitter Coupled Logic

LVPECL is another differential I/O standard. It requires two signal lines for transmitting one data bit. This standard specifies two pins per input or output. The voltage swing between these two signal lines is approximately 850 mV. The use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}) is not required. The LVPECL standard requires external resistor termination.

Library Symbols

The Xilinx library includes an extensive list of symbols designed to provide support for the variety of SelectI/O features. Most of these symbols represent variations of the five generic SelectI/O symbols.

- IBUF (input buffer)
- IBUFG (global clock input buffer)
- OBUF (output buffer)
- OBUFT (3-state output buffer)
- IOBUF (input/output buffer)

IBUF

Signals used as inputs to the Virtex-E device must source an input buffer (IBUF) via an external input port. The generic Virtex-E IBUF symbol appears in Figure 37. The extension

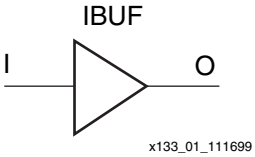

Figure 37: **Input Buffer (IBUF) Symbols**

to the base name defines which I/O standard the IBUF uses. The assumed standard is LVTTL when the generic IBUF has no specified extension.

The following list details the variations of the IBUF symbol:

- IBUF
- IBUF_LVCMOS2
- IBUF_PCI33_3
- IBUF_PCI66_3
- IBUF_GTL
- IBUF_GTLP
- IBUF_HSTL_I
- IBUF_HSTL_III
- IBUF_HSTL_IV
- IBUF_SSTL3_I
- IBUF_SSTL3_II
- IBUF_SSTL2_I
- IBUF_SSTL2_II
- IBUF_CTT
- IBUF_AGP
- IBUF_LVCMOS18
- IBUF_LVDS
- IBUF_LVPECL

When the IBUF symbol supports an I/O standard that requires a V_{REF}, the IBUF automatically configures as a differential amplifier input buffer. The V_{REF} voltage must be supplied on the V_{REF} pins. In the case of LVDS, LVPECL, and BLVDS, V_{REF} is not required.

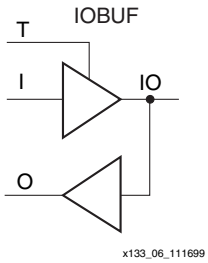

Figure 42: **Input/Output Buffer Symbol (IOBUF)**

The following list details variations of the IOBUF symbol.

- IOBUF
- IOBUF_S_2
- IOBUF_S_4
- IOBUF_S_6
- IOBUF_S_8
- IOBUF_S_12
- IOBUF_S_16
- IOBUF_S_24
- IOBUF_F_2
- IOBUF_F_4
- IOBUF_F_6
- IOBUF_F_8
- IOBUF_F_12
- IOBUF_F_16
- IOBUF_F_24
- IOBUF_LVCMOS2
- IOBUF_PCI33_3
- IOBUF_PCI66_3
- IOBUF_GTL
- IOBUF_GTLP
- IOBUF_HSTL_I
- IOBUF_HSTL_III
- IOBUF_HSTL_IV
- IOBUF_SSTL3_I
- IOBUF_SSTL3_II
- IOBUF_SSTL2_I
- IOBUF_SSTL2_II
- IOBUF_CTT
- IOBUF_AGP
- IOBUF_LVCMOS18
- IOBUF_LVDS
- IOBUF_LVPECL

When the IOBUF symbol used supports an I/O standard that requires a differential amplifier input, the IOBUF automatically configures with a differential amplifier input buffer.

The low-voltage I/O standards with a differential amplifier input require an external reference voltage input V_{REF}.

The voltage reference signal is “banked” within the Virtex-E device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 38, page 34 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

IOBUF placement restrictions require any differential amplifier input signals within a bank be of the same standard.

The Virtex-E series supports eight banks for the HQ and PQ packages. The CS package supports four V_{CCO} banks.

Additional restrictions on the Virtex-E SelectI/O IOBUF placement require that within a given V_{CCO} bank each IOBUF must share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within the same V_{CCO} bank. The LOC property can specify a location for the IOBUF.

An optional delay element is associated with the input path in each IOBUF. When the IOBUF drives an input flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Override this default with the NODELAY=TRUE property.

In the case when the IOBUF does not drive an input flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak “keeper” circuit. Control this feature by adding the appropriate symbol to the output net of the IOBUF (PULLUP, PULLDOWN, or KEEPER).

SelectI/O Properties

Access to some of the SelectI/O features (for example, location constraints, input delay, output drive strength, and slew rate) is available through properties associated with these features.

Input Delay Properties

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Use the NODELAY=TRUE property to override this default.

In the case when the IBUF does not drive a flip-flop within the IOB, the delay element by default de-activates to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

DC Characteristics

Absolute Maximum Ratings

Symbol	Description[1]			Units
V_{CCINT}	Internal Supply voltage relative to GND		–0.5 to 2.0	V
V_{CCO}	Supply voltage relative to GND		–0.5 to 4.0	V
V_{REF}	Input Reference Voltage		–0.5 to 4.0	V
V_{IN} [3]	Input voltage relative to GND		–0.5 to V_{CCO} +0.5	V
V_{TS}	Voltage applied to 3-state output		–0.5 to 4.0	V
V_{CC}	Longest Supply Voltage Rise Time from 0 V - 1.71 V		50	ms
T_{STG}	Storage temperature (ambient)		–65 to +150	°C
T_J	Junction temperature [2]	Plastic packages	+125	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time can affect device reliability.
2. For soldering guidelines and thermal considerations, see the device packaging information on www.xilinx.com.
3. Inputs configured as PCI are fully PCI compliant. This statement takes precedence over any specification that would imply that the device is not PCI compliant.

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CCINT}	Internal Supply voltage relative to GND, T_J = 0 °C to +85 °C	Commercial	1.8 – 5%	1.8 + 5%	V
	Internal Supply voltage relative to GND, T_J = –40 °C to +100 °C	Industrial	1.8 – 5%	1.8 + 5%	V
V_{CCO}	Supply voltage relative to GND, T_J = 0 °C to +85 °C	Commercial	1.2	3.6	V
	Supply voltage relative to GND, T_J = –40 °C to +100 °C	Industrial	1.2	3.6	V
T_{IN}	Input signal transition time			250	ns

IOB Output Switching Characteristics, Figure 1

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 10.

Description[2]	Symbol	Speed Grade[1]				Units
		Min	-8	-7	-6	
Propagation Delays						
O input to Pad	T_{IOOP}	1.04	2.5	2.7	2.9	ns, max
O input to Pad via transparent latch	T_{IOOLP}	1.24	2.9	3.1	3.4	ns, max
3-State Delays						
T input to Pad high-impedance (Note 2)	T_{IOTHZ}	0.73	1.5	1.7	1.9	ns, max
T input to valid data on Pad	T_{IOTON}	1.13	2.7	2.9	3.1	ns, max
T input to Pad high-impedance via transparent latch (Note 2)	$T_{IOTLPHZ}$	0.86	1.8	2.0	2.2	ns, max
T input to valid data on Pad via transparent latch	$T_{IOTLPON}$	1.26	3.0	3.2	3.4	ns, max
GTS to Pad high impedance (Note 2)	T_{GTS}	1.94	4.1	4.6	4.9	ns, max
Sequential Delays						
Clock CLK						
Minimum Pulse Width, High	T_{CH}	0.56	1.2	1.3	1.4	ns, min
Minimum Pulse Width, Low	T_{CL}	0.56	1.2	1.3	1.4	ns, min
Clock CLK to Pad	T_{IOCKP}	0.97	2.4	2.8	2.9	ns, max
Clock CLK to Pad high-impedance (synchronous) (Note 2)	T_{IOCKHZ}	0.77	1.6	2.0	2.2	ns, max
Clock CLK to valid data on Pad (synchronous)	T_{IOCKON}	1.17	2.8	3.2	3.4	ns, max
Setup and Hold Times before/after Clock CLK						
O input	T_{IOOCK} / T_{IOCKO}	0.43 / 0	0.9 / 0	1.0 / 0	1.1 / 0	ns, min
OCE input	$T_{IOOCECK}$ / $T_{IOCKOCE}$	0.28 / 0	0.55 / 0.01	0.7 / 0	0.7 / 0	ns, min
SR input (OFF)	$T_{IOSRCKO}$ / $T_{IOCKOSR}$	0.40 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
3-State Setup Times, T input	T_{IOTCK} / T_{IOCKT}	0.26 / 0	0.51 / 0	0.6 / 0	0.7 / 0	ns, min
3-State Setup Times, TCE input	$T_{IOTCECK}$ / $T_{IOCKTCE}$	0.30 / 0	0.6 / 0	0.7 / 0	0.8 / 0	ns, min
3-State Setup Times, SR input (TFF)	$T_{IOSRCKT}$ / $T_{IOCKTSR}$	0.38 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
Set/Reset Delays						
SR input to Pad (asynchronous)	T_{IOSRP}	1.30	3.1	3.3	3.5	ns, max
SR input to Pad high-impedance (asynchronous) (Note 2)	T_{IOSRHZ}	1.08	2.2	2.4	2.7	ns, max
SR input to valid data on Pad (asynchronous)	T_{IOSRON}	1.48	3.4	3.7	3.9	ns, max
GSR to Pad	T_{IOGSRQ}	3.88	7.6	8.5	9.7	ns, max

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. 3-state turn-off delays should not be adjusted.

CLB Arithmetic Switching Characteristics

Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer.

Description	Symbol	Speed Grade(1)				Units
		Min	-8	-7	-6	
Combinatorial Delays						
F operand inputs to X via XOR	T_{OPX}	0.32	0.68	0.8	0.8	ns, max
F operand input to XB output	T_{OPXB}	0.35	0.65	0.8	0.9	ns, max
F operand input to Y via XOR	T_{OPY}	0.59	1.07	1.4	1.5	ns, max
F operand input to YB output	T_{OPYB}	0.48	0.89	1.1	1.3	ns, max
F operand input to COUT output	T_{OPCYF}	0.37	0.71	0.9	1.0	ns, max
G operand inputs to Y via XOR	T_{OPGY}	0.34	0.72	0.8	0.9	ns, max
G operand input to YB output	T_{OPGYB}	0.47	0.78	1.2	1.3	ns, max
G operand input to COUT output	T_{OPCYG}	0.36	0.60	0.9	1.0	ns, max
BX initialization input to COUT	T_{BXCY}	0.19	0.36	0.51	0.57	ns, max
CIN input to X output via XOR	T_{CINX}	0.27	0.50	0.6	0.7	ns, max
CIN input to XB	T_{CINXB}	0.02	0.04	0.07	0.08	ns, max
CIN input to Y via XOR	T_{CINY}	0.26	0.45	0.7	0.7	ns, max
CIN input to YB	T_{CINYB}	0.16	0.28	0.38	0.43	ns, max
CIN input to COUT output	T_{BYP}	0.05	0.10	0.14	0.15	ns, max
Multiplier Operation						
F1/2 operand inputs to XB output via AND	T_{FANDXB}	0.10	0.30	0.35	0.39	ns, max
F1/2 operand inputs to YB output via AND	T_{FANDYB}	0.28	0.56	0.7	0.8	ns, max
F1/2 operand inputs to COUT output via AND	T_{FANDCY}	0.17	0.38	0.46	0.51	ns, max
G1/2 operand inputs to YB output via AND	T_{GANDYB}	0.20	0.46	0.55	0.7	ns, max
G1/2 operand inputs to COUT output via AND	T_{GANDCY}	0.09	0.28	0.30	0.34	ns, max
Setup and Hold Times before/after Clock CLK						
CIN input to FFX	T_{CCKX}/T_{CKCX}	0.47 / 0	1.0 / 0	1.2 / 0	1.3 / 0	ns, min
CIN input to FFY	T_{CCKY}/T_{CKCY}	0.49 / 0	0.92 / 0	1.2 / 0	1.3 / 0	ns, min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

CS144 Chip-Scale Package

XCV50E, XCV100E, XCV200E, XCV300E and XCV400E devices in CS144 Chip-scale packages have footprint compatibility. In the CS144 package, bank pairs that share a side are internally interconnected, permitting four choices for V_{CCO}. See Table 3.

Table 3: **I/O Bank Pairs and Shared Vcco Pins**

Paired Banks	Shared V_{CCO} Pins
Banks 0 & 1	A2, A13, D7
Banks 2 & 3	B12, G11, M13
Banks 4 & 5	N1, N7, N13
Banks 6 & 7	B2, G2, M2

Pins labeled I0_VREF can be used as either in all parts unless device-dependent, as indicated in the footnotes. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 4, see Table 5 is Differential Pair information.

Table 4: **CS144 — XCV50E, XCV100E, XCV200E**

Bank	Pin Description	Pin #
0	GCK3	A6
0	IO	B3
0	IO_VREF_L0N_YY	B4[2]
0	IO_L0P_YY	A4
0	IO_L1N_YY	B5
0	IO_L1P_YY	A5
0	IO_LVDS_DLL_L2N	C6
0	IO_VREF	A3[1]
0	IO_VREF	C4
0	IO_VREF	D6
1	GCK2	A7
1	IO	A8
1	IO_LVDS_DLL_L2P	B7
1	IO_L3N_YY	C8
1	IO_L3P_YY	D8
1	IO_L4N_YY	C9
1	IO_VREF_L4P_YY	D9[2]
1	IO_WRITE_L5N_YY	C10
1	IO_CS_L5P_YY	D10
1	IO_VREF	A10
1	IO_VREF	B8
1	IO_VREF	B10[1]
2	IO	D12
2	IO	F12
2	IO_DOUT_BUSY_L6P_YY	C11
2	IO_DIN_D0_L6N_YY	C12
2	IO_D1_L7N	E10
2	IO_VREF_L7P	D13[2]
2	IO_L8N_YY	E13
2	IO_D2_L8P_YY	E12
2	IO_D3_L9N	F11
2	IO_VREF_L9P	F10
2	IO_L10P	F13
2	IO_VREF	C13[1]
2	IO_VREF	D11
3	IO	H13
3	IO	K13
3	IO_L10N	G13
3	IO_VREF_L11N	H11
3	IO_D4_L11P	H12
3	IO_D5_L12N_YY	J13
3	IO_L12P_YY	H10
3	IO_VREF_L13N	J10[2]
3	IO_D6_L13P	J11
3	IO_INIT_L14N_YY	L13
3	IO_D7_L14P_YY	K10
3	IO_VREF	K11[1]
3	IO_VREF	K12
4	GCK0	K7
4	IO	M8
4	IO	M10

PQ240 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 7: **PQ240 Differential Pin Pair Summary XCV50E, XCV100E, XCV200E, XCV300E, XCV400E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	P92	P93	NA	IO_DLL_L40P
1	5	P89	P87	NA	IO_DLL_L40N
2	1	P210	P209	NA	IO_DLL_L6P
3	0	P213	P215	NA	IO_DLL_L6N
IO LVDS Total Pairs: 64, Asynchronous Outputs Pairs: 27					
0	0	P236	P237	1	VREF
1	0	P234	P235	√	-
2	0	P228	P229	√	VREF
3	0	P223	P224	√	-
4	0	P220	P221	3	-
5	0	P217	P218	3	VREF
6	1	P209	P215	NA	IO_LVDS_DLL
7	1	P205	P206	3	VREF
8	1	P202	P203	3	-
9	1	P199	P200	√	-
10	1	P194	P195	√	VREF
11	1	P191	P192	√	VREF
12	1	P188	P189	√	-
13	1	P186	P187	1	VREF
14	1	P184	P185	√	CS
15	2	P178	P177	√	DIN, D0
16	2	P174	P173	2	-
17	2	P171	P170	3	VREF
18	2	P168	P167	4	D1, VREF
19	2	P163	P162	√	D2
20	2	P160	P159	2	-
21	2	P157	P156	4	D3, VREF
22	2	P155	P154	5	VREF
23	2	P153	P152	√	-
24	3	P145	P144	4	D4, VREF
25	3	P142	P141	2	-
26	3	P139	P138	√	D5
27	3	P134	P133	4	VREF
28	3	P131	P130	3	VREF
29	3	P128	P127	2	-
30	3	P126	P125	6	VREF
31	3	P124	P123	√	INIT
32	4	P118	P117	√	-
33	4	P114	P113	√	-
34	4	P111	P110	√	VREF
35	4	P108	P107	√	VREF
36	4	P103	P102	√	-
37	4	P100	P99	3	-
38	4	P97	P96	3	VREF
39	4	P95	P94	7	VREF
40	5	P93	P87	NA	IO_LVDS_DLL
41	5	P84	P82	8	VREF
42	5	P79	P78	√	-
43	5	P74	P73	√	VREF
44	5	P71	P70	√	VREF
45	5	P68	P67	√	-
46	5	P66	P65	1	VREF
47	5	P64	P63	√	-

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P210	GCK2	1
P209	IO_LVDS_DLL_L6P	1
P208	IO_VREF	1
P207	VCCO	1
P206	IO_L7N_Y	1
P205	IO_VREF_L7P_Y	1
P204	GND	NA
P203	IO_L8N_Y	1
P202	IO_L8P_Y	1
P201[1]	IO_VREF	1
P200	IO_L9N_YY	1
P199	IO_L9P_YY	1
P198	VCCINT	NA
P197	VCCO	1
P196	GND	NA
P195	IO_L10N_YY	1
P194	IO_VREF_L10P_YY	1
P193	IO_VREF	1
P192	IO_L11N_YY	1
P191	IO_VREF_L11P_YY	1
P190	GND	NA
P189	IO_L12N_YY	1
P188	IO_L12P_YY	1
P187	IO_VREF_L13N	1
P186	IO_L13P	1
P185	IO_WRITE_L14N_YY	1
P184	IO_CS_L14P_YY	1
P183	TDI	NA
P182	GND	NA
P181	TDO	2
P180	VCCO	1
P179	CCLK	2
P178	IO_DOUT_BUSY_L15P_YY	2
P177	IO_DIN_D0_L15N_YY	2
P176	VCCO	2
P175	IO_VREF	2

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P174	IO_L16P_Y	2
P173	IO_L16N_Y	2
P172	GND	NA
P171	IO_VREF_L17P_Y	2
P170	IO_L17N_Y	2
P169	IO_VREF	2
P168	IO_VREF_L18P_Y	2
P167	IO_D1_L18N_Y	2
P166	GND	NA
P165	VCCO	2
P164	VCCINT	NA
P163	IO_D2_L19P_YY	2
P162	IO_L19N_YY	2
P161[1]	IO_VREF	2
P160	IO_L20P_Y	2
P159	IO_L20N_Y	2
P158	GND	NA
P157	IO_VREF_L21P_Y	2
P156	IO_D3_L21N_Y	2
P155	IO_L22P_Y	2
P154	IO_VREF_L22N_Y	2
P153	IO_L23P_YY	2
P152	IO_L23N_YY	2
P151	GND	NA
P150	VCCO	2
P149	IO	3
P148	VCCINT	NA
P147	IO_VREF	3
P146	VCCO	3
P145	IO_D4_L24P_Y	3
P144	IO_VREF_L24N_Y	3
P143	GND	NA
P142	IO_L25P_Y	3
P141	IO_L25N_Y	3
P140[1]	IO_VREF	3
P139	IO_L26P_YY	3

FG676 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 21: **FG676 Differential Pin Pair Summary XCV400E, XCV600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
3	0	E13	B13	NA	IO_DLL_L21N
2	1	C13	F14	NA	IO_DLL_L21P
1	5	AB13	AF13	NA	IO_DLL_L115N
0	4	AA14	AC14	NA	IO_DLL_L115P
IOLVDS Total Pairs: 183, Asynchronous Output Pairs: 97					
0	0	F7	C4	1	-
1	0	C5	G8	√	-
2	0	E7	D6	√	VREF
3	0	F8	A4	NA	-
4	0	D7	B5	NA	-
5	0	G9	E8	√	VREF
6	0	F9	A5	√	-
7	0	C7	D8	1	-
8	0	E9	B7	1	VREF
9	0	D9	A7	NA	-
10	0	G10	B8	NA	VREF
11	0	F10	C9	√	-
12	0	E10	A8	1	-
13	0	D10	G11	√	-
14	0	F11	B10	√	-
15	0	E11	C10	NA	-
16	0	D11	G12	√	-
17	0	F12	C11	√	VREF

Table 21: **FG676 Differential Pin Pair Summary XCV400E, XCV600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
18	0	E12	A11	√	-
19	0	C12	D12	1	-
20	0	H13	A12	1	VREF
21	1	F14	B13	NA	IO_LVDS_DLL
22	1	F13	E14	NA	-
23	1	A14	D14	1	VREF
24	1	H14	C14	1	-
25	1	C15	G14	√	-
26	1	D15	E15	√	VREF
27	1	F15	C16	√	-
28	1	D16	G15	-	-
29	1	A17	E16	√	-
30	1	E17	C17	√	-
31	1	D17	F16	1	-
32	1	C18	F17	√	-
33	1	G16	A18	√	VREF
34	1	G17	C19	√	-
35	1	B19	D18	1	VREF
36	1	E18	D19	1	-
37	1	B20	F18	√	-
38	1	C20	G19	√	VREF
39	1	E19	G18	√	-
40	1	D20	A21	√	-
41	1	C21	F19	√	VREF
42	1	E20	B22	√	-
43	1	D21	A23	2	-
44	1	E21	C22	√	CS
45	2	E23	F22	√	DIN, D0
46	2	E24	F20	√	-
47	2	G21	G22	2	-
48	2	F24	H20	1	VREF
49	2	E25	H21	1	-
50	2	F23	G23	√	-
51	2	H23	J20	√	VREF

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
3	IO_L97N	AA2
3	IO_L98P_YY	AC5
3	IO_L98N_YY	AB1
3	IO_D4_L99P_YY	AD3
3	IO_VREF_L99N_YY	AC1
3	IO_L100P_Y	AD1
3	IO_L100N_Y	AD4
3	IO_L101P	AD2
3	IO_L101N	AE3
3	IO_L102P_YY	AE1
3	IO_L102N_YY	AE4
3	IO_L103P_Y	AE2
3	IO_VREF_L103N_Y	AF3[1]
3	IO_L104P	AF4
3	IO_L104N	AF1
3	IO_L105P	AG3
3	IO_L105N	AF2
3	IO_L106P_Y	AG4
3	IO_L106N_Y	AG1
3	IO_L107P_YY	AH3
3	IO_D5_L107N_YY	AG2
3	IO_D6_L108P_YY	AH1
3	IO_VREF_L108N_YY	AJ2
3	IO_L109P	AH2
3	IO_L109N	AJ3
3	IO_L110P_YY	AJ1
3	IO_L110N_YY	AJ4
3	IO_L111P_YY	AK1
3	IO_VREF_L111N_YY	AK3
3	IO_L112P	AK2
3	IO_L112N	AK4
3	IO_L113P	AL1
3	IO_VREF_L113N	AL2[3]
3	IO_L114P_YY	AM1
3	IO_L114N_YY	AL3
3	IO_L115P_YY	AM2
3	IO_VREF_L115N_YY	AL4
3	IO_L116P_Y	AM3
3	IO_L116N_Y	AN1
3	IO_L117P	AM4
3	IO_L117N	AP1
3	IO_L118P_YY	AN2
3	IO_L118N_YY	AP2
3	IO_L119P_Y	AN3
3	IO_VREF_L119N_Y	AR1
3	IO_L120P	AN4
3	IO_L120N	AT1
3	IO_L121P	AR2
3	IO_VREF_L121N	AP4[1]
3	IO_L122P_Y	AT2
3	IO_L122N_Y	AR3
3	IO_D7_L123P_YY	AR4
3	IO_INIT_L123N_YY	AU2
4	GCK0	AW19
4	IO	AV3
4	IO_L124P_YY	AU4
4	IO_L124N_YY	AV5
4	IO_L125P_Y	AT6
4	IO_L125N_Y	AV4
4	IO_VREF_L126P_Y	AU6[1]
4	IO_L126N_Y	AW4
4	IO_L127P_YY	AT7
4	IO_L127N_YY	AW5
4	IO_VREF_L128P_YY	AU7
4	IO_L128N_YY	AV6
4	IO_L129P_Y	AT8
4	IO_L129N_Y	AW6
4	IO_L130P_Y	AU8
4	IO_L130N_Y	AV7
4	IO_L131P_YY	AT9
4	IO_L131N_YY	AW7

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
5	IO_L166P_YY	AV26
5	IO_L166N_YY	AW27
5	IO_L167P_Y	AU26
5	IO_L167N_Y	AV27
5	IO_L168P_Y	AT26
5	IO_L168N_Y	AW28
5	IO_L169P_YY	AU27
5	IO_L169N_YY	AV28
5	IO_L170P_YY	AW29
5	IO_VREF_L170N_YY	AT27
5	IO_L171P_Y	AW30
5	IO_L171N_Y	AU28
5	IO_L172P_Y	AV30
5	IO_L172N_Y	AV29
5	IO_L173P_YY	AW31
5	IO_VREF_L173N_YY	AU29
5	IO_L174P_YY	AV31
5	IO_L174N_YY	AT29
5	IO_L175P_Y	AW32
5	IO_VREF_L175N_Y	AU30[3]
5	IO_L176P_Y	AW33
5	IO_L176N_Y	AT30
5	IO_L177P_YY	AV33
5	IO_VREF_L177N_YY	AU31
5	IO_L178P_YY	AT31
5	IO_L178N_YY	AW34
5	IO_L179P_Y	AV32
5	IO_L179N_Y	AV34
5	IO_L180P_Y	AU32
5	IO_L180N_Y	AW35
5	IO_L181P_YY	AT32
5	IO_VREF_L181N_YY	AV35
5	IO_L182P_YY	AU33
5	IO_L182N_YY	AW36
5	IO_L183P_Y	AT33
5	IO_VREF_L183N_Y	AV36[1]

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
5	IO_L184P_Y	AU34
5	IO_L184N_Y	AU36
6	IO	W39
6	IO	AR37
6	IO	AR39
6	IO_L185N_YY	AR36
6	IO_L185P_YY	AT38
6	IO_L186N_Y	AR38
6	IO_L186P_Y	AP36
6	IO_VREF_L187N	AT39[1]
6	IO_L187P	AP37
6	IO_L188N	AP38
6	IO_L188P	AP39
6	IO_VREF_L189N_Y	AN36
6	IO_L189P_Y	AN38
6	IO_L190N_YY	AN37
6	IO_L190P_YY	AN39
6	IO_L191N	AM36
6	IO_L191P	AM38
6	IO_L192N_Y	AM37
6	IO_L192P_Y	AL36
6	IO_VREF_L193N_YY	AM39
6	IO_L193P_YY	AL37
6	IO_L194N_YY	AL38
6	IO_L194P_YY	AK36
6	IO_VREF_L195N	AL39[3]
6	IO_L195P	AK37
6	IO_L196N	AK38
6	IO_L196P	AJ36
6	IO_VREF_L197N_YY	AK39
6	IO_L197P_YY	AJ37
6	IO_L198N_YY	AJ38
6	IO_L198P_YY	AH37
6	IO_L199N	AJ39
6	IO_L199P	AH38

Table 25: **FG860 Differential Pin Pair Summary XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
120	3	AH1	AL5	1	-
121	3	AH2	AM4	3	-
122	3	AH3	AM5	√	D5
123	3	AJ1	AN3	√	VREF
124	3	AN4	AJ3	2	-
125	3	AN5	AK1	√	-
126	3	AK2	AP4	√	VREF
127	3	AK3	AP5	2	-
128	3	AR3	AL2	5	VREF
129	3	AR4	AL3	√	-
130	3	AM1	AT3	√	VREF
131	3	AM2	AT4	1	-
132	3	AT5	AN1	2	-
133	3	AU3	AN2	√	-
134	3	AP1	AP2	1	VREF
135	3	AR1	AV3	2	-
136	3	AR2	AT1	4	-
137	3	AV4	AT2	2	VREF
138	3	AU1	AU5	1	-
139	3	AU2	AW3	3	-
140	3	AV1	AW5	√	INIT
141	4	AV6	BA4	√	-
142	4	AY4	BA5	2	-
143	4	AW6	BB5	1	-
144	4	BA6	AY5	1	VREF
145	4	BB6	AY6	5	-
146	4	BA7	AV7	√	-
147	4	BB7	AW7	√	VREF
148	4	AY7	BB8	5	-
149	4	BA9	AV8	5	-
150	4	AW8	BA10	√	-
151	4	BB10	AY8	√	VREF
152	4	AV9	BA11	1	-
153	4	BB11	AW9	1	VREF

Table 25: **FG860 Differential Pin Pair Summary XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
154	4	AY9	BA12	√	-
155	4	BB12	AV10	√	VREF
156	4	BA13	AW10	2	-
157	4	BB13	AY10	2	-
158	4	AV11	BA14	√	VREF
159	4	AW11	BB14	√	-
160	4	AV12	BA15	2	-
161	4	AW12	AY15	1	-
162	4	AW13	BB15	1	-
163	4	AV14	BA16	5	-
164	4	AW14	AY16	√	-
165	4	BB16	AV15	√	VREF
166	4	AY17	AW15	5	-
167	4	BB17	AU16	5	-
168	4	AV16	AY18	√	-
169	4	AW16	BA18	√	VREF
170	4	BB19	AW17	1	-
171	4	AY19	AV18	1	-
172	4	AW18	BB20	√	-
173	4	AY20	AV19	√	VREF
174	4	BB21	AW19	2	-
175	4	AY21	AV20	2	VREF
176	5	AW20	AW21	NA	IO_LVDS_DLL
177	5	BB22	AW22	2	VREF
178	5	BB23	AW23	2	-
179	5	AV23	BA23	√	VREF
180	5	AW24	BB24	√	-
181	5	AY24	AW25	1	-
182	5	BA24	AV25	1	-
183	5	AW26	AY25	√	VREF
184	5	AV26	BA25	√	-
185	5	BB26	AV27	5	-
186	5	AY26	AU27	5	-
187	5	AW28	BB27	√	VREF

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
3	IO_L127P_YY	Y24
3	IO_VREF_L127N_YY	AB28
3	IO_L128P_YY	AC30
3	IO_L128N_YY	AA25
3	IO_L129P	W21
3	IO_L129N	AA24
3	IO_L130P_YY	AB26
3	IO_L130N_YY	AD30
3	IO_L131P_YY	Y22
3	IO_VREF_L131N_YY	AC27
3	IO_L132P	AD28
3	IO_L132N	AB25
3	IO_L133P_YY	AC26
3	IO_L133N_YY	AE30
3	IO_L134P_YY	AD27
3	IO_L134N_YY	AF30
3	IO_L135P	AF29
3	IO_VREF_L135N	AB24
3	IO_L136P_YY	AB23
3	IO_L136N_YY	AE28
3	IO_L137P_Y	AG30[3]
3	IO_L137N_Y	AC25[4]
3	IO_L138P_YY	AE26
3	IO_VREF_L138N_YY	AG29[1]
3	IO_L139P	AH30
3	IO_L139N	AC24
3	IO_L140P	AF28[3]
3	IO_L140N	AD25[4]
3	IO_D7_L141P_YY	AH29
3	IO_INIT_L141N_YY	AA22
4	GCK0	AJ16
4	IO	AB19[4]
4	IO	AC16[4]
4	IO	AC19
4	IO	AD18[4]
4	IO	AD21[4]

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
4	IO	AE15[4]
4	IO	AE18[4]
4	IO	AE21
4	IO	AE24[5]
4	IO	AF17[5]
4	IO	AF18[5]
4	IO	AJ18[4]
4	IO	AK18
4	IO	AK25[5]
4	IO	AK27[4]
4	IO	AH23[4]
4	IO	AH24[5]
4	IO_L142P_YY	AF27
4	IO_L142N_YY	AK28
4	IO_L143P_YY	AG26[4]
4	IO_L143N_YY	AH27[3]
4	IO_L144P	AD23
4	IO_L144N	AJ27
4	IO_VREF_L145P	AB21[1]
4	IO_L145N	AF25
4	IO_L146P	AC22[4]
4	IO_L146N	AH26[4]
4	IO_L147P_YY	AA21
4	IO_L147N_YY	AG25
4	IO_VREF_L148P_YY	AJ26
4	IO_L148N_YY	AD22
4	IO_L149P	AA20
4	IO_L149N	AH25
4	IO_L150P	AC21
4	IO_L150N	AF24
4	IO_L151P_YY	AG24
4	IO_L151N_YY	AK26
4	IO_VREF_L152P_YY	AJ24
4	IO_L152N_YY	AF23
4	IO_L153P	AE23
4	IO_L153N	AB20
4	IO_L154P	AC20

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
NA	VCCO_0	C12
NA	VCCO_1	B25
NA	VCCO_1	C19
NA	VCCO_1	M18
NA	VCCO_1	M17
NA	VCCO_1	L17
NA	VCCO_1	H17
NA	VCCO_1	L16
NA	VCCO_1	M16
NA	VCCO_2	F29
NA	VCCO_2	M28
NA	VCCO_2	P23
NA	VCCO_2	R20
NA	VCCO_2	P20
NA	VCCO_2	R19
NA	VCCO_2	N19
NA	VCCO_2	P19
NA	VCCO_3	AE29
NA	VCCO_3	W28
NA	VCCO_3	U23
NA	VCCO_3	U20
NA	VCCO_3	T20
NA	VCCO_3	V19
NA	VCCO_3	T19
NA	VCCO_3	U19
NA	VCCO_4	AJ25
NA	VCCO_4	AH19
NA	VCCO_4	W18
NA	VCCO_4	AC17
NA	VCCO_4	Y17
NA	VCCO_4	W17
NA	VCCO_4	W16
NA	VCCO_4	Y16
NA	VCCO_5	AJ6
NA	VCCO_5	Y15
NA	VCCO_5	W15
NA	VCCO_5	AC14

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
NA	VCCO_5	Y14
NA	VCCO_5	W14
NA	VCCO_5	W13
NA	VCCO_5	AH12
NA	VCCO_6	AE2
NA	VCCO_6	V12
NA	VCCO_6	U12
NA	VCCO_6	T12
NA	VCCO_6	U11
NA	VCCO_6	T11
NA	VCCO_6	U8
NA	VCCO_6	W3
NA	VCCO_7	F2
NA	VCCO_7	R12
NA	VCCO_7	P12
NA	VCCO_7	N12
NA	VCCO_7	R11
NA	VCCO_7	P11
NA	VCCO_7	P8
NA	VCCO_7	M3
NA	GND	Y18
NA	GND	AH7
NA	GND	AK30
NA	GND	AJ30
NA	GND	B30
NA	GND	A30
NA	GND	AK29
NA	GND	AJ29
NA	GND	AC29
NA	GND	H29
NA	GND	B29
NA	GND	A29
NA	GND	AH28
NA	GND	V28
NA	GND	N28
NA	GND	C28

Table 27: **FG900 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
120	3	AA30	W24	4	-
121	3	AA29	V20	1	-
122	3	Y27	W23	NA	-
123	3	Y26	AB30	√	D5
124	3	V21	AA28	√	VREF
125	3	Y25	AA27	4	-
126	3	W22	Y23	4	-
127	3	Y24	AB28	4	VREF
128	3	AC30	AA25	√	-
129	3	W21	AA24	2	-
130	3	AB26	AD30	√	-
131	3	Y22	AC27	√	VREF
132	3	AD28	AB25	2	-
133	3	AC26	AE30	4	-
134	3	AD27	AF30	√	-
135	3	AF29	AB24	1	VREF
136	3	AB23	AE28	4	-
137	3	AG30	AC25	3	-
138	3	AE26	AG29	4	VREF
139	3	AH30	AC24	1	-
140	3	AF28	AD25	NA	-
141	3	AH29	AA22	√	INIT
142	4	AF27	AK28	√	-
143	4	AG26	AH27	4	-
144	4	AD23	AJ27	2	-
145	4	AB21	AF25	2	VREF
146	4	AC22	AH26	2	-
147	4	AA21	AG25	√	-
148	4	AJ26	AD22	√	VREF
149	4	AA20	AH25	1	-
150	4	AC21	AF24	1	-
151	4	AG24	AK26	√	-
152	4	AJ24	AF23	√	VREF
153	4	AE23	AB20	2	-

Table 27: **FG900 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
154	4	AC20	AG23	2	-
155	4	AF22	AE22	√	-
156	4	AJ22	AG22	√	VREF
157	4	AK24	AD20	NA	-
158	4	AA19	AF21	4	-
159	4	AH22	AA18	NA	VREF
160	4	AG21	AK23	NA	-
161	4	AH21	AD19	4	-
162	4	AE20	AJ21	2	-
163	4	AG20	AF20	2	-
164	4	AC18	AF19	2	-
165	4	AJ20	AE19	√	-
166	4	AK22	AH20	√	VREF
167	4	AG19	AB17	1	-
168	4	AJ19	AD17	1	-
169	4	AA16	AA17	√	-
170	4	AK21	AB16	√	VREF
171	4	AG18	AK20	2	-
172	4	AK19	AD16	2	-
173	4	AE16	AE17	√	-
174	4	AG17	AJ17	√	VREF
175	4	AD15	AH17	NA	-
176	4	AG16	AK17	4	VREF
177	5	AF16	AH16	NA	IO_ LVDS_DLL
178	5	AC15	AG15	4	VREF
179	5	AB15	AF15	√	-
180	5	AA15	AF14	√	VREF
181	5	AH15	AK15	√	-
182	5	AB14	AF13	2	-
183	5	AH14	AJ14	2	-
184	5	AE14	AG13	√	VREF
185	5	AK13	AD13	√	-
186	5	AE13	AF12	1	-
187	5	AC13	AA13	1	-

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
7	IO_L324P_Y	L4
7	IO_L325N_YY	J1
7	IO_L325P_YY	L5
7	IO_L326N_YY	J2
7	IO_VREF_L326P_YY	K3
7	IO_L327N_Y	L7
7	IO_L327P_Y	J3
7	IO_L328N_Y	M9[5]
7	IO_L328P_Y	H2[4]
7	IO_L329N_Y	J4
7	IO_VREF_L329P_Y	K6[2]
7	IO_L330N_YY	L8
7	IO_L330P_YY	G2
7	IO_L331N_YY	H3[5]
7	IO_L331P_YY	K7[4]
7	IO_L332N_YY	G3
7	IO_VREF_L332P_YY	J5
7	IO_L333N_Y	L9
7	IO_L333P_Y	H5
7	IO_L334N_Y	J6[5]
7	IO_L334P_Y	H4[4]
7	IO_L335N_Y	G4
7	IO_L335P_Y	K8
7	IO_L336N_YY	J7
7	IO_L336P_YY	F2
7	IO_L337N_YY	F3[5]
7	IO_L337P_YY	L10[4]
7	IO_L338N_Y	E1
7	IO_VREF_L338P_Y_Y	H6
7	IO_L339N_Y	G5
7	IO_L339P_Y	E2
7	IO_L340N	K9
7	IO_L340P	D1
7	IO_L341N_Y	E3

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
7	IO_VREF_L341P_Y	J8
7	IO_L342N_Y	E4
7	IO_L342P_Y	D2
7	IO_L343N_Y	F4
7	IO_L343P_Y	D3
2	CCLK	C31
3	DONE	AM31
NA	DXN	AJ5
NA	DXP	AL5
NA	M0	AK4
NA	M1	AG7
NA	M2	AL3
NA	PROGRAM	AG28
NA	TCK	D5
NA	TDI	C30
2	TDO	K26
NA	TMS	C4
NA	VCCINT	K10
NA	VCCINT	K17
NA	VCCINT	K18
NA	VCCINT	K25
NA	VCCINT	L11
NA	VCCINT	L24
NA	VCCINT	M12
NA	VCCINT	M23
NA	VCCINT	N13
NA	VCCINT	N14
NA	VCCINT	N15
NA	VCCINT	N16
NA	VCCINT	N19
NA	VCCINT	N20
NA	VCCINT	N21

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
311	7	P2	R8	2600 2000 1000	-
312	7	N1	R9	3200 2600 2000	-
313	7	R10	P4	3200 2600 1600 1000	-
314	7	N2	P8	3200 2600 2000 1600 1000	-
315	7	P7	P6	3200 2600 2000 1600	-
316	7	N4	M1	2600 2000 1000	VREF
317	7	N3	N6	3200 1600 1000	-
318	7	M2	P9	2600 1600	-
319	7	M3	N7	3200 2600 1600 1000	-
320	7	M4	P10	2000 1000	-
321	7	N8	L1	3200 2600 2000	-
322	7	N9	L2	3200 2600 2000 1600 1000	-
323	7	K1	M7	2000 1600 1000	VREF
324	7	L4	M8	3200 1600 1000	-
325	7	L5	J1	3200 2600 2000 1600 1000	-
326	7	K3	J2	3200 2600 2000 1600 1000	VREF
327	7	J3	L7	3200 2600 1600 1000	-
328	7	H2	M9	3200 2600 1600	-
329	7	K6	J4	2600 1000	VREF
330	7	G2	L8	3200 2600 2000 1600 1000	-

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
331	7	K7	H3	2000 1600	-
332	7	J5	G3	3200 2600 2000 1600 1000	VREF
333	7	H5	L9	2600 2000 1000	-
334	7	H4	J6	3200 2600 2000	-
335	7	K8	G4	3200 2600 1600 1000	-
336	7	F2	J7	3200 2600 2000 1600 1000	-
337	7	L10	F3	3200 2600 2000 1600	-
338	7	H6	E1	2600 2000 1000	VREF
339	7	E2	G5	3200 2600 1600 1000	-
340	7	D1	K9	2600 1600	-
341	7	J8	E3	3200 2600 1600 1000	VREF
342	7	D2	E4	2600 2000 1000	-
343	7	D3	F4	3200 2600 2000	-