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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	7776
Number of Logic Elements/Cells	34992
Total RAM Bits	589824
Number of I/O	512
Number of Gates	2188742
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	680-LBGA Exposed Pad
Supplier Device Package	680-FTEBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv1600e-7fg680c

Table 9 lists the total number of bits required to configure each device.

Table 9: **Virtex-E Bitstream Lengths**

Device	# of Configuration Bits
XCV50E	630,048
XCV100E	863,840
XCV200E	1,442,016
XCV300E	1, 875,648
XCV400E	2,693,440
XCV600E	3,961,632
XCV1000E	6,587,520
XCV1600E	8,308,992
XCV2000E	10,159,648
XCV2600E	12,922,336
XCV3200E	16,283,712

Slave-Serial Mode

In slave-serial mode, the FPGA receives configuration data in bit-serial form from a serial PROM or other source of serial configuration data. The serial bitstream must be set up at the DIN input pin a short time before each rising edge of an externally generated CCLK.

For more detailed information on serial PROMs, see the PROM data sheet at **http://www.xilinx.com/bvdocs/publications/ds026.pdf**.

Multiple FPGAs can be daisy-chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed to the DOUT pin. The maximum capacity for a single LOUT/DOUT write is 2^{20}-1 (1,048,575) 32-bit words, or 33,554,4000 bits. The data on the DOUT pin changes on the rising edge of CCLK.

The change of DOUT on the rising edge of CCLK differs from previous families, but does not cause a problem for mixed configuration chains. This change was made to improve serial configuration rates for Virtex and Virtex-E only chains.

Figure 13 shows a full master/slave system. A Virtex-E device in slave-serial mode should be connected as shown in the right-most device.

Slave-serial mode is selected by applying <111> or <011> to the mode pins (M2, M1, M0). A weak pull-up on the mode pins makes slave serial the default mode if the pins are left unconnected. However, it is recommended to drive the configuration mode pins externally. Figure 14 shows slave-serial mode programming switching characteristics.

Table 10 provides more detail about the characteristics shown in Figure 14. Configuration must be delayed until the $\overline{\text{INIT}}$ pins of all daisy-chained FPGAs are High.

Table 10: **Master/Slave Serial Mode Programming Switching**

	Description	Figure References	Symbol	Values	Units
CCLK	DIN setup/hold, slave mode	1/2	T_{DCC}/T_{CCD}	5.0 / 0.0	ns, min
	DIN setup/hold, master mode	1/2	T_{DSCK}/T_{CKDS}	5.0 / 0.0	ns, min
	DOUT	3	T_{CCO}	12.0	ns, max
	High time	4	T_{CCH}	5.0	ns, min
	Low time	5	T_{CCL}	5.0	ns, min
	Maximum Frequency		F_{CC}	66	MHz, max
	Frequency Tolerance, master mode with respect to nominal			+45% –30%	

Initialization in Verilog and Synopsys

The block SelectRAM+ structures can be initialized in Verilog for both simulation and synthesis for inclusion in the EDIF output file. The simulation of the Verilog code uses a defparam to pass the initialization. The Synopsys FPGA compiler does not presently support defparam. The initialization values instead attach as attributes to the RAM by a built-in Synopsys dc_script. The translate_off statement stops synthesis translation of the defparam statements. The following code illustrates a module that employs these techniques.

Design Examples

Creating a 32-bit Single-Port RAM

The true dual-read/write port functionality of the block SelectRAM+ memory allows a single port, 128 deep by 32-bit wide RAM to be created using a single block SelectRAM+ cell as shown in Figure 35.

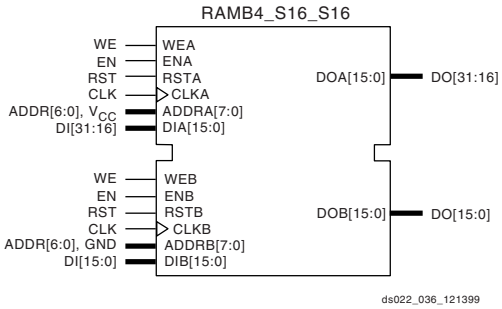

Figure 35: **Single Port 128 x 32 RAM**

Interleaving the memory space, setting the LSB of the address bus of Port A to 1 (V_{CC}), and the LSB of the address bus of Port B to 0 (GND), allows a 32-bit wide single port RAM to be created.

Creating Two Single-Port RAMs

The true dual-read/write port functionality of the block SelectRAM+ memory allows a single RAM to be split into two single port memories of 2K bits each as shown in Figure 36.

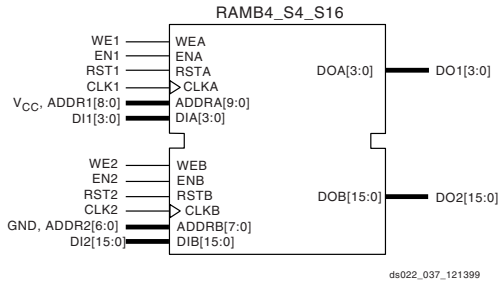

Figure 36: **512 x 4 RAM and 128 x 16 RAM**

In this example, a 512K x 4 RAM (Port A) and a 128 x 16 RAM (Port B) are created out of a single block SelectRAM+. The address space for the RAM is split by fixing the MSB of Port A to 1 (V_{CC}) for the upper 2K bits and the MSB of Port B to 0 (GND) for the lower 2K bits.

Block Memory Generation

The CoreGen program generates memory structures using the block SelectRAM+ features. This program outputs VHDL or Verilog simulation code templates and an EDIF file for inclusion in a design.

Verilog Initialization Example

```
module MYMEM (CLK, WE, ADDR, DIN, DOUT);
input CLK, WE;
input [8:0] ADDR;
input [7:0] DIN;
output [7:0] DOUT;

wire logic0, logic1;

//synopsys dc_script_begin
//set_attribute ram0 INIT_00
"0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF" -type string
//set_attribute ram0 INIT_01
"FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210" -type string
//synopsys dc_script_end

assign logic0 = 1'b0;
assign logic1 = 1'b1;

RAMB4_S8 ram0 (.WE(WE), .EN(logic1), .RST(logic0), .CLK(CLK), .ADDR(ADDR), .DI(DIN),
.DO(DOUT));
//synopsys translate_off
defparam ram0.INIT_00 =
256h'0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF;
defparam ram0.INIT_01 =
256h'FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210;
//synopsys translate_on
endmodule
```

Using SelectI/O

The Virtex-E FPGA series includes a highly configurable, high-performance I/O resource, called SelectI/O™ to provide support for a wide variety of I/O standards. The SelectI/O resource is a robust set of features including programmable control of output drive strength, slew rate, and input delay and hold time. Taking advantage of the flexibility and SelectI/O features and the design considerations described in this document can improve and simplify system level design.

Introduction

As FPGAs continue to grow in size and capacity, the larger and more complex systems designed for them demand an increased variety of I/O standards. Furthermore, as system clock speeds continue to increase, the need for high performance I/O becomes more important.

While chip-to-chip delays have an increasingly substantial impact on overall system speed, the task of achieving the desired system performance becomes more difficult with the proliferation of low-voltage I/O standards. SelectI/O, the revolutionary input/output resources of Virtex-E devices, resolve this potential problem by providing a highly configurable, high-performance alternative to the I/O resources of more conventional programmable devices. Virtex-E SelectI/O features combine the flexibility and time-to-market advantages of programmable logic with the high performance previously available only with ASICs and custom ICs.

Each SelectI/O block can support up to 20 I/O standards. Supporting such a variety of I/O standards allows the support of a wide variety of applications, from general purpose standard applications to high-speed low-voltage memory buses.

SelectI/O blocks also provide selectable output drive strengths and programmable slew rates for the LVTTL output buffers, as well as an optional, programmable weak pull-up, weak pull-down, or weak “keeper” circuit ideal for use in external bussing applications.

Each Input/Output Block (IOB) includes three registers, one each for the input, output, and 3-state signals within the IOB. These registers are optionally configurable as either a D-type flip-flop or as a level sensitive latch.

The input buffer has an optional delay element used to guarantee a zero hold time requirement for input signals registered within the IOB.

The Virtex-E SelectI/O features also provide dedicated resources for input reference voltage (V_{REF}) and output source voltage (V_{CCO}), along with a convenient banking system that simplifies board design.

By taking advantage of the built-in features and wide variety of I/O standards supported by the SelectI/O features, system-level design and board design can be greatly simplified and improved.

Fundamentals

Modern bus applications, pioneered by the largest and most influential companies in the digital electronics industry, are commonly introduced with a new I/O standard tailored specifically to the needs of that application. The bus I/O standards provide specifications to other vendors who create products designed to interface with these applications. Each standard often has its own specifications for current, voltage, I/O buffering, and termination techniques.

The ability to provide the flexibility and time-to-market advantages of programmable logic is increasingly dependent on the capability of the programmable logic device to support an ever increasing variety of I/O standards

The SelectI/O resources feature highly configurable input and output buffers which provide support for a wide variety of I/O standards. As shown in Table 18, each buffer type can support a variety of voltage requirements.

Table 18: **Virtex-E Supported I/O Standards**

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Board Termination Voltage (V_{TT})
LVTTL	3.3	3.3	N/A	N/A
LVCMOS2	2.5	2.5	N/A	N/A
LVCMOS18	1.8	1.8	N/A	N/A
SSTL3 I & II	3.3	N/A	1.50	1.50
SSTL2 I & II	2.5	N/A	1.25	1.25
GTL	N/A	N/A	0.80	1.20
GTL+	N/A	N/A	1.0	1.50
HSTL I	1.5	N/A	0.75	0.75
HSTL III & IV	1.5	N/A	0.90	1.50
CTT	3.3	N/A	1.50	1.50
AGP-2X	3.3	N/A	1.32	N/A
PCI33_3	3.3	3.3	N/A	N/A
PCI66_3	3.3	3.3	N/A	N/A
BLVDS & LVDS	2.5	N/A	N/A	N/A
LVPECL	3.3	N/A	N/A	N/A

Overview of Supported I/O Standards

This section provides a brief overview of the I/O standards supported by all Virtex-E devices.

While most I/O standards specify a range of allowed voltages, this document records typical voltage values only. Detailed information on each specification can be found on the Electronic Industry Alliance Jedec website at:

http://www.jedec.org

LVTTL — Low-Voltage TTL

The Low-Voltage TTL, or LVTTL standard is a general purpose EIA/JESDSA standard for 3.3V applications that uses an LVTTL input buffer and a Push-Pull output buffer. This standard requires a 3.3V output source voltage (V_{CCO}), but does not require the use of a reference voltage (V_{REF}) or a termination voltage (V_{TT}).

LVCMOS2 — Low-Voltage CMOS for 2.5 Volts

The Low-Voltage CMOS for 2.5 Volts or lower, or LVCMOS2 standard is an extension of the LVCMOS standard (JESD 8.-5) used for general purpose 2.5V applications. This standard requires a 2.5V output source voltage (V_{CCO}), but does not require the use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}).

LVCMOS18 — 1.8 V Low Voltage CMOS

This standard is an extension of the LVCMOS standard. It is used in general purpose 1.8 V applications. The use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}) is not required.

PCI — Peripheral Component Interface

The Peripheral Component Interface, or PCI standard specifies support for both 33 MHz and 66 MHz PCI bus applications. It uses a LVTTL input buffer and a Push-Pull output buffer. This standard does not require the use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}), however, it does require a 3.3V output source voltage (V_{CCO}).

GTL — Gunning Transceiver Logic Terminated

The Gunning Transceiver Logic, or GTL standard is a high-speed bus standard (JESD8.3) invented by Xerox. Xilinx has implemented the terminated variation for this standard. This standard requires a differential amplifier input buffer and a Open Drain output buffer.

GTL+ — Gunning Transceiver Logic Plus

The Gunning Transceiver Logic Plus, or GTL+ standard is a high-speed bus standard (JESD8.3) first used by the Pentium Pro processor.

HSTL — High-Speed Transceiver Logic

The High-Speed Transceiver Logic, or HSTL standard is a general purpose high-speed, 1.5V bus standard sponsored by IBM (EIA/JESD 8-6). This standard has four variations or classes. SelectI/O devices support Class I, III, and IV. This

Virtex-E Electrical Characteristics

Definition of Terms

Electrical and switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance: These speed files are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These speed files are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production: These speed files are released once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. Contact the factory for design considerations requiring more detailed information.

Table 1 correlates the current status of each Virtex-E device with a corresponding speed file designation.

Table 1: **Virtex-E Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XCV50E			–8, –7, –6
XCV100E			–8, –7, –6
XCV200E			–8, –7, –6
XCV300E			–8, –7, –6
XCV400E			–8, –7, –6
XCV600E			–8, –7, –6
XCV1000E			–8, –7, –6
XCV1600E			–8, –7, –6
XCV2000E			–8, –7, –6
XCV2600E			–8, –7, –6
XCV3200E			–8, –7, –6

All specifications are subject to change without notice.

CLB Distributed RAM Switching Characteristics

Description	Symbol	Speed Grade(1)				Units
		Min	-8	-7	-6	
Sequential Delays						
Clock CLK to X/Y outputs (WE active) 16 x 1 mode	$T_{SHCKO16}$	0.67	1.38	1.5	1.7	ns, max
Clock CLK to X/Y outputs (WE active) 32 x 1 mode	$T_{SHCKO32}$	0.84	1.66	1.9	2.1	ns, max
Shift-Register Mode Clock CLK to X/Y outputs	T_{REG}	1.25	2.39	2.9	3.2	ns, max
Setup and Hold Times before/after Clock CLK						
F/G address inputs	T_{AS}/T_{AH}	0.19 / 0	0.38 / 0	0.42 / 0	0.47 / 0	ns, min
BX/BY data inputs (DIN)	T_{DS}/T_{DH}	0.44 / 0	0.87 / 0	0.97 / 0	1.09 / 0	ns, min
SR input (WE)	T_{WS}/T_{WH}	0.29 / 0	0.57 / 0	0.7 / 0	0.8 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T_{WPH}	0.96	1.9	2.1	2.4	ns, min
Minimum Pulse Width, Low	T_{WPL}	0.96	1.9	2.1	2.4	ns, min
Minimum clock period to meet address write cycle time	T_{WC}	1.92	3.8	4.2	4.8	ns, min
Shift-Register Mode						
Minimum Pulse Width, High	T_{SRPH}	1.0	1.9	2.1	2.4	ns, min
Minimum Pulse Width, Low	T_{SRPL}	1.0	1.9	2.1	2.4	ns, min

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

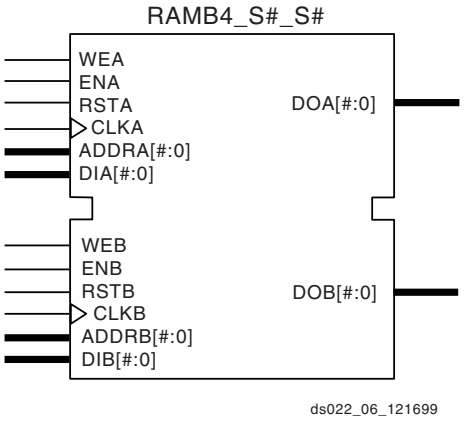

Figure 3: **Dual-Port Block SelectRAM**

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *without* DLL

Description[1]	Symbol	Device	Speed Grade[2]				Units
			Min	-8	-7	-6	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *without* DLL. For data *output* with different standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 10.	T_{ICKOF}	XCV50E	1.5	4.2	4.4	4.6	ns
		XCV100E	1.5	4.2	4.4	4.6	ns
		XCV200E	1.5	4.3	4.5	4.7	ns
		XCV300E	1.5	4.3	4.5	4.7	ns
		XCV400E	1.5	4.4	4.6	4.8	ns
		XCV600E	1.6	4.5	4.7	4.9	ns
		XCV1000E	1.7	4.6	4.8	5.0	ns
		XCV1600E	1.8	4.7	4.9	5.1	ns
		XCV2000E	1.8	4.8	5.0	5.2	ns
		XCV2600E	2.0	5.0	5.2	5.4	ns
		XCV3200E	2.2	5.2	5.4	5.6	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For other I/O standards and different loads, see Table 3 and Table 4.

DLL Clock Tolerance, Jitter, and Phase Information

All DLL output jitter and phase specifications determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers.

			CLKDLLHF		CLKDLL		
Description	**Symbol**	**F_{CLKIN}**	**Min**	**Max**	**Min**	**Max**	**Units**
Input Clock Period Tolerance	T_{IPTOL}		-	1.0	-	1.0	ns
Input Clock Jitter Tolerance (Cycle to Cycle)	T_{IJITCC}		-	± 150	-	± 300	ps
Time Required for DLL to Acquire Lock(6)	T_{LOCK}	> 60 MHz	-	20	-	20	µs
		50 - 60 MHz	-	-	-	25	µs
		40 - 50 MHz	-	-	-	50	µs
		30 - 40 MHz	-	-	-	90	µs
		25 - 30 MHz	-	-	-	120	µs
Output Jitter (cycle-to-cycle) for any DLL Clock Output(1)	T_{OJITCC}			± 60		± 60	ps
Phase Offset between CLKIN and CLKO(2)	T_{PHIO}			± 100		± 100	ps
Phase Offset between Clock Outputs on the DLL(3)	T_{PHOO}			± 140		± 140	ps
Maximum Phase Difference between CLKIN and CLKO(4)	T_{PHIOM}			± 160		± 160	ps
Maximum Phase Difference between Clock Outputs on the DLL(5)	T_{PHOOM}			± 200		± 200	ps

Notes:

1. **Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock and is based on a maximum tap delay resolution, *excluding* input clock jitter.
2. **Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* Output Jitter and input clock jitter.
3. **Phase Offset between Clock Outputs on the DLL** is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* Output Jitter and input clock jitter.
4. **Maximum Phase Difference between CLKIN an CLKO** is the sum of Output Jitter and Phase Offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).
5. **Maximum Phase DIfference between Clock Outputs on the DLL** is the sum of Output JItter and Phase Offset between any DLL clock outputs, or the greatest difference between any two DLL output rising edges sue to DLL alone (*excluding* input clock jitter).
6. Add 30% to the value for industrial grade parts.

Table 4: **CS144 — XCV50E, XCV100E, XCV200E**

Bank	Pin Description	Pin #
4	IO_L15N_YY	M11
4	IO_L15P_YY	L11
4	IO_L16N_YY	K9
4	IO_VREF_L16P_YY	N10[2]
4	IO_L17N_YY	K8
4	IO_L17P_YY	N9
4	IO_LVDS_DLL_L18P	N8
4	IO_VREF	L8
4	IO_VREF	L10
4	IO_VREF	N11[1]
5	GCK1	M7
5	IO	M4
5	IO_LVDS_DLL_L18N	M6
5	IO_L19N_YY	N5
5	IO_L19P_YY	K6
5	IO_VREF_L20N_YY	N4[2]
5	IO_L20P_YY	K5
5	IO_L21N_YY	M3
5	IO_L21P_YY	N3
5	IO_VREF	K4[1]
5	IO_VREF	L4
5	IO_VREF	L6
6	IO	G4
6	IO	J4
6	IO_L25P	H1
6	IO_VREF_L25N	H2
6	IO_L24P_YY	H3
6	IO_L24N_YY	H4
6	IO_L23P	J2
6	IO_VREF_L23N	J3[2]
6	IO_VREF	K1
6	IO_VREF	K2[1]
6	IO_L22N_YY	L1
6	IO_L22P_YY	K3

Table 4: **CS144 — XCV50E, XCV100E, XCV200E**

Bank	Pin Description	Pin #
6	IO_L26N	G1
7	IO	C2
7	IO	D3
7	IO	F3
7	IO_L26P	F2
7	IO_L27N	F4
7	IO_VREF_L27P	E1
7	IO_L28N_YY	E2
7	IO_L28P_YY	E3
7	IO_L29N	D1
7	IO_VREF_L29P	D2[2]
7	IO_VREF	C1[1]
7	IO_VREF	D4
2	CCLK	B13
3	DONE	M12
NA	M0	M1
NA	M1	L2
NA	M2	N2
NA	PROGRAM	L12
NA	TDI	A11
NA	TCK	C3
2	TDO	A12
NA	TMS	B1
NA	VCCINT	A9
NA	VCCINT	B6
NA	VCCINT	C5
NA	VCCINT	G3
NA	VCCINT	G12
NA	VCCINT	M5
NA	VCCINT	M9
NA	VCCINT	N6
0	VCCO	A2

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P138	IO_D5_L26N_YY	3
P137	VCCINT	NA
P136	VCCO	3
P135	GND	NA
P134	IO_D6_L27P_Y	3
P133	IO_VREF_L27N_Y	3
P132	IO_VREF	3
P131	IO_L28P_Y	3
P130	IO_VREF_L28N_Y	3
P129	GND	NA
P128	IO_L29P_Y	3
P127	IO_L29N_Y	3
P126	IO_VREF_L30P_Y	3
P125	IO_L30N_Y	3
P124	IO_D7_L31P_YY	3
P123	IO_INIT_L31N_YY	3
P122	PROGRAM	NA
P121	VCCO	3
P120	DONE	3
P119	GND	NA
P118	IO_L32P_YY	4
P117	IO_L32N_YY	4
P116	VCCO	4
P115	IO_VREF	4
P114	IO_L33P_YY	4
P113	IO_L33N_YY	4
P112	GND	NA
P111	IO_VREF_L34P_YY	4
P110	IO_L34N_YY	4
P109	IO_VREF	4
P108	IO_VREF_L35P_YY	4
P107	IO_L35N_YY	4
P106	GND	NA
P105	VCCO	4
P104	VCCINT	NA
P103	IO_L36P_YY	4

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P102	IO_L36N_YY	4
P101[1]	IO_VREF	4
P100	IO_L37P_Y	4
P99	IO_L37N_Y	4
P98	GND	NA
P97	IO_VREF_L38P_Y	4
P96	IO_L38N_Y	4
P95	IO_L39P	4
P94	IO_VREF_L39N	4
P93	IO_LVDS_DLL_L40P	4
P92	GCK0	4
P91	GND	NA
P90	VCCO	4
P89	GCK1	5
P88	VCCINT	NA
P87	IO_LVDS_DLL_L40N	5
P86	IO_VREF	5
P85	VCCO	5
P84	IO_VREF_L41P	5
P83	GND	NA
P82	IO_L41N	5
P81	IO	5
P80[1]	IO_VREF	5
P79	IO_L42P_YY	5
P78	IO_L42N_YY	5
P77	VCCINT	NA
P76	VCCO	5
P75	GND	NA
P74	IO_L43P_YY	5
P73	IO_VREF_L43N_YY	5
P72	IO_VREF	5
P71	IO_L44P_YY	5
P70	IO_VREF_L44N_YY	5
P69	GND	NA
P68	IO_L45P_YY	5
P67	IO_L45N_YY	5

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P66	IO_VREF_L46P	5
P65	IO_L46N	5
P64	IO_L47P_YY	5
P63	IO_L47N_YY	5
P62	M2	NA
P61	VCCO	5
P60	M0	NA
P59	GND	NA
P58	M1	NA
P57	IO_L48N_YY	6
P56	IO_L48P_YY	6
P55	VCCO	6
P54	IO_VREF	6
P53	IO_L49N_Y	6
P52	IO_L49P_Y	6
P51	GND	NA
P50	IO_VREF_L50N_Y	6
P49	IO_L50P_Y	6
P48	IO_VREF	6
P47	IO_VREF_L51N_Y	6
P46	IO_L51P_Y	6
P45	GND	NA
P44	VCCO	6
P43	VCCINT	NA
P42	IO_L52N_YY	6
P41	IO_L52P_YY	6
P40[1]	IO_VREF	6
P39	IO_L53N_Y	6
P38	IO_L53P_Y	6
P37	GND	NA
P36	IO_VREF_L54N_Y	6
P35	IO_L54P_Y	6
P34	IO_L55N_Y	6
P33	IO_VREF_L55P_Y	6
P32	VCCINT	NA
P31	IO	6

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P30	VCCO	6
P29	GND	NA
P28	IO_L56N_YY	7
P27	IO_L56P_YY	7
P26	IO_VREF	7
P25	VCCO	7
P24	IO_L57N_Y	7
P23	IO_VREF_L57P_Y	7
P22	GND	NA
P21	IO_L58N_Y	7
P20	IO_L58P_Y	7
P19[1]	IO_VREF	7
P18	IO_L59N_YY	7
P17	IO_L59P_YY	7
P16	VCCINT	NA
P15	VCCO	7
P14	GND	NA
P13	IO_L60N_Y	7
P12	IO_VREF_L60P_Y	7
P11	IO_VREF	7
P10	IO_L61N_Y	7
P9	IO_VREF_L61P_Y	7
P8	GND	NA
P7	IO_L62N_Y	7
P6	IO_L62P_Y	7
P5	IO_VREF_L63N_Y	7
P4	IO_L63P_Y	7
P3	IO	7
P2	TMS	NA
P1	GND	NA

Notes:
1. V_{REF} or I/O option only in the XCV1000E; otherwise, I/O option only.

Table 10: **BG352 — XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
NA	VCCINT	V24
NA	VCCINT	R23
NA	VCCINT	P25
NA	VCCINT	L25
NA	VCCINT	J24
0	VCCO	D19
0	VCCO	B25
0	VCCO	A17
1	VCCO	D13
1	VCCO	D7
1	VCCO	A10
2	VCCO	K1
2	VCCO	H4
2	VCCO	B2
3	VCCO	Y4
3	VCCO	U1
3	VCCO	P4
4	VCCO	AF10
4	VCCO	AE2
4	VCCO	AC8
5	VCCO	AF17
5	VCCO	AC20
5	VCCO	AC14
6	VCCO	AE25
6	VCCO	W23
6	VCCO	U26
7	VCCO	N23
7	VCCO	K26
7	VCCO	G23
NA	GND	A26
NA	GND	A25
NA	GND	A22

Table 10: **BG352 — XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
NA	GND	A19
NA	GND	A14
NA	GND	A8
NA	GND	A5
NA	GND	A2
NA	GND	A1
NA	GND	B26
NA	GND	B1
NA	GND	E26
NA	GND	E1
NA	GND	H26
NA	GND	H1
NA	GND	N1
NA	GND	P26
NA	GND	W26
NA	GND	W1
NA	GND	AB26
NA	GND	AB1
NA	GND	AE26
NA	GND	AE1
NA	GND	AF26
NA	GND	AF25
NA	GND	AF22
NA	GND	AF19
NA	GND	AF13
NA	GND	AF8
NA	GND	AF5
NA	GND	AF2
NA	GND	AF1

Notes:
1. No Connect in the XCV100E.
2. V_{REF} or I/O option only in the XCV200E and XCV300E; otherwise, I/O option only.

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
3	IO_D4_L73P_YY	W4	
3	IO_VREF_L73N_YY	W5	
3	IO_L74P_Y	Y3	
3	IO_L74N_Y	Y4	
3	IO_L75P_Y	AA1	
3	IO_L75N_Y	Y5	
3	IO_L76P_Y	AA3	
3	IO_VREF_L76N_Y	AA4	3
3	IO_L77P_Y	AB3	
3	IO_L77N_Y	AA5	
3	IO_L78P_Y	AC1	
3	IO_L78N_Y	AB4	
3	IO_L79P_YY	AC3	
3	IO_D5_L79N_YY	AB5	
3	IO_D6_L80P_YY	AC4	
3	IO_VREF_L80N_YY	AD3	
3	IO_L81P_Y	AE1	
3	IO_L81N_Y	AC5	
3	IO_L82P_Y	AD4	
3	IO_VREF_L82N_Y	AF1	4
3	IO_L83P_Y	AF2	
3	IO_L83N_Y	AD5	
3	IO_L84P_Y	AG2	
3	IO_VREF_L84N_Y	AE4	1
3	IO_L85P_YY	AH1	
3	IO_VREF_L85N_YY	AE5	
3	IO_L86P_Y	AF4	
3	IO_L86N_Y	AJ1	
3	IO_L87P_Y	AJ2	
3	IO_L87N_Y	AF5	
3	IO_L88P_Y	AG4	
3	IO_VREF_L88N_Y	AK2	
3	IO_L89P_Y	AJ3	
3	IO_L89N_Y	AG5	
3	IO_L90P_Y	AL1	

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
3	IO_VREF_L90N_Y	AH4	3
3	IO_D7_L91P_YY	AJ4	
3	IO_INIT_L91N_YY	AH5	
3	IO	U4	
4	GCK0	AL17	
4	IO	AJ8	
4	IO	AJ11	
4	IO	AK6	
4	IO	AK9	
4	IO_L92P_YY	AL4	
4	IO_L92N_YY	AJ6	
4	IO_L93P_Y	AK5	
4	IO_VREF_L93N_Y	AN3	3
4	IO_L94P_YY	AL5	
4	IO_L94N_YY	AJ7	
4	IO_VREF_L95P_YY	AM4	
4	IO_L95N_YY	AM5	
4	IO_L96P_Y	AK7	
4	IO_L96N_Y	AL6	
4	IO_L97P_YY	AM6	
4	IO_L97N_YY	AN6	
4	IO_VREF_L98P_YY	AL7	
4	IO_L98N_YY	AJ9	
4	IO_L99P_Y	AN7	
4	IO_VREF_L99N_Y	AL8	1
4	IO_L100P_Y	AM8	
4	IO_L100N_Y	AJ10	
4	IO_VREF_L101P_Y	AL9	4
4	IO_L101N_Y	AM9	
4	IO_L102P_Y	AK10	
4	IO_L102N_Y	AN9	
4	IO_VREF_L103P_YY	AL10	
4	IO_L103N_YY	AM10	
4	IO_L104P_YY	AL11	

Table 15: **BG560 Differential Pin Pair Summary**
XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
47	2	F4	C1	14	-
48	2	G5	E3	15	VREF
49	2	D2	G4	16	-
50	2	H5	E2	15	-
51	2	H4	G3	√	VREF
52	2	J5	F1	17	VREF
53	2	J4	H3	14	-
54	2	K5	H2	18	VREF
55	2	J3	K4	19	-
56	2	L5	K3	√	D1
57	2	L4	K2	√	D2
58	2	M5	L3	17	-
59	2	L1	M4	14	-
60	2	N5	M2	15	VREF
61	2	N4	N3	16	-
62	2	N2	P5	15	-
63	2	P4	P3	√	D3
64	2	P2	R5	17	-
65	2	R4	R3	14	-
66	2	R1	T4	18	VREF
67	2	T5	T3	19	VREF
68	2	T2	U3	√	-
69	3	U1	U2	19	VREF
70	3	V2	V4	18	VREF
71	3	V5	V3	14	-
72	3	W1	W3	17	-
73	3	W4	W5	√	VREF
74	3	Y3	Y4	15	-
75	3	AA1	Y5	16	-
76	3	AA3	AA4	15	VREF
77	3	AB3	AA5	14	-

Table 15: **BG560 Differential Pin Pair Summary**
XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
78	3	AC1	AB4	17	-
79	3	AC3	AB5	√	D5
80	3	AC4	AD3	√	VREF
81	3	AE1	AC5	4	-
82	3	AD4	AF1	18	VREF
83	3	AF2	AD5	14	-
84	3	AG2	AE4	20	VREF
85	3	AH1	AE5	√	VREF
86	3	AF4	AJ1	15	-
87	3	AJ2	AF5	14	-
88	3	AG4	AK2	15	VREF
89	3	AJ3	AG5	14	-
90	3	AL1	AH4	14	VREF
91	3	AJ4	AH5	√	INIT
92	4	AL4	AJ6	√	-
93	4	AK5	AN3	8	VREF
94	4	AL5	AJ7	√	-
95	4	AM4	AM5	√	VREF
96	4	AK7	AL6	3	-
97	4	AM6	AN6	√	-
98	4	AL7	AJ9	√	VREF
99	4	AN7	AL8	9	VREF
100	4	AM8	AJ10	7	-
101	4	AL9	AM9	7	VREF
102	4	AK10	AN9	2	-
103	4	AL10	AM10	√	VREF
104	4	AL11	AJ12	√	-
105	4	AN11	AK12	8	-
106	4	AL12	AM12	√	-
107	4	AK13	AL13	√	VREF
108	4	AM13	AN13	3	-

Table 15: **BG560 Differential Pin Pair Summary XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
109	4	AJ14	AK14	√	-
110	4	AM14	AN15	√	VREF
111	4	AJ15	AK15	1	-
112	4	AL15	AM16	7	-
113	4	AL16	AJ16	7	VREF
114	4	AK16	AN17	2	VREF
115	5	AM17	AM18	NA	IO_LVDS_DLL
116	5	AK18	AJ18	7	VREF
117	5	AN19	AL19	7	-
118	5	AK19	AM20	9	-
119	5	AJ19	AL20	√	VREF
120	5	AN21	AL21	√	-
121	5	AJ20	AM22	3	-
122	5	AK21	AN23	√	VREF
123	5	AJ21	AM23	√	-
124	5	AK22	AM24	8	-
125	5	AL23	AJ22	√	-
126	5	AK23	AL24	√	VREF
127	5	AN26	AJ23	13	-
128	5	AK24	AM26	7	VREF
129	5	AM27	AJ24	7	-
130	5	AL26	AK25	5	VREF
131	5	AN29	AJ25	√	VREF
132	5	AK26	AM29	√	-
133	5	AM30	AJ26	11	-
134	5	AK27	AL29	√	VREF
135	5	AN31	AJ27	√	-
136	5	AM31	AK28	12	VREF
137	6	AJ30	AH29	√	-
138	6	AH30	AK31	17	VREF
139	6	AJ31	AG29	14	-

Table 15: **BG560 Differential Pin Pair Summary XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
140	6	AG30	AK32	15	VREF
141	6	AF29	AH31	16	-
142	6	AF30	AH32	15	-
143	6	AH33	AE29	√	VREF
144	6	AE30	AG33	17	VREF
145	6	AF32	AD29	14	-
146	6	AD30	AE31	18	VREF
147	6	AC29	AE32	19	-
148	6	AC30	AD31	√	VREF
149	6	AC31	AB29	√	-
150	6	AB30	AC33	17	-
151	6	AA29	AB31	14	-
152	6	AA31	AA30	15	VREF
153	6	Y29	AA32	16	-
154	6	Y30	AA33	15	-
155	6	W29	Y32	√	VREF
156	6	W31	W30	17	-
157	6	V30	W33	14	-
158	6	V31	V29	18	VREF
159	6	U33	V32	19	VREF
160	7	U32	U31	√	-
161	7	T30	T32	19	VREF
162	7	T31	T29	18	VREF
163	7	R31	R33	14	-
164	7	R29	R30	17	-
165	7	P31	P32	√	VREF
166	7	P29	P30	15	-
167	7	N31	M32	16	-
168	7	L33	N30	15	VREF
169	7	L32	M31	14	-
170	7	L31	M30	17	-

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
0	VCCO	E34
0	VCCO	E33
0	VCCO	E30
0	VCCO	E29
0	VCCO	E27
0	VCCO	E26
1	VCCO	E10
1	VCCO	E11
1	VCCO	E13
1	VCCO	E14
1	VCCO	E6
1	VCCO	E7
2	VCCO	P5
2	VCCO	N5
2	VCCO	L5
2	VCCO	K5
2	VCCO	G5
2	VCCO	F5
3	VCCO	AP5
3	VCCO	AN5
3	VCCO	AK5
3	VCCO	AJ5
3	VCCO	AG5
3	VCCO	AF5
4	VCCO	AR10
4	VCCO	AR11
4	VCCO	AR13
4	VCCO	AR14
4	VCCO	AR6
4	VCCO	AR7
5	VCCO	AR34
5	VCCO	AR33
5	VCCO	AR30
5	VCCO	AR29
5	VCCO	AR27
5	VCCO	AR26
6	VCCO	AP35
6	VCCO	AN35
6	VCCO	AK35
6	VCCO	AJ35
6	VCCO	AG35
6	VCCO	AF35
7	VCCO	P35
7	VCCO	N35
7	VCCO	L35
7	VCCO	K35
7	VCCO	G35
7	VCCO	F35
NA	GND	Y5
NA	GND	Y4
NA	GND	Y37
NA	GND	Y36
NA	GND	Y35
NA	GND	Y3
NA	GND	W5
NA	GND	W35
NA	GND	M5
NA	GND	M4
NA	GND	M36
NA	GND	M35
NA	GND	E5
NA	GND	E35
NA	GND	E28
NA	GND	E21
NA	GND	E20
NA	GND	E19
NA	GND	E12
NA	GND	D4
NA	GND	D36
NA	GND	D28

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
6	IO_VREF_L245N_Y	AB40[1]
6	IO_L245P_Y	AC39
7	IO	F38
7	IO	H40
7	IO	H41
7	IO	J42
7	IO	K39
7	IO	L42
7	IO	N40
7	IO	T40
7	IO	U40
7	IO	V38
7	IO	W42
7	IO	Y42
7	IO	AA42
7	IO_L246N_YY	AA41
7	IO_L246P_YY	AB39
7	IO_L247N_Y	Y41
7	IO_VREF_L247P_Y	AA39[1]
7	IO_L248N_YY	Y40
7	IO_L248P_YY	Y39
7	IO_L249N_YY	Y38
7	IO_VREF_L249P_YY	W41
7	IO_L250N_Y	W40
7	IO_L250P_Y	W39
7	IO_L251N_Y	W38
7	IO_L251P_Y	V41
7	IO_L252N_YY	V39
7	IO_L252P_YY	V40
7	IO_L253N_YY	V42
7	IO_VREF_L253P_YY	U39
7	IO_L254N_Y	U41
7	IO_L254P_Y	U38
7	IO_L255N_Y	U42
7	IO_L255P_Y	T39
7	IO_L256N_YY	T41

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
7	IO_L256P_YY	T38
7	IO_L257N_Y	R39
7	IO_VREF_L257P_Y	T42
7	IO_L258N_Y	R42
7	IO_L258P_Y	R38
7	IO_L259N	R40
7	IO_L259P	P39
7	IO_L260N_Y	R41
7	IO_L260P_Y	P38
7	IO_L261N_Y	P42
7	IO_L261P_Y	N39
7	IO_L262N_Y	P40
7	IO_L262P_Y	M39
7	IO_L263N_YY	P41
7	IO_L263P_YY	M38
7	IO_L264N_YY	N42
7	IO_VREF_L264P_YY	L39
7	IO_L265N_Y	L38
7	IO_L265P_Y	N41
7	IO_L266N_YY	K40
7	IO_L266P_YY	M42
7	IO_L267N_YY	M40
7	IO_VREF_L267P_YY	K38
7	IO_L268N_Y	M41
7	IO_L268P_Y	J40
7	IO_L269N_Y	J39
7	IO_VREF_L269P_Y	L40
7	IO_L270N_YY	J38
7	IO_L270P_YY	L41
7	IO_L271N_YY	K42
7	IO_VREF_L271P_YY	H39
7	IO_L272N_Y	K41
7	IO_L272P_Y	H38
7	IO_L273N_Y	J41
7	IO_L273P_Y	G40
7	IO_L274N_YY	H42
7	IO_L274P_YY	G39

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
1	IO	J20[5]
1	IO	L18[4]
1	IO_LVDS_DLL_L34P	E16
1	IO_L35N_YY	B16
1	IO_VREF_L35P_YY	F16[2]
1	IO_L36N_YY	A16
1	IO_L36P_YY	H16
1	IO_L37N_YY	C16
1	IO_VREF_L37P_YY	K15
1	IO_L38N_YY	K16
1	IO_L38P_YY	G16
1	IO_L39N_Y	A17
1	IO_L39P_Y	E17
1	IO_L40N_Y	F17
1	IO_L40P_Y	C17
1	IO_L41N_YY	E18
1	IO_VREF_L41P_YY	A18
1	IO_L42N_YY	D18
1	IO_L42P_YY	A19
1	IO_L43N_Y	B19
1	IO_L43P_Y	G18
1	IO_L44N_Y	D19
1	IO_L44P_Y	H18
1	IO_L45N_YY	F18
1	IO_VREF_L45P_YY	F19[1]
1	IO_L46N_YY	B20
1	IO_L46P_YY	K17
1	IO_L47N_Y	D20[4]
1	IO_L47P_Y	A20[4]
1	IO_L48N_Y	G19
1	IO_L48P_Y	C20
1	IO_L49N_Y	K18
1	IO_L49P_Y	E20
1	IO_L50N_YY	B21[4]
1	IO_L50P_YY	D21[4]
1	IO_L51N_YY	F20
1	IO_L51P_YY	A21

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
1	IO_L52N_YY	C21
1	IO_VREF_L52P_YY	A22
1	IO_L53N_YY	H19
1	IO_L53P_YY	B22
1	IO_L54N_YY	E21
1	IO_L54P_YY	D22
1	IO_L55N_YY	F21
1	IO_VREF_L55P_YY	C22
1	IO_L56N_YY	H20
1	IO_L56P_YY	E22
1	IO_L57N_Y	G21
1	IO_L57P_Y	A23
1	IO_L58N_Y	A24
1	IO_L58P_Y	K19
1	IO_L59N_YY	C24
1	IO_VREF_L59P_YY	B24
1	IO_L60N_YY	H21
1	IO_L60P_YY	G22
1	IO_L61N_Y	E23
1	IO_L61P_Y	C25
1	IO_L62N_Y	D24
1	IO_L62P_Y	A26
1	IO_L63N_YY	B26
1	IO_VREF_L63P_YY	K20
1	IO_L64N_YY	D25
1	IO_L64P_YY	J21
1	IO_L65N_Y	C26[4]
1	IO_L65P_Y	F23[4]
1	IO_L66N_Y	B27
1	IO_VREF_L66P_Y	G23[1]
1	IO_L67N_Y	A27
1	IO_L67P_Y	F24
1	IO_L68N_YY	B28[3]
1	IO_L68P_YY	A28[4]
1	IO_WRITE_L69N_YY	K21
1	IO_CS_L69P_YY	C27

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
NA	GND	AP2
NA	GND	AN3
NA	GND	AM20
NA	GND	AK30
NA	GND	AG8
NA	GND	AC29
NA	GND	Y3
NA	GND	Y32
NA	GND	W21
NA	GND	V21
NA	GND	T8
NA	GND	T27
NA	GND	R21
NA	GND	P21
NA	GND	H19
NA	GND	F29
NA	GND	C11
NA	GND	B3
NA	GND	A32
NA	GND	AP3
NA	GND	AN32
NA	GND	AM24
NA	GND	AJ6
NA	GND	AG16
NA	GND	AA14
NA	GND	Y14
NA	GND	W8
NA	GND	W27
NA	GND	U14
NA	GND	T14
NA	GND	R3
NA	GND	R32
NA	GND	M6
NA	GND	H27

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
NA	GND	E5
NA	GND	C15
NA	GND	B32
NA	GND	A33
NA	GND	AP7
NA	GND	AN33
NA	GND	AM32
NA	GND	AJ12
NA	GND	AG19
NA	GND	AA15
NA	GND	Y15
NA	GND	W14
NA	GND	V14
NA	GND	U15
NA	GND	T15
NA	GND	R14
NA	GND	P14
NA	GND	M29
NA	GND	G1
NA	GND	E18
NA	GND	C20
NA	GND	B33
NA	GND	A34
NA	GND	AP28
NA	GND	AN34
NA	GND	AM33
NA	GND	AJ23
NA	GND	AG27
NA	GND	AA16
NA	GND	Y16
NA	GND	W15
NA	GND	V15
NA	GND	U16
NA	GND	T16