AMD Xilinx - XCV1600E-7FG680I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	7776
Number of Logic Elements/Cells	34992
Total RAM Bits	589824
Number of I/O	512
Number of Gates	2188742
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	680-LBGA Exposed Pad
Supplier Device Package	680-FTEBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv1600e-7fg680i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Virtex-E Ordering Information

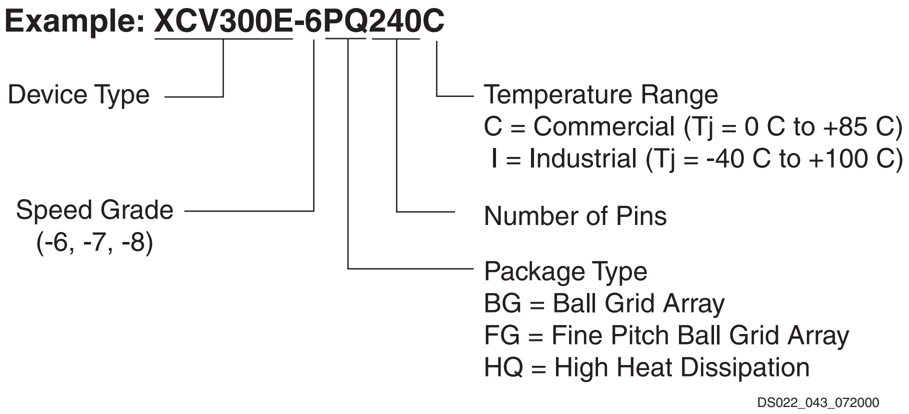

Figure 1: **Ordering Information**

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/7/99	1.0	Initial Xilinx release.
1/10/00	1.1	Re-released with spd.txt v. 1.18, FG860/900/1156 package information, and additional DLL, Select RAM and SelectI/O information.
1/28/00	1.2	Added Delay Measurement Methodology table, updated SelectI/O section, Figures 30, 54, & 55, text explaining Table 5, T_{BYP} values, buffered Hex Line info, p. 8, I/O Timing Measurement notes, notes for Tables 15, 16, and corrected F1156 pinout table footnote references.
2/29/00	1.3	Updated pinout tables, V_{CC} page 20, and corrected Figure 20.
5/23/00	1.4	Correction to table on p. 22.
7/10/00	1.5	• Numerous minor edits. • Data sheet upgraded to Preliminary. • Preview -8 numbers added to **Virtex-E Electrical Characteristics** tables.
8/1/00	1.6	• Reformatted entire document to follow new style guidelines. • Changed speed grade values in tables on pages 35-37.
9/20/00	1.7	• Min values added to **Virtex-E Electrical Characteristics** tables. • XCV2600E and XCV3200E numbers added to **Virtex-E Electrical Characteristics** tables (Module 3). • Corrected user I/O count for XCV100E device in Table 1 (Module 1). • Changed several pins to “No Connect in the XCV100E“ and removed duplicate V_{CCINT} pins in Table ~ (Module 4). • Changed pin J10 to “No connect in XCV600E” in Table 74 (Module 4). • Changed pin J30 to “VREF option only in the XCV600E” in Table 74 (Module 4). • Corrected pair 18 in Table 75 (Module 4) to be “AO in the XCV1000E, XCV1600E“.

For in-circuit debugging, an optional download and read-back cable is available. This cable connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can single-step the logic, readback the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.

Configuration

Virtex-E devices are configured by loading configuration data into the internal configuration memory. Note that attempting to load an incorrect bitstream causes configuration to fail and can damage the device.

Some of the pins used for configuration are dedicated pins, while others can be re-used as general purpose inputs and outputs once configuration is complete.

The following are dedicated pins:

- Mode pins (M2, M1, M0)
- Configuration clock pin (CCLK)
- $\overline{\text{PROGRAM}}$ pin
- DONE pin
- Boundary Scan pins (TDI, TDO, TMS, TCK)

Depending on the configuration mode chosen, CCLK can be an output generated by the FPGA, or can be generated externally and provided to the FPGA as an input. The $\overline{\text{PROGRAM}}$ pin must be pulled High prior to reconfiguration.

Note that some configuration pins can act as outputs. For correct operation, these pins require a V_{CCO} of 3.3 V or 2.5 V. At 3.3 V the pins operate as LVTTL, and at 2.5 V they operate as LVCMOS. All affected pins fall in banks 2 or 3. The configuration pins needed for SelectMap (CS, Write) are located in bank 1.

Configuration Modes

Virtex-E supports the following four configuration modes.

- Slave-serial mode
- Master-serial mode
- SelectMAP mode
- Boundary Scan mode (JTAG)

The Configuration mode pins (M2, M1, M0) select among these configuration modes with the option in each case of having the IOB pins either pulled up or left floating prior to configuration. The selection codes are listed in Table 8.

Configuration through the Boundary Scan port is always available, independent of the mode selection. Selecting the Boundary Scan mode simply turns off the other modes. The three mode pins have internal pull-up resistors, and default to a logic High if left unconnected. However, it is recommended to drive the configuration mode pins externally.

Table 8: **Configuration Codes**

Configuration Mode	M2(1)	M1	M0	CCLK Direction	Data Width	Serial D_{out}	Configuration Pull-ups(1)
Master-serial mode	0	0	0	Out	1	Yes	No
Boundary Scan mode	1	0	1	N/A	1	No	No
SelectMAP mode	1	1	0	In	8	No	No
Slave-serial mode	1	1	1	In	1	Yes	No
Master-serial mode	1	0	0	Out	1	Yes	Yes
Boundary Scan mode	0	0	1	N/A	1	No	Yes
SelectMAP mode	0	1	0	In	8	No	Yes
Slave-serial mode	0	1	1	In	1	Yes	Yes

Notes:

1. M2 is sampled continuously from power up until the end of the configuration. Toggling M2 while INIT is being held externally Low can cause the configuration pull-up settings to change.

Table 9 lists the total number of bits required to configure each device.

Table 9: **Virtex-E Bitstream Lengths**

Device	# of Configuration Bits
XCV50E	630,048
XCV100E	863,840
XCV200E	1,442,016
XCV300E	1, 875,648
XCV400E	2,693,440
XCV600E	3,961,632
XCV1000E	6,587,520
XCV1600E	8,308,992
XCV2000E	10,159,648
XCV2600E	12,922,336
XCV3200E	16,283,712

Slave-Serial Mode

In slave-serial mode, the FPGA receives configuration data in bit-serial form from a serial PROM or other source of serial configuration data. The serial bitstream must be set up at the DIN input pin a short time before each rising edge of an externally generated CCLK.

For more detailed information on serial PROMs, see the PROM data sheet at http://www.xilinx.com/bvdocs/publications/ds026.pdf.

Multiple FPGAs can be daisy-chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed to the DOUT pin. The maximum capacity for a single LOUT/DOUT write is 2^{20}-1 (1,048,575) 32-bit words, or 33,554,4000 bits. The data on the DOUT pin changes on the rising edge of CCLK.

The change of DOUT on the rising edge of CCLK differs from previous families, but does not cause a problem for mixed configuration chains. This change was made to improve serial configuration rates for Virtex and Virtex-E only chains.

Figure 13 shows a full master/slave system. A Virtex-E device in slave-serial mode should be connected as shown in the right-most device.

Slave-serial mode is selected by applying <111> or <011> to the mode pins (M2, M1, M0). A weak pull-up on the mode pins makes slave serial the default mode if the pins are left unconnected. However, it is recommended to drive the configuration mode pins externally. Figure 14 shows slave-serial mode programming switching characteristics.

Table 10 provides more detail about the characteristics shown in Figure 14. Configuration must be delayed until the $\overline{\text{INIT}}$ pins of all daisy-chained FPGAs are High.

Table 10: **Master/Slave Serial Mode Programming Switching**

	Description	Figure References	Symbol	Values	Units
CCLK	DIN setup/hold, slave mode	1/2	T_{DCC}/T_{CCD}	5.0 / 0.0	ns, min
	DIN setup/hold, master mode	1/2	T_{DSCK}/T_{CKDS}	5.0 / 0.0	ns, min
	DOUT	3	T_{CCO}	12.0	ns, max
	High time	4	T_{CCH}	5.0	ns, min
	Low time	5	T_{CCL}	5.0	ns, min
	Maximum Frequency		F_{CC}	66	MHz, max
	Frequency Tolerance, master mode with respect to nominal			+45% –30%	

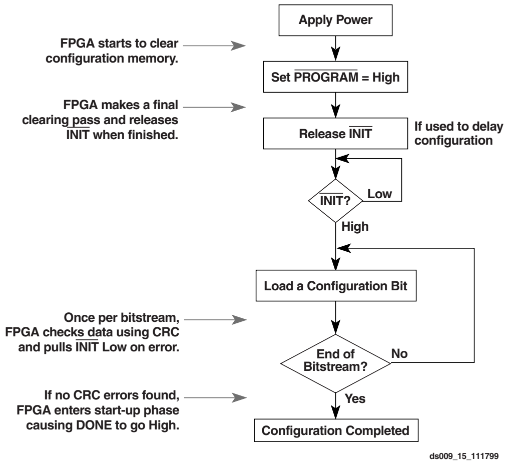

Figure 15: **Serial Configuration Flowchart**

Figure 16 shows the timing of master-serial configuration. Master-serial mode is selected by a <000> or <100> on the mode pins (M2, M1, M0). Table 10 shows the timing information for Figure 16.

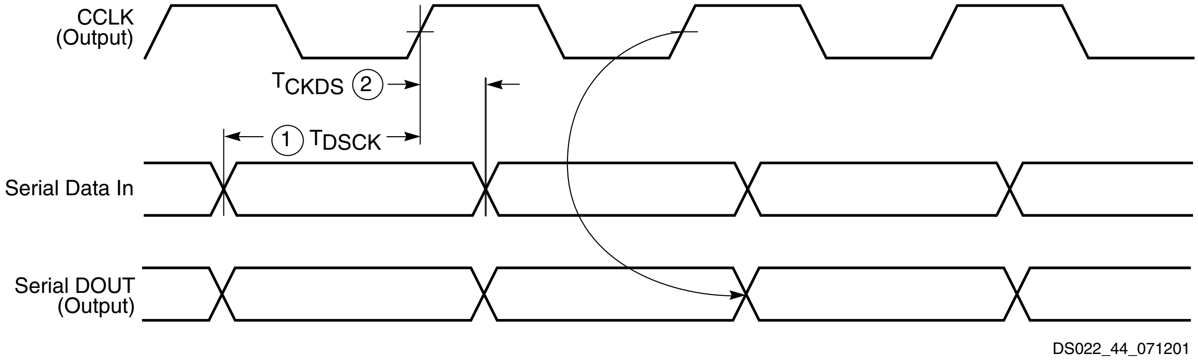

Figure 16: **Master-Serial Mode Programming Switching Characteristics**

At power-up, V_{CC} must rise from 1.0 V to V_{CC} Min in less than 50 ms, otherwise delay configuration by pulling PROGRAM Low until V_{CC} is valid.

SelectMAP Mode

The SelectMAP mode is the fastest configuration option. Byte-wide data is written into the FPGA with a BUSY flag controlling the flow of data.

An external data source provides a byte stream, CCLK, a Chip Select (CS) signal and a Write signal (WRITE). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low.

Data can also be read using the SelectMAP mode. If WRITE is not asserted, configuration data is read out of the FPGA as part of a readback operation.

After configuration, the pins of the SelectMAP port can be used as additional user I/O. Alternatively, the port can be retained to permit high-speed 8-bit readback.

Retention of the SelectMAP port is selectable on a design-by-design basis when the bitstream is generated. If retention is selected, PROHIBIT constraints are required to prevent the SelectMAP-port pins from being used as user I/O.

Multiple Virtex-E FPGAs can be configured using the SelectMAP mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, WRITE, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by asserting the CS pin of each device in turn and writing the appropriate data. See Table 11 for SelectMAP Write Timing Characteristics.

Write

Write operations send packets of configuration data into the FPGA. The sequence of operations for a multi-cycle write operation is shown below. Note that a configuration packet can be split into many such sequences. The packet does not have to complete within one assertion of CS, illustrated in Figure 17.

1. Assert WRITE and CS Low. Note that when CS is asserted on successive CCLKs, WRITE must remain either asserted or de-asserted. Otherwise, an abort is initiated, as described below.
2. Drive data onto D[7:0]. Note that to avoid contention, the data source should not be enabled while CS is Low and WRITE is High. Similarly, while WRITE is High, no more that one CS should be asserted.

Configuration through the TAP uses the CFG_IN instruction. This instruction allows data input on TDI to be converted into data packets for the internal configuration bus.

The following steps are required to configure the FPGA through the Boundary Scan port (when using TCK as a start-up clock).

1. Load the CFG_IN instruction into the Boundary Scan instruction register (IR).
2. Enter the Shift-DR (SDR) state.
3. Shift a configuration bitstream into TDI.
4. Return to Run-Test-Idle (RTI).
5. Load the JSTART instruction into IR.
6. Enter the SDR state.
7. Clock TCK through the startup sequence.
8. Return to RTI.

Configuration and readback via the TAP is always available. The Boundary Scan mode is selected by a <101> or <001> on the mode pins (M2, M1, M0). For details on TAP characteristics, refer to XAPP139.

Configuration Sequence

The configuration of Virtex-E devices is a three-phase process. First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user, as described below. The configuration process can also be initiated by asserting $\overline{\text{PROGRAM}}$. The end of the memory-clearing phase is signalled by $\overline{\text{INIT}}$ going High, and the completion of the entire process is signalled by DONE going High.

The power-up timing of configuration signals is shown in Figure 20.

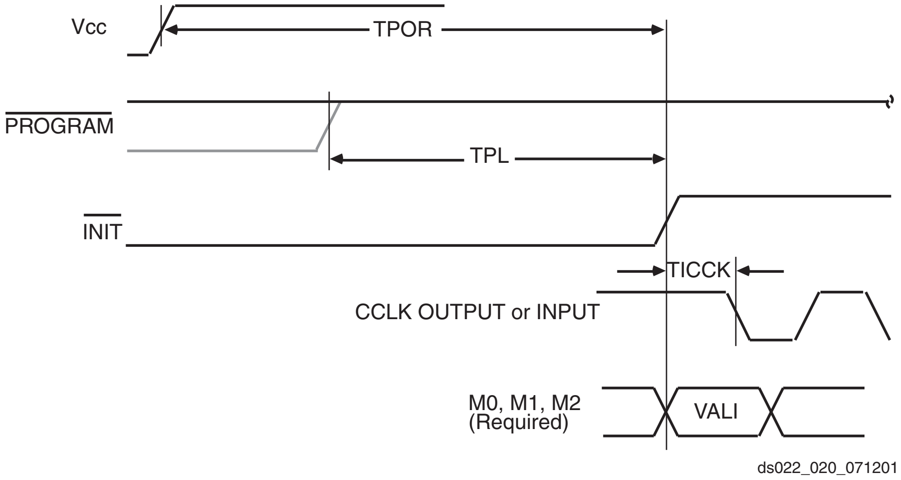

Figure 20: **Power-Up Timing Configuration Signals**

The corresponding timing characteristics are listed in Table 12.

Table 12: **Power-up Timing Characteristics**

Description	Symbol	Value	Units
Power-on Reset[1]	T_{POR}	2.0	ms, max
Program Latency	T_{PL}	100.0	µs, max
CCLK (output) Delay	T_{ICCK}	0.5	µs, min
		4.0	µs, max
Program Pulse Width	$T_{PROGRAM}$	300	ns, min

Notes:

1. T_{POR} delay is the initialization time required after V_{CCINT} and V_{CCO} in Bank 2 reach the recommended operating voltage.

Delaying Configuration

$\overline{\text{INIT}}$ can be held Low using an open-drain driver. An open-drain is required since $\overline{\text{INIT}}$ is a bidirectional open-drain pin that is held Low by the FPGA while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

Start-Up Sequence

The default Start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary.

One CCLK cycle later, the Global Set/Reset (GSR) and Global Write Enable (GWE) signals are released. This permits

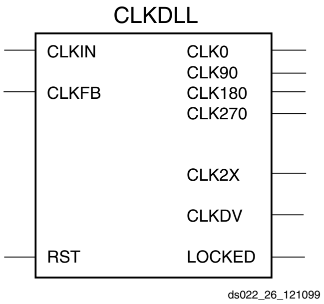

Figure 22: **Standard DLL Symbol CLKDLL**

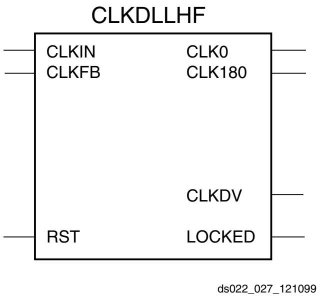

Figure 23: **High Frequency DLL Symbol CLKDLLHF**

BUFGDLL Pin Descriptions

Use the BUFGDLL macro as the simplest way to provide zero propagation delay for a high-fanout on-chip clock from an external input. This macro uses the IBUFG, CLKDLL and BUFG primitives to implement the most basic DLL application as shown in Figure 24.

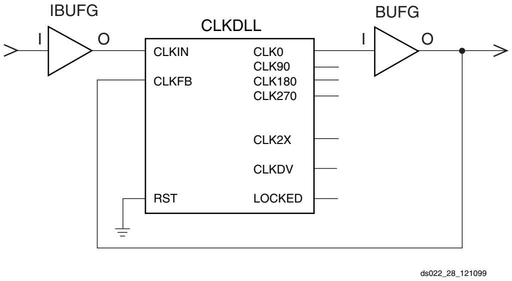

Figure 24: **BUFGDLL Schematic**

This symbol does not provide access to the advanced clock domain controls or to the clock multiplication or clock division features of the DLL. This symbol also does not provide access to the RST, or LOCKED pins of the DLL. For access to these features, a designer must use the library DLL primitives described in the following sections.

Source Clock Input — I

The I pin provides the user source clock, the clock signal on which the DLL operates, to the BUFGDLL. For the BUFGDLL macro the source clock frequency must fall in the low frequency range as specified in the data sheet. The BUFGDLL requires an external signal source clock. Therefore, only an external input port can source the signal that drives the BUFGDLL I pin.

Clock Output — O

The clock output pin O represents a delay-compensated version of the source clock (I) signal. This signal, sourced by a global clock buffer BUFG symbol, takes advantage of the dedicated global clock routing resources of the device.

The output clock has a 50-50 duty cycle unless you deactivate the duty cycle correction property.

CLKDLL Primitive Pin Descriptions

The library CLKDLL primitives provide access to the complete set of DLL features needed when implementing more complex applications with the DLL.

Source Clock Input — CLKIN

The CLKIN pin provides the user source clock (the clock signal on which the DLL operates) to the DLL. The CLKIN frequency must fall in the ranges specified in the data sheet. A global clock buffer (BUFG) driven from another CLKDLL, one of the global clock input buffers (IBUFG), or an IO_LVDS_DLL pin on the same edge of the device (top or bottom) must source this clock signal. There are four IO_LVDS_DLL input pins that can be used as inputs to the DLLs. This makes a total of eight usable input pins for DLLs in the Virtex-E family.

Feedback Clock Input — CLKFB

The DLL requires a reference or feedback signal to provide the delay-compensated output. Connect only the CLK0 or CLK2X DLL outputs to the feedback clock input (CLKFB) pin to provide the necessary feedback to the DLL. The feedback clock input can also be provided through one of the following pins.

IBUFG - Global Clock Input Pad

IO_LVDS_DLL - the pin adjacent to IBUFG

If an IBUFG sources the CLKFB pin, the following special rules apply.

1. An external input port must source the signal that drives the IBUFG I pin.
2. The CLK2X output must feedback to the device if both the CLK0 and CLK2X outputs are driving off chip devices.
3. That signal must directly drive only OBUFs and nothing else.

These rules enable the software determine which DLL clock output sources the CLKFB pin.

Reset Input — RST

When the reset pin RST activates the LOCKED signal deactivates within four source clock cycles. The RST pin, active High, must either connect to a dynamic signal or tied to

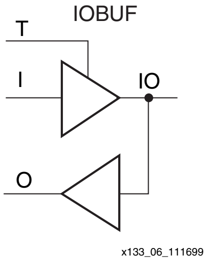

Figure 42: **Input/Output Buffer Symbol (IOBUF)**

The following list details variations of the IOBUF symbol.

- IOBUF
- IOBUF_S_2
- IOBUF_S_4
- IOBUF_S_6
- IOBUF_S_8
- IOBUF_S_12
- IOBUF_S_16
- IOBUF_S_24
- IOBUF_F_2
- IOBUF_F_4
- IOBUF_F_6
- IOBUF_F_8
- IOBUF_F_12
- IOBUF_F_16
- IOBUF_F_24
- IOBUF_LVCMOS2
- IOBUF_PCI33_3
- IOBUF_PCI66_3
- IOBUF_GTL
- IOBUF_GTLP
- IOBUF_HSTL_I
- IOBUF_HSTL_III
- IOBUF_HSTL_IV
- IOBUF_SSTL3_I
- IOBUF_SSTL3_II
- IOBUF_SSTL2_I
- IOBUF_SSTL2_II
- IOBUF_CTT
- IOBUF_AGP
- IOBUF_LVCMOS18
- IOBUF_LVDS
- IOBUF_LVPECL

When the IOBUF symbol used supports an I/O standard that requires a differential amplifier input, the IOBUF automatically configures with a differential amplifier input buffer. The low-voltage I/O standards with a differential amplifier input require an external reference voltage input V_{REF}.

The voltage reference signal is "banked" within the Virtex-E device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 38, page 34 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

IOBUF placement restrictions require any differential amplifier input signals within a bank be of the same standard.

The Virtex-E series supports eight banks for the HQ and PQ packages. The CS package supports four V_{CCO} banks.

Additional restrictions on the Virtex-E SelectI/O IOBUF placement require that within a given V_{CCO} bank each IOBUF must share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within the same V_{CCO} bank. The LOC property can specify a location for the IOBUF.

An optional delay element is associated with the input path in each IOBUF. When the IOBUF drives an input flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Override this default with the NODELAY=TRUE property.

In the case when the IOBUF does not drive an input flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak "keeper" circuit. Control this feature by adding the appropriate symbol to the output net of the IOBUF (PULLUP, PULLDOWN, or KEEPER).

SelectI/O Properties

Access to some of the SelectI/O features (for example, location constraints, input delay, output drive strength, and slew rate) is available through properties associated with these features.

Input Delay Properties

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Use the NODELAY=TRUE property to override this default.

In the case when the IBUF does not drive a flip-flop within the IOB, the delay element by default de-activates to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

IOB Input Switching Characteristics Standard Adjustments

			Speed Grade(1)				Units
Description	**Symbol**	**Standard**	**Min**	**-8**	**-7**	**-6**	
Data Input Delay Adjustments							
Standard-specific data input delay adjustments	T_{ILVTTL}	LVTTL	0.0	0.0	0.0	0.0	ns
	$T_{ILVCMOS2}$	LVCMOS2	–0.02	0.0	0.0	0.0	ns
	$T_{ILVCMOS18}$	LVCMOS18	0.12	+0.20	+0.20	+0.20	ns
	T_{ILVDS}	LVDS	0.00	+0.15	+0.15	+0.15	ns
	$T_{ILVPECL}$	LVPECL	0.00	+0.15	+0.15	+0.15	ns
	T_{IPCI33_3}	PCI, 33 MHz, 3.3 V	–0.05	+0.08	+0.08	+0.08	ns
	T_{IPCI66_3}	PCI, 66 MHz, 3.3 V	–0.05	–0.11	–0.11	–0.11	ns
	T_{IGTL}	GTL	+0.10	+0.14	+0.14	+0.14	ns
	$T_{IGTLPLUS}$	GTL+	+0.06	+0.14	+0.14	+0.14	ns
	T_{IHSTL}	HSTL	+0.02	+0.04	+0.04	+0.04	ns
	T_{ISSTL2}	SSTL2	–0.04	+0.04	+0.04	+0.04	ns
	T_{ISSTL3}	SSTL3	–0.02	+0.04	+0.04	+0.04	ns
	T_{ICTT}	CTT	+0.01	+0.10	+0.10	+0.10	ns
	T_{IAGP}	AGP	–0.03	+0.04	+0.04	+0.04	ns

Notes:

1. Input timing i for LVTTL is measured at 1.4 V. For other I/O standards, see Table 4.

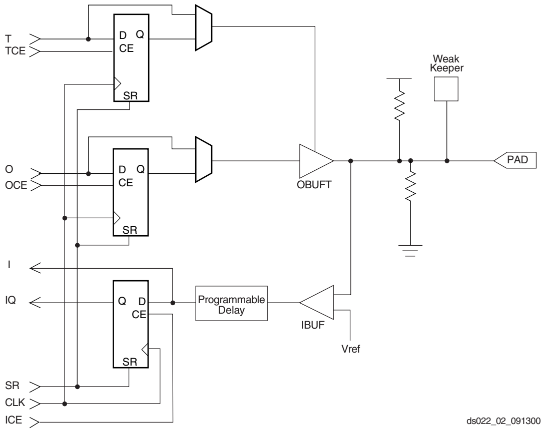

Figure 1: **Virtex-E Input/Output Block (IOB)**

IOB Output Switching Characteristics, Figure 1

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 10.

		Speed Grade(1)				
Description(2)	**Symbol**	**Min**	**-8**	**-7**	**-6**	**Units**
Propagation Delays						
O input to Pad	T_{IOOP}	1.04	2.5	2.7	2.9	ns, max
O input to Pad via transparent latch	T_{IOOLP}	1.24	2.9	3.1	3.4	ns, max
3-State Delays						
T input to Pad high-impedance (Note 2)	T_{IOTHZ}	0.73	1.5	1.7	1.9	ns, max
T input to valid data on Pad	T_{IOTON}	1.13	2.7	2.9	3.1	ns, max
T input to Pad high-impedance via transparent latch (Note 2)	$T_{IOTLPHZ}$	0.86	1.8	2.0	2.2	ns, max
T input to valid data on Pad via transparent latch	$T_{IOTLPON}$	1.26	3.0	3.2	3.4	ns, max
GTS to Pad high impedance (Note 2)	T_{GTS}	1.94	4.1	4.6	4.9	ns, max
Sequential Delays						
Clock CLK						
Minimum Pulse Width, High	T_{CH}	0.56	1.2	1.3	1.4	ns, min
Minimum Pulse Width, Low	T_{CL}	0.56	1.2	1.3	1.4	ns, min
Clock CLK to Pad	T_{IOCKP}	0.97	2.4	2.8	2.9	ns, max
Clock CLK to Pad high-impedance (synchronous) (Note 2)	T_{IOCKHZ}	0.77	1.6	2.0	2.2	ns, max
Clock CLK to valid data on Pad (synchronous)	T_{IOCKON}	1.17	2.8	3.2	3.4	ns, max
Setup and Hold Times before/after Clock CLK						
O input	T_{IOOCK} / T_{IOCKO}	0.43 / 0	0.9 / 0	1.0 / 0	1.1 / 0	ns, min
OCE input	$T_{IOOCECK}$ / $T_{IOCKOCE}$	0.28 / 0	0.55 / 0.01	0.7 / 0	0.7 / 0	ns, min
SR input (OFF)	$T_{IOSRCKO}$ / $T_{IOCKOSR}$	0.40 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
3-State Setup Times, T input	T_{IOTCK} / T_{IOCKT}	0.26 / 0	0.51 / 0	0.6 / 0	0.7 / 0	ns, min
3-State Setup Times, TCE input	$T_{IOTCECK}$ / $T_{IOCKTCE}$	0.30 / 0	0.6 / 0	0.7 / 0	0.8 / 0	ns, min
3-State Setup Times, SR input (TFF)	$T_{IOSRCKT}$ / $T_{IOCKTSR}$	0.38 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
Set/Reset Delays						
SR input to Pad (asynchronous)	T_{IOSRP}	1.30	3.1	3.3	3.5	ns, max
SR input to Pad high-impedance (asynchronous) (Note 2)	T_{IOSRHZ}	1.08	2.2	2.4	2.7	ns, max
SR input to valid data on Pad (asynchronous)	T_{IOSRON}	1.48	3.4	3.7	3.9	ns, max
GSR to Pad	T_{IOGSRQ}	3.88	7.6	8.5	9.7	ns, max

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. 3-state turn-off delays should not be adjusted.

Block RAM Switching Characteristics

		Speed Grade[1]				
Description	**Symbol**	**Min**	**-8**	**-7**	**-6**	**Units**
Sequential Delays						
Clock CLK to DOUT output	T_{BCKO}	0.63	2.46	3.1	3.5	ns, max
Setup and Hold Times before Clock CLK						
ADDR inputs	T_{BACK}/T_{BCKA}	0.42 / 0	0.9 / 0	1.0 / 0	1.1 / 0	ns, min
DIN inputs	T_{BDCK}/T_{BCKD}	0.42 / 0	0.9 / 0	1.0 / 0	1.1 / 0	ns, min
EN input	T_{BECK}/T_{BCKE}	0.97 / 0	2.0 / 0	2.2 / 0	2.5 / 0	ns, min
RST input	T_{BRCK}/T_{BCKR}	0.9 / 0	1.8 / 0	2.1 / 0	2.3 / 0	ns, min
WEN input	T_{BWCK}/T_{BCKW}	0.86 / 0	1.7 / 0	2.0 / 0	2.2 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T_{BPWH}	0.6	1.2	1.35	1.5	ns, min
Minimum Pulse Width, Low	T_{BPWL}	0.6	1.2	1.35	1.5	ns, min
CLKA -> CLKB setup time for different ports	T_{BCCS}	1.2	2.4	2.7	3.0	ns, min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

TBUF Switching Characteristics

		Speed Grade				
Description	**Symbol**	**Min**	**-8**	**-7**	**-6**	**Units**
Combinatorial Delays						
IN input to OUT output	T_{IO}	0.0	0.0	0.0	0 .0	ns, max
TRI input to OUT output high-impedance	T_{OFF}	0.05	0.092	0.10	0.11	ns, max
TRI input to valid data on OUT output	T_{ON}	0.05	0.092	0.10	0.11	ns, max

JTAG Test Access Port Switching Characteristics

Description	Symbol	Value	Units
TMS and TDI Setup times before TCK	T_{TAPTK}	4.0	ns, min
TMS and TDI Hold times after TCK	T_{TCKTAP}	2.0	ns, min
Output delay from clock TCK to output TDO	T_{TCKTDO}	11.0	ns, max
Maximum TCK clock frequency	F_{TCK}	33	MHz, max

Table 12: **BG432 — XCV300E, XCV400E, XCV600E**

Bank	Pin Description	Pin #
6	VCCO	AL31
7	VCCO	A31
7	VCCO	L28
7	VCCO	L31
NA	GND	A2
NA	GND	A3
NA	GND	A7
NA	GND	A9
NA	GND	A14
NA	GND	A18
NA	GND	A23
NA	GND	A25
NA	GND	A29
NA	GND	A30
NA	GND	B1
NA	GND	B2
NA	GND	B30
NA	GND	B31
NA	GND	C1
NA	GND	C31
NA	GND	D16
NA	GND	G1
NA	GND	G31
NA	GND	J1
NA	GND	J31
NA	GND	P1
NA	GND	P31
NA	GND	T4
NA	GND	T28
NA	GND	V1
NA	GND	V31
NA	GND	AC1
NA	GND	AC31
NA	GND	AE1
NA	GND	AE31
NA	GND	AH16
NA	GND	AJ1
NA	GND	AJ31
NA	GND	AK1
NA	GND	AK2
NA	GND	AK30
NA	GND	AK31
NA	GND	AL2
NA	GND	AL3
NA	GND	AL7
NA	GND	AL9
NA	GND	AL14
NA	GND	AL18
NA	GND	AL23
NA	GND	AL25
NA	GND	AL29
NA	GND	AL30

Notes:

1. V_{REF} or I/O option only in the XCV600E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV400E, XCV600E; otherwise, I/O option only.

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
1	IO_L23P_Y	A17
1	IO_L24N_YY	B17
1	IO_VREF_L24P_YY	A18
1	IO_L25N_YY	D16
1	IO_L25P_YY	C17
1	IO_L26N_YY	B18
1	IO_VREF_L26P_YY	A19
1	IO_L27N_YY	D17
1	IO_L27P_YY	C18
1	IO_WRITE_L28N_YY	A20
1	IO_CS_L28P_YY	C19
2	IO	D18[1]
2	IO	E19[1]
2	IO	E20
2	IO	F20
2	IO	G21
2	IO	G22[1]
2	IO	J22
2	IO	L19[1]
2	IO_D3	K20
2	IO_DOUT_BUSY_L29P_YY	C21
2	IO_DIN_D0_L29N_YY	D20
2	IO_L30P_YY	C22
2	IO_L30N_YY	D21
2	IO_VREF_L31P_YY	D22
2	IO_L31N_YY	E21
2	IO_L32P_YY	E22
2	IO_L32N_YY	F18
2	IO_VREF_L33P_YY	F21
2	IO_L33N_YY	F19
2	IO_L34P_Y	F22
2	IO_L34N_Y	G19
2	IO_L35P_Y	G20
2	IO_L35N_Y	G18
2	IO_VREF_L36P_Y	H18
2	IO_D1_L36N_Y	H22
2	IO_D2_L37P_YY	H20
2	IO_L37N_YY	H19
2	IO_L38P_YY	H21
2	IO_L38N_YY	J19
2	IO_L39P_YY	J18
2	IO_L39N_YY	J20
2	IO_L40P_Y	K18
2	IO_L40N_Y	J21
2	IO_L41P	K22
2	IO_VREF_L41N	K21
2	IO_L42P_Y	K19
2	IO_L42N_Y	L22
2	IO_L43P_YY	L21
2	IO_L43N_YY	L18
2	IO_L44P_YY	L17
2	IO_L44N_YY	L20
3	IO	M21[1]
3	IO	P22
3	IO	R20[1]
3	IO	R22
3	IO	T19
3	IO	U18[1]
3	IO	V20
3	IO	V21
3	IO	Y22[1]
3	IO_L45P_YY	M18
3	IO_L45N_YY	M20
3	IO_L46P_Y	M19
3	IO_L46N_Y	M17
3	IO_D4_L47P_Y	N22
3	IO_VREF_L47N_Y	N21
3	IO_L48P_YY	N20
3	IO_L48N_YY	N18
3	IO_L49P_YY	N19
3	IO_L49N_YY	P21
3	IO_L50P_YY	P20

Table 19: **FG456 Differential Pin Pair Summary XCV200E, XCV300E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
88	5	V7	AB3	√	-
89	6	Y2	W3	√	-
90	6	V3	V4	√	-
91	6	U4	Y1	√	VREF
92	6	W1	V2	√	-
93	6	U2	T3	√	VREF
94	6	V1	T5	2	-
95	6	U1	R5	1	-
96	6	T1	R4	2	VREF
97	6	P3	R2	√	-
98	6	R1	P5	√	-
99	6	N5	P2	√	-
100	6	N4	P1	2	-
101	6	N2	N3	1	VREF
102	6	M4	N1	2	-
103	6	M6	M3	√	-
104	7	L4	L3	√	-
105	7	L1	L5	√	-
106	7	K2	L6	2	-
107	7	K3	K4	2	VREF
108	7	K5	K1	√	-
109	7	J2	J3	√	-
110	7	H1	J5	√	-
111	7	H3	H2	√	-
112	7	H4	G1	2	VREF
113	7	F2	F1	2	-
114	7	G3	H5	√	-
115	7	E2	E1	√	VREF
116	7	G5	F3	√	-
117	7	D2	E3	√	VREF
118	7	C1	F5	√	-

Notes:
1. AO in the XCV200E.
2. AO in the XCV300E.

FG676 Fine-Pitch Ball Grid Array Package

XCV400E and XCV600E devices in the FG676 fine-pitch Ball Grid Array package have footprint compatibility. Pins labeled I0_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 20, see Table 21 for Differential Pair information.

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
0	GCK3	E13
0	IO	A6
0	IO	A9[1]
0	IO	A10[1]
0	IO	B3
0	IO	B4[1]
0	IO	B12[1]
0	IO	C6
0	IO	C8
0	IO	D5
0	IO	D13[1]
0	IO	G13
0	IO_L0N_Y	C4
0	IO_L0P_Y	F7
0	IO_L1N_YY	G8
0	IO_L1P_YY	C5
0	IO_VREF_L2N_YY	D6
0	IO_L2P_YY	E7
0	IO_L3N	A4
0	IO_L3P	F8
0	IO_L4N	B5
0	IO_L4P	D7
0	IO_VREF_L5N_YY	E8
0	IO_L5P_YY	G9
0	IO_L6N_YY	A5
0	IO_L6P_YY	F9
0	IO_L7N_Y	D8
0	IO_L7P_Y	C7
0	IO_VREF_L8N_Y	B7[2]
0	IO_L8P_Y	E9

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
4	IO_L98N_YY	AB19
4	IO_L99P_YY	AC20
4	IO_L99N_YY	AA18
4	IO_L100P_Y	AC19
4	IO_L100N_Y	AD20
4	IO_VREF_L101P_Y	AF20[2]
4	IO_L101N_Y	AB18
4	IO_L102P	AD19
4	IO_L102N	Y17
4	IO_L103P	AE19
4	IO_VREF_L103N	AD18
4	IO_L104P_YY	AF19
4	IO_L104N_YY	AA17
4	IO_L105P_Y	AC17
4	IO_L105N_Y	AB17
4	IO_L106P_YY	Y16
4	IO_L106N_YY	AE17
4	IO_L107P_YY	AF17
4	IO_L107N_YY	AA16
4	IO_L108P	AD17
4	IO_L108N	AB16
4	IO_L109P_YY	AC16
4	IO_L109N_YY	AD16
4	IO_VREF_L110P_YY	AC15
4	IO_L110N_YY	Y15
4	IO_L111P_YY	AD15
4	IO_L111N_YY	AA15
4	IO_L112P_Y	W14
4	IO_L112N_Y	AB15
4	IO_VREF_L113P_Y	AF15
4	IO_L113N_Y	Y14
4	IO_L114P	AD14
4	IO_L114N	AB14
4	IO_LVDS_DLL_L115P	AC14
5	GCK1	AB13
5	IO	Y13[1]
5	IO	AD7
5	IO	AD13
5	IO	AE4
5	IO	AE7
5	IO	AE12[1]
5	IO	AF3[1]
5	IO	AF5
5	IO	AF10[1]
5	IO	AF11[1]
5	IO_LVDS_DLL_L115N	AF13
5	IO_L116P_Y	AA13
5	IO_VREF_L116N_Y	AF12
5	IO_L117P_Y	AC13
5	IO_L117N_Y	W13
5	IO_L118P_YY	AA12
5	IO_L118N_YY	AD12
5	IO_L119P_YY	AC12
5	IO_VREF_L119N_YY	AB12
5	IO_L120P_YY	AD11
5	IO_L120N_YY	Y12
5	IO_L121P	AB11
5	IO_L121N	AD10
5	IO_L122P_YY	AC11
5	IO_L122N_YY	AE10
5	IO_L123P_YY	AC10
5	IO_L123N_YY	AA11
5	IO_L124P_Y	Y11
5	IO_L124N_Y	AD9
5	IO_L125P_YY	AB10
5	IO_L125N_YY	AF9
5	IO_L126P_YY	AD8
5	IO_VREF_L126N_YY	AA10
5	IO_L127P_YY	AE8
5	IO_L127N_YY	Y10
5	IO_L128P_Y	AC9
5	IO_VREF_L128N_Y	AF8[2]
5	IO_L129P_Y	AF7

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
NA	GND	D20
NA	GND	D12
NA	GND	C39
NA	GND	C37
NA	GND	C3
NA	GND	C20
NA	GND	C1
NA	GND	B39
NA	GND	B38
NA	GND	B2
NA	GND	B1
NA	GND	AW39
NA	GND	AW38
NA	GND	AW37
NA	GND	AW3
NA	GND	AW2
NA	GND	AW1
NA	GND	AV39
NA	GND	AV38
NA	GND	AV2
NA	GND	AV1
NA	GND	AU39
NA	GND	AU37
NA	GND	AU3
NA	GND	AU20
NA	GND	AU1
NA	GND	AT4
NA	GND	AT36
NA	GND	AT28
NA	GND	AT20
NA	GND	AT12
NA	GND	AR5
NA	GND	AR35
NA	GND	AR28
NA	GND	AR21
NA	GND	AR20
NA	GND	AR19
NA	GND	AR12
NA	GND	AH5
NA	GND	AH4
NA	GND	AH36
NA	GND	AH35
NA	GND	AA5
NA	GND	AA35
NA	GND	A39
NA	GND	A38
NA	GND	A37
NA	GND	A3
NA	GND	A2
NA	GND	A1

Notes:

1. V_{REF} or I/O option only in the XCV1000E, 1600E, 2000E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV1600E, 2000E; otherwise, I/O option only.
3. V_{REF} or I/O option only in the XCV2000E; otherwise, I/O option only.

Table 23: **FG680 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
52	1	B8	A8	√	VREF
53	1	A7	D9	√	-
54	1	B7	C8	3	-
55	1	A6	D8	3	-
56	1	B6	C7	√	VREF
57	1	A5	D7	√	-
58	1	B5	C6	5	VREF
59	1	A4	D6	5	-
60	1	D5	B4	√	CS
61	2	E3	C2	√	DIN, D0
62	2	D3	F3	6	-
63	2	D2	G4	4	VREF
64	2	G3	E2	4	-
65	2	H4	E1	6	VREF
66	2	H3	F2	√	-
67	2	J4	F1	4	-
68	2	J3	G2	6	-
69	2	G1	K4	√	VREF
70	2	H2	K3	√	-
71	2	H1	L4	7	VREF
72	2	J2	L3	4	-
73	2	J1	M3	√	VREF
74	2	K2	N4	√	-
75	2	K1	N3	4	-
76	2	L2	P4	√	D1
77	2	P3	L1	√	D2
78	2	R4	M2	6	-
79	2	R3	M1	4	-
80	2	T4	N2	4	-
81	2	N1	T3	6	VREF
82	2	P2	U5	√	-
83	2	P1	U4	4	-
84	2	R2	U3	6	-
85	2	V5	R1	√	D3
86	2	V4	T2	√	-
87	2	V3	T1	7	-
88	2	W4	U2	4	-
89	2	W3	U1	√	VREF
90	2	AA3	V2	√	-
91	2	AA4	V1	4	VREF
92	2	AB2	W2	√	-
93	3	AB4	W1	4	VREF
94	3	AB5	Y2	√	-
95	3	AC2	Y1	√	VREF
96	3	AC3	AA1	4	-
97	3	AC4	AA2	7	-
98	3	AC5	AB1	√	-
99	3	AD3	AC1	√	VREF
100	3	AD1	AD4	6	-
101	3	AD2	AE3	4	-
102	3	AE1	AE4	√	-
103	3	AE2	AF3	6	VREF
104	3	AF4	AF1	4	-
105	3	AG3	AF2	4	-
106	3	AG4	AG1	6	-
107	3	AH3	AG2	√	D5
108	3	AH1	AJ2	√	VREF
109	3	AH2	AJ3	4	-
110	3	AJ1	AJ4	√	-
111	3	AK1	AK3	√	VREF
112	3	AK2	AK4	4	-
113	3	AL1	AL2	7	VREF
114	3	AM1	AL3	√	-
115	3	AM2	AL4	√	VREF
116	3	AM3	AN1	6	-
117	3	AM4	AP1	4	-
118	3	AN2	AP2	√	-
119	3	AN3	AR1	6	VREF

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
7	IO_L275N_Y	G38
7	IO_VREF_L275P_Y	G42
7	IO_L276N_Y	G41
7	IO_L276P_Y	F40
7	IO_L277N	F42
7	IO_L277P	F41
7	IO_L278N_Y	F39
7	IO_VREF_L278P_Y	E42
7	IO_L279N_Y	E40
7	IO_L279P_Y	E41
7	IO_L280N_Y	E39
7	IO_L280P_Y	D41
2	CCLK	B4
3	DONE	AW2
NA	DXN	BA38
NA	DXP	AW38
NA	M0	AW41
NA	M1	AV37
NA	M2	BA39
NA	PROGRAM	AV2
NA	TCK	B38
NA	TDI	B5
2	TDO	D5
NA	TMS	B39
NA	VCCINT	F9
NA	VCCINT	F10
NA	VCCINT	F17
NA	VCCINT	F18
NA	VCCINT	F25
NA	VCCINT	F26
NA	VCCINT	F33
NA	VCCINT	F34
NA	VCCINT	J6
NA	VCCINT	J37
NA	VCCINT	K6

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
NA	VCCINT	K37
NA	VCCINT	T6
NA	VCCINT	T37
NA	VCCINT	U6
NA	VCCINT	U37
NA	VCCINT	V6
NA	VCCINT	V37
NA	VCCINT	AE6
NA	VCCINT	AE37
NA	VCCINT	AF6
NA	VCCINT	AF37
NA	VCCINT	AG6
NA	VCCINT	AG37
NA	VCCINT	AN6
NA	VCCINT	AN37
NA	VCCINT	AP6
NA	VCCINT	AP37
NA	VCCINT	AU9
NA	VCCINT	AU10
NA	VCCINT	AU17
NA	VCCINT	AU18
NA	VCCINT	AU25
NA	VCCINT	AU26
NA	VCCINT	AU33
NA	VCCINT	AU34
NA	VCCO_0	F23
NA	VCCO_0	F24
NA	VCCO_0	F28
NA	VCCO_0	F29
NA	VCCO_0	F31
NA	VCCO_0	F32
NA	VCCO_0	F35
NA	VCCO_0	F36
NA	VCCO_1	F11
NA	VCCO_1	F12
NA	VCCO_1	F14

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
2	IO	D29[5]
2	IO	G26[4]
2	IO	H24[4]
2	IO	H25[4]
2	IO	H28[5]
2	IO	J25[4]
2	IO	J27[5]
2	IO	K30[4]
2	IO	M24[4]
2	IO	M25[4]
2	IO	N20
2	IO	N23[4]
2	IO	P26[5]
2	IO	P27[5]
2	IO	P30[4]
2	IO	R30
2	IO_DOUT_BUSY_L70P_YY	J22
2	IO_DIN_D0_L70N_YY	E27
2	IO_L71P	C29[4]
2	IO_L71N	D28[3]
2	IO_L72P_Y	G25
2	IO_L72N_Y	E25
2	IO_VREF_L73P_YY	E28[1]
2	IO_L73N_YY	C30
2	IO_L74P_Y	K22[4]
2	IO_L74N_Y	F27[3]
2	IO_L75P_YY	D30
2	IO_L75N_YY	J23
2	IO_VREF_L76P_Y	L21
2	IO_L76N_Y	F28
2	IO_L77P_YY	G28
2	IO_L77N_YY	E30
2	IO_L78P_YY	G27
2	IO_L78N_YY	E29
2	IO_L79P	K23
2	IO_L79N	H26
2	IO_VREF_L80P_YY	F30
2	IO_L80N_YY	L22
2	IO_L81P_YY	H27
2	IO_L81N_YY	G29
2	IO_L82P	G30
2	IO_L82N	M21
2	IO_L83P_YY	J24
2	IO_L83N_YY	J26
2	IO_VREF_L84P_YY	H30
2	IO_L84N_YY	L23
2	IO_L85P_YY	K26[4]
2	IO_L85N_YY	J28[3]
2	IO_L86P_YY	J29
2	IO_L86N_YY	K24
2	IO_L87P_YY	K27[4]
2	IO_VREF_L87N_YY	J30
2	IO_D1_L88P	M22
2	IO_D2_L88N	K29
2	IO_L89P_YY	K28[3]
2	IO_L89N_YY	L25[4]
2	IO_L90P	N21
2	IO_L90N	K25
2	IO_L91P_YY	L24
2	IO_L91N_YY	L27
2	IO_L92P_Y	L29[4]
2	IO_L92N_Y	M23[4]
2	IO_L93P_YY	L26
2	IO_L93N_YY	L28
2	IO_VREF_L94P	L30[1]
2	IO_L94N	M27
2	IO_L95P_YY	M26
2	IO_L95N_YY	M29
2	IO_L96P_YY	N29
2	IO_L96N_YY	M30
2	IO_L97P	N25
2	IO_L97N	N27
2	IO_VREF_L98P_YY	N30
2	IO_D3_L98N_YY	P21

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
3	IO_L127P_YY	Y24
3	IO_VREF_L127N_YY	AB28
3	IO_L128P_YY	AC30
3	IO_L128N_YY	AA25
3	IO_L129P	W21
3	IO_L129N	AA24
3	IO_L130P_YY	AB26
3	IO_L130N_YY	AD30
3	IO_L131P_YY	Y22
3	IO_VREF_L131N_YY	AC27
3	IO_L132P	AD28
3	IO_L132N	AB25
3	IO_L133P_YY	AC26
3	IO_L133N_YY	AE30
3	IO_L134P_YY	AD27
3	IO_L134N_YY	AF30
3	IO_L135P	AF29
3	IO_VREF_L135N	AB24
3	IO_L136P_YY	AB23
3	IO_L136N_YY	AE28
3	IO_L137P_Y	AG30[3]
3	IO_L137N_Y	AC25[4]
3	IO_L138P_YY	AE26
3	IO_VREF_L138N_YY	AG29[1]
3	IO_L139P	AH30
3	IO_L139N	AC24
3	IO_L140P	AF28[3]
3	IO_L140N	AD25[4]
3	IO_D7_L141P_YY	AH29
3	IO_INIT_L141N_YY	AA22
4	GCK0	AJ16
4	IO	AB19[4]
4	IO	AC16[4]
4	IO	AC19
4	IO	AD18[4]
4	IO	AD21[4]
4	IO	AE15[4]
4	IO	AE18[4]
4	IO	AE21
4	IO	AE24[5]
4	IO	AF17[5]
4	IO	AF18[5]
4	IO	AJ18[4]
4	IO	AK18
4	IO	AK25[5]
4	IO	AK27[4]
4	IO	AH23[4]
4	IO	AH24[5]
4	IO_L142P_YY	AF27
4	IO_L142N_YY	AK28
4	IO_L143P_YY	AG26[4]
4	IO_L143N_YY	AH27[3]
4	IO_L144P	AD23
4	IO_L144N	AJ27
4	IO_VREF_L145P	AB21[1]
4	IO_L145N	AF25
4	IO_L146P	AC22[4]
4	IO_L146N	AH26[4]
4	IO_L147P_YY	AA21
4	IO_L147N_YY	AG25
4	IO_VREF_L148P_YY	AJ26
4	IO_L148N_YY	AD22
4	IO_L149P	AA20
4	IO_L149N	AH25
4	IO_L150P	AC21
4	IO_L150N	AF24
4	IO_L151P_YY	AG24
4	IO_L151N_YY	AK26
4	IO_VREF_L152P_YY	AJ24
4	IO_L152N_YY	AF23
4	IO_L153P	AE23
4	IO_L153N	AB20
4	IO_L154P	AC20

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
7	IO	E3
7	IO	F1[4]
7	IO	G1[5]
7	IO	G4[5]
7	IO	H3[5]
7	IO	J1[4]
7	IO	J3[4]
7	IO	J4[4]
7	IO	J6[4]
7	IO	L10[4]
7	IO	N2[4]
7	IO	N8[4]
7	IO	N10[4]
7	IO	P3[5]
7	IO	P9[4]
7	IO	R1[5]
7	IO	T3[4]
7	IO_L247P	R10
7	IO_L248N_YY	R5[3]
7	IO_L248P_YY	R6[4]
7	IO_L249N_YY	R8
7	IO_VREF_L249P_YY	R4[2]
7	IO_L250N_YY	R7
7	IO_L250P_YY	R3
7	IO_L251N_YY	P10
7	IO_VREF_L251P_YY	P6
7	IO_L252N_YY	P5
7	IO_L252P_YY	P2
7	IO_L253N	P7
7	IO_L253P	P4
7	IO_L254N_YY	N4
7	IO_L254P_YY	R2
7	IO_L255N_YY	N7
7	IO_VREF_L255P_YY	P1
7	IO_L256N	M6
7	IO_L256P	N6
7	IO_L257N_YY	N5
7	IO_L257P_YY	N1
7	IO_L258N_YY	M4
7	IO_L258P_YY	M5
7	IO_L259N	M2
7	IO_VREF_L259P	M1[1]
7	IO_L260N_YY	L4
7	IO_L260P_YY	L2
7	IO_L261N_Y	M7[4]
7	IO_L261P_Y	L5[4]
7	IO_L262N_YY	L1
7	IO_L262P_YY	M8
7	IO_L263N	K2
7	IO_L263P	M9
7	IO_L264N	L3[4]
7	IO_L264P	M10[4]
7	IO_L265N_YY	K5
7	IO_L265P_YY	K1
7	IO_L266N_YY	L6
7	IO_VREF_L266P_YY	K3
7	IO_L267N_YY	L7
7	IO_L267P_YY	K4
7	IO_L268N_YY	L8
7	IO_L268P_YY	J5
7	IO_L269N_YY	K6
7	IO_VREF_L269P_YY	H4
7	IO_L270N_YY	H1
7	IO_L270P_YY	K7
7	IO_L271N	J7
7	IO_L271P	J2
7	IO_L272N_YY	H5
7	IO_L272P_YY	G2
7	IO_L273N_YY	L9
7	IO_VREF_L273P_YY	G5
7	IO_L274N	F3
7	IO_L274P	K8