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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

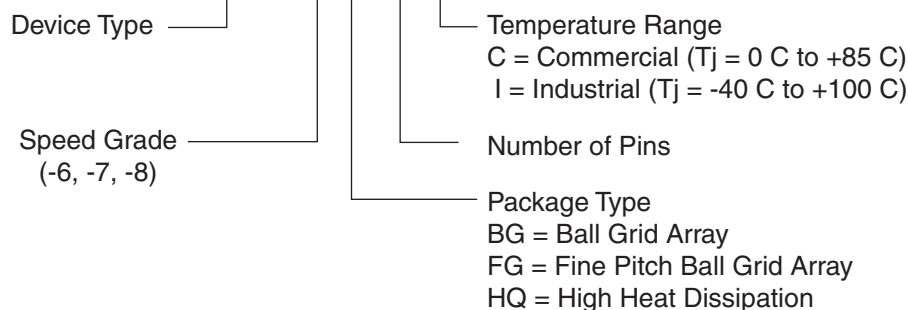
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	7776
Number of Logic Elements/Cells	34992
Total RAM Bits	589824
Number of I/O	660
Number of Gates	2188742
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	860-BGA Exposed Pad
Supplier Device Package	860-FBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv1600e-7fg860c

Virtex-E Ordering Information

Example: XCV300E-6PQ240C



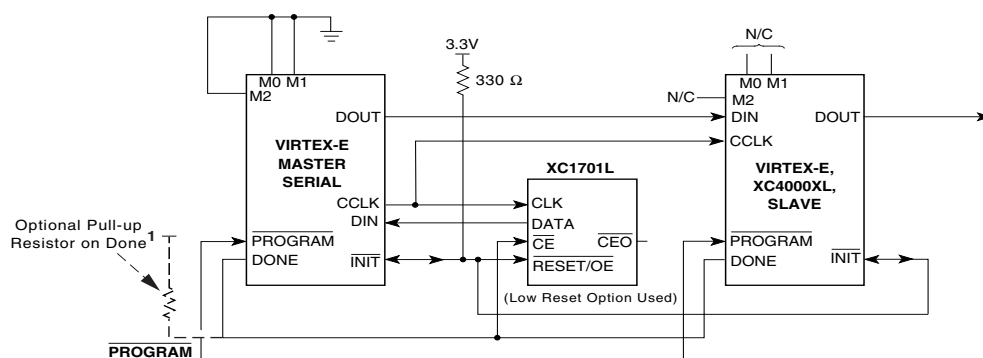
DS022_043_072000

Figure 1: Ordering Information

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/7/99	1.0	Initial Xilinx release.
1/10/00	1.1	Re-released with spd.txt v. 1.18, FG860/900/1156 package information, and additional DLL, Select RAM and SelectI/O information.
1/28/00	1.2	Added Delay Measurement Methodology table, updated SelectI/O section, Figures 30, 54, & 55, text explaining Table 5, T _{BYP} values, buffered Hex Line info, p. 8, I/O Timing Measurement notes, notes for Tables 15, 16, and corrected F1156 pinout table footnote references.
2/29/00	1.3	Updated pinout tables, V _{CC} page 20, and corrected Figure 20.
5/23/00	1.4	Correction to table on p. 22.
7/10/00	1.5	- Numerous minor edits. - Data sheet upgraded to Preliminary. - Preview -8 numbers added to Virtex-E Electrical Characteristics tables.
8/1/00	1.6	- Reformatted entire document to follow new style guidelines. - Changed speed grade values in tables on pages 35-37.
9/20/00	1.7	- Min values added to Virtex-E Electrical Characteristics tables. - XCV2600E and XCV3200E numbers added to Virtex-E Electrical Characteristics tables (Module 3). - Corrected user I/O count for XCV100E device in Table 1 (Module 1). - Changed several pins to "No Connect in the XCV100E" and removed duplicate V_{CCINT} pins in Table ~ (Module 4). - Changed pin J10 to "No connect in XCV600E" in Table 74 (Module 4). - Changed pin J30 to "VREF option only in the XCV600E" in Table 74 (Module 4). - Corrected pair 18 in Table 75 (Module 4) to be "AO in the XCV1000E, XCV1600E".



Note 1: If none of the Virtex FPGAs have been selected to drive DONE, an external pull-up resistor of 330 Ω should be added to the common DONE line. (For Spartan-XL devices, add a 4.7K Ω pull-up resistor.) This pull-up is not needed if the DriveDONE attribute is set. If used, DriveDONE should be selected only for the last device in the configuration chain.

XCVE ds_013_050103

Figure 13: Master/Slave Serial Mode Circuit Diagram

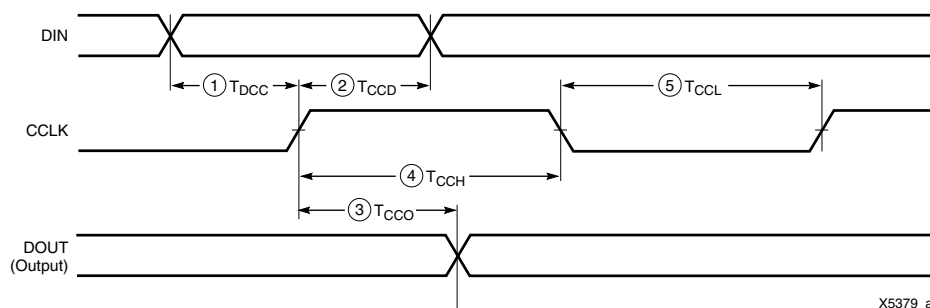


Figure 14: Slave-Serial Mode Programming Switching Characteristics

Master-Serial Mode

In master-serial mode, the CCLK output of the FPGA drives a Xilinx Serial PROM that feeds bit-serial data to the DIN input. The FPGA accepts this data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge. The maximum capacity for a single LOUT/DOUT write is $2^{20}-1$ (1,048,575) 32-bit words, or 33,554,400 bits.

The interface is identical to slave-serial except that an internal oscillator is used to generate the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK, which always starts at a slow default frequency. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration. Switching to a lower frequency is prohibited.

The CCLK frequency is set using the ConfigRate option in the bitstream generation software. The maximum CCLK fre-

quency that can be selected is 60 MHz. When selecting a CCLK frequency, ensure that the serial PROM and any daisy-chained FPGAs are fast enough to support the clock rate.

On power-up, the CCLK frequency is approximately 2.5 MHz. This frequency is used until the ConfigRate bits have been loaded when the frequency changes to the selected ConfigRate. Unless a different frequency is specified in the design, the default ConfigRate is 4 MHz.

In a full master/slave system (Figure 13), the left-most device operates in master-serial mode. The remaining devices operate in slave-serial mode. The SPROM $\overline{\text{RESET}}$ pin is driven by $\overline{\text{INIT}}$, and the $\overline{\text{CE}}$ input is driven by DONE. There is the potential for contention on the DONE pin, depending on the start-up sequence options chosen.

The sequence of operations necessary to configure a Virtex-E FPGA serially appears in **Figure 15**.

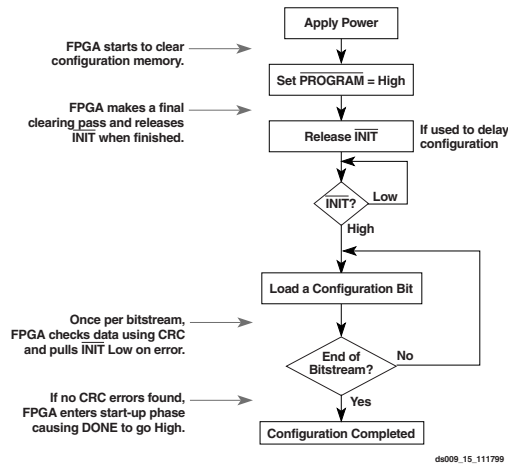


Figure 15: Serial Configuration Flowchart

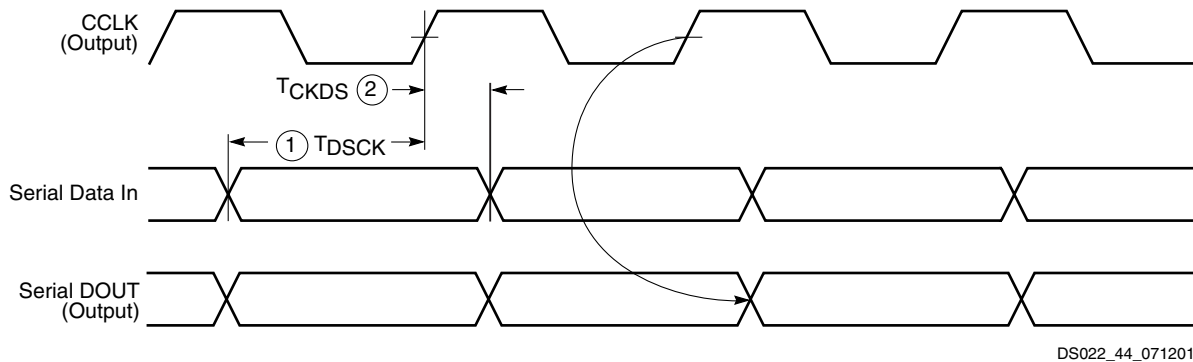


Figure 16: Master-Serial Mode Programming Switching Characteristics

At power-up, V_{CC} must rise from 1.0 V to V_{CC} Min in less than 50 ms, otherwise delay configuration by pulling $\overline{PROGRAM}$ Low until V_{CC} is valid.

SelectMAP Mode

The SelectMAP mode is the fastest configuration option. Byte-wide data is written into the FPGA with a $BUSY$ flag controlling the flow of data.

An external data source provides a byte stream, CCLK, a Chip Select ($\overline{CS}$) signal and a Write signal ($\overline{WRITE}$). If $BUSY$ is asserted (High) by the FPGA, the data must be held until $BUSY$ goes Low.

Data can also be read using the SelectMAP mode. If $\overline{WRITE}$ is not asserted, configuration data is read out of the FPGA as part of a readback operation.

After configuration, the pins of the SelectMAP port can be used as additional user I/O. Alternatively, the port can be retained to permit high-speed 8-bit readback.

Retention of the SelectMAP port is selectable on a design-by-design basis when the bitstream is generated. If retention is selected, PROHIBIT constraints are required to prevent the SelectMAP-port pins from being used as user I/O.

Figure 16 shows the timing of master-serial configuration. Master-serial mode is selected by a <000> or <100> on the mode pins (M2, M1, M0). Table 10 shows the timing information for Figure 16.

Multiple Virtex-E FPGAs can be configured using the SelectMAP mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, $\overline{WRITE}$, and $BUSY$ pins of all the devices in parallel. The individual devices are loaded separately by asserting the $\overline{CS}$ pin of each device in turn and writing the appropriate data. See Table 11 for SelectMAP Write Timing Characteristics.

Write

Write operations send packets of configuration data into the FPGA. The sequence of operations for a multi-cycle write operation is shown below. Note that a configuration packet can be split into many such sequences. The packet does not have to complete within one assertion of $\overline{CS}$, illustrated in Figure 17.

1. Assert $\overline{WRITE}$ and $\overline{CS}$ Low. Note that when $\overline{CS}$ is asserted on successive CCLKs, $\overline{WRITE}$ must remain either asserted or de-asserted. Otherwise, an abort is initiated, as described below.
2. Drive data onto D[7:0]. Note that to avoid contention, the data source should not be enabled while $\overline{CS}$ is Low and $\overline{WRITE}$ is High. Similarly, while $\overline{WRITE}$ is High, no more than one $\overline{CS}$ should be asserted.

DLL Properties

Properties provide access to some of the Virtex-E series DLL features, (for example, clock division and duty cycle correction).

Duty Cycle Correction Property

The 1x clock outputs, CLK0, CLK90, CLK180, and CLK270, use the duty-cycle corrected default, exhibiting a 50/50 duty cycle. The `DUTY_CYCLE_CORRECTION` property (by default TRUE) controls this feature. To deactivate the DLL duty-cycle correction for the 1x clock outputs, attach the `DUTY_CYCLE_CORRECTION=FALSE` property to the DLL symbol.

Clock Divide Property

The `CLKDV_DIVIDE` property specifies how the signal on the CLKDV pin is frequency divided with respect to the CLK0 pin. The values allowed for this property are 1.5, 2, 2.5, 3, 4, 5, 8, or 16; the default value is 2.

Startup Delay Property

This property, `STARTUP_WAIT`, takes on a value of TRUE or FALSE (the default value). When TRUE the device configuration DONE signal waits until the DLL locks before going to High.

Virtex-E DLL Location Constraints

As shown in [Figure 26](#), there are four additional DLLs in the Virtex-E devices, for a total of eight per Virtex-E device. These DLLs are located in silicon, at the top and bottom of the two innermost block SelectRAM columns. The location constraint LOC, attached to the DLL symbol with the identifier DLL0S, DLL0P, DLL1S, DLL1P, DLL2S, DLL2P, DLL3S, or DLL3P, controls the DLL location.

The LOC property uses the following form:

LOC = DLL0P

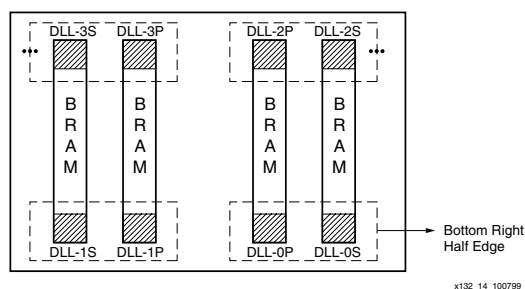


Figure 26: Virtex Series DLLs

Design Factors

Use the following design considerations to avoid pitfalls and improve success designing with Xilinx devices.

Input Clock

The output clock signal of a DLL, essentially a delayed version of the input clock signal, reflects any instability on the input clock in the output waveform. For this reason the quality of the DLL input clock relates directly to the quality of the output clock waveforms generated by the DLL. The DLL input clock requirements are specified in the data sheet.

In most systems a crystal oscillator generates the system clock. The DLL can be used with any commercially available quartz crystal oscillator. For example, most crystal oscillators produce an output waveform with a frequency tolerance of 100 PPM, meaning 0.01 percent change in the clock period. The DLL operates reliably on an input waveform with a frequency drift of up to 1 ns — orders of magnitude in excess of that needed to support any crystal oscillator in the industry. However, the cycle-to-cycle jitter must be kept to less than 300 ps in the low frequencies and 150 ps for the high frequencies.

Input Clock Changes

Changing the period of the input clock beyond the maximum drift amount requires a manual reset of the CLKDLL. Failure to reset the DLL produces an unreliable lock signal and output clock.

It is possible to stop the input clock with little impact to the DLL. Stopping the clock should be limited to less than 100 μ s to keep device cooling to a minimum. The clock should be stopped during a Low phase, and when restored the full High period should be seen. During this time, LOCKED stays High and remains High when the clock is restored.

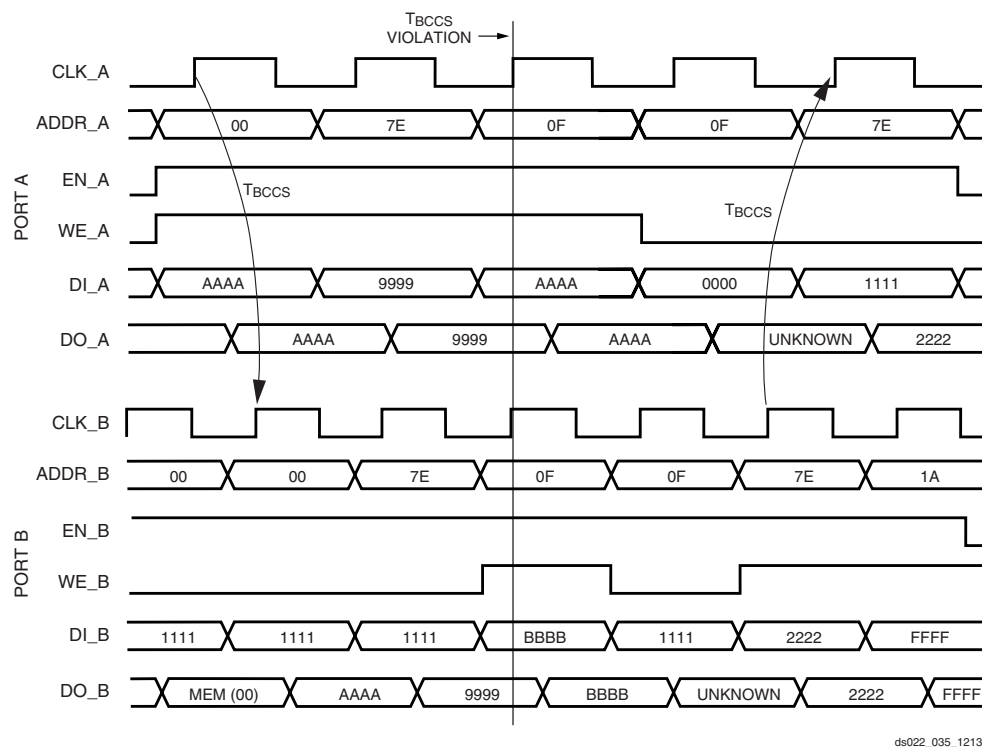
When the clock is stopped, one to four more clocks are still observed as the delay line is flushed. When the clock is restarted, the output clocks are not observed for one to four clocks as the delay line is filled. The most common case is two or three clocks.

In a similar manner, a phase shift of the input clock is also possible. The phase shift propagates to the output one to four clocks after the original shift, with no disruption to the CLKDLL control.

Output Clocks

As mentioned earlier in the DLL pin descriptions, some restrictions apply regarding the connectivity of the output pins. The DLL clock outputs can drive an OBUF, a global clock buffer BUFG, or they can route directly to destination clock pins. The only BUFGs that the DLL clock outputs can drive are the two on the same edge of the device (top or bottom). In addition, the CLK2X output of the secondary DLL can connect directly to the CLKIN of the primary DLL in the same quadrant.

Do not use the DLL output clock signals until after activation of the LOCKED signal. Prior to the activation of the LOCKED signal, the DLL output clocks are not valid and can exhibit glitches, spikes, or other spurious movement.



ds022_035_121399

Figure 34: Timing Diagram for a True Dual-port Read/Write Block SelectRAM+ Memory

At the third rising edge of CLKA, the T_{BCCS} parameter is violated with two writes to memory location 0x0F. The DOA and DOB buses reflect the contents of the DIA and DIB buses, but the stored value at 0x0F is invalid.

At the fourth rising edge of CLKA, a read operation is performed at memory location 0x0F and invalid data is present on the DOA bus. Port B also executes a read operation to memory location 0x0F and also reads invalid data.

At the fifth rising edge of CLKA a read operation is performed that does not violate the T_{BCCS} parameter to the previous write of 0x7E by Port B. The DOA bus reflects the recently written value by Port B.

Initialization

The block SelectRAM+ memory can initialize during the device configuration sequence. The 16 initialization properties of 64 hex values each (a total of 4096 bits) set the initialization of each RAM. These properties appear in Table 17. Any initialization properties not explicitly set configure as zeros. Partial initialization strings pad with zeros. Initialization strings greater than 64 hex values generate an error. The RAMs can be simulated with the initialization values using generics in VHDL simulators and parameters in Verilog simulators.

Initialization in VHDL and Synopsys

The block SelectRAM+ structures can be initialized in VHDL for both simulation and synthesis for inclusion in the EDIF output file. The simulation of the VHDL code uses a generic to pass the initialization. Synopsys FPGA compiler does not

presently support generics. The initialization values instead attach as attributes to the RAM by a built-in Synopsys `dc_script`. The `translate_off` statement stops synthesis translation of the generic statements. The following code illustrates a module that employs these techniques.

Table 17: RAM Initialization Properties

Property	Memory Cells
INIT_00	255 to 0
INIT_01	511 to 256
INIT_02	767 to 512
INIT_03	1023 to 768
INIT_04	1279 to 1024
INIT_05	1535 to 1280
INIT_06	1791 to 1536
INIT_07	2047 to 1792
INIT_08	2303 to 2048
INIT_09	2559 to 2304
INIT_0a	2815 to 2560
INIT_0b	3071 to 2816
INIT_0c	3327 to 3072
INIT_0d	3583 to 3328
INIT_0e	3839 to 3584
INIT_0f	4095 to 3840

standard requires a Differential Amplifier input buffer and a Push-Pull output buffer.

SSTL3 — Stub Series Terminated Logic for 3.3V

The Stub Series Terminated Logic for 3.3V, or SSTL3 standard is a general purpose 3.3V memory bus standard also sponsored by Hitachi and IBM (JESD8-8). This standard has two classes, I and II. SelectI/O devices support both classes for the SSTL3 standard. This standard requires a Differential Amplifier input buffer and an Push-Pull output buffer.

SSTL2 — Stub Series Terminated Logic for 2.5V

The Stub Series Terminated Logic for 2.5V, or SSTL2 standard is a general purpose 2.5V memory bus standard sponsored by Hitachi and IBM (JESD8-9). This standard has two classes, I and II. SelectI/O devices support both classes for the SSTL2 standard. This standard requires a Differential Amplifier input buffer and an Push-Pull output buffer.

CTT — Center Tap Terminated

The Center Tap Terminated, or CTT standard is a 3.3V memory bus standard sponsored by Fujitsu (JESD8-4). This standard requires a Differential Amplifier input buffer and a Push-Pull output buffer.

AGP-2X — Advanced Graphics Port

The Intel AGP standard is a 3.3V Advanced Graphics Port-2X bus standard used with the Pentium II processor for graphics applications. This standard requires a Push-Pull output buffer and a Differential Amplifier input buffer.

LVDS — Low Voltage Differential Signal

LVDS is a differential I/O standard. It requires that one data bit is carried through two signal lines. As with all differential signaling standards, LVDS has an inherent noise immunity over single-ended I/O standards. The voltage swing between two signal lines is approximately 350mV. The use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}) is not required. LVDS requires the use of two pins per input or output. LVDS requires external resistor termination.

BLVDS — Bus LVDS

This standard allows for bidirectional LVDS communication between two or more devices. The external resistor termination is different than the one for standard LVDS.

LVPECL — Low Voltage Positive Emitter Coupled Logic

LVPECL is another differential I/O standard. It requires two signal lines for transmitting one data bit. This standard specifies two pins per input or output. The voltage swing between these two signal lines is approximately 850 mV. The use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}) is not required. The LVPECL standard requires external resistor termination.

Library Symbols

The Xilinx library includes an extensive list of symbols designed to provide support for the variety of SelectI/O features. Most of these symbols represent variations of the five generic SelectI/O symbols.

- IBUF (input buffer)
- IBUFG (global clock input buffer)
- OBUF (output buffer)
- OBUFT (3-state output buffer)
- IOBUF (input/output buffer)

IBUF

Signals used as inputs to the Virtex-E device must source an input buffer (IBUF) via an external input port. The generic Virtex-E IBUF symbol appears in Figure 37. The extension

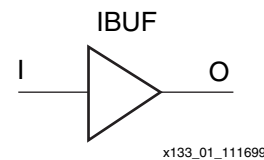


Figure 37: Input Buffer (IBUF) Symbols

to the base name defines which I/O standard the IBUF uses. The assumed standard is LVTTTL when the generic IBUF has no specified extension.

The following list details the variations of the IBUF symbol:

- IBUF
- IBUF_LVCMOS2
- IBUF_PCI33_3
- IBUF_PCI66_3
- IBUF_GTL
- IBUF_GTLP
- IBUF_HSTL_I
- IBUF_HSTL_III
- IBUF_HSTL_IV
- IBUF_SSTL3_I
- IBUF_SSTL3_II
- IBUF_SSTL2_I
- IBUF_SSTL2_II
- IBUF_CTT
- IBUF_AGP
- IBUF_LVCMOS18
- IBUF_LVDS
- IBUF_LVPECL

When the IBUF symbol supports an I/O standard that requires a V_{REF} , the IBUF automatically configures as a differential amplifier input buffer. The V_{REF} voltage must be supplied on the V_{REF} pins. In the case of LVDS, LVPECL, and BLVDS, V_{REF} is not required.

The voltage reference signal is “banked” within the Virtex-E device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 38 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

IBUF placement restrictions require that any differential amplifier input signals within a bank be of the same standard. How to specify a specific location for the IBUF via the LOC property is described below. Table 19 summarizes the Virtex-E input standards compatibility requirements.

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element by default activates to ensure a zero hold-time requirement. The NODELAY=TRUE property overrides this default.

When the IBUF does not drive a flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

Table 19: Xilinx Input Standards Compatibility Requirements

Rule 1	Standards with the same input V_{CCO} , output V_{CCO} , and V_{REF} can be placed within the same bank.
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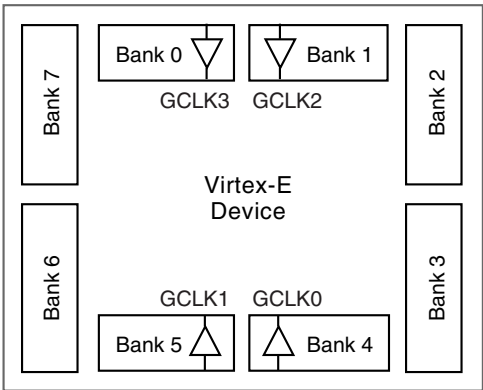


Figure 38: Virtex-E I/O Banks

IBUFG

Signals used as high fanout clock inputs to the Virtex-E device should drive a global clock input buffer (IBUFG) via an external input port in order to take advantage of one of the four dedicated global clock distribution networks. The output of the IBUFG should only drive a CLKDLL,

CLKDLLHF, or BUFG symbol. The generic Virtex-E IBUFG symbol appears in Figure 39.

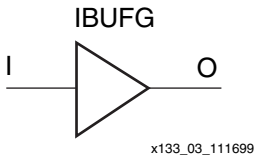


Figure 39: Virtex-E Global Clock Input Buffer (IBUFG) Symbol

The extension to the base name determines which I/O standard is used by the IBUFG. With no extension specified for the generic IBUFG symbol, the assumed standard is LVTTTL.

The following list details variations of the IBUFG symbol.

- IBUFG
- IBUFG_LVCMOS2
- IBUFG_PCI33_3
- IBUFG_PCI66_3
- IBUFG_GTL
- IBUFG_GTLP
- IBUFG_HSTL_I
- IBUFG_HSTL_III
- IBUFG_HSTL_IV
- IBUFG_SSTL3_I
- IBUFG_SSTL3_II
- IBUFG_SSTL2_I
- IBUFG_SSTL2_II
- IBUFG_CTT
- IBUFG_AGP
- IBUFG_LVCMOS18
- IBUFG_LVDS
- IBUFG_LVPECL

When the IBUFG symbol supports an I/O standard that requires a differential amplifier input, the IBUFG automatically configures as a differential amplifier input buffer. The low-voltage I/O standards with a differential amplifier input require an external reference voltage input V_{REF} .

The voltage reference signal is “banked” within the Virtex-E device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 38 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

IBUFG placement restrictions require any differential amplifier input signals within a bank be of the same standard. The LOC property can specify a location for the IBUFG.

As an added convenience, the BUFGP can be used to instantiate a high fanout clock input. The BUFGP symbol

SSTL3_I

A sample circuit illustrating a valid termination technique for SSTL3_I appears in Figure 49. DC voltage specifications appear in Table 28.

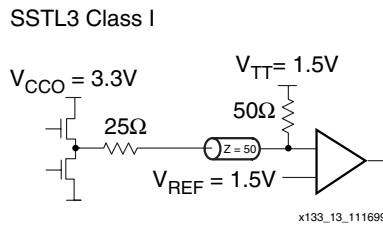


Figure 49: Terminated SSTL3 Class I

Table 28: SSTL3_I Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} = V_{REF} + 0.2$	1.5	1.7	3.9 ⁽¹⁾
$V_{IL} = V_{REF} - 0.2$	-0.3 ⁽²⁾	1.3	1.5
$V_{OH} = V_{REF} + 0.6$	1.9	-	-
$V_{OL} = V_{REF} - 0.6$	-	-	1.1
I_{OH} at V_{OH} (mA)	-8	-	-
I_{OL} at V_{OL} (mA)	8	-	-

Notes:

1. V_{IH} maximum is $V_{CCO} + 0.3$
2. V_{IL} minimum does not conform to the formula

SSTL3_II

A sample circuit illustrating a valid termination technique for SSTL3_II appears in Figure 50. DC voltage specifications appear in Table 29.

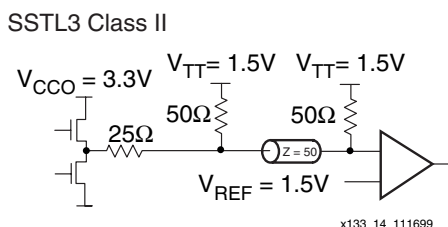


Figure 50: Terminated SSTL3 Class II

Table 29: SSTL3_II Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} = V_{REF} + 0.2$	1.5	1.7	3.9 ⁽¹⁾
$V_{IL} = V_{REF} - 0.2$	-0.3 ⁽²⁾	1.3	1.5
$V_{OH} = V_{REF} + 0.8$	2.1	-	-
$V_{OL} = V_{REF} - 0.8$	-	-	0.9
I_{OH} at V_{OH} (mA)	-16	-	-
I_{OL} at V_{OL} (mA)	16	-	-

Notes:

1. V_{IH} maximum is $V_{CCO} + 0.3$
2. V_{IL} minimum does not conform to the formula

SSTL2_I

A sample circuit illustrating a valid termination technique for SSTL2_I appears in Figure 51. DC voltage specifications appear in Table 30.

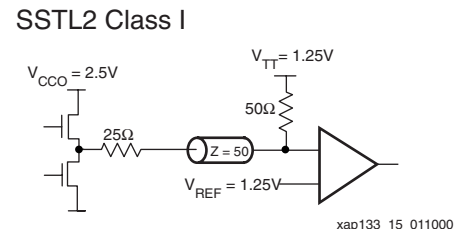


Figure 51: Terminated SSTL2 Class I

Table 30: SSTL2_I Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
$V_{REF} = 0.5 \times V_{CCO}$	1.15	1.25	1.35
$V_{TT} = V_{REF} + N^{(1)}$	1.11	1.25	1.39
$V_{IH} = V_{REF} + 0.18$	1.33	1.43	3.0 ⁽²⁾
$V_{IL} = V_{REF} - 0.18$	-0.3 ⁽³⁾	1.07	1.17
$V_{OH} = V_{REF} + 0.61$	1.76	-	-
$V_{OL} = V_{REF} - 0.61$	-	-	0.74
I_{OH} at V_{OH} (mA)	-7.6	-	-
I_{OL} at V_{OL} (mA)	7.6	-	-

Notes:

1. N must be greater than or equal to -0.04 and less than or equal to 0.04.
2. V_{IH} maximum is $V_{CCO} + 0.3$.
3. V_{IL} minimum does not conform to the formula.

Table 4: CS144 — XCV50E, XCV100E, XCV200E

Bank	Pin Description	Pin #
4	IO_L15N_YY	M11
4	IO_L15P_YY	L11
4	IO_L16N_YY	K9
4	IO_VREF_L16P_YY	N10 ²
4	IO_L17N_YY	K8
4	IO_L17P_YY	N9
4	IO_LVDS_DLL_L18P	N8
4	IO_VREF	L8
4	IO_VREF	L10
4	IO_VREF	N11 ¹
5	GCK1	M7
5	IO	M4
5	IO_LVDS_DLL_L18N	M6
5	IO_L19N_YY	N5
5	IO_L19P_YY	K6
5	IO_VREF_L20N_YY	N4 ²
5	IO_L20P_YY	K5
5	IO_L21N_YY	M3
5	IO_L21P_YY	N3
5	IO_VREF	K4 ¹
5	IO_VREF	L4
5	IO_VREF	L6
6	IO	G4
6	IO	J4
6	IO_L25P	H1
6	IO_VREF_L25N	H2
6	IO_L24P_YY	H3
6	IO_L24N_YY	H4
6	IO_L23P	J2
6	IO_VREF_L23N	J3 ²
6	IO_VREF	K1
6	IO_VREF	K2 ¹
6	IO_L22N_YY	L1
6	IO_L22P_YY	K3

Table 4: CS144 — XCV50E, XCV100E, XCV200E

Bank	Pin Description	Pin #
6	IO_L26N	G1
7	IO	C2
7	IO	D3
7	IO	F3
7	IO_L26P	F2
7	IO_L27N	F4
7	IO_VREF_L27P	E1
7	IO_L28N_YY	E2
7	IO_L28P_YY	E3
7	IO_L29N	D1
7	IO_VREF_L29P	D2 ²
7	IO_VREF	C1 ¹
7	IO_VREF	D4
2	CCLK	B13
3	DONE	M12
NA	M0	M1
NA	M1	L2
NA	M2	N2
NA	PROGRAM	L12
NA	TDI	A11
NA	TCK	C3
2	TDO	A12
NA	TMS	B1
NA	VCCINT	A9
NA	VCCINT	B6
NA	VCCINT	C5
NA	VCCINT	G3
NA	VCCINT	G12
NA	VCCINT	M5
NA	VCCINT	M9
NA	VCCINT	N6
0	VCCO	A2

BG352 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A check (✓) in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock

Table 11: BG352 Differential Pin Pair Summary
XCV100E, XCV200E, XCV300E

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	AE13	AC13	NA	IO LVDS 55
1	5	AF14	AD14	NA	IO LVDS 55
2	1	B14	A13	NA	IO LVDS 9
3	0	D14	A15	NA	IO LVDS 9
IO LVDS					
Total Outputs: 87, Asynchronous Output Pairs: 43					
0	0	B23	D21	✓	VREF_0
1	0	D20	A23	✓	-
2	0	B22	C21	✓	VREF_0
3	0	A21	B20	2	-
4	0	B19	C19	✓	VREF_0
5	0	C18	D17	✓	-
6	0	A18	C17	2	-
7	0	C16	B17	✓	-
8	0	D15	A16	✓	VREF_0
9	1	A13	A15	✓	GCLK LVDS 3/2
10	1	A12	C13	2	-
11	1	C12	B12	✓	VREF_1
12	1	B11	A11	✓	-
13	1	D11	C11	2	-
14	1	C10	B9	✓	-
15	1	C9	B8	✓	VREF_1
16	1	A7	D9	1	-
17	1	B6	A6	✓	VREF_1
18	1	A4	C7	✓	-

Table 11: BG352 Differential Pin Pair Summary
XCV100E, XCV200E, XCV300E

Pair	Bank	P Pin	N Pin	AO	Other Functions
19	1	D6	C6	✓	VREF_1
20	1	C4	D5	✓	CS
21	2	E4	D3	✓	DIN_D0
22	2	D2	C1	✓	VREF_2
23	2	G4	F3	✓	-
24	2	E2	F2	✓	VREF_2
25	2	F1	J4	2	-
26	2	H2	G1	✓	D1
27	2	J3	J2	✓	D2
28	2	J1	L4	1	-
29	2	L3	L2	✓	-
30	2	M4	M3	✓	D3
31	2	M2	M1	2	-
32	2	N4	N2	✓	-
33	3	R1	R2	2	-
34	3	R3	R4	✓	VREF_3
35	3	T2	U2	✓	-
36	3	T4	V1	1	-
37	3	U3	U4	✓	D5
38	3	V3	V4	✓	VREF_3
39	3	Y1	Y2	1	-
40	3	AA2	Y3	✓	VREF_3
41	3	AC1	AB2	✓	-
42	3	AA4	AC2	✓	VREF_3
43	3	AC3	AD2	✓	INIT
44	4	AC5	AD4	✓	-
45	4	AE4	AF3	✓	VREF_4
46	4	AC7	AD6	✓	-
47	4	AE5	AE6	✓	VREF_4
48	4	AF6	AC9	2	-
49	4	AE8	AF7	✓	VREF_4
50	4	AD9	AE9	✓	-
51	4	AF9	AC11	2	-
52	4	AD11	AE11	✓	-
53	4	AC12	AD12	✓	VREF_4
54	4	AE12	AF12	2	-

Table 12: BG432 — XCV300E, XCV400E, XCV600E

Bank	Pin Description	Pin #
6	VCCO	AL31
7	VCCO	A31
7	VCCO	L28
7	VCCO	L31
NA	GND	A2
NA	GND	A3
NA	GND	A7
NA	GND	A9
NA	GND	A14
NA	GND	A18
NA	GND	A23
NA	GND	A25
NA	GND	A29
NA	GND	A30
NA	GND	B1
NA	GND	B2
NA	GND	B30
NA	GND	B31
NA	GND	C1
NA	GND	C31
NA	GND	D16
NA	GND	G1
NA	GND	G31
NA	GND	J1
NA	GND	J31
NA	GND	P1
NA	GND	P31
NA	GND	T4
NA	GND	T28
NA	GND	V1
NA	GND	V31
NA	GND	AC1
NA	GND	AC31
NA	GND	AE1
NA	GND	AE31

Table 12: BG432 — XCV300E, XCV400E, XCV600E

Bank	Pin Description	Pin #
NA	GND	AH16
NA	GND	AJ1
NA	GND	AJ31
NA	GND	AK1
NA	GND	AK2
NA	GND	AK30
NA	GND	AK31
NA	GND	AL2
NA	GND	AL3
NA	GND	AL7
NA	GND	AL9
NA	GND	AL14
NA	GND	AL18
NA	GND	AL23
NA	GND	AL25
NA	GND	AL29
NA	GND	AL30

Notes:

1. V_{REF} or I/O option only in the XCV600E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV400E, XCV600E; otherwise, I/O option only.

BG432 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A ✓ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 13: BG432 Differential Pin Pair Summary
XCV300E, XCV400E, XC600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	AL16	AH15	NA	IO_DLL_L86P
1	5	AK16	AL17	NA	IO_DLL_L86N
2	1	A16	B16	NA	IO_DLL_L16P
3	0	D17	C17	NA	IO_DLL_L16N
IO LVDS					
Total Outputs: 137, Asynchronous Output Pairs: 63					
0	0	D27	B29	1	-
1	0	C27	B28	✓	-
2	0	A28	D26	✓	VREF
3	0	C26	B27	2	-
4	0	A27	D25	✓	-
5	0	C25	D24	✓	VREF
6	0	D23	B25	1	-
7	0	B24	C24	1	VREF
8	0	A24	D22	✓	VREF
9	0	B22	C22	✓	-
10	0	D20	C21	✓	-
11	0	C20	B21	✓	-
12	0	D19	A20	✓	-
13	0	A19	B19	✓	VREF
14	0	D18	B18	1	-
15	0	B17	C18	1	VREF

Table 13: BG432 Differential Pin Pair Summary
XCV300E, XCV400E, XC600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
16	1	B16	C17	NA	IO_LVDS_DLL
17	1	B15	A15	1	VREF
18	1	D15	C15	1	-
19	1	A13	B14	✓	VREF
20	1	D14	B13	✓	-
21	1	B12	C13	✓	-
22	1	C12	D13	✓	-
23	1	C11	D12	✓	-
24	1	C10	B10	✓	VREF
25	1	D10	C9	1	VREF
26	1	B8	A8	1	-
27	1	B7	C8	✓	VREF
28	1	A6	D8	✓	-
29	1	D7	B6	2	-
30	1	C6	A5	✓	VREF
31	1	D6	B5	✓	-
32	1	C5	A4	1	-
33	1	D5	B4	✓	CS, WRITE
34	2	D3	C2	✓	DIN, D0, BUSY
35	2	D2	E4	3	-
36	2	D1	E3	4	-
37	2	E2	F4	1	VREF
38	2	E1	F3	5	-
39	2	F2	G4	1	-
40	2	G3	G2	✓	VREF
41	2	H3	H2	4	-
42	2	H1	J4	1	VREF
43	2	J2	K4	✓	D1
44	2	K2	K1	✓	D2
45	2	L2	M4	4	-
46	2	M3	M2	1	-
47	2	N4	N3	1	-

Table 13: BG432 Differential Pin Pair Summary
XCV300E, XCV400E, XC600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
112	6	AB29	AB28	√	VREF
113	6	AA29	AB31	√	-
114	6	Y29	Y28	4	-
115	6	Y31	Y30	1	-
116	6	W30	W29	1	-
117	6	V29	V28	√	VREF
118	6	U29	V30	4	-
119	6	U30	U28	1	VREF
120	7	R29	T31	√	-
121	7	R31	R30	1	VREF
122	7	P28	P29	4	-
123	7	N30	P30	√	VREF
124	7	N31	N28	1	-
125	7	M28	M29	1	-
126	7	L30	M30	4	-
127	7	K30	K31	√	-
128	7	J30	K28	√	VREF
129	7	J28	J29	1	VREF
130	7	G30	H30	4	-
131	7	F31	H28	√	VREF
132	7	G28	G29	1	-
133	7	E30	E31	5	-
134	7	F28	F29	1	VREF
135	7	D30	D31	4	-
136	7	E28	E29	3	-

Notes:

1. AO in the XCV300E, 600E.
2. AO in the XCV300E.
3. AO in the XCV400E, 600E.
4. AO in the XCV300E, 400E.
5. AO in the XCV600E.

BG560 Ball Grid Array Packages

XCV1000E, XCV1600E, and XCV2000E devices in BG560 Ball Grid Array packages have footprint compatibility. Pins labeled IO_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF} it can be used as general I/O. Immediately following Table 14, see Table 15 for Differential Pair information.

Table 14: BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin#	See Note
0	GCK3	A17	
0	IO	A27	
0	IO	B25	
0	IO	C28	
0	IO	C30	
0	IO	D30	
0	IO_L0N	E28	
0	IO_VREF_L0P	D29	3
0	IO_L1N_YY	D28	
0	IO_L1P_YY	A31	
0	IO_VREF_L2N_YY	E27	
0	IO_L2P_YY	C29	
0	IO_L3N_Y	B30	
0	IO_L3P_Y	D27	
0	IO_L4N_YY	E26	
0	IO_L4P_YY	B29	
0	IO_VREF_L5N_YY	D26	
0	IO_L5P_YY	C27	
0	IO_L6N_Y	E25	
0	IO_VREF_L6P_Y	A28	1
0	IO_L7N_Y	D25	
0	IO_L7P_Y	C26	
0	IO_VREF_L8N_Y	E24	4
0	IO_L8P_Y	B26	
0	IO_L9N_Y	C25	
0	IO_L9P_Y	D24	
0	IO_VREF_L10N_YY	E23	
0	IO_L10P_YY	A25	
0	IO_L11N_YY	D23	

Table 15: BG560 Differential Pin Pair Summary
XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
47	2	F4	C1	14	-
48	2	G5	E3	15	VREF
49	2	D2	G4	16	-
50	2	H5	E2	15	-
51	2	H4	G3	√	VREF
52	2	J5	F1	17	VREF
53	2	J4	H3	14	-
54	2	K5	H2	18	VREF
55	2	J3	K4	19	-
56	2	L5	K3	√	D1
57	2	L4	K2	√	D2
58	2	M5	L3	17	-
59	2	L1	M4	14	-
60	2	N5	M2	15	VREF
61	2	N4	N3	16	-
62	2	N2	P5	15	-
63	2	P4	P3	√	D3
64	2	P2	R5	17	-
65	2	R4	R3	14	-
66	2	R1	T4	18	VREF
67	2	T5	T3	19	VREF
68	2	T2	U3	√	-
69	3	U1	U2	19	VREF
70	3	V2	V4	18	VREF
71	3	V5	V3	14	-
72	3	W1	W3	17	-
73	3	W4	W5	√	VREF
74	3	Y3	Y4	15	-
75	3	AA1	Y5	16	-
76	3	AA3	AA4	15	VREF
77	3	AB3	AA5	14	-

Table 15: BG560 Differential Pin Pair Summary
XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
78	3	AC1	AB4	17	-
79	3	AC3	AB5	√	D5
80	3	AC4	AD3	√	VREF
81	3	AE1	AC5	4	-
82	3	AD4	AF1	18	VREF
83	3	AF2	AD5	14	-
84	3	AG2	AE4	20	VREF
85	3	AH1	AE5	√	VREF
86	3	AF4	AJ1	15	-
87	3	AJ2	AF5	14	-
88	3	AG4	AK2	15	VREF
89	3	AJ3	AG5	14	-
90	3	AL1	AH4	14	VREF
91	3	AJ4	AH5	√	INIT
92	4	AL4	AJ6	√	-
93	4	AK5	AN3	8	VREF
94	4	AL5	AJ7	√	-
95	4	AM4	AM5	√	VREF
96	4	AK7	AL6	3	-
97	4	AM6	AN6	√	-
98	4	AL7	AJ9	√	VREF
99	4	AN7	AL8	9	VREF
100	4	AM8	AJ10	7	-
101	4	AL9	AM9	7	VREF
102	4	AK10	AN9	2	-
103	4	AL10	AM10	√	VREF
104	4	AL11	AJ12	√	-
105	4	AN11	AK12	8	-
106	4	AL12	AM12	√	-
107	4	AK13	AL13	√	VREF
108	4	AM13	AN13	3	-

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
NA	GND	P14
NA	GND	P13
NA	GND	P12
NA	GND	P11
NA	GND	P10
NA	GND	N2
NA	GND	N17
NA	GND	N16
NA	GND	N15
NA	GND	N14
NA	GND	N13
NA	GND	N12
NA	GND	N11
NA	GND	N10
NA	GND	M17
NA	GND	M16
NA	GND	M15
NA	GND	M14
NA	GND	M13
NA	GND	M12
NA	GND	M11
NA	GND	M10
NA	GND	L17
NA	GND	L16
NA	GND	L15
NA	GND	L14
NA	GND	L13
NA	GND	L12
NA	GND	L11
NA	GND	L10
NA	GND	K17
NA	GND	K16
NA	GND	K15
NA	GND	K14
NA	GND	K13
NA	GND	K12
NA	GND	K11

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
NA	GND	K10
NA	GND	J25
NA	GND	J2
NA	GND	E5
NA	GND	E22
NA	GND	D4
NA	GND	D23
NA	GND	C3
NA	GND	C24
NA	GND	B9
NA	GND	B25
NA	GND	B2
NA	GND	B18
NA	GND	B14
NA	GND	AF26
NA	GND	AF1
NA	GND	AE9
NA	GND	AE25
NA	GND	AE2
NA	GND	AE18
NA	GND	AE13
NA	GND	AD3
NA	GND	AD24
NA	GND	AC4
NA	GND	AC23
NA	GND	AB5
NA	GND	AB22
NA	GND	A26
NA	GND	A1

Notes:

1. NC in the XCV400E.
2. V_{REF} or I/O option only in the XCV600E; otherwise, I/O option only.

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
2	IO_L63N	G4
2	IO_L64P	G3
2	IO_L64N	E2
2	IO_VREF_L65P_Y	H4
2	IO_L65N_Y	E1
2	IO_L66P_YY	H3
2	IO_L66N_YY	F2
2	IO_L67P	J4
2	IO_L67N	F1
2	IO_L68P_Y	J3
2	IO_L68N_Y	G2
2	IO_VREF_L69P_YY	G1
2	IO_L69N_YY	K4
2	IO_L70P_YY	H2
2	IO_L70N_YY	K3
2	IO_VREF_L71P	H1 ³
2	IO_L71N	L4
2	IO_L72P	J2
2	IO_L72N	L3
2	IO_VREF_L73P_YY	J1
2	IO_L73N_YY	M3
2	IO_L74P_YY	K2
2	IO_L74N_YY	N4
2	IO_L75P	K1
2	IO_L75N	N3
2	IO_VREF_L76P_YY	L2
2	IO_D1_L76N_YY	P4
2	IO_D2_L77P_YY	P3
2	IO_L77N_YY	L1
2	IO_L78P_Y	R4
2	IO_L78N_Y	M2
2	IO_L79P	R3
2	IO_L79N	M1
2	IO_L80P	T4
2	IO_L80N	N2
2	IO_VREF_L81P_Y	N1 ¹

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
2	IO_L81N_Y	T3
2	IO_L82P_YY	P2
2	IO_L82N_YY	U5
2	IO_L83P	P1
2	IO_L83N	U4
2	IO_L84P_Y	R2
2	IO_L84N_Y	U3
2	IO_VREF_L85P_YY	V5
2	IO_D3_L85N_YY	R1
2	IO_L86P_YY	V4
2	IO_L86N_YY	T2
2	IO_L87P	V3
2	IO_L87N	T1
2	IO_L88P	W4
2	IO_L88N	U2
2	IO_VREF_L89P_YY	W3
2	IO_L89N_YY	U1
2	IO_L90P_YY	AA3
2	IO_L90N_YY	V2
2	IO_VREF_L91P	AA4 ²
2	IO_L91N	V1
2	IO_L92P_YY	AB2
2	IO_L92N_YY	W2
3	IO	AP3
3	IO	AT3
3	IO	AB3
3	IO_L93P	AB4
3	IO_VREF_L93N	W1 ²
3	IO_L94P_YY	AB5
3	IO_L94N_YY	Y2
3	IO_L95P_YY	AC2
3	IO_VREF_L95N_YY	Y1
3	IO_L96P	AC3
3	IO_L96N	AA1
3	IO_L97P	AC4

FG680 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A ✓ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 23: FG680 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
GCLK LVDS					
3	0	A20	C22	NA	IO_DLL_L29N
2	1	D21	A19	NA	IO_DLL_L29P
1	5	AU22	AT22	NA	IO_DLL_L155N
0	4	AW19	AT21	NA	IO_DLL_L155P
IO LVDS					
Total Pairs: 247, Asynchronous Output Pairs: 111					
0	0	A36	C35	5	-
1	0	B35	D34	5	VREF
2	0	A35	C34	✓	-
3	0	B34	D33	✓	VREF
4	0	A34	C33	3	-
5	0	B33	D32	3	-
6	0	D31	C32	✓	-
7	0	C31	A33	✓	VREF
8	0	B31	B32	5	-
9	0	D30	A32	5	VREF
10	0	C30	A31	✓	-
11	0	D29	B30	✓	VREF
12	0	C29	A30	2	-
13	0	B29	A29	2	-
14	0	A28	B28	✓	VREF
15	0	B27	C28	✓	-
16	0	A27	D27	5	-
17	0	B26	C27	5	-

Table 23: FG680 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
18	0	C26	D26	✓	-
19	0	D25	A26	✓	VREF
20	0	C25	B25	3	-
21	0	D24	A25	3	-
22	0	B23	A24	✓	-
23	0	A23	C24	✓	VREF
24	0	B22	B24	5	-
25	0	A22	E23	5	-
26	0	B21	D23	✓	-
27	0	A21	C23	✓	VREF
28	0	B20	E22	2	-
29	1	A19	C22	NA	IO_LVDS_DLL
30	1	B19	C21	2	VREF
31	1	A18	C19	2	-
32	1	B18	D19	✓	VREF
33	1	A17	C18	✓	-
34	1	B17	D18	5	-
35	1	A16	E18	5	-
36	1	D17	C17	✓	VREF
37	1	E17	B16	✓	-
38	1	C16	A15	3	-
39	1	D16	B15	3	-
40	1	B14	A14	✓	VREF
41	1	A13	C15	✓	-
42	1	B13	D15	5	-
43	1	A12	C14	5	-
44	1	C13	D14	✓	-
45	1	D13	B12	✓	VREF
46	1	C12	A11	2	-
47	1	C11	B11	2	-
48	1	D11	A10	✓	VREF
49	1	C10	B10	✓	-
50	1	D10	A9	5	VREF
51	1	C9	B9	5	-

Table 25: FG860 Differential Pin Pair Summary
XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
120	3	AH1	AL5	1	-
121	3	AH2	AM4	3	-
122	3	AH3	AM5	√	D5
123	3	AJ1	AN3	√	VREF
124	3	AN4	AJ3	2	-
125	3	AN5	AK1	√	-
126	3	AK2	AP4	√	VREF
127	3	AK3	AP5	2	-
128	3	AR3	AL2	5	VREF
129	3	AR4	AL3	√	-
130	3	AM1	AT3	√	VREF
131	3	AM2	AT4	1	-
132	3	AT5	AN1	2	-
133	3	AU3	AN2	√	-
134	3	AP1	AP2	1	VREF
135	3	AR1	AV3	2	-
136	3	AR2	AT1	4	-
137	3	AV4	AT2	2	VREF
138	3	AU1	AU5	1	-
139	3	AU2	AW3	3	-
140	3	AV1	AW5	√	INIT
141	4	AV6	BA4	√	-
142	4	AY4	BA5	2	-
143	4	AW6	BB5	1	-
144	4	BA6	AY5	1	VREF
145	4	BB6	AY6	5	-
146	4	BA7	AV7	√	-
147	4	BB7	AW7	√	VREF
148	4	AY7	BB8	5	-
149	4	BA9	AV8	5	-
150	4	AW8	BA10	√	-
151	4	BB10	AY8	√	VREF
152	4	AV9	BA11	1	-
153	4	BB11	AW9	1	VREF

Table 25: FG860 Differential Pin Pair Summary
XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
154	4	AY9	BA12	√	-
155	4	BB12	AV10	√	VREF
156	4	BA13	AW10	2	-
157	4	BB13	AY10	2	-
158	4	AV11	BA14	√	VREF
159	4	AW11	BB14	√	-
160	4	AV12	BA15	2	-
161	4	AW12	AY15	1	-
162	4	AW13	BB15	1	-
163	4	AV14	BA16	5	-
164	4	AW14	AY16	√	-
165	4	BB16	AV15	√	VREF
166	4	AY17	AW15	5	-
167	4	BB17	AU16	5	-
168	4	AV16	AY18	√	-
169	4	AW16	BA18	√	VREF
170	4	BB19	AW17	1	-
171	4	AY19	AV18	1	-
172	4	AW18	BB20	√	-
173	4	AY20	AV19	√	VREF
174	4	BB21	AW19	2	-
175	4	AY21	AV20	2	VREF
176	5	AW20	AW21	NA	IO_LVDS_DLL
177	5	BB22	AW22	2	VREF
178	5	BB23	AW23	2	-
179	5	AV23	BA23	√	VREF
180	5	AW24	BB24	√	-
181	5	AY24	AW25	1	-
182	5	BA24	AV25	1	-
183	5	AW26	AY25	√	VREF
184	5	AV26	BA25	√	-
185	5	BB26	AV27	5	-
186	5	AY26	AU27	5	-
187	5	AW28	BB27	√	VREF

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
4	IO_L178N_YY	AL28
4	IO_L179P_YY	AE24 ⁴
4	IO_L179N_YY	AN28 ⁵
4	IO_L180P_Y	AJ27
4	IO_L180N_Y	AH26
4	IO_L181P_Y	AG25
4	IO_L181N_Y	AK27
4	IO_L182P	AM28 ⁴
4	IO_L182N	AF24 ⁵
4	IO_L183P_YY	AJ26
4	IO_L183N_YY	AP27
4	IO_VREF_L184P_YY	AK26
4	IO_L184N_YY	AN27
4	IO_L185P	AE23 ⁴
4	IO_L185N	AM27 ⁵
4	IO_L186P_Y	AL26
4	IO_L186N_Y	AP26
4	IO_VREF_L187P_Y	AN26 ²
4	IO_L187N_Y	AJ25
4	IO_L188P	AG24 ⁴
4	IO_L188N	AP25 ⁵
4	IO_L189P_YY	AF23
4	IO_L189N_YY	AM26
4	IO_VREF_L190P_YY	AJ24
4	IO_L190N_YY	AN25
4	IO_L191P_Y	AE22
4	IO_L191N_Y	AM25
4	IO_L192P_Y	AK24
4	IO_L192N_Y	AH23
4	IO_VREF_L193P_YY	AF22
4	IO_L193N_YY	AP24
4	IO_L194P_YY	AL24
4	IO_L194N_YY	AK23
4	IO_L195P_Y	AG22

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
4	IO_L195N_Y	AN23
4	IO_L196P_Y	AP23
4	IO_L196N_Y	AM23
4	IO_L197P_Y	AH22
4	IO_L197N_Y	AP22
4	IO_L198P_Y	AL23
4	IO_L198N_Y	AF21
4	IO_L199P_YY	AL22
4	IO_L199N_YY	AJ22
4	IO_VREF_L200P_YY	AK22
4	IO_L200N_YY	AM22
4	IO_L201P_YY	AG21 ⁴
4	IO_L201N_YY	AJ21 ⁵
4	IO_L202P_Y	AP21
4	IO_L202N_Y	AE20
4	IO_L203P_Y	AH21
4	IO_L203N_Y	AL21
4	IO_L204P	AN21 ⁴
4	IO_L204N	AF20 ⁵
4	IO_L205P_YY	AK21
4	IO_L205N_YY	AP20
4	IO_VREF_L206P_YY	AE19
4	IO_L206N_YY	AN20
4	IO_L207P_Y	AG20 ⁴
4	IO_L207N_Y	AL20 ⁵
4	IO_L208P_Y	AH20
4	IO_L208N_Y	AK20
4	IO_L209P_Y	AN19
4	IO_L209N_Y	AJ20
4	IO_L210P	AF19 ⁴
4	IO_L210N	AP19 ⁵
4	IO_L211P_YY	AM19
4	IO_L211N_YY	AH19
4	IO_VREF_L212P_YY	AJ19

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
NA	GND	R15
NA	GND	P15
NA	GND	L3
NA	GND	G7
NA	GND	E30
NA	GND	C24
NA	GND	B34
NA	GND	AP32
NA	GND	AM1
NA	GND	AM34
NA	GND	AJ29
NA	GND	AF9
NA	GND	AA17
NA	GND	Y17
NA	GND	W16
NA	GND	V16
NA	GND	U17
NA	GND	T17
NA	GND	R16
NA	GND	P16
NA	GND	L32
NA	GND	G28
NA	GND	D4
NA	GND	C32
NA	GND	A1
NA	GND	AP33
NA	GND	AM2
NA	GND	AL4
NA	GND	AH1
NA	GND	AF26
NA	GND	AA18
NA	GND	Y18
NA	GND	W17
NA	GND	V17

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
NA	GND	U18
NA	GND	T18
NA	GND	R17
NA	GND	P17
NA	GND	J9
NA	GND	G34
NA	GND	D31
NA	GND	C33
NA	GND	A2
NA	GND	AB17
NA	GND	AB18
NA	GND	N17
NA	GND	N18
NA	GND	U13
NA	GND	V13
NA	GND	U22
NA	GND	V22

Notes:

1. V_{REF} or I/O option only in the XCV1600E, XCV2000E, XCV2600E, and XCV3200E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV2000E, XCV2600E, and XCV3200E; otherwise, I/O option only.
3. No Connect in the XCV1000E, XCV1600E.
4. No Connect in the XCV1000E.
5. I/O in the XCV1000E.