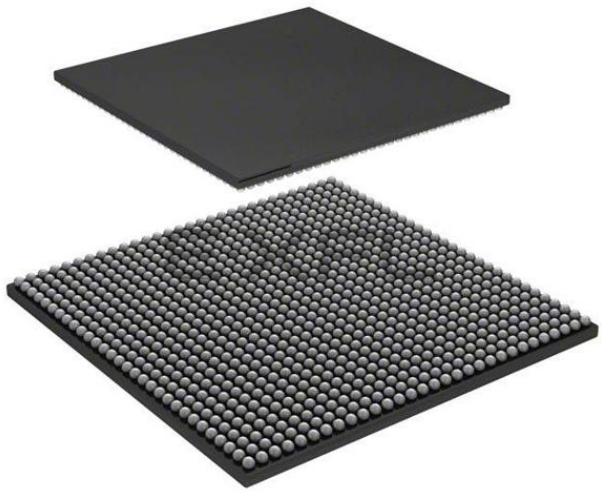
AMD Xilinx - XCV1600E-7FG900C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	7776
Number of Logic Elements/Cells	34992
Total RAM Bits	589824
Number of I/O	700
Number of Gates	2188742
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	900-BBGA
Supplier Device Package	900-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv1600e-7fg900c

Table 1: **Virtex-E Field-Programmable Gate Array Family Members**

Device	System Gates	Logic Gates	CLB Array	Logic Cells	Differential I/O Pairs	User I/O	BlockRAM Bits	Distributed RAM Bits
XCV50E	71,693	20,736	16 x 24	1,728	83	176	65,536	24,576
XCV100E	128,236	32,400	20 x 30	2,700	83	196	81,920	38,400
XCV200E	306,393	63,504	28 x 42	5,292	119	284	114,688	75,264
XCV300E	411,955	82,944	32 x 48	6,912	137	316	131,072	98,304
XCV400E	569,952	129,600	40 x 60	10,800	183	404	163,840	153,600
XCV600E	985,882	186,624	48 x 72	15,552	247	512	294,912	221,184
XCV1000E	1,569,178	331,776	64 x 96	27,648	281	660	393,216	393,216
XCV1600E	2,188,742	419,904	72 x 108	34,992	344	724	589,824	497,664
XCV2000E	2,541,952	518,400	80 x 120	43,200	344	804	655,360	614,400
XCV2600E	3,263,755	685,584	92 x 138	57,132	344	804	753,664	812,544
XCV3200E	4,074,387	876,096	104 x 156	73,008	344	804	851,968	1,038,336

Virtex-E Compared to Virtex Devices

The Virtex-E family offers up to 43,200 logic cells in devices up to 30% faster than the Virtex family.

I/O performance is increased to 622 Mb/s using Source Synchronous data transmission architectures and synchronous system performance up to 240 MHz using singled-ended SelectI/O technology. Additional I/O standards are supported, notably LVPECL, LVDS, and BLVDS, which use two pins per signal. Almost all signal pins can be used for these new standards.

Virtex-E devices have up to 640 Kb of faster (250 MHz) block SelectRAM, but the individual RAMs are the same size and structure as in the Virtex family. They also have eight DLLs instead of the four in Virtex devices. Each individual DLL is slightly improved with easier clock mirroring and 4x frequency multiplication.

V_{CCINT}, the supply voltage for the internal logic and memory, is 1.8 V, instead of 2.5 V for Virtex devices. Advanced processing and 0.18 µm design rules have resulted in smaller dice, faster speed, and lower power consumption.

I/O pins are 3 V tolerant, and can be 5 V tolerant with an external 100 Ω resistor. PCI 5 V is not supported. With the addition of appropriate external resistors, any pin can tolerate any voltage desired.

Banking rules are different. With Virtex devices, all input buffers are powered by V_{CCINT}. With Virtex-E devices, the LVTTL, LVCMOS2, and PCI input buffers are powered by the I/O supply voltage V_{CCO}.

The Virtex-E family is not bitstream-compatible with the Virtex family, but Virtex designs can be compiled into equivalent Virtex-E devices.

The same device in the same package for the Virtex-E and Virtex families are pin-compatible with some minor exceptions. See the data sheet pinout section for details.

General Description

The Virtex-E FPGA family delivers high-performance, high-capacity programmable logic solutions. Dramatic increases in silicon efficiency result from optimizing the new architecture for place-and-route efficiency and exploiting an aggressive 6-layer metal 0.18 µm CMOS process. These advances make Virtex-E FPGAs powerful and flexible alternatives to mask-programmed gate arrays. The Virtex-E family includes the nine members in Table 1.

Building on experience gained from Virtex FPGAs, the Virtex-E family is an evolutionary step forward in programmable logic design. Combining a wide variety of programmable system features, a rich hierarchy of fast, flexible interconnect resources, and advanced process technology, the Virtex-E family delivers a high-speed and high-capacity programmable logic solution that enhances design flexibility while reducing time-to-market.

Virtex-E Architecture

Virtex-E devices feature a flexible, regular architecture that comprises an array of configurable logic blocks (CLBs) surrounded by programmable input/output blocks (IOBs), all interconnected by a rich hierarchy of fast, versatile routing

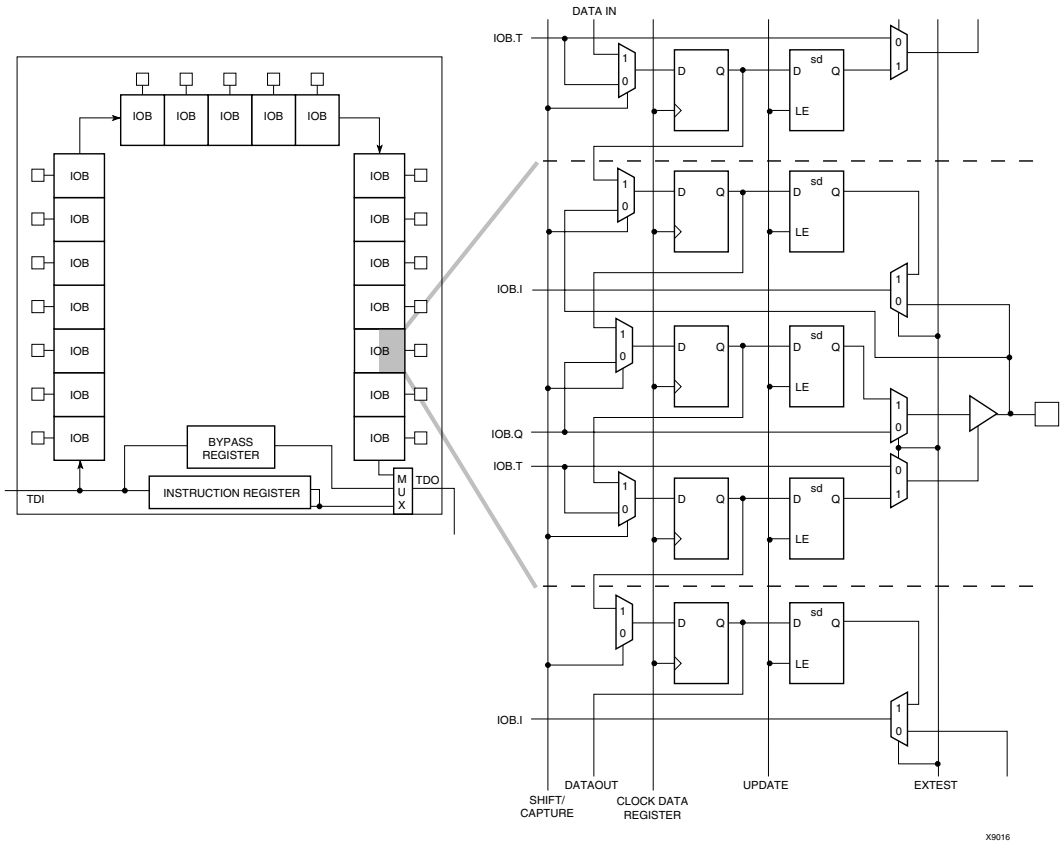

Figure 11: **Virtex-E Family Boundary Scan Logic**

Instruction Set

The Virtex-E series Boundary Scan instruction set also includes instructions to configure the device and read back configuration data (CFG_IN, CFG_OUT, and JSTART). The complete instruction set is coded as shown in Table 6..

Table 6: **Boundary Scan Instructions**

Boundary Scan Command	Binary Code(4:0)	Description
EXTEST	00000	Enables Boundary Scan EXTEST operation
SAMPLE/ PRELOAD	00001	Enables Boundary Scan SAMPLE/PRELOAD operation
USER1	00010	Access user-defined register 1
USER2	00011	Access user-defined register 2
CFG_OUT	00100	Access the configuration bus for read operations.

Table 6: **Boundary Scan Instructions *(Continued)***

Boundary Scan Command	Binary Code(4:0)	Description
CFG_IN	00101	Access the configuration bus for write operations.
INTEST	00111	Enables Boundary Scan INTEST operation
USERCODE	01000	Enables shifting out USER code
IDCODE	01001	Enables shifting out of ID Code
HIGHZ	01010	3-states output pins while enabling the Bypass Register
JSTART	01100	Clock the start-up sequence when StartupClk is TCK
BYPASS	11111	Enables BYPASS
RESERVED	All other codes	Xilinx reserved instructions

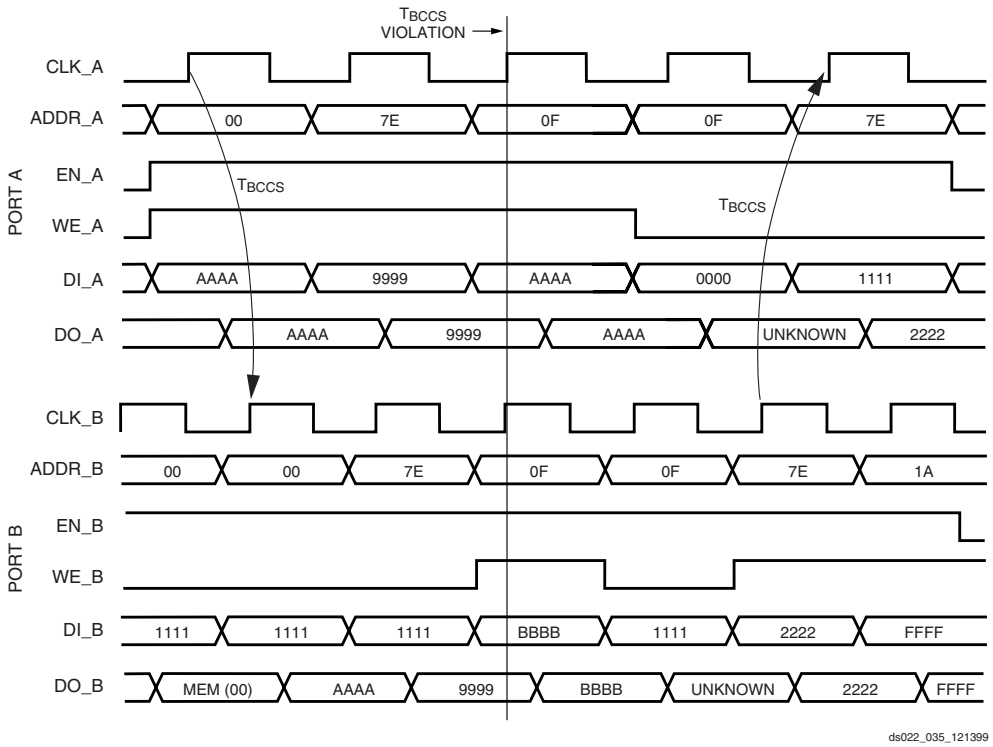

Figure 34: **Timing Diagram for a True Dual-port Read/Write Block SelectRAM+ Memory**

At the third rising edge of CLKA, the T_{BCCS} parameter is violated with two writes to memory location 0x0F. The DOA and DOB buses reflect the contents of the DIA and DIB buses, but the stored value at 0x0F is invalid.

At the fourth rising edge of CLKA, a read operation is performed at memory location 0x0F and invalid data is present on the DOA bus. Port B also executes a read operation to memory location 0x0F and also reads invalid data.

At the fifth rising edge of CLKA a read operation is performed that does not violate the T_{BCCS} parameter to the previous write of 0x7E by Port B. THe DOA bus reflects the recently written value by Port B.

Initialization

The block SelectRAM+ memory can initialize during the device configuration sequence. The 16 initialization properties of 64 hex values each (a total of 4096 bits) set the initialization of each RAM. These properties appear in Table 17. Any initialization properties not explicitly set configure as zeros. Partial initialization strings pad with zeros. Initialization strings greater than 64 hex values generate an error. The RAMs can be simulated with the initialization values using generics in VHDL simulators and parameters in Verilog simulators.

Initialization in VHDL and Synopsys

The block SelectRAM+ structures can be initialized in VHDL for both simulation and synthesis for inclusion in the EDIF output file. The simulation of the VHDL code uses a generic to pass the initialization. Synopsys FPGA compiler does not presently support generics. The initialization values instead attach as attributes to the RAM by a built-in Synopsys dc_script. The translate_off statement stops synthesis translation of the generic statements. The following code illustrates a module that employs these techniques.

Table 17: **RAM Initialization Properties**

Property	Memory Cells
INIT_00	255 to 0
INIT_01	511 to 256
INIT_02	767 to 512
INIT_03	1023 to 768
INIT_04	1279 to 1024
INIT_05	1535 to 1280
INIT_06	1791 to 2047
INIT_07	2047 to 1792
INIT_08	2303 to 2048
INIT_09	2559 to 2304
INIT_0a	2815 to 2560
INIT_0b	3071 to 2816
INIT_0c	3327 to 3072
INIT_0d	3583 to 3328
INIT_0e	3839 to 3584
INIT_0f	4095 to 3840

LVTTL 3-state output buffers have selectable drive strengths.

The format for LVTTL OBUFT symbol names is as follows:

OBUFT_<slew_rate>_<drive_strength>

where <slew_rate> is either F (Fast) or S (Slow), and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

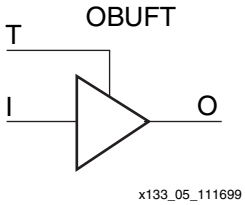

Figure 41: **3-State Output Buffer Symbol (OBUFT)**

The following list details variations of the OBUFT symbol.

- OBUFT
- OBUFT_S_2
- OBUFT_S_4
- OBUFT_S_6
- OBUFT_S_8
- OBUFT_S_12
- OBUFT_S_16
- OBUFT_S_24
- OBUFT_F_2
- OBUFT_F_4
- OBUFT_F_6
- OBUFT_F_8
- OBUFT_F_12
- OBUFT_F_16
- OBUFT_F_24
- OBUFT_LVCMOS2
- OBUFT_PCI33_3
- OBUFT_PCI66_3
- OBUFT_GTL
- OBUFT_GTLP
- OBUFT_HSTL_I
- OBUFT_HSTL_III
- OBUFT_HSTL_IV
- OBUFT_SSTL3_I
- OBUFT_SSTL3_II
- OBUFT_SSTL2_I
- OBUFT_SSTL2_II
- OBUFT_CTT
- OBUFT_AGP
- OBUFT_LVCMOS18
- OBUFT_LVDS
- OBUFT_LVPECL

The Virtex-E series supports eight banks for the HQ and PQ packages. The CS package supports four V_{CCO} banks.

The SelectI/O OBUFT placement restrictions require that within a given V_{CCO} bank each OBUFT share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within the same V_{CCO} bank.

The LOC property can specify a location for the OBUFT.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak “keeper” circuit. Control this feature by adding the appropriate symbol to the output net of the OBUFT (PULLUP, PULLDOWN, or KEEPER).

The weak “keeper” circuit requires the input buffer within the IOB to sample the I/O signal. So, OBUFTs programmed for an I/O standard that requires a V_{REF} have automatic placement of a V_{REF} in the bank with an OBUFT configured with a weak “keeper” circuit. This restriction does not affect most circuit design as applications using an OBUFT configured with a weak “keeper” typically implement a bidirectional I/O. In this case the IBUF (and the corresponding V_{REF}) are explicitly placed.

The LOC property can specify a location for the OBUFT.

IOBUF

Use the IOBUF symbol for bidirectional signals that require both an input buffer and a 3-state output buffer with an active high 3-state pin. The generic input/output buffer IOBUF appears in Figure 42.

The extension to the base name defines which I/O standard the IOBUF uses. With no extension specified for the generic IOBUF symbol, the assumed standard is LVTTL input buffer and slew rate limited LVTTL with 12 mA drive strength for the output buffer.

The LVTTL IOBUF additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL bidirectional buffers have selectable output drive strengths.

The format for LVTTL IOBUF symbol names is as follows:

IOBUF_<slew_rate>_<drive_strength>

where <slew_rate> is either F (Fast) or S (Slow), and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

IOB Input Switching Characteristics Standard Adjustments

Description	Symbol	Standard	Speed Grade(1)				Units
			Min	-8	-7	-6	
Data Input Delay Adjustments							
Standard-specific data input delay adjustments	T_{ILVTTL}	LVTTL	0.0	0.0	0.0	0.0	ns
	$T_{ILVCMOS2}$	LVCMOS2	–0.02	0.0	0.0	0.0	ns
	$T_{ILVCMOS18}$	LVCMOS18	0.12	+0.20	+0.20	+0.20	ns
	T_{ILVDS}	LVDS	0.00	+0.15	+0.15	+0.15	ns
	$T_{ILVPECL}$	LVPECL	0.00	+0.15	+0.15	+0.15	ns
	T_{IPCI33_3}	PCI, 33 MHz, 3.3 V	–0.05	+0.08	+0.08	+0.08	ns
	T_{IPCI66_3}	PCI, 66 MHz, 3.3 V	–0.05	–0.11	–0.11	–0.11	ns
	T_{IGTL}	GTL	+0.10	+0.14	+0.14	+0.14	ns
	$T_{IGTLPLUS}$	GTL+	+0.06	+0.14	+0.14	+0.14	ns
	T_{IHSTL}	HSTL	+0.02	+0.04	+0.04	+0.04	ns
	T_{ISSTL2}	SSTL2	–0.04	+0.04	+0.04	+0.04	ns
	T_{ISSTL3}	SSTL3	–0.02	+0.04	+0.04	+0.04	ns
	T_{ICTT}	CTT	+0.01	+0.10	+0.10	+0.10	ns
	T_{IAGP}	AGP	–0.03	+0.04	+0.04	+0.04	ns

Notes:
1. Input timing i for LVTTL is measured at 1.4 V. For other I/O standards, see Table 4.

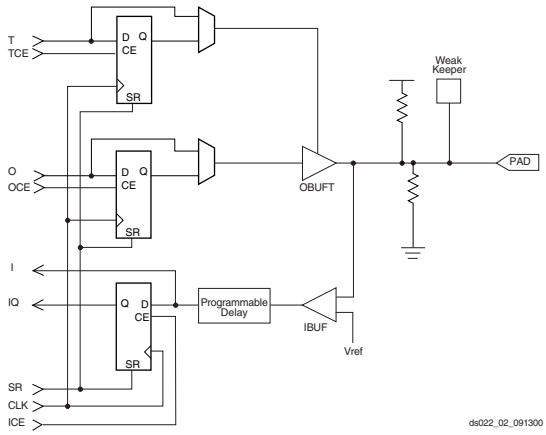

Figure 1: **Virtex-E Input/Output Block (IOB)**

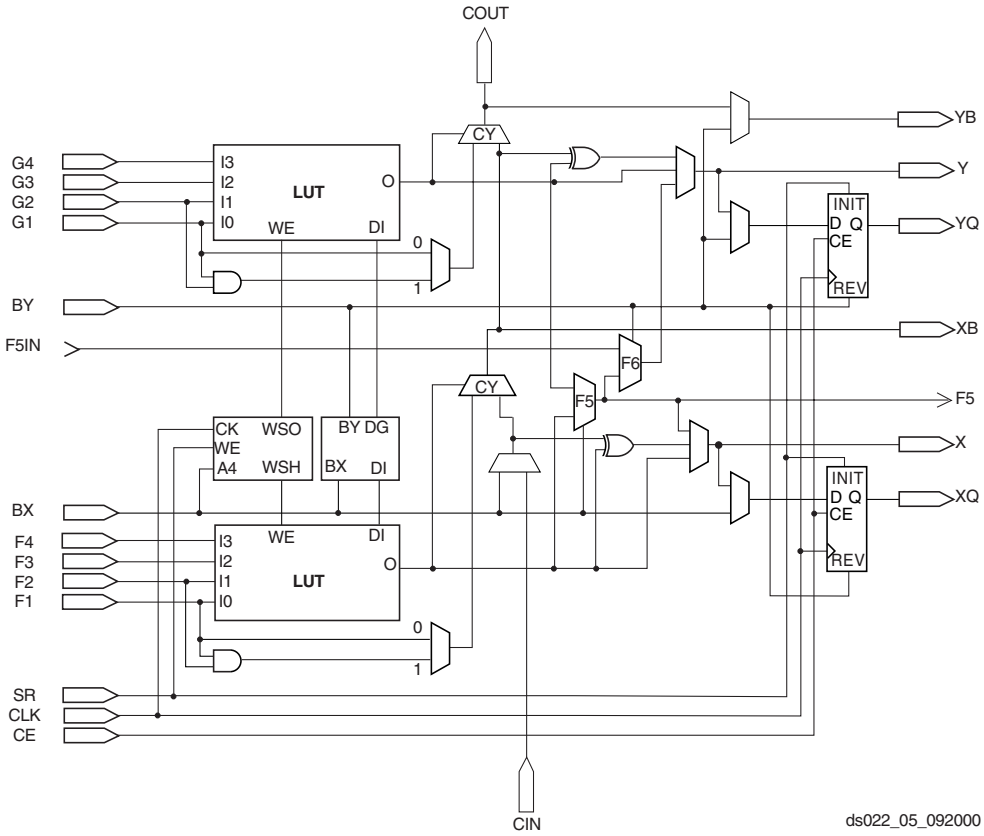

Figure 2: **Detailed View of Virtex-E Slice**

CLB Distributed RAM Switching Characteristics

Description	Symbol	Speed Grade(1)				Units
		Min	-8	-7	-6	
Sequential Delays						
Clock CLK to X/Y outputs (WE active) 16 x 1 mode	$T_{SHCKO16}$	0.67	1.38	1.5	1.7	ns, max
Clock CLK to X/Y outputs (WE active) 32 x 1 mode	$T_{SHCKO32}$	0.84	1.66	1.9	2.1	ns, max
Shift-Register Mode Clock CLK to X/Y outputs	T_{REG}	1.25	2.39	2.9	3.2	ns, max
Setup and Hold Times before/after Clock CLK						
F/G address inputs	T_{AS}/T_{AH}	0.19 / 0	0.38 / 0	0.42 / 0	0.47 / 0	ns, min
BX/BY data inputs (DIN)	T_{DS}/T_{DH}	0.44 / 0	0.87 / 0	0.97 / 0	1.09 / 0	ns, min
SR input (WE)	T_{WS}/T_{WH}	0.29 / 0	0.57 / 0	0.7 / 0	0.8 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T_{WPH}	0.96	1.9	2.1	2.4	ns, min
Minimum Pulse Width, Low	T_{WPL}	0.96	1.9	2.1	2.4	ns, min
Minimum clock period to meet address write cycle time	T_{WC}	1.92	3.8	4.2	4.8	ns, min
Shift-Register Mode						
Minimum Pulse Width, High	T_{SRPH}	1.0	1.9	2.1	2.4	ns, min
Minimum Pulse Width, Low	T_{SRPL}	1.0	1.9	2.1	2.4	ns, min

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

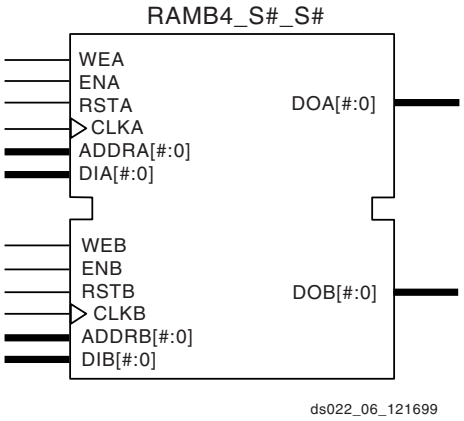

Figure 3: **Dual-Port Block SelectRAM**

Global Clock Set-Up and Hold for LVTTL Standard, *without* DLL

Description[1]	Symbol	Device	Speed Grade[2, 3]				Units
			Min	-8	-7	-6	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in **IOB Input Switching Characteristics Standard Adjustments**, page 8.							
Full Delay	T_{PSFD}/T_{PHFD}	XCV50E	1.8 / 0	1.8 / 0	1.8 / 0	1.8 / 0	ns
Global Clock and IFF, without DLL		XCV100E	1.8 / 0	1.8 / 0	1.8 / 0	1.8 / 0	ns
		XCV200E	1.9 / 0	1.9 / 0	1.9 / 0	1.9 / 0	ns
		XCV300E	2.0 / 0	2.0 / 0	2.0 / 0	2.0 / 0	ns
		XCV400E	2.0 / 0	2.0 / 0	2.0 / 0	2.0 / 0	ns
		XCV600E	2.1 / 0	2.1 / 0	2.1 / 0	2.1 / 0	ns
		XCV1000E	2.3 / 0	2.3 / 0	2.3 / 0	2.3 / 0	ns
		XCV1600E	2.5 / 0	2.5 / 0	2.5 / 0	2.5 / 0	ns
		XCV2000E	2.5 / 0	2.5 / 0	2.5 / 0	2.5 / 0	ns
		XCV2600E	2.7 / 0	2.7 / 0	2.7 / 0	2.7 / 0	ns
		XCV3200E	2.8 / 0	2.8 / 0	2.8 / 0	2.8 / 0	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P138	IO_D5_L26N_YY	3
P137	VCCINT	NA
P136	VCCO	3
P135	GND	NA
P134	IO_D6_L27P_Y	3
P133	IO_VREF_L27N_Y	3
P132	IO_VREF	3
P131	IO_L28P_Y	3
P130	IO_VREF_L28N_Y	3
P129	GND	NA
P128	IO_L29P_Y	3
P127	IO_L29N_Y	3
P126	IO_VREF_L30P_Y	3
P125	IO_L30N_Y	3
P124	IO_D7_L31P_YY	3
P123	IO_INIT_L31N_YY	3
P122	PROGRAM	NA
P121	VCCO	3
P120	DONE	3
P119	GND	NA
P118	IO_L32P_YY	4
P117	IO_L32N_YY	4
P116	VCCO	4
P115	IO_VREF	4
P114	IO_L33P_YY	4
P113	IO_L33N_YY	4
P112	GND	NA
P111	IO_VREF_L34P_YY	4
P110	IO_L34N_YY	4
P109	IO_VREF	4
P108	IO_VREF_L35P_YY	4
P107	IO_L35N_YY	4
P106	GND	NA
P105	VCCO	4
P104	VCCINT	NA
P103	IO_L36P_YY	4

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P102	IO_L36N_YY	4
P101[1]	IO_VREF	4
P100	IO_L37P_Y	4
P99	IO_L37N_Y	4
P98	GND	NA
P97	IO_VREF_L38P_Y	4
P96	IO_L38N_Y	4
P95	IO_L39P	4
P94	IO_VREF_L39N	4
P93	IO_LVDS_DLL_L40P	4
P92	GCK0	4
P91	GND	NA
P90	VCCO	4
P89	GCK1	5
P88	VCCINT	NA
P87	IO_LVDS_DLL_L40N	5
P86	IO_VREF	5
P85	VCCO	5
P84	IO_VREF_L41P	5
P83	GND	NA
P82	IO_L41N	5
P81	IO	5
P80[1]	IO_VREF	5
P79	IO_L42P_YY	5
P78	IO_L42N_YY	5
P77	VCCINT	NA
P76	VCCO	5
P75	GND	NA
P74	IO_L43P_YY	5
P73	IO_VREF_L43N_YY	5
P72	IO_VREF	5
P71	IO_L44P_YY	5
P70	IO_VREF_L44N_YY	5
P69	GND	NA
P68	IO_L45P_YY	5
P67	IO_L45N_YY	5

HQ240 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 9: **HQ240 Differential Pin Pair Summary XCV600E, XCV1000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	P92	P93	NA	IO _DLL_L40P
1	5	P89	P87	NA	IO _DLL_L40N
2	1	P210	P209	NA	IO _DLL_L6P
3	0	P213	P215	NA	IO _DLL_L6N
IO LVDS Total Pairs: 64, Asynchronous Output Pairs: 53					
0	0	P236	P237	NA	VREF
1	0	P234	P235	√	-
2	0	P228	P229	√	VREF
3	0	P223	P224	√	-
4	0	P220	P221	√	-
5	0	P217	P218	√	VREF
6	1	P209	P215	NA	IO_LVDS_DLL
7	1	P205	P206	√	VREF
8	1	P202	P203	√	-
9	1	P199	P200	√	-
10	1	P194	P195	√	VREF
11	1	P191	P192	√	VREF
12	1	P188	P189	√	-
13	1	P186	P187	NA	VREF
14	1	P184	P185	√	CS
15	2	P178	P177	√	DIN, D0

Table 9: **HQ240 Differential Pin Pair Summary XCV600E, XCV1000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
16	2	P174	P173	√	-
17	2	P171	P170	√	VREF
18	2	P168	P167	√	D1
19	2	P163	P162	√	D2
20	2	P160	P159	√	-
21	2	P157	P156	√	D3
22	2	P155	P154	1	VREF
23	2	P153	P152	√	-
24	3	P145	P144	√	D4, VREF
25	3	P142	P141	√	-
26	3	P139	P138	√	D5
27	3	P134	P133	√	VREF
28	3	P131	P130	√	VREF
29	3	P128	P127	√	-
30	3	P126	P125	1	VREF
31	3	P124	P123	√	INIT
32	4	P118	P117	√	-
33	4	P114	P113	√	-
34	4	P111	P110	√	VREF
35	4	P108	P107	√	VREF
36	4	P103	P102	√	-
37	4	P100	P99	√	-
38	4	P97	P96	√	VREF
39	4	P95	P94	NA	VREF
40	5	P93	P87	NA	IO_LVDS_DLL
41	5	P84	P82	NA	VREF
42	5	P79	P78	√	-
43	5	P74	P73	√	VREF
44	5	P71	P70	√	VREF
45	5	P68	P67	√	-
46	5	P66	P65	NA	VREF
47	5	P64	P63	√	-

Table 15: **BG560 Differential Pin Pair Summary XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
171	7	J33	M29	√	-
172	7	K31	L30	√	VREF
173	7	H33	L29	4	-
174	7	H32	J31	18	VREF
175	7	H31	K29	14	-
176	7	G32	J30	20	VREF
177	7	G31	J29	√	VREF
178	7	E32	E33	15	-
179	7	F31	H29	14	-
180	7	E31	D32	15	VREF
181	7	C33	G29	14	-
182	7	D31	F30	14	VREF

Notes:
1. AO in the XCV1600E.
2. AO in the XCV2000E.
3. AO in the XCV1600E, 2000E.
4. AO in the XCV1000E, 1600E.
5. AO in the XCV1000E, 2000E.
6. AO in the XCV1000E.
7. AO in the XCV1000E, 1600E, 2000E.
8. AO in the XCV600E, 1600E.
9. AO in the XCV400E, 600E, 1600E.
10. AO in the XCV400E, 600E, 1000E, 2000E.
11. AO in the XCV400E, 600E, 1000E.
12. AO in the XCV400E, 1000E, 2000E.
13. AO in the XCV400E, 600E, 1000E, 1600E.
14. AO in the XCV400E, 1000E, 1600E.
15. AO in the XCV600E, 1000E, 2000E.
16. AO in the XCV600E, 2000E.
17. AO in the XCV400E, 600E, 1600E, 2000E.
18. AO in the XCV600E, 1000E, 1600E, 2000E.
19. AO in the XCV400E, 600E, 2000E.
20. AO in the XCV400E, 1000E.

FG256 Fine-Pitch Ball Grid Array Packages

XCV50E, XCV100E, XCV200E, and XCV300E devices in FG256 fine-pitch Ball Grid Array packages have footprint compatibility. Pins labeled I0_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 16, see Table 17 for Differential Pair information.

Table 16: **FG256 Package — XCV50E, XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
0	GCK3	B8
0	IO	B3
0	IO	E7
0	IO	D8
0	IO_L0N_Y	C5
0	IO_VREF_L0P_Y	A3[2]
0	IO_L1N_YY	D5
0	IO_L1P_YY	E6
0	IO_VREF_L2N_YY	B4
0	IO_L2P_YY	A4
0	IO_L3N_Y	D6
0	IO_L3P_Y	B5
0	IO_VREF_L4N_YY	C6[1]
0	IO_L4P_YY	A5
0	IO_L5N_YY	B6
0	IO_L5P_YY	C7
0	IO_L6N_Y	D7
0	IO_L6P_Y	C8
0	IO_VREF_L7N_Y	B7
0	IO_L7P_Y	A6
0	IO_LVDS_DLL_L8N	A7
1	GCK2	C9
1	IO	B10
1	IO_LVDS_DLL_L8P	A8
1	IO_L9N_Y	D9
1	IO_L9P_Y	A9
1	IO_L10N_Y	E10
1	IO_VREF_L10P_Y	B9

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
NA	VCCINT	T15
NA	VCCINT	T16
NA	VCCINT	U6
NA	VCCINT	U17
NA	VCCINT	V5
NA	VCCINT	V18
NA	VCCO_7	L7
NA	VCCO_7	K7
NA	VCCO_7	K6
NA	VCCO_7	J6
NA	VCCO_7	H6
NA	VCCO_7	G6
NA	VCCO_6	N7
NA	VCCO_6	M7
NA	VCCO_6	T6
NA	VCCO_6	R6
NA	VCCO_6	P6
NA	VCCO_6	N6
NA	VCCO_5	U10
NA	VCCO_5	U9
NA	VCCO_5	U8
NA	VCCO_5	U7
NA	VCCO_5	T11
NA	VCCO_5	T10
NA	VCCO_4	U16
NA	VCCO_4	U15
NA	VCCO_4	U14
NA	VCCO_4	U13
NA	VCCO_4	T13
NA	VCCO_4	T12
NA	VCCO_3	T17
NA	VCCO_3	R17
NA	VCCO_3	P17
NA	VCCO_3	N17
NA	VCCO_3	N16
NA	VCCO_3	M16

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
NA	VCCO_2	K17
NA	VCCO_2	J17
NA	VCCO_2	H17
NA	VCCO_2	G17
NA	VCCO_2	L16
NA	VCCO_2	K16
NA	VCCO_1	G13
NA	VCCO_1	G12
NA	VCCO_1	F16
NA	VCCO_1	F15
NA	VCCO_1	F14
NA	VCCO_1	F13
NA	VCCO_0	G11
NA	VCCO_0	G10
NA	VCCO_0	F10
NA	VCCO_0	F9
NA	VCCO_0	F8
NA	VCCO_0	F7
NA	GND	AB22
NA	GND	AB1
NA	GND	AA21
NA	GND	AA2
NA	GND	Y20
NA	GND	Y3
NA	GND	P14
NA	GND	P13
NA	GND	P12
NA	GND	P11
NA	GND	P10
NA	GND	P9
NA	GND	N14
NA	GND	N13
NA	GND	N12
NA	GND	N11
NA	GND	N10
NA	GND	N9

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
1	IO_L40P_YY	D20
1	IO_L41N_YY	F19
1	IO_VREF_L41P_YY	C21
1	IO_L42N_YY	B22
1	IO_L42P_YY	E20
1	IO_L43N_Y	A23
1	IO_L43P_Y	D21
1	IO_WRITE_L44N_YY	C22
1	IO_CS_L44P_YY	E21
2	IO	D25[1]
2	IO	D26
2	IO	E26
2	IO	F26
2	IO	H26[1]
2	IO	K26[1]
2	IO	M25[1]
2	IO	N26[1]
2	IO_D1	K24
2	IO_DOUT_BUSY_L45P_YY	E23
2	IO_DIN_D0_L45N_YY	F22
2	IO_L46P_YY	E24
2	IO_L46N_YY	F20
2	IO_L47P_Y	G21
2	IO_L47N_Y	G22
2	IO_VREF_L48P_Y	F24
2	IO_L48N_Y	H20
2	IO_L49P_Y	E25
2	IO_L49N_Y	H21
2	IO_L50P_YY	F23
2	IO_L50N_YY	G23
2	IO_VREF_L51P_YY	H23
2	IO_L51N_YY	J20
2	IO_L52P_YY	G24
2	IO_L52N_YY	H22
2	IO_L53P_Y	J21
2	IO_L53N_Y	G25

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
2	IO_VREF_L54P_Y	G26[2]
2	IO_L54N_Y	J22
2	IO_L55P_YY	H24
2	IO_L55N_YY	J23
2	IO_L56P_YY	J24
2	IO_VREF_L56N_YY	K20
2	IO_D2_L57P_YY	K22
2	IO_L57N_YY	K21
2	IO_L58P_YY	H25
2	IO_L58N_YY	K23
2	IO_L59P_Y	L20
2	IO_L59N_Y	J26
2	IO_L60P_Y	K25
2	IO_L60N_Y	L22
2	IO_L61P_Y	L21
2	IO_L61N_Y	L23
2	IO_L62P_Y	M20
2	IO_L62N_Y	L24
2	IO_VREF_L63P_YY	M23
2	IO_D3_L63N_YY	M22
2	IO_L64P_YY	L26
2	IO_L64N_YY	M21
2	IO_L65P_Y	N19
2	IO_L65N_Y	M24
2	IO_VREF_L66P_Y	M26
2	IO_L66N_Y	N20
2	IO_L67P_YY	N24
2	IO_L67N_YY	N21
2	IO_L68P_YY	N23
2	IO_L68N_YY	N22
3	IO	P24
3	IO	P26[1]
3	IO	R26[1]
3	IO	T26[1]
3	IO	U26[1]
3	IO	W25

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
6	IO_VREF_L200N_YY	AH39
6	IO_L200P_YY	AG38
6	IO_L201N_YY	AG36
6	IO_L201P_YY	AG39
6	IO_L202N_Y	AG37
6	IO_L202P_Y	AF39
6	IO_L203N	AF36
6	IO_L203P	AE38
6	IO_L204N	AF37
6	IO_L204P	AF38
6	IO_VREF_L205N_Y	AE39[1]
6	IO_L205P_Y	AE36
6	IO_L206N_YY	AD38
6	IO_L206P_YY	AE37
6	IO_L207N	AD39
6	IO_L207P	AD36
6	IO_L208N_Y	AC38
6	IO_L208P_Y	AC39
6	IO_VREF_L209N_YY	AD37
6	IO_L209P_YY	AB38
6	IO_L210N_YY	AC35
6	IO_L210P_YY	AB39
6	IO_L211N	AC36
6	IO_L211P	AA38
6	IO_L212N	AC37
6	IO_L212P	AA39
6	IO_VREF_L213N_YY	AB35
6	IO_L213P_YY	Y38
6	IO_L214N_YY	AB36
6	IO_L214P_YY	Y39
6	IO_VREF_L215N	AB37[2]
6	IO_L215P	AA36
7	IO	C38
7	IO	B37
7	IO	F37

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
7	IO_L216N_YY	AA37
7	IO_L216P_YY	W38
7	IO_L217N	W37
7	IO_VREF_L217P	V39[2]
7	IO_L218N_YY	W36
7	IO_L218P_YY	U39
7	IO_L219N_YY	V38
7	IO_VREF_L219P_YY	U38
7	IO_L220N	V37
7	IO_L220P	T39
7	IO_L221N	V36
7	IO_L221P	T38
7	IO_L222N_YY	V35
7	IO_L222P_YY	R39
7	IO_L223N_YY	U37
7	IO_VREF_L223P_YY	U36
7	IO_L224N_Y	R38
7	IO_L224P_Y	U35
7	IO_L225N	P39
7	IO_L225P	T37
7	IO_L226N_YY	P38
7	IO_L226P_YY	T36
7	IO_L227N_Y	N39
7	IO_VREF_L227P_Y	N38[1]
7	IO_L228N	R37
7	IO_L228P	M39
7	IO_L229N	R36
7	IO_L229P	M38
7	IO_L230N_Y	P37
7	IO_L230P_Y	L39
7	IO_L231N_YY	P36
7	IO_L231P_YY	N37
7	IO_L232N_YY	L38
7	IO_VREF_L232P_YY	N36
7	IO_L233N	K39
7	IO_L233P	M37

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
NA	GND	C42
NA	GND	C41
NA	GND	C40
NA	GND	C3
NA	GND	C2
NA	GND	C1
NA	GND	BB41
NA	GND	BB40
NA	GND	BB4
NA	GND	BB39
NA	GND	BB3
NA	GND	BB2
NA	GND	BA42
NA	GND	BA41
NA	GND	BA40
NA	GND	BA3
NA	GND	BA2
NA	GND	BA1
NA	GND	B42
NA	GND	B41
NA	GND	B40
NA	GND	B3
NA	GND	B2
NA	GND	B1
NA	GND	AY42
NA	GND	AY41
NA	GND	AY40
NA	GND	AY3
NA	GND	AY2
NA	GND	AY1
NA	GND	AW42
NA	GND	AW4
NA	GND	AW39
NA	GND	AW1
NA	GND	AV5
NA	GND	AV38
NA	GND	AV30

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
NA	GND	AV22
NA	GND	AV21
NA	GND	AV13
NA	GND	AU6
NA	GND	AU37
NA	GND	AU30
NA	GND	AU22
NA	GND	AU21
NA	GND	AU13
NA	GND	AK6
NA	GND	AK5
NA	GND	AK38
NA	GND	AK37
NA	GND	AB6
NA	GND	AB5
NA	GND	AB38
NA	GND	AB37
NA	GND	AA6
NA	GND	AA5
NA	GND	AA38
NA	GND	AA37
NA	GND	A41
NA	GND	A40
NA	GND	A4
NA	GND	A39
NA	GND	A3
NA	GND	A2

Notes:
1. V_{REF} or I/O option only in the XCV1600E, 2000E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV2000E; otherwise, I/O option only.

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
NA	GND	AG27
NA	GND	D27
NA	GND	AF26
NA	GND	E26
NA	GND	F25
NA	GND	AE25
NA	GND	G24
NA	GND	AJ23
NA	GND	AD24
NA	GND	H23
NA	GND	B23
NA	GND	AC23
NA	GND	AB22
NA	GND	V22
NA	GND	N22
NA	GND	AH18
NA	GND	AB18
NA	GND	J18
NA	GND	C18
NA	GND	U17
NA	GND	T17
NA	GND	R17
NA	GND	P17
NA	GND	U16
NA	GND	T16
NA	GND	R16
NA	GND	P16
NA	GND	U15
NA	GND	T15
NA	GND	R15
NA	GND	P15
NA	GND	U14
NA	GND	T14
NA	GND	R14
NA	GND	P14
NA	GND	AH13
NA	GND	AB13

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
NA	GND	J13
NA	GND	C13
NA	GND	V9
NA	GND	N9
NA	GND	J9
NA	GND	AJ8
NA	GND	AC8
NA	GND	H8
NA	GND	AD7
NA	GND	B8
NA	GND	AE6
NA	GND	G7
NA	GND	F6
NA	GND	AF5
NA	GND	E5
NA	GND	AG4
NA	GND	D4
NA	GND	V3
NA	GND	N3
NA	GND	C3
NA	GND	AK2
NA	GND	AH3
NA	GND	AC2
NA	GND	H2
NA	GND	B2
NA	GND	A2
NA	GND	AK1
NA	GND	AJ2
NA	GND	AJ1
NA	GND	A1
NA	GND	B1

Notes:

1. V_{REF} or I/O option only in the XCV1000E and XCV1600E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV1600E; otherwise, I/O option only.
3. I/O option only in the XCV600E.
4. No Connect in the XCV600E.
5. No Connect in the XCV600E, 1000E.

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
6	IO_VREF_L265N_Y	AJ3
6	IO_L265P_Y	AG5
6	IO_L266N_YY	AD9[4]
6	IO_L266P_YY	AJ2[5]
6	IO_L267N_YY	AC10
6	IO_L267P_YY	AH2
6	IO_L268N_Y	AH3
6	IO_L268P_Y	AF5
6	IO_L269N_Y	AE8[4]
6	IO_L269P_Y	AG3[5]
6	IO_L270N_Y	AE7
6	IO_L270P_Y	AG2
6	IO_VREF_L271N_YY	AF6
6	IO_L271P_YY	AG1
6	IO_L272N_YY	AC9[4]
6	IO_L272P_YY	AG4[5]
6	IO_L273N_YY	AE6
6	IO_L273P_YY	AF3
6	IO_VREF_L274N_Y	AF1[2]
6	IO_L274P_Y	AF4
6	IO_L275N	AB10[4]
6	IO_L275P	AF2[5]
6	IO_L276N_Y	AC8
6	IO_L276P_Y	AE1
6	IO_VREF_L277N_YY	AD5
6	IO_L277P_YY	AE3
6	IO_L278N_YY	AC7
6	IO_L278P_YY	AD1
6	IO_L279N_Y	AD6
6	IO_L279P_Y	AD2
6	IO_VREF_L280N_YY	AB8
6	IO_L280P_YY	AC1
6	IO_L281N_YY	AC5
6	IO_L281P_YY	AC2

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
6	IO_L282N_Y	AA9
6	IO_L282P_Y	AC3
6	IO_L283N_Y	AC4
6	IO_L283P_Y	AD4
6	IO_L284N_Y	AA8
6	IO_L284P_Y	AB6
6	IO_L285N	AB1
6	IO_L285P	Y10
6	IO_L286N_Y	AB2
6	IO_L286P_Y	AA7
6	IO_VREF_L287N_Y	AA4
6	IO_L287P_Y	AA1
6	IO_L288N_YY	Y9[4]
6	IO_L288P_YY	AB4[5]
6	IO_L289N_YY	AA2
6	IO_L289P_YY	Y8
6	IO_L290N_Y	AA6
6	IO_L290P_Y	AA5
6	IO_L291N_Y	AB3[4]
6	IO_L291P_Y	Y7[5]
6	IO_L292N_Y	Y1
6	IO_L292P_Y	W10
6	IO_VREF_L293N_YY	Y5
6	IO_L293P_YY	Y2
6	IO_L294N_YY	W9[4]
6	IO_L294P_YY	W2[5]
6	IO_L295N_YY	W7
6	IO_L295P_YY	Y4
6	IO_L296N_Y	W1
6	IO_L296P_Y	Y6
6	IO_L297N_Y	W6[4]
6	IO_L297P_Y	W3[5]
6	IO_L298N_Y	V9
6	IO_L298P_Y	W4

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
NA	VCCO_7	K5
NA	VCCO_7	F1
NA	VCCO_7	T11
NA	VCCO_7	T12
NA	VCCO_7	R11
NA	VCCO_7	R12
NA	VCCO_7	P3
NA	VCCO_7	P11
NA	VCCO_7	P12
NA	VCCO_7	N11
NA	GND	K32
NA	GND	R4
NA	GND	AN1
NA	GND	AM11
NA	GND	AK5
NA	GND	AH28
NA	GND	AD32
NA	GND	AA20
NA	GND	Y20
NA	GND	W19
NA	GND	V19
NA	GND	U20
NA	GND	T20
NA	GND	R19
NA	GND	P19
NA	GND	H8
NA	GND	F12
NA	GND	C2
NA	GND	B1
NA	GND	A7
NA	GND	AP1
NA	GND	AN2
NA	GND	AM15

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
NA	GND	AK17
NA	GND	AH34
NA	GND	AC6
NA	GND	AA21
NA	GND	Y21
NA	GND	W20
NA	GND	V20
NA	GND	U21
NA	GND	T21
NA	GND	R20
NA	GND	P20
NA	GND	H16
NA	GND	F23
NA	GND	C3
NA	GND	B2
NA	GND	A28
NA	GND	AP34
NA	GND	AM3
NA	GND	AL31
NA	GND	AH7
NA	GND	AD3
NA	GND	AA19
NA	GND	Y19
NA	GND	W18
NA	GND	V18
NA	GND	U19
NA	GND	T19
NA	GND	R18
NA	GND	P18
NA	GND	J26
NA	GND	F6
NA	GND	C1
NA	GND	C34
NA	GND	A3

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
71	1	A27	G24	3200 2000 1000	-
72	1	G25	B27	3200 1600	-
73	1	C27	E26	3200 2600 2000 1600 1000	VREF
74	1	B28	J24	3200 2600 2000 1600 1000	-
75	1	H25	K24	3200 2600	-
76	1	F26	D27	3200 1000	-
77	1	C28	G26	3200 1000	-
78	1	J25	E27	2000 1600	-
79	1	H26	A30	3200 2600 2000 1600 1000	VREF
80	1	B29	G27	3200 2600 2000 1600 1000	-
81	1	C29	F27	3200 2600 1000	-
82	1	F28	E28	3200 2000 1000	VREF
83	1	B30	L25	3200 2000 1000	-
84	1	E29	B31	3200 1600 1000	-
85	1	D30	A31	3200 2600 2000 1600 1000	CS
86	2	D32	J27	3200 2600 2000 1600 1000	DIN, D0
87	2	E31	F30	3200 2600 2000	-
88	2	G29	F32	2600 2000 1000	-
89	2	E32	G30	3200 2600 1600 1000	VREF
90	2	M25	G31	2600 1600	-

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
91	2	L26	D33	3200 2600 1600 1000	-
92	2	D34	H29	2600 2000 1000	VREF
93	2	J28	E33	3200 2600 2000 1600	-
94	2	H28	H30	3200 2600 2000 1600 1000	-
95	2	H32	K28	3200 2600 1600 1000	-
96	2	L27	F33	3200 2600 2000	-
97	2	M26	E34	2600 2000 1000	-
98	2	H31	G32	3200 2600 2000 1600 1000	VREF
99	2	N25	J31	2000 1600	-
100	2	J30	G33	3200 2600 2000 1600 1000	-
101	2	H34	J29	2600 1000	VREF
102	2	M27	H33	3200 2600 1600	-
103	2	K29	J34	3200 2600 1600 1000	-
104	2	L29	J33	3200 2600 2000 1600 1000	VREF
105	2	M28	K34	3200 2600 2000 1600 1000	-
106	2	N27	L34	3200 1600 1000	-
107	2	K33	P26	2000 1600 1000	D1
108	2	R25	M34	3200 2600 2000	-
109	2	L31	L33	2000 1000	-
110	2	P27	M33	3200 2600 1600 1000	-

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
231	5	AH14	AP12	3200 2600 2000 1600 1000	-
232	5	AJ14	AL14	3200 2600 1000	-
233	5	AF13	AN12	3200 2000 1000	-
234	5	AF14	AP11	3200 2000 1000	-
235	5	AN11	AH13	3200 1600 1000	-
236	5	AM12	AL12	3200 2600 2000 1600 1000	-
237	5	AJ13	AP10	3200 2600 2000 1600 1000	VREF
238	5	AK12	AM10	2600 1600 1000	-
239	5	AP9	AK11	2600 1600 1000	-
240	5	AL11	AL10	3200 2600 2000 1600 1000	VREF
241	5	AE13	AM9	3200 2600 2000 1600 1000	-
242	5	AF12	AP8	3200 2600	-
243	5	AL9	AH11	3200 2000 1000	VREF
244	5	AF11	AN8	3200 2000 1000	-
245	5	AM8	AG11	3200 1600	-
246	5	AL8	AK9	3200 2600 2000 1600 1000	VREF
247	5	AH10	AN7	3200 2600 2000 1600 1000	-
248	5	AE12	AJ9	3200 2600	-
249	5	AM7	AL7	3200 1000	-
250	5	AG10	AN6	3200 1000	-

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
251	5	AK8	AH9	2000 1600	-
252	5	AP5	AJ8	3200 2600 2000 1600 1000	VREF
253	5	AE11	AN5	3200 2600 2000 1600 1000	-
254	5	AF10	AM6	3200 2600 1000	-
255	5	AL6	AG9	3200 2000 1000	VREF
256	5	AH8	AP4	3200 2000 1000	-
257	5	AN4	AJ7	3200 1600 1000	-
258	5	AM5	AK6	3200 2600 2000 1600 1000	-
259	6	AF8	AH6	3200 2600 2000 1600 1000	-
260	6	AK3	AE9	3200 2600 2000	-
261	6	AL2	AD10	2600 2000 1000	-
262	6	AH4	AL1	3200 2600 1600 1000	VREF
263	6	AK1	AG6	2600 1600	-
264	6	AK2	AF7	3200 2600 1600 1000	-
265	6	AG5	AJ3	2600 2000 1000	VREF
266	6	AJ2	AD9	3200 2600 2000 1600	-
267	6	AH2	AC10	3200 2600 2000 1600 1000	-
268	6	AF5	AH3	3200 2600 1600 1000	-
269	6	AG3	AE8	3200 2600 2000	-