# AMD Xilinx - XCV1600E-8FG680C Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 7776 |
| Number of Logic Elements/Cells | 34992 |
| Total RAM Bits | 589824 |
| Number of I/O | 512 |
| Number of Gates | 2188742 |
| Voltage - Supply | 1.71V ~ 1.89V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 680-LBGA Exposed Pad |
| Supplier Device Package | 680-FTEBGA (40x40) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xcv1600e-8fg680c |

Email: info@E-XFL.COM Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

# Virtex™-E 1.8 V Field Programmable Gate Arrays

DS022-2 (v2.8) January 16, 2006

**Production Product Specification**

## Architectural Description

### Virtex-E Array

The Virtex-E user-programmable gate array, shown in Figure 1, comprises two major configurable elements: configurable logic blocks (CLBs) and input/output blocks (IOBs).

- CLBs provide the functional elements for constructing logic
- IOBs provide the interface between the package pins and the CLBs

CLBs interconnect through a general routing matrix (GRM). The GRM comprises an array of routing switches located at the intersections of horizontal and vertical routing channels. Each CLB nests into a VersaBlock™ that also provides local routing resources to connect the CLB to the GRM.

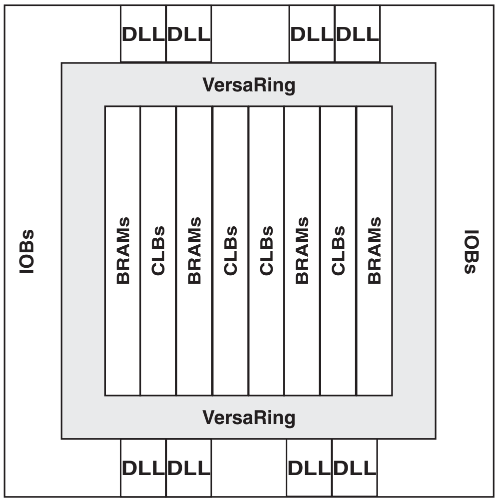

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*Figure 1:* **Virtex-E Architecture Overview**

The VersaRing™ I/O interface provides additional routing resources around the periphery of the device. This routing improves I/O routability and facilitates pin locking.

The Virtex-E architecture also includes the following circuits that connect to the GRM.

- Dedicated block memories of 4096 bits each
- Clock DLLs for clock-distribution delay compensation and clock domain control
- 3-State buffers (BUFTs) associated with each CLB that drive dedicated segmentable horizontal routing resources

Values stored in static memory cells control the configurable logic elements and interconnect resources. These values load into the memory cells on power-up, and can reload if necessary to change the function of the device.

### Input/Output Block

The Virtex-E IOB, Figure 2, features SelectI/O+ inputs and outputs that support a wide variety of I/O signalling standards, see Table 1.

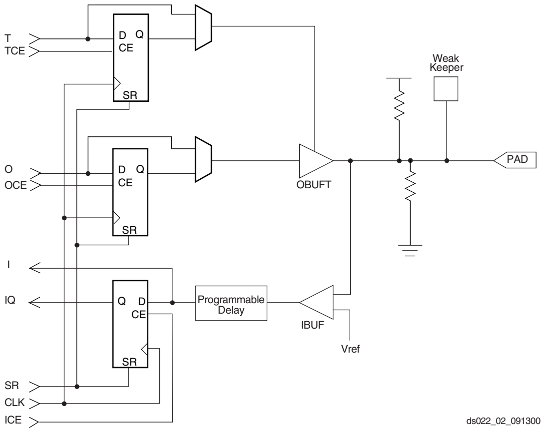

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*Figure 2:* **Virtex-E Input/Output Block (IOB)**

The three IOB storage elements function either as edge-triggered D-type flip-flops or as level-sensitive latches. Each IOB has a clock signal (CLK) shared by the three flip-flops and independent clock enable signals for each flip-flop.

For in-circuit debugging, an optional download and read-back cable is available. This cable connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can single-step the logic, readback the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.

## Configuration

Virtex-E devices are configured by loading configuration data into the internal configuration memory. Note that attempting to load an incorrect bitstream causes configuration to fail and can damage the device.

Some of the pins used for configuration are dedicated pins, while others can be re-used as general purpose inputs and outputs once configuration is complete.

The following are dedicated pins:

- Mode pins (M2, M1, M0)
- Configuration clock pin (CCLK)
- $\overline{\text{PROGRAM}}$ pin
- DONE pin
- Boundary Scan pins (TDI, TDO, TMS, TCK)

Depending on the configuration mode chosen, CCLK can be an output generated by the FPGA, or can be generated externally and provided to the FPGA as an input. The $\overline{\text{PROGRAM}}$ pin must be pulled High prior to reconfiguration.

Note that some configuration pins can act as outputs. For correct operation, these pins require a $V_{CCO}$ of 3.3 V or 2.5 V. At 3.3 V the pins operate as LVTTL, and at 2.5 V they operate as LVCMOS. All affected pins fall in banks 2 or 3. The configuration pins needed for SelectMap (CS, Write) are located in bank 1.

### Configuration Modes

Virtex-E supports the following four configuration modes.

- Slave-serial mode
- Master-serial mode
- SelectMAP mode
- Boundary Scan mode (JTAG)

The Configuration mode pins (M2, M1, M0) select among these configuration modes with the option in each case of having the IOB pins either pulled up or left floating prior to configuration. The selection codes are listed in Table 8.

Configuration through the Boundary Scan port is always available, independent of the mode selection. Selecting the Boundary Scan mode simply turns off the other modes. The three mode pins have internal pull-up resistors, and default to a logic High if left unconnected. However, it is recommended to drive the configuration mode pins externally.

*Table 8:* **Configuration Codes**

| Configuration Mode | M2[(1)] | M1 | M0 | CCLK Direction | Data Width | Serial $D_{out}$ | Configuration Pull-ups[(1)] |
|---|---|---|---|---|---|---|---|
| Master-serial mode | 0 | 0 | 0 | Out | 1 | Yes | No |
| Boundary Scan mode | 1 | 0 | 1 | N/A | 1 | No | No |
| SelectMAP mode | 1 | 1 | 0 | In | 8 | No | No |
| Slave-serial mode | 1 | 1 | 1 | In | 1 | Yes | No |
| Master-serial mode | 1 | 0 | 0 | Out | 1 | Yes | Yes |
| Boundary Scan mode | 0 | 0 | 1 | N/A | 1 | No | Yes |
| SelectMAP mode | 0 | 1 | 0 | In | 8 | No | Yes |
| Slave-serial mode | 0 | 1 | 1 | In | 1 | Yes | Yes |

**Notes:**

1. M2 is sampled continuously from power up until the end of the configuration. Toggling M2 while INIT is being held externally Low can cause the configuration pull-up settings to change.

Table 9 lists the total number of bits required to configure each device.

*Table 9:* **Virtex-E Bitstream Lengths**

| Device | # of Configuration Bits |
|---|---|
| XCV50E | 630,048 |
| XCV100E | 863,840 |
| XCV200E | 1,442,016 |
| XCV300E | 1, 875,648 |
| XCV400E | 2,693,440 |
| XCV600E | 3,961,632 |
| XCV1000E | 6,587,520 |
| XCV1600E | 8,308,992 |
| XCV2000E | 10,159,648 |
| XCV2600E | 12,922,336 |
| XCV3200E | 16,283,712 |

## *Slave-Serial Mode*

In slave-serial mode, the FPGA receives configuration data in bit-serial form from a serial PROM or other source of serial configuration data. The serial bitstream must be set up at the DIN input pin a short time before each rising edge of an externally generated CCLK.

For more detailed information on serial PROMs, see the PROM data sheet at http://www.xilinx.com/bvdocs/publications/ds026.pdf.

Multiple FPGAs can be daisy-chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed to the DOUT pin. The maximum capacity for a single LOUT/DOUT write is $2^{20}$-1 (1,048,575) 32-bit words, or 33,554,4000 bits. The data on the DOUT pin changes on the rising edge of CCLK.

The change of DOUT on the rising edge of CCLK differs from previous families, but does not cause a problem for mixed configuration chains. This change was made to improve serial configuration rates for Virtex and Virtex-E only chains.

Figure 13 shows a full master/slave system. A Virtex-E device in slave-serial mode should be connected as shown in the right-most device.

Slave-serial mode is selected by applying <111> or <011> to the mode pins (M2, M1, M0). A weak pull-up on the mode pins makes slave serial the default mode if the pins are left unconnected. However, it is recommended to drive the configuration mode pins externally. Figure 14 shows slave-serial mode programming switching characteristics.

Table 10 provides more detail about the characteristics shown in Figure 14. Configuration must be delayed until the $\overline{\text{INIT}}$ pins of all daisy-chained FPGAs are High.

*Table 10:* **Master/Slave Serial Mode Programming Switching**

| | Description | Figure References | Symbol | Values | Units |
|---|---|---|---|---|---|
| CCLK | DIN setup/hold, slave mode | 1/2 | $T_{DCC}/T_{CCD}$ | 5.0 / 0.0 | ns, min |
| | DIN setup/hold, master mode | 1/2 | $T_{DSCK}/T_{CKDS}$ | 5.0 / 0.0 | ns, min |
| | DOUT | 3 | $T_{CCO}$ | 12.0 | ns, max |
| | High time | 4 | $T_{CCH}$ | 5.0 | ns, min |
| | Low time | 5 | $T_{CCL}$ | 5.0 | ns, min |
| | Maximum Frequency | | $F_{CC}$ | 66 | MHz, max |
| | Frequency Tolerance, master mode with respect to nominal | | | +45% –30% | |

Input termination techniques include the following.

- None
- Parallel (Shunt)

These termination techniques can be applied in any combination. A generic example of each combination of termination methods appears in Figure 43.

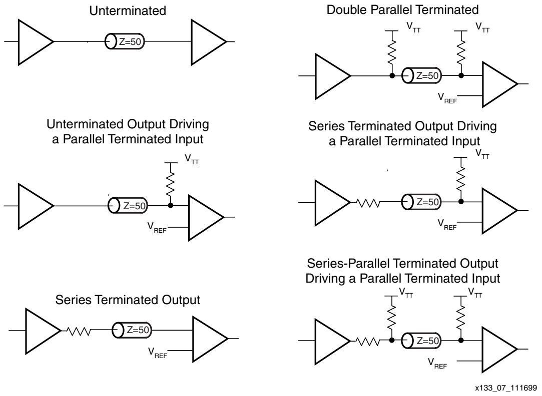

*Figure 43:* **Overview of Standard Input and Output Termination Methods**

## *Simultaneous Switching Guidelines*

Ground bounce can occur with high-speed digital ICs when multiple outputs change states simultaneously, causing undesired transient behavior on an output, or in the internal logic. This problem is also referred to as the Simultaneous Switching Output (SSO) problem.

Ground bounce is primarily due to current changes in the combined inductance of ground pins, bond wires, and ground metallization. The IC internal ground level deviates from the external system ground level for a short duration (a few nanoseconds) after multiple outputs change state simultaneously.

Ground bounce affects stable Low outputs and all inputs because they interpret the incoming signal by comparing it to the internal ground. If the ground bounce amplitude exceeds the actual instantaneous noise margin, then a non-changing input can be interpreted as a short pulse with a polarity opposite to the ground bounce.

Table 21 provides guidelines for the maximum number of simultaneously switching outputs allowed per output power/ground pair to avoid the effects of ground bounce. See Table 22 for the number of effective output power/ground pairs for each Virtex-E device and package combination.

*Table 21:* **Guidelines for Max Number of Simultaneously Switching Outputs per Power/Ground Pair**

| Standard | Package | | |
|---|---|---|---|
| | **BGA, CS, FGA** | **HQ** | **PQ, TQ** |
| LVTTL Slow Slew Rate, 2 mA drive | 68 | 49 | 36 |
| LVTTL Slow Slew Rate, 4 mA drive | 41 | 31 | 20 |
| LVTTL Slow Slew Rate, 6 mA drive | 29 | 22 | 15 |
| LVTTL Slow Slew Rate, 8 mA drive | 22 | 17 | 12 |
| LVTTL Slow Slew Rate, 12 mA drive | 17 | 12 | 9 |
| LVTTL Slow Slew Rate, 16 mA drive | 14 | 10 | 7 |
| LVTTL Slow Slew Rate, 24 mA drive | 9 | 7 | 5 |
| LVTTL Fast Slew Rate, 2 mA drive | 40 | 29 | 21 |
| LVTTL Fast Slew Rate, 4 mA drive | 24 | 18 | 12 |
| LVTTL Fast Slew Rate, 6 mA drive | 17 | 13 | 9 |
| LVTTL Fast Slew Rate, 8 mA drive | 13 | 10 | 7 |
| LVTTL Fast Slew Rate, 12 mA drive | 10 | 7 | 5 |
| LVTTL Fast Slew Rate, 16 mA drive | 8 | 6 | 4 |
| LVTTL Fast Slew Rate, 24 mA drive | 5 | 4 | 3 |
| LVCMOS | 10 | 7 | 5 |
| PCI | 8 | 6 | 4 |
| GTL | 4 | 4 | 4 |
| GTL+ | 4 | 4 | 4 |

*Table 44:* **Bidirectional I/O Library Macros**

| Name | Inputs | Bidirectional | Outputs |
|---|---|---|---|
| IOBUFDS_FD_LVDS | D, T, C | IO, IOB | Q |
| IOBUFDS_FDE_LVDS | D, T, CE, C | IO, IOB | Q |
| IOBUFDS_FDC_LVDS | D, T, C, CLR | IO, IOB | Q |
| IOBUFDS_FDCE_LVDS | D, T, CE, C, CLR | IO, IOB | Q |
| IOBUFDS_FDP_LVDS | D, T, C, PRE | IO, IOB | Q |
| IOBUFDS_FDPE_LVDS | D, T, CE, C, PRE | IO, IOB | Q |
| IOBUFDS_FDR_LVDS | D, T, C, R | IO, IOB | Q |
| IOBUFDS_FDRE_LVDS | D, T, CE, C, R | IO, IOB | Q |
| IOBUFDS_FDS_LVDS | D, T, C, S | IO, IOB | Q |
| IOBUFDS_FDSE_LVDS | D, T, CE, C, S | IO, IOB | Q |
| IOBUFDS_LD_LVDS | D, T, G | IO, IOB | Q |
| IOBUFDS_LDE_LVDS | D, T, GE, G | IO, IOB | Q |
| IOBUFDS_LDC_LVDS | D, T, G, CLR | IO, IOB | Q |
| IOBUFDS_LDCE_LVDS | D, T, GE, G, CLR | IO, IOB | Q |
| IOBUFDS_LDP_LVDS | D, T, G, PRE | IO, IOB | Q |
| IOBUFDS_LDPE_LVDS | D, T, GE, G, PRE | IO, IOB | Q |

## Revision History

The following table shows the revision history for this document.

| Date | Version | Revision |
|---|---|---|
| 12/7/99 | 1.0 | Initial Xilinx release. |
| 1/10/00 | 1.1 | Re-released with spd.txt v. 1.18, FG860/900/1156 package information, and additional DLL, Select RAM and SelectI/O information. |
| 1/28/00 | 1.2 | Added Delay Measurement Methodology table, updated SelectI/O section, Figures 30, 54, & 55, text explaining Table 5, $T_{BYP}$ values, buffered Hex Line info, p. 8, I/O Timing Measurement notes, notes for Tables 15, 16, and corrected F1156 pinout table footnote references. |
| 2/29/00 | 1.3 | Updated pinout tables, $V_{CC}$ page 20, and corrected Figure 20. |
| 5/23/00 | 1.4 | Correction to table on p. 22. |
| 7/10/00 | 1.5 | • Numerous minor edits.<br>• Data sheet upgraded to Preliminary.<br>• Preview -8 numbers added to **Virtex-E Electrical Characteristics** tables. |
| 8/1/00 | 1.6 | • Reformatted entire document to follow new style guidelines.<br>• Changed speed grade values in tables on pages 35-37. |

## Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply. This is the time required to reach the nominal power supply voltage of the device[1] from 0V. The fastest ramp rate is 0V to nominal voltage in 2 ms, and the slowest allowed ramp rate is 0V to nominal voltage in 50 ms. For more details on power supply requirements, see XAPP158 on www.xilinx.com.

| Product (Commercial Grade) | Description(2) | Current Requirement(3) |
|---|---|---|
| XCV50E - XCV600E | Minimum required current supply | 500 mA |
| XCV812E - XCV2000E | Minimum required current supply | 1 A |
| XCV2600E - XCV3200E | Minimum required current supply | 1.2 A |
| Virtex-E Family, Industrial Grade | Minimum required current supply | 2 A |

**Notes:**

1. Ramp rate used for this specification is from 0 - 1.8 V DC. Peak current occurs on or near the internal power-on reset threshold and lasts for less than 3 ms.
2. Devices are guaranteed to initialize properly with the minimum current available from the power supply as noted above.
3. Larger currents might result if ramp rates are forced to be faster.

## DC Input and Output Levels

Values for $V_{IL}$ and $V_{IH}$ are recommended input voltages. Values for $I_{OL}$ and $I_{OH}$ are guaranteed over the recommended operating conditions at the $V_{OL}$ and $V_{OH}$ test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum $V_{CCO}$ with the respective $V_{OL}$ and $V_{OH}$ voltage levels shown. Other standards are sample tested.

| Input/Output Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| LVTTL(1) | – 0.5 | 0.8 | 2.0 | 3.6 | 0.4 | 2.4 | 24 | – 24 |
| LVCMOS2 | – 0.5 | 0.7 | 1.7 | 2.7 | 0.4 | 1.9 | 12 | – 12 |
| LVCMOS18 | – 0.5 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | 1.95 | 0.4 | $V_{CCO}$ – 0.4 | 8 | – 8 |
| PCI, 3.3 V | – 0.5 | 30% $V_{CCO}$ | 50% $V_{CCO}$ | $V_{CCO}$ + 0.5 | 10% $V_{CCO}$ | 90% $V_{CCO}$ | Note 2 | Note 2 |
| GTL | – 0.5 | $V_{REF}$ – 0.05 | $V_{REF}$ + 0.05 | 3.6 | 0.4 | n/a | 40 | n/a |
| GTL+ | – 0.5 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.6 | n/a | 36 | n/a |
| HSTL I(3) | – 0.5 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.4 | $V_{CCO}$ – 0.4 | 8 | –8 |
| HSTL III | – 0.5 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.4 | $V_{CCO}$ – 0.4 | 24 | –8 |
| HSTL IV | – 0.5 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.4 | $V_{CCO}$ – 0.4 | 48 | –8 |
| SSTL3 I | – 0.5 | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 3.6 | $V_{REF}$ – 0.6 | $V_{REF}$ + 0.6 | 8 | –8 |
| SSTL3 II | – 0.5 | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 3.6 | $V_{REF}$ – 0.8 | $V_{REF}$ + 0.8 | 16 | –16 |
| SSTL2 I | – 0.5 | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 3.6 | $V_{REF}$ – 0.61 | $V_{REF}$ + 0.61 | 7.6 | –7.6 |
| SSTL2 II | – 0.5 | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 3.6 | $V_{REF}$ – 0.80 | $V_{REF}$ + 0.80 | 15.2 | –15.2 |

## Calculation of $T_{ioop}$ as a Function of Capacitance

$T_{ioop}$ is the propagation delay from the O Input of the IOB to the pad. The values for $T_{ioop}$ are based on the standard capacitive load ($C_{sl}$) for each I/O standard as listed in Table 3.

*Table 3:* **Constants for Use in Calculation of $T_{ioop}$**

| Standard | Csl (pF) | fl (ns/pF) |
|---|---|---|
| LVTTL Fast Slew Rate, 2mA drive | 35 | 0.41 |
| LVTTL Fast Slew Rate, 4mA drive | 35 | 0.20 |
| LVTTL Fast Slew Rate, 6mA drive | 35 | 0.13 |
| LVTTL Fast Slew Rate, 8mA drive | 35 | 0.079 |
| LVTTL Fast Slew Rate, 12mA drive | 35 | 0.044 |
| LVTTL Fast Slew Rate, 16mA drive | 35 | 0.043 |
| LVTTL Fast Slew Rate, 24mA drive | 35 | 0.033 |
| LVTTL Slow Slew Rate, 2mA drive | 35 | 0.41 |
| LVTTL Slow Slew Rate, 4mA drive | 35 | 0.20 |
| LVTTL Slow Slew Rate, 6mA drive | 35 | 0.10 |
| LVTTL Slow Slew Rate, 8mA drive | 35 | 0.086 |
| LVTTL Slow Slew Rate, 12mA drive | 35 | 0.058 |
| LVTTL Slow Slew Rate, 16mA drive | 35 | 0.050 |
| LVTTL Slow Slew Rate, 24mA drive | 35 | 0.048 |
| LVCMOS2 | 35 | 0.041 |
| LVCMOS18 | 35 | 0.050 |
| PCI 33 MHZ 3.3 V | 10 | 0.050 |
| PCI 66 MHz 3.3 V | 10 | 0.033 |
| GTL | 0 | 0.014 |
| GTL+ | 0 | 0.017 |
| HSTL Class I | 20 | 0.022 |
| HSTL Class III | 20 | 0.016 |
| HSTL Class IV | 20 | 0.014 |
| SSTL2 Class I | 30 | 0.028 |
| SSTL2 Class II | 30 | 0.016 |
| SSTL3 Class I | 30 | 0.029 |
| SSTL3 Class II | 30 | 0.016 |
| CTT | 20 | 0.035 |
| AGP | 10 | 0.037 |

**Notes:**
1. I/O parameter measurements are made with the capacitance values shown above. See the application examples (in Module 2 of this data sheet) for appropriate terminations.
2. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

For other capacitive loads, use the formulas below to calculate the corresponding $T_{ioop}$:

$$T_{ioop} = T_{ioop} + T_{opadjust} + (C_{load} - C_{sl}) * fl$$

where:

$T_{opadjust}$ is reported above in the Output Delay Adjustment section.

$C_{load}$ is the capacitive load for the design.

*Table 4:* **Delay Measurement Methodology**

| Standard | $V_L$[1] | $V_H$[1] | Meas. Point | $V_{REF}$ (Typ)[2] |
|---|---|---|---|---|
| LVTTL | 0 | 3 | 1.4 | - |
| LVCMOS2 | 0 | 2.5 | 1.125 | - |
| PCI33_3 | Per PCI Spec | | | - |
| PCI66_3 | Per PCI Spec | | | - |
| GTL | $V_{REF}$ –0.2 | $V_{REF}$ +0.2 | $V_{REF}$ | 0.80 |
| GTL+ | $V_{REF}$ –0.2 | $V_{REF}$ +0.2 | $V_{REF}$ | 1.0 |
| HSTL Class I | $V_{REF}$ –0.5 | $V_{REF}$ +0.5 | $V_{REF}$ | 0.75 |
| HSTL Class III | $V_{REF}$ –0.5 | $V_{REF}$ +0.5 | $V_{REF}$ | 0.90 |
| HSTL Class IV | $V_{REF}$ –0.5 | $V_{REF}$ +0.5 | $V_{REF}$ | 0.90 |
| SSTL3 I & II | $V_{REF}$ –1.0 | $V_{REF}$ +1.0 | $V_{REF}$ | 1.5 |
| SSTL2 I & II | $V_{REF}$ –0.75 | $V_{REF}$ +0.75 | $V_{REF}$ | 1.25 |
| CTT | $V_{REF}$ –0.2 | $V_{REF}$ +0.2 | $V_{REF}$ | 1.5 |
| AGP | $V_{REF}$ – ($0.2xV_{CCO}$) | $V_{REF}$ + ($0.2xV_{CCO}$) | $V_{REF}$ | Per AGP Spec |
| LVDS | 1.2 –0.125 | 1.2 + 0.125 | 1.2 | |
| LVPECL | 1.6 –0.3 | 1.6 + 0.3 | 1.6 | |

**Notes:**
1. Input waveform switches between $V_L$ and $V_H$.
2. Measurements are made at $V_{REF}$ (Typ), Maximum, and Minimum. Worst-case values are reported.

   I/O parameter measurements are made with the capacitance values shown in Table 3. See the application examples (in Module 2 of this data sheet) for appropriate terminations.

   I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

| Date | Version | Revision |
|---|---|---|
| 07/23/01 | 2.2 | - Under **Absolute Maximum Ratings**, changed ($T_{SOL}$) to 220 °C.<br>- Changes made to SSTL symbol names in **IOB Input Switching Characteristics Standard Adjustments** table. |
| 07/26/01 | 2.3 | - Removed $T_{SOL}$ parameter and added footnote to **Absolute Maximum Ratings** table. |
| 9/18/01 | 2.4 | - Reworded power supplies footnote to **Absolute Maximum Ratings** table. |
| 10/25/01 | 2.5 | - Updated the speed grade designations used in data sheets, and added Table 1, which shows the current speed grade designation for each device.<br>- Added XCV2600E and XCV3200E values to **DC Characteristics Over Recommended Operating Conditions** and **Power-On Power Supply Requirements** tables. |
| 11/09/01 | 2.6 | - Updated the **Power-On Power Supply Requirements** table. |
| 02/01/02 | 2.7 | - Updated footnotes to the **DC Input and Output Levels** and **DLL Clock Tolerance, Jitter, and Phase Information** tables. |
| 07/17/02 | 2.8 | - Data sheet designation upgraded from Preliminary to Production.<br>- Removed mention of MIL-M-38510/605 specification.<br>- Added link to XAPP158 from the **Power-On Power Supply Requirements** section. |
| 09/10/02 | 2.9 | - Revised $V_{IN}$ in **Absolute Maximum Ratings** table.<br>- Added Clock CLK switching characteristics to Table **2, "IOB Input Switching Characteristics," on page 6** and **IOB Output Switching Characteristics, Figure 1**. |
| 12/22/02 | 2.9.1 | - Added footnote regarding $V_{IN}$ PCI compliance to **Absolute Maximum Ratings** table.<br>- The fastest ramp rate is 0V to nominal voltage in 2 ms |
| 03/14/03 | 2.9.2 | - Under **Power-On Power Supply Requirements**, the fastest ramp rate is no longer a "suggested" rate. |

## Virtex-E Data Sheet

The Virtex-E Data Sheet contains the following modules:

- DS022-1, Virtex-E 1.8V FPGAs: **Introduction and Ordering Information (Module 1)**
- DS022-2, Virtex-E 1.8V FPGAs: **Functional Description (Module 2)**
- DS022-3, Virtex-E 1.8V FPGAs: **DC and Switching Characteristics (Module 3)**
- DS022-4, Virtex-E 1.8V FPGAs: **Pinout Tables (Module 4)**

*Table 4:* **CS144 — XCV50E, XCV100E, XCV200E**

| Bank | Pin Description | Pin # |
|---|---|---|
| 1 | VCCO | A13 |
| 1 | VCCO | D7 |
| 2 | VCCO | B12 |
| 3 | VCCO | G11 |
| 3 | VCCO | M13 |
| 4 | VCCO | N13 |
| 5 | VCCO | N1 |
| 5 | VCCO | N7 |
| 6 | VCCO | M2 |
| 7 | VCCO | B2 |
| 7 | VCCO | G2 |
| | | |
| NA | GND | A1 |
| NA | GND | B9 |
| NA | GND | B11 |
| NA | GND | C7 |
| NA | GND | D5 |
| NA | GND | E4 |
| NA | GND | E11 |
| NA | GND | F1 |
| NA | GND | G10 |
| NA | GND | J1 |
| NA | GND | J12 |
| NA | GND | L3 |
| NA | GND | L5 |
| NA | GND | L7 |
| NA | GND | L9 |
| NA | GND | N12 |

**Notes:**

1. $V_{REF}$ or I/O option only in the XCV200E; otherwise, I/O option only.
2. $V_{REF}$ or I/O option only in the XCV100E, 200E; otherwise, I/O option only.

## CS144 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

*Table 5:* **CS144 Differential Pin Pair Summary XCV50E, XCV100E, XCV200E**

| Pair | Bank | P Pin | N Pin | AO | Other Functions |
|---|---|---|---|---|---|
| Global Differential Clock | | | | | |
| 0 | 4 | K7 | N8 | NA | IO_DLL_L18P |
| 1 | 5 | M7 | M6 | NA | IO_DLL_L18N |
| 2 | 1 | A7 | B7 | NA | IO_DLL_L2P |
| 3 | 0 | A6 | C6 | NA | IO_DLL_L2N |
| IO LVDS<br>Total Pairs: 30, Asynchronous Output Pairs: 18 | | | | | |
| 0 | 0 | A4 | B4 | √ | VREF |
| 1 | 0 | A5 | B5 | √ | - |
| 2 | 1 | B7 | C6 | NA | IO_LVDS_DLL |
| 3 | 1 | D8 | C8 | √ | - |
| 4 | 1 | D9 | C9 | √ | VREF |
| 5 | 1 | D10 | C10 | √ | CS, WRITE |
| 6 | 2 | C11 | C12 | √ | DIN, D0 |
| 7 | 2 | D13 | E10 | 1 | D1, VREF |
| 8 | 2 | E12 | E13 | √ | D2 |
| 9 | 2 | F10 | F11 | 1 | D3, VREF |
| 10 | 3 | F13 | G13 | NA | - |
| 11 | 3 | H12 | H11 | 1 | D4, VREF |
| 12 | 3 | H10 | J13 | √ | D5 |
| 13 | 3 | J11 | J10 | 1 | D6, VREF |
| 14 | 3 | K10 | L13 | √ | INIT |
| 15 | 4 | L11 | M11 | √ | - |
| 16 | 4 | N10 | K9 | √ | VREF |
| 17 | 4 | N9 | K8 | √ | - |

*Table 6:* **PQ240 — XCV50E, XCV100E, XCV200E, XCV300E, XCV400E**

| Pin # | Pin Description | Bank |
|---|---|---|
| P137 | VCCINT | NA |
| P104 | VCCINT | NA |
| P88 | VCCINT | NA |
| P77 | VCCINT | NA |
| P43 | VCCINT | NA |
| P32 | VCCINT | NA |
| P16 | VCCINT | NA |
| | | |
| P240 | VCCO | 7 |
| P232 | VCCO | 0 |
| P226 | VCCO | 0 |
| P212 | VCCO | 0 |
| P207 | VCCO | 1 |
| P197 | VCCO | 1 |
| P180 | VCCO | 1 |
| P176 | VCCO | 2 |
| P165 | VCCO | 2 |
| P150 | VCCO | 2 |
| P146 | VCCO | 3 |
| P136 | VCCO | 3 |
| P121 | VCCO | 3 |
| P116 | VCCO | 4 |
| P105 | VCCO | 4 |
| P90 | VCCO | 4 |
| P85 | VCCO | 5 |
| P76 | VCCO | 5 |
| P61 | VCCO | 5 |
| P55 | VCCO | 6 |
| P44 | VCCO | 6 |
| P30 | VCCO | 6 |
| P25 | VCCO | 7 |
| P15 | VCCO | 7 |
| | | |
| P233 | GND | NA |
| P227 | GND | NA |
| P219 | GND | NA |
| P211 | GND | NA |
| P204 | GND | NA |
| P196 | GND | NA |
| P190 | GND | NA |
| P182 | GND | NA |
| P172 | GND | NA |
| P166 | GND | NA |
| P158 | GND | NA |
| P151 | GND | NA |
| P143 | GND | NA |
| P135 | GND | NA |
| P129 | GND | NA |
| P119 | GND | NA |
| P112 | GND | NA |
| P106 | GND | NA |
| P98 | GND | NA |
| P91 | GND | NA |
| P83 | GND | NA |
| P75 | GND | NA |
| P69 | GND | NA |
| P59 | GND | NA |
| P51 | GND | NA |
| P45 | GND | NA |
| P37 | GND | NA |
| P29 | GND | NA |
| P22 | GND | NA |
| P14 | GND | NA |
| P8 | GND | NA |
| P1 | GND | NA |

**Notes:**

1. $V_{REF}$ or I/O option only in the XCV100E, 200E, 300E, 400E; otherwise, I/O option only.
2. $V_{REF}$ or I/O option only in the XCV200E, 300E, 400E; otherwise, I/O option only.
3. $V_{REF}$ or I/O option only in the XCV400E; otherwise, I/O option only.

*Table 12:* **BG432 — XCV300E, XCV400E, XCV600E**

| Bank | Pin Description | Pin # |
|---|---|---|
| 4 | IO_L70N_Y | AK4 |
| 4 | IO_L71P_YY | AJ5 |
| 4 | IO_L71N_YY | AH6 |
| 4 | IO_VREF_L72P_YY | AL4 |
| 4 | IO_L72N_YY | AK5 |
| 4 | IO_L73P_Y | AJ6 |
| 4 | IO_L73N_Y | AH7 |
| 4 | IO_L74P_YY | AL5 |
| 4 | IO_L74N_YY | AK6 |
| 4 | IO_VREF_L75P_YY | AJ7 |
| 4 | IO_L75N_YY | AL6 |
| 4 | IO_L76P_Y | AH9 |
| 4 | IO_L76N_Y | AJ8 |
| 4 | IO_VREF_L77P_Y | AK8[1] |
| 4 | IO_L77N_Y | AJ9 |
| 4 | IO_VREF_L78P_YY | AL8 |
| 4 | IO_L78N_YY | AK9 |
| 4 | IO_L79P_YY | AK10 |
| 4 | IO_L79N_YY | AL10 |
| 4 | IO_L80P_YY | AH12 |
| 4 | IO_L80N_YY | AK11 |
| 4 | IO_L81P_YY | AJ12 |
| 4 | IO_L81N_YY | AK12 |
| 4 | IO_L82P_YY | AH13 |
| 4 | IO_L82N_YY | AJ13 |
| 4 | IO_VREF_L83P_YY | AL13 |
| 4 | IO_L83N_YY | AK14 |
| 4 | IO_L84P_Y | AH14 |
| 4 | IO_L84N_Y | AJ14 |
| 4 | IO_VREF_L85P_Y | AK15[2] |
| 4 | IO_L85N_Y | AJ15 |
| 4 | IO_LVDS_DLL_L86P | AH15 |
| | | |
| 5 | GCK1 | AK16 |
| 5 | IO | AH20 |
| 5 | IO | AJ19 |
| 5 | IO | AJ23 |
| 5 | IO | AJ24 |
| 5 | IO_LVDS_DLL_L86N | AL17 |
| 5 | IO_L87P_Y | AK17 |
| 5 | IO_VREF_L87N_Y | AJ17[2] |
| 5 | IO_L88P_Y | AH17 |
| 5 | IO_L88N_Y | AK18 |
| 5 | IO_L89P_YY | AL19 |
| 5 | IO_VREF_L89N_YY | AJ18 |
| 5 | IO_L90P_YY | AH18 |
| 5 | IO_L90N_YY | AL20 |
| 5 | IO_L91P_YY | AK20 |
| 5 | IO_L91N_YY | AH19 |
| 5 | IO_L92P_YY | AJ20 |
| 5 | IO_L92N_YY | AK21 |
| 5 | IO_L93P_YY | AJ21 |
| 5 | IO_L93N_YY | AL22 |
| 5 | IO_L94P_YY | AJ22 |
| 5 | IO_VREF_L94N_YY | AK23 |
| 5 | IO_L95P_Y | AH22 |
| 5 | IO_VREF_L95N_Y | AL24[1] |
| 5 | IO_L96P_Y | AK24 |
| 5 | IO_L96N_Y | AH23 |
| 5 | IO_L97P_YY | AK25 |
| 5 | IO_VREF_L97N_YY | AJ25 |
| 5 | IO_L98P_YY | AL26 |
| 5 | IO_L98N_YY | AK26 |
| 5 | IO_L99P_Y | AH25 |
| 5 | IO_L99N_Y | AL27 |
| 5 | IO_L100P_YY | AJ26 |
| 5 | IO_VREF_L100N_YY | AK27 |
| 5 | IO_L101P_YY | AH26 |
| 5 | IO_L101N_YY | AL28 |
| 5 | IO_L102P_Y | AJ27 |
| 5 | IO_L102N_Y | AK28 |
| | | |

*Table 21:* **FG676 Differential Pin Pair Summary XCV400E, XCV600E**

| Pair | Bank | P Pin | N Pin | AO | Other Functions |
|---|---|---|---|---|---|
| 120 | 5 | AD11 | Y12 | √ | - |
| 121 | 5 | AB11 | AD10 | NA | - |
| 122 | 5 | AC11 | AE10 | √ | - |
| 123 | 5 | AC10 | AA11 | √ | - |
| 124 | 5 | Y11 | AD9 | 1 | - |
| 125 | 5 | AB10 | AF9 | √ | - |
| 126 | 5 | AD8 | AA10 | √ | VREF |
| 127 | 5 | AE8 | Y10 | √ | - |
| 128 | 5 | AC9 | AF8 | 1 | VREF |
| 129 | 5 | AF7 | AB9 | 1 | - |
| 130 | 5 | AA9 | AF6 | √ | - |
| 131 | 5 | AC8 | AC7 | √ | VREF |
| 132 | 5 | AD6 | Y9 | √ | - |
| 133 | 5 | AE5 | AA8 | √ | - |
| 134 | 5 | AC6 | AB8 | √ | VREF |
| 135 | 5 | AD5 | AA7 | √ | - |
| 136 | 5 | AF4 | AC5 | 2 | - |
| 137 | 6 | AC3 | AA5 | √ | - |
| 138 | 6 | AB4 | AC2 | √ | - |
| 139 | 6 | AA4 | W6 | 2 | - |
| 140 | 6 | Y5 | AB3 | 1 | VREF |
| 141 | 6 | V7 | AB2 | 1 | - |
| 142 | 6 | Y4 | AB1 | √ | - |
| 143 | 6 | W5 | V5 | √ | VREF |
| 144 | 6 | V6 | AA1 | √ | - |
| 145 | 6 | Y3 | W4 | 2 | - |
| 146 | 6 | U7 | Y1 | 1 | VREF |
| 147 | 6 | V4 | W1 | √ | - |
| 148 | 6 | U6 | W2 | √ | VREF |
| 149 | 6 | T5 | V3 | √ | - |
| 150 | 6 | U4 | U5 | √ | - |
| 151 | 6 | U3 | T7 | 2 | - |
| 152 | 6 | T6 | U2 | 1 | - |
| 153 | 6 | T4 | U1 | 1 | - |
| 154 | 6 | T3 | R7 | 1 | - |
| 155 | 6 | R6 | R4 | √ | VREF |
| 156 | 6 | R5 | R3 | √ | - |
| 157 | 6 | P7 | P8 | 2 | - |
| 158 | 6 | P6 | R1 | 1 | VREF |
| 159 | 6 | P4 | P5 | √ | - |
| 160 | 7 | N8 | N5 | √ | - |
| 161 | 7 | N3 | N6 | √ | - |
| 162 | 7 | M2 | N4 | 1 | VREF |
| 163 | 7 | M7 | N7 | 2 | - |
| 164 | 7 | M3 | M6 | √ | - |
| 165 | 7 | M5 | M4 | √ | VREF |
| 166 | 7 | L7 | L3 | 1 | - |
| 167 | 7 | K2 | L6 | 1 | - |
| 168 | 7 | K1 | L4 | 1 | - |
| 169 | 7 | L5 | K3 | 2 | - |
| 170 | 7 | J3 | K5 | √ | - |
| 171 | 7 | J4 | K4 | √ | - |
| 172 | 7 | K6 | H3 | √ | VREF |
| 173 | 7 | G3 | K7 | √ | - |
| 174 | 7 | H1 | J5 | 1 | VREF |
| 175 | 7 | J6 | G2 | 2 | - |
| 176 | 7 | F1 | J7 | √ | - |
| 177 | 7 | G4 | H4 | √ | VREF |
| 178 | 7 | H5 | F3 | 1 | - |
| 179 | 7 | H6 | E2 | 2 | - |
| 180 | 7 | F4 | G5 | 1 | VREF |
| 181 | 7 | G6 | H7 | 2 | - |
| 182 | 7 | E4 | E3 | √ | - |

**Notes:**

1. AO in the XCV600E.
2. AO in the XCV400E.

*Table 23:* **FG680 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E, XCV2000E**

| Pair | Bank | P Pin | N Pin | AO | Other Functions |
|---|---|---|---|---|---|
| 188 | 6 | AP39 | AP38 | 4 | - |
| 189 | 6 | AN38 | AN36 | 6 | VREF |
| 190 | 6 | AN39 | AN37 | √ | - |
| 191 | 6 | AM38 | AM36 | 4 | - |
| 192 | 6 | AL36 | AM37 | 6 | - |
| 193 | 6 | AL37 | AM39 | √ | VREF |
| 194 | 6 | AK36 | AL38 | √ | - |
| 195 | 6 | AK37 | AL39 | 7 | VREF |
| 196 | 6 | AJ36 | AK38 | 4 | - |
| 197 | 6 | AJ37 | AK39 | √ | VREF |
| 198 | 6 | AH37 | AJ38 | √ | - |
| 199 | 6 | AH38 | AJ39 | 4 | - |
| 200 | 6 | AG38 | AH39 | √ | VREF |
| 201 | 6 | AG39 | AG36 | √ | - |
| 202 | 6 | AF39 | AG37 | 6 | - |
| 203 | 6 | AE38 | AF36 | 4 | - |
| 204 | 6 | AF38 | AF37 | 4 | - |
| 205 | 6 | AE36 | AE39 | 6 | VREF |
| 206 | 6 | AE37 | AD38 | √ | - |
| 207 | 6 | AD36 | AD39 | 4 | - |
| 208 | 6 | AC39 | AC38 | 6 | - |
| 209 | 6 | AB38 | AD37 | √ | VREF |
| 210 | 6 | AB39 | AC35 | √ | - |
| 211 | 6 | AA38 | AC36 | 7 | - |
| 212 | 6 | AA39 | AC37 | 4 | - |
| 213 | 6 | Y38 | AB35 | √ | VREF |
| 214 | 6 | Y39 | AB36 | √ | - |
| 215 | 6 | AA36 | AB37 | 4 | VREF |
| 216 | 7 | W38 | AA37 | √ | - |
| 217 | 7 | V39 | W37 | 4 | VREF |
| 218 | 7 | U39 | W36 | √ | - |
| 219 | 7 | U38 | V38 | √ | VREF |
| 220 | 7 | T39 | V37 | 4 | - |
| 221 | 7 | T38 | V36 | 7 | - |
| 222 | 7 | R39 | V35 | √ | - |
| 223 | 7 | U36 | U37 | √ | VREF |
| 224 | 7 | U35 | R38 | 6 | - |
| 225 | 7 | T37 | P39 | 4 | - |
| 226 | 7 | T36 | P38 | √ | - |
| 227 | 7 | N38 | N39 | 6 | VREF |
| 228 | 7 | M39 | R37 | 4 | - |
| 229 | 7 | M38 | R36 | 4 | - |
| 230 | 7 | L39 | P37 | 6 | - |
| 231 | 7 | N37 | P36 | √ | - |
| 232 | 7 | N36 | L38 | √ | VREF |
| 233 | 7 | M37 | K39 | 4 | - |
| 234 | 7 | L37 | K38 | √ | - |
| 235 | 7 | L36 | J39 | √ | VREF |
| 236 | 7 | K37 | J38 | 4 | - |
| 237 | 7 | K36 | H39 | √ | VREF |
| 238 | 7 | J37 | H38 | √ | - |
| 239 | 7 | G38 | G39 | √ | VREF |
| 240 | 7 | F39 | J36 | 6 | - |
| 241 | 7 | F38 | H37 | 4 | - |
| 242 | 7 | E39 | H36 | √ | - |
| 243 | 7 | E38 | G37 | 6 | VREF |
| 244 | 7 | D39 | G36 | 4 | - |
| 245 | 7 | F36 | D38 | 4 | VREF |
| 246 | 7 | E37 | D37 | 6 | - |

**Notes:**

1. AO in the XCV1000E, 1600E, 2000E.
2. AO in the XCV600E, 1000E, 1600E.
3. AO in the XCV600E, 1000E.
4. AO in the XCV1000E, 1600E.
5. AO in the XCV1000E, 2000E.
6. AO in the XCV600E, 1000E, 2000E.
7. AO in the XCV1000E.
8. AO in the XCV2000E.

*Table 24:* **FG860 — XCV1000E, XCV1600E, XCV2000E**

| Bank | Pin Description | Pin # |
|---|---|---|
| 2 | IO_D1_L87N_YY | P2 |
| 2 | IO_D2_L88P_YY | P3 |
| 2 | IO_L88N_YY | L4 |
| 2 | IO_L89P_Y | P1 |
| 2 | IO_L89N_Y | R2 |
| 2 | IO_L90P_Y | M5 |
| 2 | IO_L90N_Y | R3 |
| 2 | IO_L91P_Y | M4 |
| 2 | IO_L91N_Y | R1 |
| 2 | IO_L92P | N4 |
| 2 | IO_L92N | T2 |
| 2 | IO_L93P_Y | P5 |
| 2 | IO_L93N_Y | T3 |
| 2 | IO_VREF_L94P_Y | P4 |
| 2 | IO_L94N_Y | T1 |
| 2 | IO_L95P_YY | U2 |
| 2 | IO_L95N_YY | R4 |
| 2 | IO_L96P_Y | U3 |
| 2 | IO_L96N_Y | T5 |
| 2 | IO_L97P_Y | T4 |
| 2 | IO_L97N_Y | V2 |
| 2 | IO_VREF_L98P_YY | U5 |
| 2 | IO_D3_L98N_YY | V3 |
| 2 | IO_L99P_YY | V1 |
| 2 | IO_L99N_YY | V5 |
| 2 | IO_L100P_Y | W2 |
| 2 | IO_L100N_Y | V4 |
| 2 | IO_L101P_Y | W5 |
| 2 | IO_L101N_Y | W1 |
| 2 | IO_VREF_L102P_YY | Y2 |
| 2 | IO_L102N_YY | W4 |
| 2 | IO_L103P_YY | Y1 |
| 2 | IO_L103N_YY | Y5 |
| 2 | IO_VREF_L104P_Y | AA1[1] |
| 2 | IO_L104N_Y | Y4 |
| 2 | IO_L105P_YY | AA4 |
| 2 | IO_L105N_YY | AA2 |

*Table 24:* **FG860 — XCV1000E, XCV1600E, XCV2000E**

| Bank | Pin Description | Pin # |
|---|---|---|
| | | |
| 3 | IO | AB4 |
| 3 | IO | AC2 |
| 3 | IO | AD1 |
| 3 | IO | AE3 |
| 3 | IO | AF4 |
| 3 | IO | AH5 |
| 3 | IO | AJ2 |
| 3 | IO | AL1 |
| 3 | IO | AM3 |
| 3 | IO | AP3 |
| 3 | IO | AR5 |
| 3 | IO | AU4 |
| 3 | IO | AB2 |
| 3 | IO_L106P_Y | AB3 |
| 3 | IO_VREF_L106N_Y | AC4[1] |
| 3 | IO_L107P_YY | AB1 |
| 3 | IO_L107N_YY | AC5 |
| 3 | IO_L108P_YY | AD4 |
| 3 | IO_VREF_L108N_YY | AC3 |
| 3 | IO_L109P_Y | AC1 |
| 3 | IO_L109N_Y | AD5 |
| 3 | IO_L110P_Y | AE4 |
| 3 | IO_L110N_Y | AD3 |
| 3 | IO_L111P_YY | AE5 |
| 3 | IO_L111N_YY | AD2 |
| 3 | IO_D4_L112P_YY | AE1 |
| 3 | IO_VREF_L112N_YY | AF5 |
| 3 | IO_L113P_Y | AE2 |
| 3 | IO_L113N_Y | AG4 |
| 3 | IO_L114P_Y | AG5 |
| 3 | IO_L114N_Y | AF1 |
| 3 | IO_L115P_YY | AH4 |
| 3 | IO_L115N_YY | AF2 |
| 3 | IO_L116P_Y | AF3 |
| 3 | IO_VREF_L116N_Y | AJ4 |
| 3 | IO_L117P_Y | AG1 |

*Table 24:* **FG860 — XCV1000E, XCV1600E, XCV2000E**

| Bank | Pin Description | Pin # |
|---|---|---|
| 6 | IO | AJ40 |
| 6 | IO | AL41 |
| 6 | IO | AN38 |
| 6 | IO | AN42 |
| 6 | IO | AP41 |
| 6 | IO | AR39 |
| 6 | IO_L211N_YY | AV41 |
| 6 | IO_L211P_YY | AV42 |
| 6 | IO_L212N_Y | AW40 |
| 6 | IO_L212P_Y | AU41 |
| 6 | IO_L213N_Y | AV39 |
| 6 | IO_L213P_Y | AU42 |
| 6 | IO_VREF_L214N_Y | AT41 |
| 6 | IO_L214P_Y | AU38 |
| 6 | IO_L215N | AT42 |
| 6 | IO_L215P | AV40 |
| 6 | IO_L216N_Y | AR41 |
| 6 | IO_L216P_Y | AU39 |
| 6 | IO_VREF_L217N_Y | AR42 |
| 6 | IO_L217P_Y | AU40 |
| 6 | IO_L218N_YY | AT38 |
| 6 | IO_L218P_YY | AP42 |
| 6 | IO_L219N_Y | AN41 |
| 6 | IO_L219P_Y | AT39 |
| 6 | IO_L220N_Y | AT40 |
| 6 | IO_L220P_Y | AM40 |
| 6 | IO_VREF_L221N_YY | AR38 |
| 6 | IO_L221P_YY | AM41 |
| 6 | IO_L222N_YY | AM42 |
| 6 | IO_L222P_YY | AR40 |
| 6 | IO_VREF_L223N_Y | AL40[2] |
| 6 | IO_L223P_Y | AP38 |
| 6 | IO_L224N_Y | AP39 |
| 6 | IO_L224P_Y | AL42 |
| 6 | IO_VREF_L225N_YY | AP40 |
| 6 | IO_L225P_YY | AK40 |
| 6 | IO_L226N_YY | AK41 |
| 6 | IO_L226P_YY | AN39 |
| 6 | IO_L227N_Y | AK42 |
| 6 | IO_L227P_Y | AN40 |
| 6 | IO_VREF_L228N_YY | AM38 |
| 6 | IO_L228P_YY | AJ41 |
| 6 | IO_L229N_YY | AJ42 |
| 6 | IO_L229P_YY | AM39 |
| 6 | IO_L230N_Y | AH40 |
| 6 | IO_L230P_Y | AH41 |
| 6 | IO_L231N_Y | AL38 |
| 6 | IO_L231P_Y | AH42 |
| 6 | IO_L232N_Y | AL39 |
| 6 | IO_L232P_Y | AG41 |
| 6 | IO_L233N | AK39 |
| 6 | IO_L233P | AG40 |
| 6 | IO_L234N_Y | AJ38 |
| 6 | IO_L234P_Y | AG42 |
| 6 | IO_VREF_L235N_Y | AF42 |
| 6 | IO_L235P_Y | AJ39 |
| 6 | IO_L236N_YY | AF41 |
| 6 | IO_L236P_YY | AH38 |
| 6 | IO_L237N_Y | AE42 |
| 6 | IO_L237P_Y | AH39 |
| 6 | IO_L238N_Y | AG38 |
| 6 | IO_L238P_Y | AE41 |
| 6 | IO_VREF_L239N_YY | AG39 |
| 6 | IO_L239P_YY | AD42 |
| 6 | IO_L240N_YY | AD40 |
| 6 | IO_L240P_YY | AF39 |
| 6 | IO_L241N_Y | AD41 |
| 6 | IO_L241P_Y | AE38 |
| 6 | IO_L242N_Y | AE39 |
| 6 | IO_L242P_Y | AC40 |
| 6 | IO_VREF_L243N_YY | AD38 |
| 6 | IO_L243P_YY | AC41 |
| 6 | IO_L244N_YY | AB42 |
| 6 | IO_L244P_YY | AC38 |

## FG860 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

*Table 25:* **FG860 Differential Pin Pair Summary XCV1000E, XCV1600E, XCV2000E**

| Pair | Bank | P Pin | N Pin | AO | Other Functions |
|---|---|---|---|---|---|
| Global Differential Clock | | | | | |
| 3 | 0 | C22 | A22 | NA | IO_DLL_L34N |
| 2 | 1 | B22 | D22 | NA | IO_DLL_L34P |
| 1 | 5 | AY22 | AW21 | NA | IO_DLL_L176N |
| 0 | 4 | BA22 | AW20 | NA | IO_DLL_L176P |
| IO LVDS<br>Total Pairs: 281, Asynchronous Output Pairs: 111 | | | | | |
| 0 | 0 | D38 | A38 | 2 | - |
| 1 | 0 | E37 | B37 | 1 | - |
| 2 | 0 | C39 | A37 | 1 | VREF |
| 3 | 0 | C38 | B36 | 1 | - |
| 4 | 0 | B35 | A36 | √ | - |
| 5 | 0 | D37 | A35 | √ | VREF |
| 6 | 0 | A34 | C37 | 5 | - |
| 7 | 0 | B33 | E36 | 5 | - |
| 8 | 0 | C32 | A33 | √ | - |
| 9 | 0 | B32 | C36 | √ | VREF |
| 10 | 0 | D35 | A32 | 1 | - |
| 11 | 0 | C35 | C31 | 1 | VREF |
| 12 | 0 | A31 | E34 | √ | - |
| 13 | 0 | C30 | D34 | √ | VREF |
| 14 | 0 | E33 | B30 | 2 | - |
| 15 | 0 | D33 | A30 | 2 | - |
| 16 | 0 | B29 | C33 | √ | VREF |
| 17 | 0 | A29 | E32 | √ | - |
| 18 | 0 | C28 | D32 | 2 | - |
| 19 | 0 | B28 | E31 | 1 | - |
| 20 | 0 | A28 | D31 | 1 | - |
| 21 | 0 | C27 | D30 | 5 | - |
| 22 | 0 | B27 | E29 | √ | - |
| 23 | 0 | A27 | D29 | √ | VREF |
| 24 | 0 | D28 | C26 | 5 | - |
| 25 | 0 | F27 | B26 | 5 | - |
| 26 | 0 | C25 | E27 | √ | - |
| 27 | 0 | B25 | D27 | √ | VREF |
| 28 | 0 | D26 | A25 | 1 | - |
| 29 | 0 | E25 | A24 | 1 | - |
| 30 | 0 | B24 | D25 | √ | - |
| 31 | 0 | A23 | E24 | √ | VREF |
| 32 | 0 | E23 | C23 | 2 | - |
| 33 | 0 | D23 | B23 | 2 | VREF |
| 34 | 1 | D22 | A22 | NA | IO_LVDS_DLL |
| 35 | 1 | B21 | D21 | 2 | VREF |
| 36 | 1 | A21 | D20 | 2 | - |
| 37 | 1 | D19 | C20 | √ | VREF |
| 38 | 1 | E19 | B20 | √ | - |
| 39 | 1 | A19 | D18 | 1 | - |
| 40 | 1 | C19 | E18 | 1 | - |
| 41 | 1 | E17 | B19 | √ | VREF |
| 42 | 1 | D16 | A18 | √ | - |
| 43 | 1 | B18 | E16 | 5 | - |
| 44 | 1 | A17 | F16 | 5 | - |
| 45 | 1 | E15 | C17 | √ | VREF |
| 46 | 1 | D14 | B17 | √ | - |
| 47 | 1 | E14 | A16 | 5 | - |
| 48 | 1 | D13 | C16 | 1 | - |
| 49 | 1 | D12 | B16 | 1 | - |
| 50 | 1 | E12 | A15 | 2 | - |
| 51 | 1 | C11 | C15 | √ | - |

*Table 25:* **FG860 Differential Pin Pair Summary XCV1000E, XCV1600E, XCV2000E**

| Pair | Bank | P Pin | N Pin | AO | Other Functions |
|---|---|---|---|---|---|
| 188 | 5 | AY27 | AV28 | √ | - |
| 189 | 5 | BA27 | AW29 | 5 | - |
| 190 | 5 | BB28 | AV29 | 1 | - |
| 191 | 5 | AY28 | AW30 | 1 | - |
| 192 | 5 | BA28 | AW31 | 2 | - |
| 193 | 5 | BB29 | AV31 | √ | - |
| 194 | 5 | AY29 | AY32 | √ | VREF |
| 195 | 5 | AW32 | BB30 | 2 | - |
| 196 | 5 | AV32 | AY30 | 2 | - |
| 197 | 5 | BA30 | AW33 | √ | VREF |
| 198 | 5 | BB31 | AV33 | √ | - |
| 199 | 5 | AY34 | BA31 | 1 | VREF |
| 200 | 5 | AW34 | BB32 | 1 | - |
| 201 | 5 | BA32 | AY35 | √ | VREF |
| 202 | 5 | BB33 | AW35 | √ | - |
| 203 | 5 | AV35 | BB34 | 5 | - |
| 204 | 5 | AY36 | BA34 | 5 | - |
| 205 | 5 | BB35 | AV36 | √ | VREF |
| 206 | 5 | BA35 | AY37 | √ | - |
| 207 | 5 | BB36 | BA36 | 5 | - |
| 208 | 5 | AW37 | BB37 | 1 | VREF |
| 209 | 5 | BA37 | AY38 | 1 | - |
| 210 | 5 | BB38 | AY39 | 2 | - |
| 211 | 6 | AV42 | AV41 | √ | - |
| 212 | 6 | AU41 | AW40 | 3 | - |
| 213 | 6 | AU42 | AV39 | 1 | - |
| 214 | 6 | AU38 | AT41 | 2 | VREF |
| 215 | 6 | AV40 | AT42 | 4 | - |
| 216 | 6 | AU39 | AR41 | 2 | - |
| 217 | 6 | AU40 | AR42 | 1 | VREF |
| 218 | 6 | AP42 | AT38 | √ | - |
| 219 | 6 | AT39 | AN41 | 2 | - |
| 220 | 6 | AM40 | AT40 | 1 | - |
| 221 | 6 | AM41 | AR38 | √ | VREF |
| 222 | 6 | AR40 | AM42 | √ | - |
| 223 | 6 | AP38 | AL40 | 5 | VREF |
| 224 | 6 | AL42 | AP39 | 2 | - |
| 225 | 6 | AK40 | AP40 | √ | VREF |
| 226 | 6 | AN39 | AK41 | √ | - |
| 227 | 6 | AN40 | AK42 | 2 | - |
| 228 | 6 | AJ41 | AM38 | √ | VREF |
| 229 | 6 | AM39 | AJ42 | √ | - |
| 230 | 6 | AH41 | AH40 | 3 | - |
| 231 | 6 | AH42 | AL38 | 1 | - |
| 232 | 6 | AG41 | AL39 | 2 | - |
| 233 | 6 | AG40 | AK39 | 4 | - |
| 234 | 6 | AG42 | AJ38 | 2 | - |
| 235 | 6 | AJ39 | AF42 | 1 | VREF |
| 236 | 6 | AH38 | AF41 | √ | - |
| 237 | 6 | AH39 | AE42 | 2 | - |
| 238 | 6 | AE41 | AG38 | 1 | - |
| 239 | 6 | AD42 | AG39 | √ | VREF |
| 240 | 6 | AF39 | AD40 | √ | - |
| 241 | 6 | AE38 | AD41 | 5 | - |
| 242 | 6 | AC40 | AE39 | 2 | - |
| 243 | 6 | AC41 | AD38 | √ | VREF |
| 244 | 6 | AC38 | AB42 | √ | - |
| 245 | 6 | AC39 | AB40 | 2 | VREF |
| 246 | 7 | AB39 | AA41 | √ | - |
| 247 | 7 | AA39 | Y41 | 2 | VREF |
| 248 | 7 | Y39 | Y40 | √ | - |
| 249 | 7 | W41 | Y38 | √ | VREF |
| 250 | 7 | W39 | W40 | 2 | - |
| 251 | 7 | V41 | W38 | 5 | - |
| 252 | 7 | V40 | V39 | √ | - |
| 253 | 7 | U39 | V42 | √ | VREF |
| 254 | 7 | U38 | U41 | 1 | - |
| 255 | 7 | T39 | U42 | 2 | - |

*Table 27:* **FG900 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E**

| Pair | Bank | P Pin | N Pin | AO | Other Functions |
|---|---|---|---|---|---|
| 120 | 3 | AA30 | W24 | 4 | - |
| 121 | 3 | AA29 | V20 | 1 | - |
| 122 | 3 | Y27 | W23 | NA | - |
| 123 | 3 | Y26 | AB30 | √ | D5 |
| 124 | 3 | V21 | AA28 | √ | VREF |
| 125 | 3 | Y25 | AA27 | 4 | - |
| 126 | 3 | W22 | Y23 | 4 | - |
| 127 | 3 | Y24 | AB28 | 4 | VREF |
| 128 | 3 | AC30 | AA25 | √ | - |
| 129 | 3 | W21 | AA24 | 2 | - |
| 130 | 3 | AB26 | AD30 | √ | - |
| 131 | 3 | Y22 | AC27 | √ | VREF |
| 132 | 3 | AD28 | AB25 | 2 | - |
| 133 | 3 | AC26 | AE30 | 4 | - |
| 134 | 3 | AD27 | AF30 | √ | - |
| 135 | 3 | AF29 | AB24 | 1 | VREF |
| 136 | 3 | AB23 | AE28 | 4 | - |
| 137 | 3 | AG30 | AC25 | 3 | - |
| 138 | 3 | AE26 | AG29 | 4 | VREF |
| 139 | 3 | AH30 | AC24 | 1 | - |
| 140 | 3 | AF28 | AD25 | NA | - |
| 141 | 3 | AH29 | AA22 | √ | INIT |
| 142 | 4 | AF27 | AK28 | √ | - |
| 143 | 4 | AG26 | AH27 | 4 | - |
| 144 | 4 | AD23 | AJ27 | 2 | - |
| 145 | 4 | AB21 | AF25 | 2 | VREF |
| 146 | 4 | AC22 | AH26 | 2 | - |
| 147 | 4 | AA21 | AG25 | √ | - |
| 148 | 4 | AJ26 | AD22 | √ | VREF |
| 149 | 4 | AA20 | AH25 | 1 | - |
| 150 | 4 | AC21 | AF24 | 1 | - |
| 151 | 4 | AG24 | AK26 | √ | - |
| 152 | 4 | AJ24 | AF23 | √ | VREF |
| 153 | 4 | AE23 | AB20 | 2 | - |
| 154 | 4 | AC20 | AG23 | 2 | - |
| 155 | 4 | AF22 | AE22 | √ | - |
| 156 | 4 | AJ22 | AG22 | √ | VREF |
| 157 | 4 | AK24 | AD20 | NA | - |
| 158 | 4 | AA19 | AF21 | 4 | - |
| 159 | 4 | AH22 | AA18 | NA | VREF |
| 160 | 4 | AG21 | AK23 | NA | - |
| 161 | 4 | AH21 | AD19 | 4 | - |
| 162 | 4 | AE20 | AJ21 | 2 | - |
| 163 | 4 | AG20 | AF20 | 2 | - |
| 164 | 4 | AC18 | AF19 | 2 | - |
| 165 | 4 | AJ20 | AE19 | √ | - |
| 166 | 4 | AK22 | AH20 | √ | VREF |
| 167 | 4 | AG19 | AB17 | 1 | - |
| 168 | 4 | AJ19 | AD17 | 1 | - |
| 169 | 4 | AA16 | AA17 | √ | - |
| 170 | 4 | AK21 | AB16 | √ | VREF |
| 171 | 4 | AG18 | AK20 | 2 | - |
| 172 | 4 | AK19 | AD16 | 2 | - |
| 173 | 4 | AE16 | AE17 | √ | - |
| 174 | 4 | AG17 | AJ17 | √ | VREF |
| 175 | 4 | AD15 | AH17 | NA | - |
| 176 | 4 | AG16 | AK17 | 4 | VREF |
| 177 | 5 | AF16 | AH16 | NA | IO_ LVDS_DLL |
| 178 | 5 | AC15 | AG15 | 4 | VREF |
| 179 | 5 | AB15 | AF15 | √ | - |
| 180 | 5 | AA15 | AF14 | √ | VREF |
| 181 | 5 | AH15 | AK15 | √ | - |
| 182 | 5 | AB14 | AF13 | 2 | - |
| 183 | 5 | AH14 | AJ14 | 2 | - |
| 184 | 5 | AE14 | AG13 | √ | VREF |
| 185 | 5 | AK13 | AD13 | √ | - |
| 186 | 5 | AE13 | AF12 | 1 | - |
| 187 | 5 | AC13 | AA13 | 1 | - |

*Table 28:* **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

| Bank | Pin Description | Pin # |
|---|---|---|
| 6 | IO_VREF_L265N_Y | AJ3 |
| 6 | IO_L265P_Y | AG5 |
| 6 | IO_L266N_YY | AD9[4] |
| 6 | IO_L266P_YY | AJ2[5] |
| 6 | IO_L267N_YY | AC10 |
| 6 | IO_L267P_YY | AH2 |
| 6 | IO_L268N_Y | AH3 |
| 6 | IO_L268P_Y | AF5 |
| 6 | IO_L269N_Y | AE8[4] |
| 6 | IO_L269P_Y | AG3[5] |
| 6 | IO_L270N_Y | AE7 |
| 6 | IO_L270P_Y | AG2 |
| 6 | IO_VREF_L271N_YY | AF6 |
| 6 | IO_L271P_YY | AG1 |
| 6 | IO_L272N_YY | AC9[4] |
| 6 | IO_L272P_YY | AG4[5] |
| 6 | IO_L273N_YY | AE6 |
| 6 | IO_L273P_YY | AF3 |
| 6 | IO_VREF_L274N_Y | AF1[2] |
| 6 | IO_L274P_Y | AF4 |
| 6 | IO_L275N | AB10[4] |
| 6 | IO_L275P | AF2[5] |
| 6 | IO_L276N_Y | AC8 |
| 6 | IO_L276P_Y | AE1 |
| 6 | IO_VREF_L277N_YY | AD5 |
| 6 | IO_L277P_YY | AE3 |
| 6 | IO_L278N_YY | AC7 |
| 6 | IO_L278P_YY | AD1 |
| 6 | IO_L279N_Y | AD6 |
| 6 | IO_L279P_Y | AD2 |
| 6 | IO_VREF_L280N_YY | AB8 |
| 6 | IO_L280P_YY | AC1 |
| 6 | IO_L281N_YY | AC5 |
| 6 | IO_L281P_YY | AC2 |
| 6 | IO_L282N_Y | AA9 |
| 6 | IO_L282P_Y | AC3 |
| 6 | IO_L283N_Y | AC4 |
| 6 | IO_L283P_Y | AD4 |
| 6 | IO_L284N_Y | AA8 |
| 6 | IO_L284P_Y | AB6 |
| 6 | IO_L285N | AB1 |
| 6 | IO_L285P | Y10 |
| 6 | IO_L286N_Y | AB2 |
| 6 | IO_L286P_Y | AA7 |
| 6 | IO_VREF_L287N_Y | AA4 |
| 6 | IO_L287P_Y | AA1 |
| 6 | IO_L288N_YY | Y9[4] |
| 6 | IO_L288P_YY | AB4[5] |
| 6 | IO_L289N_YY | AA2 |
| 6 | IO_L289P_YY | Y8 |
| 6 | IO_L290N_Y | AA6 |
| 6 | IO_L290P_Y | AA5 |
| 6 | IO_L291N_Y | AB3[4] |
| 6 | IO_L291P_Y | Y7[5] |
| 6 | IO_L292N_Y | Y1 |
| 6 | IO_L292P_Y | W10 |
| 6 | IO_VREF_L293N_YY | Y5 |
| 6 | IO_L293P_YY | Y2 |
| 6 | IO_L294N_YY | W9[4] |
| 6 | IO_L294P_YY | W2[5] |
| 6 | IO_L295N_YY | W7 |
| 6 | IO_L295P_YY | Y4 |
| 6 | IO_L296N_Y | W1 |
| 6 | IO_L296P_Y | Y6 |
| 6 | IO_L297N_Y | W6[4] |
| 6 | IO_L297P_Y | W3[5] |
| 6 | IO_L298N_Y | V9 |
| 6 | IO_L298P_Y | W4 |