AMD Xilinx - XCV2000E-6BG560C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	9600
Number of Logic Elements/Cells	43200
Total RAM Bits	655360
Number of I/O	404
Number of Gates	2541952
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	560-LBGA Exposed Pad, Metal
Supplier Device Package	560-MBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv2000e-6bg560c

forces a storage element into the initialization state specified for it in the configuration. BY forces it into the opposite state. Alternatively, these signals can be configured to operate asynchronously. All of the control signals are independently invertible, and are shared by the two flip-flops within the slice.

Additional Logic

The F5 multiplexer in each slice combines the function generator outputs. This combination provides either a function generator that can implement any 5-input function, a 4:1 multiplexer, or selected functions of up to nine inputs.

Similarly, the F6 multiplexer combines the outputs of all four function generators in the CLB by selecting one of the F5-multiplexer outputs. This permits the implementation of any 6-input function, an 8:1 multiplexer, or selected functions of up to 19 inputs.

Each CLB has four direct feedthrough paths, two per slice. These paths provide extra data input lines or additional local routing that does not consume logic resources.

Arithmetic Logic

Dedicated carry logic provides fast arithmetic carry capability for high-speed arithmetic functions. The Virtex-E CLB supports two separate carry chains, one per Slice. The height of the carry chains is two bits per CLB.

The arithmetic logic includes an XOR gate that allows a 2-bit full adder to be implemented within a slice. In addition, a dedicated AND gate improves the efficiency of multiplier implementation. The dedicated carry path can also be used to cascade function generators for implementing wide logic functions.

BUFTs

Each Virtex-E CLB contains two 3-state drivers (BUFTs) that can drive on-chip buses. See **Dedicated Routing**. Each Virtex-E BUFT has an independent 3-state control pin and an independent input pin.

Block SelectRAM

Virtex-E FPGAs incorporate large block SelectRAM memories. These complement the Distributed SelectRAM memories that provide shallow RAM structures implemented in CLBs.

Block SelectRAM memory blocks are organized in columns, starting at the left (column 0) and right outside edges and inserted every 12 CLB columns (see notes for smaller devices). Each memory block is four CLBs high, and each memory column extends the full height of the chip, immediately adjacent (to the right, except for column 0) of the CLB column locations indicated in Table 3.

Table 3: **CLB/Block RAM Column Locations**

XCV Device /Col.	0	12	24	36	48	60	72	84	96	108	120	138	156
50E	Columns 0, 6, 18, & 24												
100E	Columns 0, 12, 18, & 30												
200E	Columns 0, 12, 30, & 42												
300E	√	√		√	√								
400E	√	√			√	√							
600E	√	√	√		√	√	√						
1000E	√	√	√				√	√	√				
1600E	√	√	√	√			√	√	√	√			
2000E	√	√	√	√				√	√	√	√		
2600E	√	√	√	√					√	√	√	√	
3200E	√	√	√	√						√	√	√	√

Table 4 shows the amount of block SelectRAM memory that is available in each Virtex-E device.

Table 4: **Virtex-E Block SelectRAM Amounts**

Virtex-E Device	# of Blocks	Block SelectRAM Bits
XCV50E	16	65,536
XCV100E	20	81,920
XCV200E	28	114,688
XCV300E	32	131,072
XCV400E	40	163,840
XCV600E	72	294,912
XCV1000E	96	393,216
XCV1600E	144	589,824
XCV2000E	160	655,360
XCV2600E	184	753,664
XCV3200E	208	851,968

As illustrated in Figure 6, each block SelectRAM cell is a fully synchronous dual-ported (True Dual Port) 4096-bit RAM with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.

The DLL also operates as a clock mirror. By driving the output from a DLL off-chip and then back on again, the DLL can be used to deskew a board level clock among multiple devices.

To guarantee that the system clock is operating correctly prior to the FPGA starting up after configuration, the DLL can delay the completion of the configuration process until after it has achieved lock. For more information about DLL functionality, see the Design Consideration section of the data sheet.

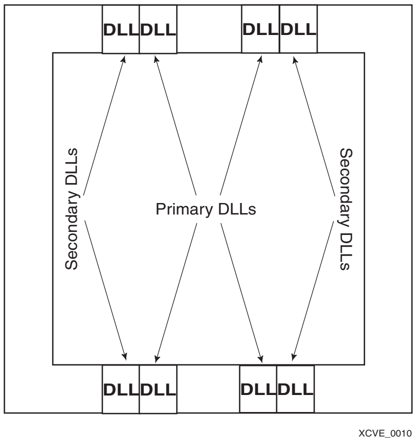

Figure 10: **DLL Locations**

Boundary Scan

Virtex-E devices support all the mandatory Boundary Scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, INTEST, SAMPLE/PRELOAD, BYPASS, IDCODE, USERCODE, and HIGHZ instructions. The TAP also supports two internal scan chains and configuration/readback of the device.

The JTAG input pins (TDI, TMS, TCK) do not have a V_{CCO} requirement and operate with either 2.5 V or 3.3 V input signalling levels. The output pin (TDO) is sourced from the V_{CCO} in bank 2, and for proper operation of LVTTL 3.3 V levels, the bank should be supplied with 3.3 V.

Boundary Scan operation is independent of individual IOB configurations, and unaffected by package type. All IOBs, including un-bonded ones, are treated as independent 3-state bidirectional pins in a single scan chain. Retention of the bidirectional test capability after configuration facilitates the testing of external interconnections, provided the user design or application is turned off.

Table 6 lists the Boundary Scan instructions supported in Virtex-E FPGAs. Internal signals can be captured during EXTEST by connecting them to un-bonded or unused IOBs. They can also be connected to the unused outputs of IOBs defined as unidirectional input pins.

Before the device is configured, all instructions except USER1 and USER2 are available. After configuration, all instructions are available. During configuration, it is recommended that those operations using the Boundary Scan register (SAMPLE/PRELOAD, INTEST, EXTEST) not be performed.

In addition to the test instructions outlined above, the Boundary Scan circuitry can be used to configure the FPGA, and also to read back the configuration data.

Figure 11 is a diagram of the Virtex-E Series Boundary Scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

Data Registers

The primary data register is the Boundary Scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out, and 3-State Control. Non-IOB pins have appropriate partial bit population if input-only or output-only. Each EXTEST CAPTURED-OR state captures all In, Out, and 3-state pins.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream Boundary Scan device.

The FPGA supports up to two additional internal scan chains that can be specified using the BSCAN macro. The macro provides two user pins (SEL1 and SEL2) which are decodes of the USER1 and USER2 instructions respectively. For these instructions, two corresponding pins (T DO1 and TDO2) allow user scan data to be shifted out of TDO.

Likewise, there are individual clock pins (DRCK1 and DRCK2) for each user register. There is a common input pin (TDI) and shared output pins that represent the state of the TAP controller (RESET, SHIFT, and UPDATE).

Bit Sequence

The order within each IOB is: In, Out, 3-State. The input-only pins contribute only the In bit to the Boundary Scan I/O data register, while the output-only pins contributes all three bits.

From a cavity-up view of the chip (as shown in EPIC), starting in the upper right chip corner, the Boundary Scan data-register bits are ordered as shown in Figure 12.

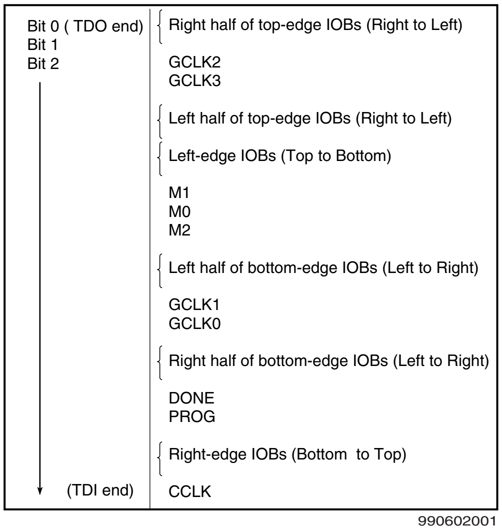

Figure 12: **Boundary Scan Bit Sequence**

BSDL (Boundary Scan Description Language) files for Virtex-E Series devices are available on the Xilinx web site in the File Download area.

Identification Registers

The IDCODE register is supported. By using the IDCODE, the device connected to the JTAG port can be determined.

The IDCODE register has the following binary format:

vvvv:ffff:fffa:aaaa:aaaa:cccc:cccc:ccc1

where

v = the die version number

f = the family code (05 for Virtex-E family)

a = the number of CLB rows (ranges from 16 for

XCV50E to 104 for XCV3200E)

c = the company code (49h for Xilinx)

The USERCODE register is supported. By using the USERCODE, a user-programmable identification code can be loaded and shifted out for examination. The identification code (see Table 7) is embedded in the bitstream during bitstream generation and is valid only after configuration.

Table 7: **IDCODEs Assigned to Virtex-E FPGAs**

FPGA	IDCODE
XCV50E	v0A10093h
XCV100E	v0A14093h
XCV200E	v0A1C093h
XCV300E	v0A20093h
XCV400E	v0A28093h
XCV600E	v0A30093h
XCV1000E	v0A40093h
XCV1600E	v0A48093h
XCV2000E	v0A50093h
XCV2600E	v0A5C093h
XCV3200E	v0A68093h

Note:

Attempting to load an incorrect bitstream causes configuration to fail and can damage the device.

Including Boundary Scan in a Design

Since the Boundary Scan pins are dedicated, no special element needs to be added to the design unless an internal data register (USER1 or USER2) is desired.

If an internal data register is used, insert the Boundary Scan symbol and connect the necessary pins as appropriate.

For in-circuit debugging, an optional download and read-back cable is available. This cable connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can single-step the logic, readback the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.

Configuration

Virtex-E devices are configured by loading configuration data into the internal configuration memory. Note that attempting to load an incorrect bitstream causes configuration to fail and can damage the device.

Some of the pins used for configuration are dedicated pins, while others can be re-used as general purpose inputs and outputs once configuration is complete.

The following are dedicated pins:

- Mode pins (M2, M1, M0)
- Configuration clock pin (CCLK)
- $\overline{\text{PROGRAM}}$ pin
- DONE pin
- Boundary Scan pins (TDI, TDO, TMS, TCK)

Depending on the configuration mode chosen, CCLK can be an output generated by the FPGA, or can be generated externally and provided to the FPGA as an input. The $\overline{\text{PROGRAM}}$ pin must be pulled High prior to reconfiguration.

Note that some configuration pins can act as outputs. For correct operation, these pins require a V_{CCO} of 3.3 V or 2.5 V. At 3.3 V the pins operate as LVTTL, and at 2.5 V they operate as LVCMOS. All affected pins fall in banks 2 or 3. The configuration pins needed for SelectMap (CS, Write) are located in bank 1.

Configuration Modes

Virtex-E supports the following four configuration modes.

- Slave-serial mode
- Master-serial mode
- SelectMAP mode
- Boundary Scan mode (JTAG)

The Configuration mode pins (M2, M1, M0) select among these configuration modes with the option in each case of having the IOB pins either pulled up or left floating prior to configuration. The selection codes are listed in Table 8.

Configuration through the Boundary Scan port is always available, independent of the mode selection. Selecting the Boundary Scan mode simply turns off the other modes. The three mode pins have internal pull-up resistors, and default to a logic High if left unconnected. However, it is recommended to drive the configuration mode pins externally.

Table 8: **Configuration Codes**

Configuration Mode	M2(1)	M1	M0	CCLK Direction	Data Width	Serial D_{out}	Configuration Pull-ups(1)
Master-serial mode	0	0	0	Out	1	Yes	No
Boundary Scan mode	1	0	1	N/A	1	No	No
SelectMAP mode	1	1	0	In	8	No	No
Slave-serial mode	1	1	1	In	1	Yes	No
Master-serial mode	1	0	0	Out	1	Yes	Yes
Boundary Scan mode	0	0	1	N/A	1	No	Yes
SelectMAP mode	0	1	0	In	8	No	Yes
Slave-serial mode	0	1	1	In	1	Yes	Yes

Notes:

1. M2 is sampled continuously from power up until the end of the configuration. Toggling M2 while INIT is being held externally Low can cause the configuration pull-up settings to change.

Table 9 lists the total number of bits required to configure each device.

Table 9: **Virtex-E Bitstream Lengths**

Device	# of Configuration Bits
XCV50E	630,048
XCV100E	863,840
XCV200E	1,442,016
XCV300E	1, 875,648
XCV400E	2,693,440
XCV600E	3,961,632
XCV1000E	6,587,520
XCV1600E	8,308,992
XCV2000E	10,159,648
XCV2600E	12,922,336
XCV3200E	16,283,712

Slave-Serial Mode

In slave-serial mode, the FPGA receives configuration data in bit-serial form from a serial PROM or other source of serial configuration data. The serial bitstream must be set up at the DIN input pin a short time before each rising edge of an externally generated CCLK.

For more detailed information on serial PROMs, see the PROM data sheet at http://www.xilinx.com/bvdocs/publications/ds026.pdf.

Multiple FPGAs can be daisy-chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed to the DOUT pin. The maximum capacity for a single LOUT/DOUT write is 2^{20}-1 (1,048,575) 32-bit words, or 33,554,4000 bits. The data on the DOUT pin changes on the rising edge of CCLK.

The change of DOUT on the rising edge of CCLK differs from previous families, but does not cause a problem for mixed configuration chains. This change was made to improve serial configuration rates for Virtex and Virtex-E only chains.

Figure 13 shows a full master/slave system. A Virtex-E device in slave-serial mode should be connected as shown in the right-most device.

Slave-serial mode is selected by applying <111> or <011> to the mode pins (M2, M1, M0). A weak pull-up on the mode pins makes slave serial the default mode if the pins are left unconnected. However, it is recommended to drive the configuration mode pins externally. Figure 14 shows slave-serial mode programming switching characteristics.

Table 10 provides more detail about the characteristics shown in Figure 14. Configuration must be delayed until the $\overline{\text{INIT}}$ pins of all daisy-chained FPGAs are High.

Table 10: **Master/Slave Serial Mode Programming Switching**

	Description	Figure References	Symbol	Values	Units
CCLK	DIN setup/hold, slave mode	1/2	T_{DCC}/T_{CCD}	5.0 / 0.0	ns, min
	DIN setup/hold, master mode	1/2	T_{DSCK}/T_{CKDS}	5.0 / 0.0	ns, min
	DOUT	3	T_{CCO}	12.0	ns, max
	High time	4	T_{CCH}	5.0	ns, min
	Low time	5	T_{CCL}	5.0	ns, min
	Maximum Frequency		F_{CC}	66	MHz, max
	Frequency Tolerance, master mode with respect to nominal			+45% –30%	

Application Examples

Creating a design with the SelectI/O features requires the instantiation of the desired library symbol within the design code. At the board level, designers need to know the termination techniques required for each I/O standard.

This section describes some common application examples illustrating the termination techniques recommended by each of the standards supported by the SelectI/O features.

Termination Examples

Circuit examples involving typical termination techniques for each of the SelectI/O standards follow. For a full range of accepted values for the DC voltage specifications for each standard, refer to the table associated with each figure.

The resistors used in each termination technique example and the transmission lines depicted represent board level components and are not meant to represent components on the device.

GTL

A sample circuit illustrating a valid termination technique for GTL is shown in Figure 44.

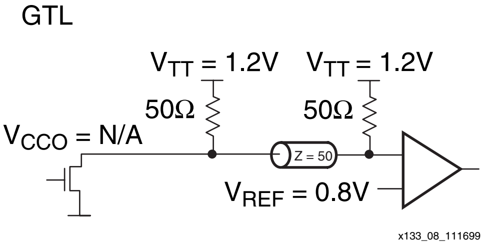

Figure 44: **Terminated GTL**

Table 23 lists DC voltage specifications.

Table 23: **GTL Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	-	N/A	-
$V_{REF} = N \times V_{TT}$[1]	0.74	0.8	0.86
V_{TT}	1.14	1.2	1.26
$V_{IH} = V_{REF} + 0.05$	0.79	0.85	-
$V_{IL} = V_{REF} - 0.05$	-	0.75	0.81
V_{OH}	-	-	-
V_{OL}	-	0.2	0.4
I_{OH} at V_{OH}(mA)	-	-	-
I_{OL}at V_{OL}(mA) at 0.4V	32	-	-
I_{OL}at V_{OL}(mA) at 0.2V	-	-	40

Notes:

1. N must be greater than or equal to 0.653 and less than or equal to 0.68.

GTL+

A sample circuit illustrating a valid termination technique for GTL+ appears in Figure 45. DC voltage specifications appear in Table 24.

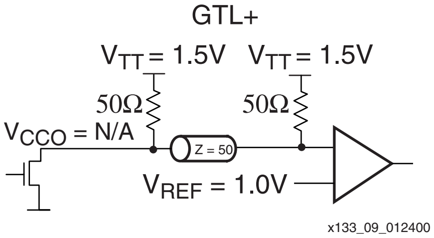

Figure 45: **Terminated GTL+**

Table 24: **GTL+ Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	-	-	-
$V_{REF} = N \times V_{TT}$[1]	0.88	1.0	1.12
V_{TT}	1.35	1.5	1.65
$V_{IH} = V_{REF} + 0.1$	0.98	1.1	-
$V_{IL} = V_{REF} - 0.1$	-	0.9	1.02
V_{OH}	-	-	-
V_{OL}	0.3	0.45	0.6
I_{OH} at V_{OH} (mA)	-	-	-
I_{OL}at V_{OL} (mA) at 0.6V	36	-	-
I_{OL}at V_{OL} (mA) at 0.3V	-	-	48

Notes:

1. N must be greater than or equal to 0.653 and less than or equal to 0.68.

SSTL3_I

A sample circuit illustrating a valid termination technique for SSTL3_I appears in Figure 49. DC voltage specifications appear in Table 28.

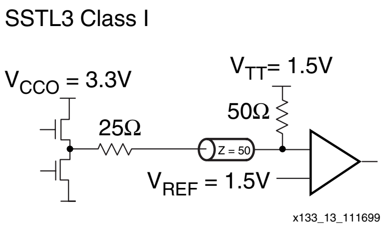

Figure 49: **Terminated SSTL3 Class I**

Table 28: **SSTL3_I Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	**3.0**	**3.3**	**3.6**
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} = V_{REF} + 0.2$	1.5	1.7	$3.9^{(1)}$
$V_{IL} = V_{REF} – 0.2$	$–0.3^{(2)}$	1.3	1.5
$V_{OH} = V_{REF} + 0.6$	1.9	-	-
$V_{OL} = V_{REF} – 0.6$	-	-	1.1
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL}at V_{OL} (mA)	8	-	-

Notes:

1. V_{IH} maximum is V_{CCO} + 0.3
2. V_{IL} minimum does not conform to the formula

SSTL3_II

A sample circuit illustrating a valid termination technique for SSTL3_II appears in Figure 50. DC voltage specifications appear in Table 29.

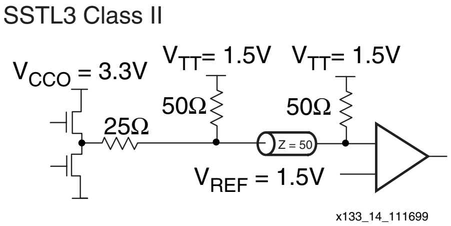

Figure 50: **Terminated SSTL3 Class II**

Table 29: **SSTL3_II Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} = V_{REF} + 0.2$	1.5	1.7	$3.9^{(1)}$
$V_{IL}= V_{REF} – 0.2$	$–0.3^{(2)}$	1.3	1.5
$V_{OH} = V_{REF} + 0.8$	2.1	-	-
$V_{OL}= V_{REF} – 0.8$	-	-	0.9
I_{OH} at V_{OH} (mA)	–16	-	-
I_{OL}at V_{OL} (mA)	16	-	-

Notes:

1. V_{IH} maximum is V_{CCO} + 0.3
2. V_{IL} minimum does not conform to the formula

SSTL2_I

A sample circuit illustrating a valid termination technique for SSTL2_I appears in Figure 51. DC voltage specifications appear in Table 30.

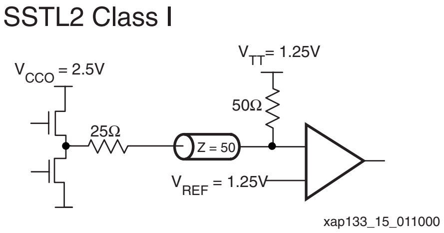

Figure 51: **Terminated SSTL2 Class I**

Table 30: **SSTL2_I Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
$V_{REF} = 0.5 \times V_{CCO}$	1.15	1.25	1.35
$V_{TT} = V_{REF} + N^{(1)}$	1.11	1.25	1.39
$V_{IH} = V_{REF} + 0.18$	1.33	1.43	$3.0^{(2)}$
$V_{IL} = V_{REF} – 0.18$	$–0.3^{(3)}$	1.07	1.17
$V_{OH} = V_{REF} + 0.61$	1.76	-	-
$V_{OL}= V_{REF} – 0.61$	-	-	0.74
I_{OH} at V_{OH} (mA)	–7.6	-	-
I_{OL}at V_{OL} (mA)	7.6	-	-

Notes:

1. N must be greater than or equal to -0.04 and less than or equal to 0.04.
2. V_{IH} maximum is V_{CCO} + 0.3.
3. V_{IL} minimum does not conform to the formula.

Table 6: **PQ240 — XCV50E, XCV100E, XCV200E, XCV300E, XCV400E**

Pin #	Pin Description	Bank
P137	VCCINT	NA
P104	VCCINT	NA
P88	VCCINT	NA
P77	VCCINT	NA
P43	VCCINT	NA
P32	VCCINT	NA
P16	VCCINT	NA
P240	VCCO	7
P232	VCCO	0
P226	VCCO	0
P212	VCCO	0
P207	VCCO	1
P197	VCCO	1
P180	VCCO	1
P176	VCCO	2
P165	VCCO	2
P150	VCCO	2
P146	VCCO	3
P136	VCCO	3
P121	VCCO	3
P116	VCCO	4
P105	VCCO	4
P90	VCCO	4
P85	VCCO	5
P76	VCCO	5
P61	VCCO	5
P55	VCCO	6
P44	VCCO	6
P30	VCCO	6
P25	VCCO	7
P15	VCCO	7
P233	GND	NA
P227	GND	NA
P219	GND	NA
P211	GND	NA
P204	GND	NA
P196	GND	NA
P190	GND	NA
P182	GND	NA
P172	GND	NA
P166	GND	NA
P158	GND	NA
P151	GND	NA
P143	GND	NA
P135	GND	NA
P129	GND	NA
P119	GND	NA
P112	GND	NA
P106	GND	NA
P98	GND	NA
P91	GND	NA
P83	GND	NA
P75	GND	NA
P69	GND	NA
P59	GND	NA
P51	GND	NA
P45	GND	NA
P37	GND	NA
P29	GND	NA
P22	GND	NA
P14	GND	NA
P8	GND	NA
P1	GND	NA

Notes:

1. V_{REF} or I/O option only in the XCV100E, 200E, 300E, 400E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV200E, 300E, 400E; otherwise, I/O option only.
3. V_{REF} or I/O option only in the XCV400E; otherwise, I/O option only.

Table 10: **BG352 — XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
6	IO_L74P _Y	R25
6	IO_L75N	R26
6	IO_L75P	P24
6	IO	P23[1]
6	IO	N26
7	IO_L76N_YY	N25
7	IO_L76P_YY	N24
7	IO	M26[1]
7	IO_L77N	M25
7	IO_L77P	M24
7	IO_L78N _Y	M23
7	IO_VREF_7_L78P _Y	L26
7	IO_L79N_YY	K25
7	IO_L79P_YY	L24
7	IO	L23[1]
7	IO_L80N	J26
7	IO_L80P	J25
7	IO	K24[1]
7	IO_L81N_YY	K23
7	IO_L81P_YY	H25
7	IO_L82N _Y	J23
7	IO_VREF_7_L82P _Y	G26
7	IO_L83N _Y	G25
7	IO_L83P _Y	H24
7	IO	H23
7	IO	F26[1]
7	IO	F25[1]
7	IO_L84N_Y	G24
7	IO_VREF_7_L84P_Y	D26
7	IO_L85N_YY	E25
7	IO_L85P_YY	F24
7	IO	F23[1]
7	IO_L86N_YY	D25

Table 10: **BG352 — XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
7	IO_VREF_7_L86P_YY	E24[2]
7	IO	C26
7	IO	E23[1]
7	IO	D24[1]
7	IO	C25
NA	TDI	B3
NA	TDO	D4
NA	CCLK	C3
NA	TCK	C24
NA	TMS	D23
NA	PROGRAM	AC4
NA	DONE	AD3
NA	DXN	AD23
NA	DXP	AE24
NA	M2	AC23
NA	M0	AD24
NA	M1	AB23
NA	VCCINT	A20
NA	VCCINT	B16
NA	VCCINT	C14
NA	VCCINT	D12
NA	VCCINT	D10
NA	VCCINT	K4
NA	VCCINT	L1
NA	VCCINT	P2
NA	VCCINT	T1
NA	VCCINT	W2
NA	VCCINT	AC10
NA	VCCINT	AF11
NA	VCCINT	AE14
NA	VCCINT	AF16
NA	VCCINT	AE19

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
7	IO	J1
7	IO	J4
7	IO	L2[1]
7	IO_L104N_YY	L3
7	IO_L104P_YY	L4
7	IO_L105N_YY	L5
7	IO_L105P_YY	L1
7	IO_L106N_Y	L6
7	IO_L106P_Y	K2
7	IO_L107N_Y	K4
7	IO_VREF_L107P_Y	K3
7	IO_L108N_YY	K1
7	IO_L108P_YY	K5
7	IO_L109N_YY	J3
7	IO_L109P_YY	J2
7	IO_L110N_YY	J5
7	IO_L110P_YY	H1
7	IO_L111N_YY	H2
7	IO_L111P_YY	H3
7	IO_L112N_Y	G1
7	IO_VREF_L112P_Y	H4
7	IO_L113N_Y	F1
7	IO_L113P_Y	F2
7	IO_L114N_YY	H5
7	IO_L114P_YY	G3
7	IO_L115N_YY	E1
7	IO_VREF_L115P_YY	E2
7	IO_L116N_YY	F3
7	IO_L116P_YY	G5
7	IO_L117N_YY	E3
7	IO_VREF_L117P_YY	D2
7	IO_L118N_YY	F5
7	IO_L118P_YY	C1
2	CCLK	B22
3	DONE	Y19
NA	DXN	Y5
NA	DXP	V6
NA	M0	AB2
NA	M1	U5
NA	M2	Y4
NA	PROGRAM	W20
NA	TCK	C4
NA	TDI	B20
2	TDO	A21
NA	TMS	D3
NA	NC	W19
NA	NC	W4
NA	NC	D19
NA	NC	D4
NA	VCCINT	E5
NA	VCCINT	E18
NA	VCCINT	F6
NA	VCCINT	F17
NA	VCCINT	G7
NA	VCCINT	G8
NA	VCCINT	G9
NA	VCCINT	G14
NA	VCCINT	G15
NA	VCCINT	H7
NA	VCCINT	G16
NA	VCCINT	H16
NA	VCCINT	J7
NA	VCCINT	J16
NA	VCCINT	P7
NA	VCCINT	P16
NA	VCCINT	R7
NA	VCCINT	R16
NA	VCCINT	T7
NA	VCCINT	T8
NA	VCCINT	T9
NA	VCCINT	T14

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
NA	VCCINT	T15
NA	VCCINT	T16
NA	VCCINT	U6
NA	VCCINT	U17
NA	VCCINT	V5
NA	VCCINT	V18
NA	VCCO_7	L7
NA	VCCO_7	K7
NA	VCCO_7	K6
NA	VCCO_7	J6
NA	VCCO_7	H6
NA	VCCO_7	G6
NA	VCCO_6	N7
NA	VCCO_6	M7
NA	VCCO_6	T6
NA	VCCO_6	R6
NA	VCCO_6	P6
NA	VCCO_6	N6
NA	VCCO_5	U10
NA	VCCO_5	U9
NA	VCCO_5	U8
NA	VCCO_5	U7
NA	VCCO_5	T11
NA	VCCO_5	T10
NA	VCCO_4	U16
NA	VCCO_4	U15
NA	VCCO_4	U14
NA	VCCO_4	U13
NA	VCCO_4	T13
NA	VCCO_4	T12
NA	VCCO_3	T17
NA	VCCO_3	R17
NA	VCCO_3	P17
NA	VCCO_3	N17
NA	VCCO_3	N16
NA	VCCO_3	M16

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
NA	VCCO_2	K17
NA	VCCO_2	J17
NA	VCCO_2	H17
NA	VCCO_2	G17
NA	VCCO_2	L16
NA	VCCO_2	K16
NA	VCCO_1	G13
NA	VCCO_1	G12
NA	VCCO_1	F16
NA	VCCO_1	F15
NA	VCCO_1	F14
NA	VCCO_1	F13
NA	VCCO_0	G11
NA	VCCO_0	G10
NA	VCCO_0	F10
NA	VCCO_0	F9
NA	VCCO_0	F8
NA	VCCO_0	F7
NA	GND	AB22
NA	GND	AB1
NA	GND	AA21
NA	GND	AA2
NA	GND	Y20
NA	GND	Y3
NA	GND	P14
NA	GND	P13
NA	GND	P12
NA	GND	P11
NA	GND	P10
NA	GND	P9
NA	GND	N14
NA	GND	N13
NA	GND	N12
NA	GND	N11
NA	GND	N10
NA	GND	N9

Table 21: **FG676 Differential Pin Pair Summary XCV400E, XCV600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
52	2	G24	H22	√	-
53	2	J21	G25	2	-
54	2	G26	J22	1	VREF
55	2	H24	J23	√	-
56	2	J24	K20	√	VREF
57	2	K22	K21	√	D2
58	2	H25	K23	√	-
59	2	L20	J26	2	-
60	2	K25	L22	1	-
61	2	L21	L23	1	-
62	2	M20	L24	1	-
63	2	M23	M22	√	D3
64	2	L26	M21	√	-
65	2	N19	M24	2	-
66	2	M26	N20	1	VREF
67	2	N24	N21	√	-
68	2	N23	N22	√	-
69	3	P21	P23	√	-
70	3	P22	R25	1	VREF
71	3	P19	P20	2	-
72	3	R21	R22	√	-
73	3	R24	R23	√	VREF
74	3	T24	R20	1	-
75	3	T22	U24	1	-
76	3	T23	U25	1	-
77	3	T21	U20	2	-
78	3	U22	V26	√	-
79	3	T20	U23	√	D5
80	3	V24	U21	√	VREF
81	3	V23	W24	√	-
82	3	V22	W26	1	VREF
83	3	Y25	V21	2	-
84	3	V20	AA26	√	-
85	3	Y24	W23	√	VREF
86	3	AA24	Y23	1	-
87	3	AB26	W21	2	-
88	3	Y22	W22	1	VREF
89	3	AA23	AB24	2	-
90	3	W20	AC24	√	-
91	3	AB23	Y21	√	INIT
92	4	AC22	AD26	√	-
93	4	AD23	AA20	1	-
94	4	Y19	AC21	√	-
95	4	AD22	AB20	√	VREF
96	4	AE22	Y18	NA	-
97	4	AF22	AA19	NA	-
98	4	AD21	AB19	√	VREF
99	4	AC20	AA18	√	-
100	4	AC19	AD20	1	-
101	4	AF20	AB18	1	VREF
102	4	AD19	Y17	NA	-
103	4	AE19	AD18	NA	VREF
104	4	AF19	AA17	√	-
105	4	AC17	AB17	1	-
106	4	Y16	AE17	√	-
107	4	AF17	AA16	√	-
108	4	AD17	AB16	NA	-
109	4	AC16	AD16	√	-
110	4	AC15	Y15	√	VREF
111	4	AD15	AA15	√	-
112	4	W14	AB15	1	-
113	4	AF15	Y14	1	VREF
114	4	AD14	AB14	NA	-
115	5	AC14	AF13	NA	IO_LVDS_DLL
116	5	AA13	AF12	1	VREF
117	5	AC13	W13	1	-
118	5	AA12	AD12	√	-
119	5	AC12	AB12	√	VREF

FG680 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 23: **FG680 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
GCLK LVDS					
3	0	A20	C22	NA	IO_DLL_L29N
2	1	D21	A19	NA	IO_DLL_L29P
1	5	AU22	AT22	NA	IO_DLL_L155N
0	4	AW19	AT21	NA	IO_DLL_L155P
IO LVDS Total Pairs: 247, Asynchronous Output Pairs: 111					
0	0	A36	C35	5	-
1	0	B35	D34	5	VREF
2	0	A35	C34	√	-
3	0	B34	D33	√	VREF
4	0	A34	C33	3	-
5	0	B33	D32	3	-
6	0	D31	C32	√	-
7	0	C31	A33	√	VREF
8	0	B31	B32	5	-
9	0	D30	A32	5	VREF
10	0	C30	A31	√	-
11	0	D29	B30	√	VREF
12	0	C29	A30	2	-
13	0	B29	A29	2	-
14	0	A28	B28	√	VREF
15	0	B27	C28	√	-
16	0	A27	D27	5	-
17	0	B26	C27	5	-
18	0	C26	D26	√	-
19	0	D25	A26	√	VREF
20	0	C25	B25	3	-
21	0	D24	A25	3	-
22	0	B23	A24	√	-
23	0	A23	C24	√	VREF
24	0	B22	B24	5	-
25	0	A22	E23	5	-
26	0	B21	D23	√	-
27	0	A21	C23	√	VREF
28	0	B20	E22	2	-
29	1	A19	C22	NA	IO_LVDS_DLL
30	1	B19	C21	2	VREF
31	1	A18	C19	2	-
32	1	B18	D19	√	VREF
33	1	A17	C18	√	-
34	1	B17	D18	5	-
35	1	A16	E18	5	-
36	1	D17	C17	√	VREF
37	1	E17	B16	√	-
38	1	C16	A15	3	-
39	1	D16	B15	3	-
40	1	B14	A14	√	VREF
41	1	A13	C15	√	-
42	1	B13	D15	5	-
43	1	A12	C14	5	-
44	1	C13	D14	√	-
45	1	D13	B12	√	VREF
46	1	C12	A11	2	-
47	1	C11	B11	2	-
48	1	D11	A10	√	VREF
49	1	C10	B10	√	-
50	1	D10	A9	5	VREF
51	1	C9	B9	5	-

Table 23: **FG680 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
120	3	AN4	AT1	4	-
121	3	AR2	AP4	4	VREF
122	3	AT2	AR3	6	-
123	3	AR4	AU2	√	INIT
124	4	AU4	AV5	√	-
125	4	AT6	AV4	5	-
126	4	AU6	AW4	5	VREF
127	4	AT7	AW5	√	-
128	4	AU7	AV6	√	VREF
129	4	AT8	AW6	3	-
130	4	AU8	AV7	3	-
131	4	AT9	AW7	√	-
132	4	AV8	AU9	√	VREF
133	4	AW8	AT10	5	-
134	4	AV9	AU10	5	VREF
135	4	AW9	AT11	√	-
136	4	AV10	AU11	√	VREF
137	4	AW10	AU12	2	-
138	4	AV11	AT13	2	-
139	4	AW11	AU13	√	VREF
140	4	AT14	AV12	√	-
141	4	AU14	AW12	5	-
142	4	AT15	AV13	5	-
143	4	AU15	AW13	√	-
144	4	AV14	AT16	√	VREF
145	4	AW14	AU16	3	-
146	4	AV15	AR17	3	-
147	4	AW15	AT17	√	-
148	4	AU17	AV16	√	VREF
149	4	AR18	AW16	5	-
150	4	AT18	AV17	5	-
151	4	AU18	AW17	√	-
152	4	AT19	AV18	√	VREF
153	4	AU19	AW18	2	-
154	4	AU21	AV19	2	VREF
155	5	AT21	AT22	NA	IO_LVDS_DLL
156	5	AV20	AR22	8	VREF
157	5	AV23	AW21	√	VREF
158	5	AU23	AV21	√	-
159	5	AT23	AW22	5	-
160	5	AR23	AV22	5	-
161	5	AV24	AW23	√	VREF
162	5	AW24	AU24	√	-
163	5	AW25	AT24	3	-
164	5	AV25	AU25	3	-
165	5	AW26	AT25	√	VREF
166	5	AV26	AW27	√	-
167	5	AU26	AV27	5	-
168	5	AT26	AW28	5	-
169	5	AU27	AV28	√	-
170	5	AW29	AT27	√	VREF
171	5	AW30	AU28	2	-
172	5	AV30	AV29	2	-
173	5	AW31	AU29	√	VREF
174	5	AV31	AT29	√	-
175	5	AW32	AU30	5	VREF
176	5	AW33	AT30	5	-
177	5	AV33	AU31	√	VREF
178	5	AT31	AW34	√	-
179	5	AV32	AV34	3	-
180	5	AU32	AW35	3	-
181	5	AT32	AV35	√	VREF
182	5	AU33	AW36	√	-
183	5	AT33	AV36	5	VREF
184	5	AU34	AU36	5	-
185	6	AT38	AR36	√	-
186	6	AP36	AR38	6	-
187	6	AP37	AT39	4	VREF

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
1	IO_L57N_Y	D9
1	IO_VREF_L57P_Y	A12[2]
1	IO_L58N_Y	E9
1	IO_L58P_Y	C12
1	IO_L59N_YY	B12
1	IO_VREF_L59P_YY	D8
1	IO_L60N_YY	A11
1	IO_L60P_YY	E8
1	IO_L61N_Y	C7
1	IO_L61P_Y	A10
1	IO_L62N_Y	C6
1	IO_L62P_Y	B10
1	IO_L63N_YY	A9
1	IO_VREF_L63P_YY	B9
1	IO_L64N_YY	A8
1	IO_L64P_YY	E7
1	IO_L65N_Y	B8
1	IO_L65P_Y	C5
1	IO_L66N_Y	A7
1	IO_VREF_L66P_Y	A6
1	IO_L67N_Y	B7
1	IO_L67P_Y	D6
1	IO_L68N_Y	A5
1	IO_L68P_Y	C4
1	IO_WRITE_L69N_YY	B6
1	IO_CS_L69P_YY	E6
2	IO	H2
2	IO	H3
2	IO	J1
2	IO	K5
2	IO	M2
2	IO	N1
2	IO	R5
2	IO	U1
2	IO	U4
2	IO	W3
2	IO	Y3
2	IO	AA3
2	IO_DOUT_BUSY_L70P_YY	F5
2	IO_DIN_D0_L70N_YY	D2
2	IO_L71P_Y	E4
2	IO_L71N_Y	E2
2	IO_L72P_Y	D3
2	IO_L72N_Y	F2
2	IO_VREF_L73P_Y	E1
2	IO_L73N_Y	F4
2	IO_L74P	G2
2	IO_L74N	E3
2	IO_L75P_Y	F1
2	IO_L75N_Y	G5
2	IO_VREF_L76P_Y	G1
2	IO_L76N_Y	F3
2	IO_L77P_YY	G4
2	IO_L77N_YY	H1
2	IO_L78P_Y	J2
2	IO_L78N_Y	G3
2	IO_L79P_Y	H5
2	IO_L79N_Y	K2
2	IO_VREF_L80P_YY	H4
2	IO_L80N_YY	K1
2	IO_L81P_YY	L2
2	IO_L81N_YY	L3
2	IO_VREF_L82P_Y	L1[2]
2	IO_L82N_Y	J5
2	IO_L83P_Y	J4
2	IO_L83N_Y	M3
2	IO_VREF_L84P_YY	J3
2	IO_L84N_YY	M1
2	IO_L85P_YY	N2
2	IO_L85N_YY	K4
2	IO_L86P_Y	N3
2	IO_L86N_Y	K3
2	IO_VREF_L87P_YY	L5

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
7	IO_L275N_Y	G38
7	IO_VREF_L275P_Y	G42
7	IO_L276N_Y	G41
7	IO_L276P_Y	F40
7	IO_L277N	F42
7	IO_L277P	F41
7	IO_L278N_Y	F39
7	IO_VREF_L278P_Y	E42
7	IO_L279N_Y	E40
7	IO_L279P_Y	E41
7	IO_L280N_Y	E39
7	IO_L280P_Y	D41
2	CCLK	B4
3	DONE	AW2
NA	DXN	BA38
NA	DXP	AW38
NA	M0	AW41
NA	M1	AV37
NA	M2	BA39
NA	PROGRAM	AV2
NA	TCK	B38
NA	TDI	B5
2	TDO	D5
NA	TMS	B39
NA	VCCINT	F9
NA	VCCINT	F10
NA	VCCINT	F17
NA	VCCINT	F18
NA	VCCINT	F25
NA	VCCINT	F26
NA	VCCINT	F33
NA	VCCINT	F34
NA	VCCINT	J6
NA	VCCINT	J37
NA	VCCINT	K6

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
NA	VCCINT	K37
NA	VCCINT	T6
NA	VCCINT	T37
NA	VCCINT	U6
NA	VCCINT	U37
NA	VCCINT	V6
NA	VCCINT	V37
NA	VCCINT	AE6
NA	VCCINT	AE37
NA	VCCINT	AF6
NA	VCCINT	AF37
NA	VCCINT	AG6
NA	VCCINT	AG37
NA	VCCINT	AN6
NA	VCCINT	AN37
NA	VCCINT	AP6
NA	VCCINT	AP37
NA	VCCINT	AU9
NA	VCCINT	AU10
NA	VCCINT	AU17
NA	VCCINT	AU18
NA	VCCINT	AU25
NA	VCCINT	AU26
NA	VCCINT	AU33
NA	VCCINT	AU34
NA	VCCO_0	F23
NA	VCCO_0	F24
NA	VCCO_0	F28
NA	VCCO_0	F29
NA	VCCO_0	F31
NA	VCCO_0	F32
NA	VCCO_0	F35
NA	VCCO_0	F36
NA	VCCO_1	F11
NA	VCCO_1	F12
NA	VCCO_1	F14

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
1	IO	J20[5]
1	IO	L18[4]
1	IO_LVDS_DLL_L34P	E16
1	IO_L35N_YY	B16
1	IO_VREF_L35P_YY	F16[2]
1	IO_L36N_YY	A16
1	IO_L36P_YY	H16
1	IO_L37N_YY	C16
1	IO_VREF_L37P_YY	K15
1	IO_L38N_YY	K16
1	IO_L38P_YY	G16
1	IO_L39N_Y	A17
1	IO_L39P_Y	E17
1	IO_L40N_Y	F17
1	IO_L40P_Y	C17
1	IO_L41N_YY	E18
1	IO_VREF_L41P_YY	A18
1	IO_L42N_YY	D18
1	IO_L42P_YY	A19
1	IO_L43N_Y	B19
1	IO_L43P_Y	G18
1	IO_L44N_Y	D19
1	IO_L44P_Y	H18
1	IO_L45N_YY	F18
1	IO_VREF_L45P_YY	F19[1]
1	IO_L46N_YY	B20
1	IO_L46P_YY	K17
1	IO_L47N_Y	D20[4]
1	IO_L47P_Y	A20[4]
1	IO_L48N_Y	G19
1	IO_L48P_Y	C20
1	IO_L49N_Y	K18
1	IO_L49P_Y	E20
1	IO_L50N_YY	B21[4]
1	IO_L50P_YY	D21[4]
1	IO_L51N_YY	F20
1	IO_L51P_YY	A21
1	IO_L52N_YY	C21
1	IO_VREF_L52P_YY	A22
1	IO_L53N_YY	H19
1	IO_L53P_YY	B22
1	IO_L54N_YY	E21
1	IO_L54P_YY	D22
1	IO_L55N_YY	F21
1	IO_VREF_L55P_YY	C22
1	IO_L56N_YY	H20
1	IO_L56P_YY	E22
1	IO_L57N_Y	G21
1	IO_L57P_Y	A23
1	IO_L58N_Y	A24
1	IO_L58P_Y	K19
1	IO_L59N_YY	C24
1	IO_VREF_L59P_YY	B24
1	IO_L60N_YY	H21
1	IO_L60P_YY	G22
1	IO_L61N_Y	E23
1	IO_L61P_Y	C25
1	IO_L62N_Y	D24
1	IO_L62P_Y	A26
1	IO_L63N_YY	B26
1	IO_VREF_L63P_YY	K20
1	IO_L64N_YY	D25
1	IO_L64P_YY	J21
1	IO_L65N_Y	C26[4]
1	IO_L65P_Y	F23[4]
1	IO_L66N_Y	B27
1	IO_VREF_L66P_Y	G23[1]
1	IO_L67N_Y	A27
1	IO_L67P_Y	F24
1	IO_L68N_YY	B28[3]
1	IO_L68P_YY	A28[4]
1	IO_WRITE_L69N_YY	K21
1	IO_CS_L69P_YY	C27

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
6	IO	AC5[4]
6	IO	AD1[4]
6	IO	AE5[5]
6	IO_L212N_YY	AF3
6	IO_L212P_YY	AC6
6	IO_L213N	AH2[4]
6	IO_L213P	AG2[3]
6	IO_L214N	AB9
6	IO_L214P	AE4
6	IO_VREF_L215N_YY	AE3[1]
6	IO_L215P_YY	AH1
6	IO_L216N_Y	AB8[4]
6	IO_L216P_Y	AD6[3]
6	IO_L217N_YY	AG1
6	IO_L217P_YY	AA10
6	IO_VREF_L218N	AA9
6	IO_L218P	AD4
6	IO_L219N_YY	AD5
6	IO_L219P_YY	AD2
6	IO_L220N_YY	AD3
6	IO_L220P_YY	AF2
6	IO_L221N	AA8
6	IO_L221P	AA7
6	IO_VREF_L222N_YY	AF1
6	IO_L222P_YY	Y9
6	IO_L223N_YY	AB6
6	IO_L223P_YY	AC4
6	IO_L224N	AE1
6	IO_L224P	W8
6	IO_L225N_YY	Y8
6	IO_L225P_YY	AB4
6	IO_VREF_L226N_YY	AB3
6	IO_L226P_YY	W9
6	IO_L227N_YY	AA5[4]
6	IO_L227P_YY	W10[3]
6	IO_L228N_YY	AB1
6	IO_L228P_YY	V10
6	IO_L229N_YY	Y7[4]
6	IO_VREF_L229P_YY	AC1
6	IO_L230N	V11
6	IO_L230P	AA3
6	IO_L231N_YY	AA2[3]
6	IO_L231P_YY	U10[4]
6	IO_L232N	W7
6	IO_L232P	AA6
6	IO_L233N_YY	Y6
6	IO_L233P_YY	Y4
6	IO_L234N_Y	AA1[4]
6	IO_L234P_Y	V7[4]
6	IO_L235N_YY	Y3
6	IO_L235P_YY	Y2
6	IO_VREF_L236N	Y5[1]
6	IO_L236P	W5
6	IO_L237N_YY	W4
6	IO_L237P_YY	W6
6	IO_L238N_YY	V6
6	IO_L238P_YY	W2
6	IO_L239N	U9
6	IO_L239P	V4
6	IO_VREF_L240N_YY	AB2
6	IO_L240P_YY	T8
6	IO_L241N_YY	U5
6	IO_L241P_YY	W1
6	IO_L242N	Y1
6	IO_L242P	T9
6	IO_L243N_YY	T7
6	IO_L243P_YY	U3
6	IO_VREF_L244N_YY	T5
6	IO_L244P_YY	V2
6	IO_L245N_YY	R9[4]
6	IO_L245P_YY	T6[3]
6	IO_VREF_L246N_YY	T4[2]
6	IO_L246P_YY	U2
6	IO_L247N	T1

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
111	2	M31	R26	2600 1600	-
112	2	N30	P28	3200 1600 1000	-
113	2	N29	N33	2600 2000 1000	VREF
114	2	T25	N34	3200 2600 2000 1600	-
115	2	P34	R27	3200 2600 2000 1600 1000	-
116	2	P29	P31	3200 2600 1600 1000	-
117	2	P33	T26	3200 2600 2000	-
118	2	R34	R28	2600 2000 1000	-
119	2	N31	N32	2000 1600 1000	D3
120	2	P30	R33	2000 1600	-
121	2	R29	T34	3200 2600 2000 1600 1000	-
122	2	R30	T30	1000	-
123	2	T28	R31	3200 1600	-
124	2	T29	U27	3200 2600 1600 1000	-
125	2	T31	T33	2000 1600 1000	VREF
126	2	U28	T32	2000 1600 1000	-
127	2	U29	U33	3200 2600 1600 1000	VREF
128	2	V33	U31	3200 2600 2000 1600 1000	-
129	3	V26	V30	3200 2600 1600 1000	VREF
130	3	W34	V28	2000 1600 1000	-
131	3	W32	W30	2000 1600 1000	VREF
132	3	V29	Y34	3200 2600 1600 1000	-
133	3	W29	Y33	3200 1600	-
134	3	W26	W28	1000	-
135	3	Y31	Y30	3200 2600 2000 1600 1000	-
136	3	AA34	W31	2000 1600	-
137	3	AA33	Y29	2000 1600 1000	VREF
138	3	W25	AB34	2600 2000 1000	-
139	3	Y28	AB33	3200 2600 2000	-
140	3	AA30	Y26	3200 2600 1600 1000	-
141	3	Y27	AA31	3200 2600 2000 1600 1000	-
142	3	AA27	AA29	3200 2600 2000 1600	-
143	3	AB32	AB29	2600 2000 1000	VREF
144	3	AA28	AC34	3200 1600 1000	-
145	3	Y25	AD34	2600 1600	-
146	3	AB30	AC33	3200 2600 1600 1000	-
147	3	AA26	AC32	2000 1000	-
148	3	AD33	AB28	3200 2600 2000	-
149	3	AE34	AB27	3200 2600 2000 1600 1000	D5
150	3	AE33	AC30	2000 1600 1000	VREF
151	3	AA25	AE32	3200 1600 1000	-
152	3	AE31	AD29	3200 2600 2000 1600 1000	-