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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	9600
Number of Logic Elements/Cells	43200
Total RAM Bits	655360
Number of I/O	512
Number of Gates	2541952
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	680-LBGA Exposed Pad
Supplier Device Package	680-FTEBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv2000e-7fg680c

Dedicated Routing

Some classes of signal require dedicated routing resources to maximize performance. In the Virtex-E architecture, dedicated routing resources are provided for two classes of signal.

- Horizontal routing resources are provided for on-chip 3-state buses. Four partitionable bus lines are provided per CLB row, permitting multiple buses within a row, as shown in Figure 8.
- Two dedicated nets per CLB propagate carry signals vertically to the adjacent CLB. Global Clock Distribution Network
- DLL Location

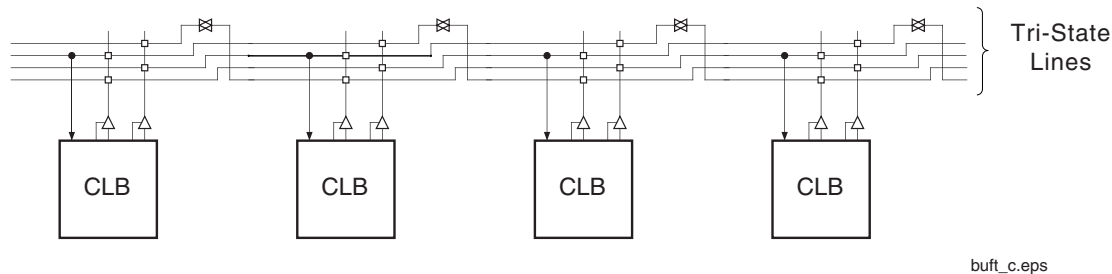


Figure 8: BUFT Connections to Dedicated Horizontal Bus Lines

Global Clock Distribution

Virtex-E provides high-speed, low-skew clock distribution through the global routing resources described above. A typical clock distribution net is shown in Figure 9.

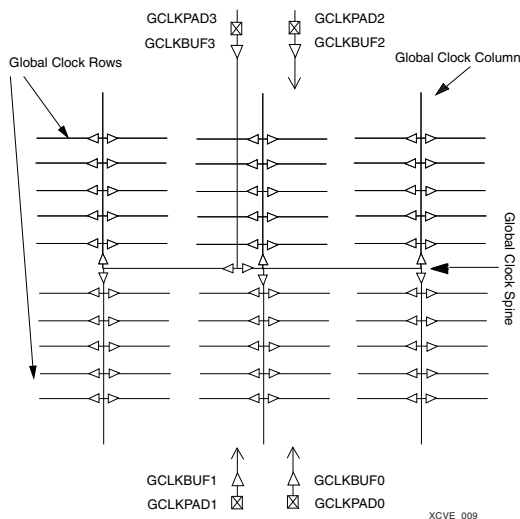


Figure 9: Global Clock Distribution Network

Clock Routing

Clock Routing resources distribute clocks and other signals with very high fanout throughout the device. Virtex-E devices include two tiers of clock routing resources referred to as global and local clock routing resources.

- The global routing resources are four dedicated global nets with dedicated input pins that are designed to distribute high-fanout clock signals with minimal skew. Each global clock net can drive all CLB, IOB, and block RAM clock pins. The global nets can be driven only by global buffers. There are four global buffers, one for each global net.
- The local clock routing resources consist of 24 backbone lines, 12 across the top of the chip and 12 across bottom. From these lines, up to 12 unique signals per column can be distributed via the 12 longlines in the column. These local resources are more flexible than the global resources since they are not restricted to routing only to clock pins.

Four global buffers are provided, two at the top center of the device and two at the bottom center. These drive the four global nets that in turn drive any clock pin.

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is selected either from these pads or from signals in the general purpose routing.

Digital Delay-Locked Loops

There are eight DLLs (Delay-Locked Loops) per device, with four located at the top and four at the bottom, Figure 10. The DLLs can be used to eliminate skew between the clock input pad and the internal clock input pins throughout the device. Each DLL can drive two global clock networks. The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element. Additional delay is introduced such that clock edges arrive at internal flip-flops synchronized with clock edges arriving at the input.

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock, and can double the clock or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

Data Registers

The primary data register is the Boundary Scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out, and 3-State Control. Non-IOB pins have appropriate partial bit population if input-only or output-only. Each EXTEST CAPTURED-OR state captures all In, Out, and 3-state pins.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream Boundary Scan device.

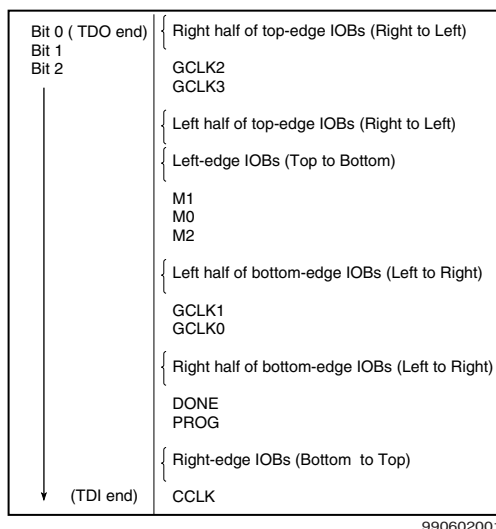
The FPGA supports up to two additional internal scan chains that can be specified using the BSCAN macro. The macro provides two user pins (SEL1 and SEL2) which are decodes of the USER1 and USER2 instructions respectively. For these instructions, two corresponding pins (TDO1 and TDO2) allow user scan data to be shifted out of TDO.

Likewise, there are individual clock pins (DRCK1 and DRCK2) for each user register. There is a common input pin (TDI) and shared output pins that represent the state of the TAP controller (RESET, SHIFT, and UPDATE).

Bit Sequence

The order within each IOB is: In, Out, 3-State. The input-only pins contribute only the In bit to the Boundary Scan I/O data register, while the output-only pins contribute all three bits.

From a cavity-up view of the chip (as shown in EPIC), starting in the upper right chip corner, the Boundary Scan data-register bits are ordered as shown in [Figure 12](#).



990602001

Figure 12: Boundary Scan Bit Sequence

BSDL (Boundary Scan Description Language) files for Virtex-E Series devices are available on the Xilinx web site in the File Download area.

Identification Registers

The IDCODE register is supported. By using the IDCODE, the device connected to the JTAG port can be determined.

The IDCODE register has the following binary format:

vvvv:ffff:ffa:aaaa:aaaa:cccc:cccc:ccc1

where

v = the die version number

f = the family code (05 for Virtex-E family)

a = the number of CLB rows (ranges from 16 for XCV50E to 104 for XCV3200E)

c = the company code (49h for Xilinx)

The USERCODE register is supported. By using the USERCODE, a user-programmable identification code can be loaded and shifted out for examination. The identification code (see [Table 7](#)) is embedded in the bitstream during bitstream generation and is valid only after configuration.

Table 7: IDCODEs Assigned to Virtex-E FPGAs

FPGA	IDCODE
XCV50E	v0A10093h
XCV100E	v0A14093h
XCV200E	v0A1C093h
XCV300E	v0A20093h
XCV400E	v0A28093h
XCV600E	v0A30093h
XCV1000E	v0A40093h
XCV1600E	v0A48093h
XCV2000E	v0A50093h
XCV2600E	v0A5C093h
XCV3200E	v0A68093h

Note:

Attempting to load an incorrect bitstream causes configuration to fail and can damage the device.

Including Boundary Scan in a Design

Since the Boundary Scan pins are dedicated, no special element needs to be added to the design unless an internal data register (USER1 or USER2) is desired.

If an internal data register is used, insert the Boundary Scan symbol and connect the necessary pins as appropriate.

VHDL Initialization Example

```

library IEEE;
use IEEE.std_logic_1164.all;

entity MYMEM is
port (CLK, WE:in std_logic;
ADDR: in std_logic_vector(8 downto 0);
DIN: in std_logic_vector(7 downto 0);
DOUT: out std_logic_vector(7 downto 0));
end MYMEM;

architecture BEHAVE of MYMEM is
signal logic0, logic1: std_logic;

component RAMB4_S8
--synopsys translate_off
generic( INIT_00,INIT_01, INIT_02, INIT_03, INIT_04, INIT_05, INIT_06, INIT_07,
INIT_08, INIT_09, INIT_0a, INIT_0b, INIT_0c, INIT_0d, INIT_0e, INIT_0f : BIT_VECTOR(255
downto 0)
:= X"0000000000000000000000000000000000000000000000000000000000000000");
--synopsys translate_on
port (WE, EN, RST, CLK: in STD_LOGIC;
ADDR: in STD_LOGIC_VECTOR(8 downto 0);
DI: in STD_LOGIC_VECTOR(7 downto 0);
DO: out STD_LOGIC_VECTOR(7 downto 0));
end component;

--synopsys dc_script_begin
--set_attribute ram0 INIT_00
"0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF" -type string
--set_attribute ram0 INIT_01
"FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210" -type string
--synopsys dc_script_end

begin
logic0 <='0';
logic1 <='1';

ram0: RAMB4_S8
--synopsys translate_off
generic map (
INIT_00 => X"0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF",
INIT_01 => X"FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210")
--synopsys translate_on
port map (WE=>WE, EN=>logic1, RST=>logic0, CLK=>CLK,ADDR=>ADDR, DI=>DIN, DO=>DOUT);
end BEHAVE;

```

The voltage reference signal is “banked” within the Virtex-E device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 38 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

IBUF placement restrictions require that any differential amplifier input signals within a bank be of the same standard. How to specify a specific location for the IBUF via the LOC property is described below. Table 19 summarizes the Virtex-E input standards compatibility requirements.

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element by default activates to ensure a zero hold-time requirement. The NODELAY=TRUE property overrides this default.

When the IBUF does not drive a flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

Table 19: Xilinx Input Standards Compatibility Requirements

Rule 1	Standards with the same input V_{CCO} , output V_{CCO} , and V_{REF} can be placed within the same bank.
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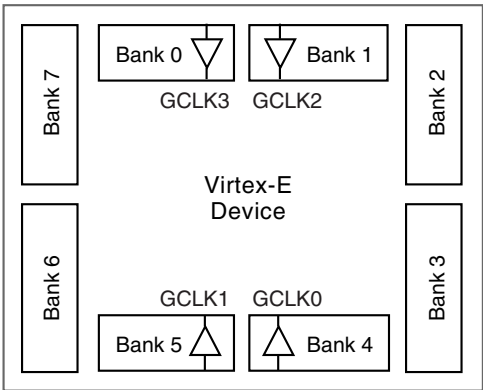


Figure 38: Virtex-E I/O Banks

IBUFG

Signals used as high fanout clock inputs to the Virtex-E device should drive a global clock input buffer (IBUFG) via an external input port in order to take advantage of one of the four dedicated global clock distribution networks. The output of the IBUFG should only drive a CLKDLL,

CLKDLLHF, or BUFG symbol. The generic Virtex-E IBUFG symbol appears in Figure 39.

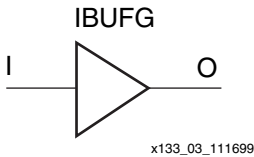


Figure 39: Virtex-E Global Clock Input Buffer (IBUFG) Symbol

The extension to the base name determines which I/O standard is used by the IBUFG. With no extension specified for the generic IBUFG symbol, the assumed standard is LVTTTL.

The following list details variations of the IBUFG symbol.

- IBUFG
- IBUFG_LVCMOS2
- IBUFG_PCI33_3
- IBUFG_PCI66_3
- IBUFG_GTL
- IBUFG_GTLP
- IBUFG_HSTL_I
- IBUFG_HSTL_III
- IBUFG_HSTL_IV
- IBUFG_SSTL3_I
- IBUFG_SSTL3_II
- IBUFG_SSTL2_I
- IBUFG_SSTL2_II
- IBUFG_CTT
- IBUFG_AGP
- IBUFG_LVCMOS18
- IBUFG_LVDS
- IBUFG_LVPECL

When the IBUFG symbol supports an I/O standard that requires a differential amplifier input, the IBUFG automatically configures as a differential amplifier input buffer. The low-voltage I/O standards with a differential amplifier input require an external reference voltage input V_{REF} .

The voltage reference signal is “banked” within the Virtex-E device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 38 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

IBUFG placement restrictions require any differential amplifier input signals within a bank be of the same standard. The LOC property can specify a location for the IBUFG.

As an added convenience, the BUFGP can be used to instantiate a high fanout clock input. The BUFGP symbol

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used, see [Figure 2](#). The values listed below are worst-case. Precise values are provided by the timing analyzer.

		Speed Grade ⁽¹⁾				Units
Description	Symbol	Min	-8	-7	-6	
Combinatorial Delays						
4-input function: F/G inputs to X/Y outputs	T _{ILO}	0.19	0.40	0.42	0.47	ns, max
5-input function: F/G inputs to F5 output	T _{IF5}	0.36	0.76	0.8	0.9	ns, max
5-input function: F/G inputs to X output	T _{IF5X}	0.35	0.74	0.8	0.9	ns, max
6-input function: F/G inputs to Y output via F6 MUX	T _{IF6Y}	0.35	0.74	0.9	1.0	ns, max
6-input function: F5IN input to Y output	T _{F5INY}	0.04	0.11	0.20	0.22	ns, max
Incremental delay routing through transparent latch to XQ/YQ outputs	T _{IFNCTL}	0.27	0.63	0.7	0.8	ns, max
BY input to YB output	T _{BYYB}	0.19	0.38	0.46	0.51	ns, max
Sequential Delays						
FF Clock CLK to XQ/YQ outputs	T _{CKO}	0.34	0.78	0.9	1.0	ns, max
Latch Clock CLK to XQ/YQ outputs	T _{CKLO}	0.40	0.77	0.9	1.0	ns, max
Setup and Hold Times before/after Clock CLK						
4-input function: F/G Inputs	T _{ICK} / T _{CKI}	0.39 / 0	0.9 / 0	1.0 / 0	1.1 / 0	ns, min
5-input function: F/G inputs	T _{IF5CK} / T _{CKIF5}	0.55 / 0	1.3 / 0	1.4 / 0	1.5 / 0	ns, min
6-input function: F5IN input	T _{F5INCK} / T _{CKF5IN}	0.27 / 0	0.6 / 0	0.8 / 0	0.8 / 0	ns, min
6-input function: F/G inputs via F6 MUX	T _{IF6CK} / T _{CKIF6}	0.58 / 0	1.3 / 0	1.5 / 0	1.6 / 0	ns, min
BX/BY inputs	T _{DICK} / T _{CKDI}	0.25 / 0	0.6 / 0	0.7 / 0	0.8 / 0	ns, min
CE input	T _{CECK} / T _{CKCE}	0.28 / 0	0.55 / 0	0.7 / 0	0.7 / 0	ns, min
SR/BY inputs (synchronous)	T _{RCK} / T _{CKR}	0.24 / 0	0.46 / 0	0.52 / 0	0.6 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T _{CH}	0.56	1.2	1.3	1.4	ns, min
Minimum Pulse Width, Low	T _{CL}	0.56	1.2	1.3	1.4	ns, min
Set/Reset						
Minimum Pulse Width, SR/BY inputs	T _{RPW}	0.94	1.9	2.1	2.4	ns, min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T _{RQ}	0.39	0.8	0.9	1.0	ns, max
Toggle Frequency (MHz) (for export control)	F _{TOG}	-	416	400	357	MHz

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Block RAM Switching Characteristics

		Speed Grade ⁽¹⁾				Units
Description	Symbol	Min	-8	-7	-6	
Sequential Delays						
Clock CLK to DOUT output	T _{BCKO}	0.63	2.46	3.1	3.5	ns, max
Setup and Hold Times before Clock CLK						
ADDR inputs	T _{BACK} /T _{BCKA}	0.42 / 0	0.9 / 0	1.0 / 0	1.1 / 0	ns, min
DIN inputs	T _{BDCK} /T _{BCKD}	0.42 / 0	0.9 / 0	1.0 / 0	1.1 / 0	ns, min
EN input	T _{BECK} /T _{BCKE}	0.97 / 0	2.0 / 0	2.2 / 0	2.5 / 0	ns, min
RST input	T _{BRCK} /T _{BCKR}	0.9 / 0	1.8 / 0	2.1 / 0	2.3 / 0	ns, min
WEN input	T _{BWCK} /T _{BCKW}	0.86 / 0	1.7 / 0	2.0 / 0	2.2 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T _{BPWH}	0.6	1.2	1.35	1.5	ns, min
Minimum Pulse Width, Low	T _{BPWL}	0.6	1.2	1.35	1.5	ns, min
CLKA -> CLKB setup time for different ports	T _{BCCS}	1.2	2.4	2.7	3.0	ns, min

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

TBUF Switching Characteristics

		Speed Grade				Units
Description	Symbol	Min	-8	-7	-6	
Combinatorial Delays						
IN input to OUT output	T _{IO}	0.0	0.0	0.0	0.0	ns, max
TRI input to OUT output high-impedance	T _{OFF}	0.05	0.092	0.10	0.11	ns, max
TRI input to valid data on OUT output	T _{ON}	0.05	0.092	0.10	0.11	ns, max

JTAG Test Access Port Switching Characteristics

Description	Symbol	Value	Units
TMS and TDI Setup times before TCK	T_{TAPTK}	4.0	ns, min
TMS and TDI Hold times after TCK	T_{TCKTAP}	2.0	ns, min
Output delay from clock TCK to output TDO	T_{TCKTDO}	11.0	ns, max
Maximum TCK clock frequency	F_{TCK}	33	MHz, max

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/7/99	1.0	Initial Xilinx release.
1/10/00	1.1	Re-released with spd.txt v. 1.18, FG860/900/1156 package information, and additional DLL, Select RAM and SelectI/O information.
1/28/00	1.2	Added Delay Measurement Methodology table, updated SelectI/O section, Figures 30, 54, & 55, text explaining Table 5, T_{BYP} values, buffered Hex Line info, p. 8, I/O Timing Measurement notes, notes for Tables 15, 16, and corrected F1156 pinout table footnote references.
2/29/00	1.3	Updated pinout tables, V_{CC} page 20, and corrected Figure 20.
5/23/00	1.4	Correction to table on p. 22.
7/10/00	1.5	- Numerous minor edits. - Data sheet upgraded to Preliminary. - Preview -8 numbers added to Virtex-E Electrical Characteristics tables.
8/1/00	1.6	- Reformatted entire document to follow new style guidelines. - Changed speed grade values in tables on pages 35-37.
9/20/00	1.7	- Min values added to Virtex-E Electrical Characteristics tables. - XCV2600E and XCV3200E numbers added to Virtex-E Electrical Characteristics tables (Module 3). - Corrected user I/O count for XCV100E device in Table 1 (Module 1). - Changed several pins to "No Connect in the XCV100E" and removed duplicate V_{CCINT} pins in Table ~ (Module 4). - Changed pin J10 to "No connect in XCV600E" in Table 74 (Module 4). - Changed pin J30 to "VREF option only in the XCV600E" in Table 74 (Module 4). - Corrected pair 18 in Table 75 (Module 4) to be "AO in the XCV1000E, XCV1600E".
11/20/00	1.8	- Upgraded speed grade -8 numbers in Virtex-E Electrical Characteristics tables to Preliminary. - Updated minimums in Table 13 and added notes to Table 14. - Added to note 2 to Absolute Maximum Ratings. - Changed speed grade -8 numbers for $T_{SHCKO32}$, T_{REG}, T_{BCCS}, and T_{ICKOF}. - Changed all minimum hold times to -0.4 under Global Clock Set-Up and Hold for LVTTTL Standard, with DLL. - Revised maximum T_{DLLPW} in -6 speed grade for DLL Timing Parameters. - Changed GCLK0 to BA22 for FG860 package in Table 46.
2/12/01	1.9	- Revised footnote for Table 14. - Added numbers to Virtex-E Electrical Characteristics tables for XCV1000E and XCV2000E devices. - Updated Table 27 and Table 78 to include values for XCV400E and XCV600E devices. - Revised Table 62 to include pinout information for the XCV400E and XCV600E devices in the BG560 package. - Updated footnotes 1 and 2 for Table 76 to include XCV2600E and XCV3200E devices.
4/02/01	2.0	- Updated numerous values in Virtex-E Switching Characteristics tables. - Converted data sheet to modularized format. See the Virtex-E Data Sheet section.
4/19/01	2.1	Updated values in Virtex-E Switching Characteristics tables.

Low Voltage Differential Signals

The Virtex-E family incorporates low-voltage signalling (LVDS and LVPECL). Two pins are utilized for these signals to be connected to a Virtex-E device. These are known as differential pin pairs. Each differential pin pair has a Positive (P) and a Negative (N) pin. These pairs are labeled in the following manner.

IO_L#[P/N]

where

L = LVDS or LVPECL pin

= Pin Pair Number

P = Positive

N = Negative

I/O pins for differential signals can either be synchronous or asynchronous, input or output. The pin pairs can be used for synchronous input and output signals as well as asynchronous input signals. However, only some of the low-voltage pairs can be used for asynchronous output signals.

Differential signals require the pins of a pair to switch almost simultaneously. If the signals driving the pins are from IOB flip-flops, they are synchronous. If the signals driving the pins are from internal logic, they are asynchronous. [Table 2](#) defines the names and function of the different types of low-voltage pin pairs in the Virtex-E family.

Table 2: LVDS Pin Pairs

Pin Name	Description
IO_L#[P/N] Example: IO_L22N	Represents a general IO or a synchronous input/output differential signal. When used as a differential signal, N means Negative I/O and P means Positive I/O.
IO_L#[P/N]_Y Example: IO_L22N_Y	Represents a general IO or a synchronous input/output differential signal, or a part-dependent asynchronous output differential signal.
IO_L#[P/N]_YY Example: O_L22N_YY	Represents a general IO or a synchronous input/output differential signal, or an asynchronous output differential signal.
IO_LVDS_DLL_L#[P/N] Example: IO_LVDS_DLL_L16N	Represents a general IO or a synchronous input/output differential signal, a differential clock input signal, or a DLL input. When used as a differential clock input, this pin is paired with the adjacent GCK pin. The GCK pin is always the positive input in the differential clock input configuration.

Virtex-E Package Pinouts

The Virtex-E family of FPGAs is available in 12 popular packages, including chip-scale, plastic and high heat-dissipation quad flat packs, and ball grid and fine-pitch ball grid arrays. Family members have footprint compatibility across devices provided in the same package. The pinout tables in

this section indicate function, pin, and bank information for each package/device combination. Following each pinout table is an additional table summarizing information specific to differential pin pairs for all devices provided in that package.

CS144 Chip-Scale Package

XCV50E, XCV100E, XCV200E, XCV300E and XCV400E devices in CS144 Chip-scale packages have footprint compatibility. In the CS144 package, bank pairs that share a side are internally interconnected, permitting four choices for V_{CCO} . See [Table 3](#).

Table 3: I/O Bank Pairs and Shared V_{CCO} Pins

Paired Banks	Shared V_{CCO} Pins
Banks 0 & 1	A2, A13, D7
Banks 2 & 3	B12, G11, M13
Banks 4 & 5	N1, N7, N13
Banks 6 & 7	B2, G2, M2

Pins labeled IO_VREF can be used as either in all parts unless device-dependent, as indicated in the footnotes. If the pin is not used as V_{REF} , it can be used as general I/O. Immediately following [Table 4](#), see [Table 5](#) is Differential Pair information.

Table 4: CS144 — XCV50E, XCV100E, XCV200E

Bank	Pin Description	Pin #
0	GCK3	A6
0	IO	B3
0	IO_VREF_L0N_YY	B4 ²
0	IO_L0P_YY	A4
0	IO_L1N_YY	B5
0	IO_L1P_YY	A5
0	IO_LVDS_DLL_L2N	C6
0	IO_VREF	A3 ¹
0	IO_VREF	C4
0	IO_VREF	D6
1	GCK2	A7
1	IO	A8
1	IO_LVDS_DLL_L2P	B7
1	IO_L3N_YY	C8
1	IO_L3P_YY	D8
1	IO_L4N_YY	C9
1	IO_VREF_L4P_YY	D9 ²
1	IO_WRITE_L5N_YY	C10
1	IO_CS_L5P_YY	D10

Table 4: CS144 — XCV50E, XCV100E, XCV200E

Bank	Pin Description	Pin #
1	IO_VREF	A10
1	IO_VREF	B8
1	IO_VREF	B10 ¹
2	IO	D12
2	IO	F12
2	IO_DOUT_BUSY_L6P_YY	C11
2	IO_DIN_D0_L6N_YY	C12
2	IO_D1_L7N	E10
2	IO_VREF_L7P	D13 ²
2	IO_L8N_YY	E13
2	IO_D2_L8P_YY	E12
2	IO_D3_L9N	F11
2	IO_VREF_L9P	F10
2	IO_L10P	F13
2	IO_VREF	C13 ¹
2	IO_VREF	D11
3	IO	H13
3	IO	K13
3	IO_L10N	G13
3	IO_VREF_L11N	H11
3	IO_D4_L11P	H12
3	IO_D5_L12N_YY	J13
3	IO_L12P_YY	H10
3	IO_VREF_L13N	J10 ²
3	IO_D6_L13P	J11
3	IO_INIT_L14N_YY	L13
3	IO_D7_L14P_YY	K10
3	IO_VREF	K11 ¹
3	IO_VREF	K12
4	GCK0	K7
4	IO	M8
4	IO	M10

Table 8: HQ240 — XCV600E, XCV1000E

Pin #	Pin Description	Bank
P66	IO_VREF_L46P	5
P65	IO_L46N	5
P64	IO_L47P_YY	5
P63	IO_L47N_YY	5
P62	M2	NA
P61	VCCO	5
P60	M0	NA
P59	GND	NA
P58	M1	NA
P57	IO_L48N_YY	6
P56	IO_L48P_YY	6
P55	VCCO	6
P54	IO_VREF	6
P53	IO_L49N_Y	6
P52	IO_L49P_Y	6
P51	GND	NA
P50	IO_VREF_L50N_Y	6
P49	IO_L50P_Y	6
P48	IO_VREF	6
P47	IO_VREF_L51N_Y	6
P46	IO_L51P_Y	6
P45	GND	NA
P44	VCCO	6
P43	VCCINT	NA
P42	IO_L52N_YY	6
P41	IO_L52P_YY	6
P40 ¹	IO_VREF	6
P39	IO_L53N_Y	6
P38	IO_L53P_Y	6
P37	GND	NA
P36	IO_VREF_L54N_Y	6
P35	IO_L54P_Y	6
P34	IO_L55N_Y	6
P33	IO_VREF_L55P_Y	6
P32	VCCINT	NA
P31	IO	6

Table 8: HQ240 — XCV600E, XCV1000E

Pin #	Pin Description	Bank
P30	VCCO	6
P29	GND	NA
P28	IO_L56N_YY	7
P27	IO_L56P_YY	7
P26	IO_VREF	7
P25	VCCO	7
P24	IO_L57N_Y	7
P23	IO_VREF_L57P_Y	7
P22	GND	NA
P21	IO_L58N_Y	7
P20	IO_L58P_Y	7
P19 ¹	IO_VREF	7
P18	IO_L59N_YY	7
P17	IO_L59P_YY	7
P16	VCCINT	NA
P15	VCCO	7
P14	GND	NA
P13	IO_L60N_Y	7
P12	IO_VREF_L60P_Y	7
P11	IO_VREF	7
P10	IO_L61N_Y	7
P9	IO_VREF_L61P_Y	7
P8	GND	NA
P7	IO_L62N_Y	7
P6	IO_L62P_Y	7
P5	IO_VREF_L63N_Y	7
P4	IO_L63P_Y	7
P3	IO	7
P2	TMS	NA
P1	GND	NA

Notes:

1. V_{REF} or I/O option only in the XCV1000E; otherwise, I/O option only.

Table 14: BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin#	See Note
1	IO_L43N_Y	C5	
1	IO_VREF_L43P_Y	E7	3
1	IO_WRITE_L44N_YY	D6	
1	IO_CS_L44P_YY	A2	
2	IO	D3	
2	IO	F3	
2	IO	G1	
2	IO	J2	
2	IO_DOUT_BUSY_L45P_YY	D4	
2	IO_DIN_D0_L45N_YY	E4	
2	IO_L46P_Y	F5	
2	IO_VREF_L46N_Y	B3	3
2	IO_L47P_Y	F4	
2	IO_L47N_Y	C1	
2	IO_VREF_L48P_Y	G5	
2	IO_L48N_Y	E3	
2	IO_L49P_Y	D2	
2	IO_L49N_Y	G4	
2	IO_L50P_Y	H5	
2	IO_L50N_Y	E2	
2	IO_VREF_L51P_YY	H4	
2	IO_L51N_YY	G3	
2	IO_L52P_Y	J5	
2	IO_VREF_L52N_Y	F1	1
2	IO_L53P_Y	J4	
2	IO_L53N_Y	H3	
2	IO_VREF_L54P_Y	K5	4
2	IO_L54N_Y	H2	
2	IO_L55P_Y	J3	
2	IO_L55N_Y	K4	
2	IO_VREF_L56P_YY	L5	
2	IO_D1_L56N_YY	K3	
2	IO_D2_L57P_YY	L4	
2	IO_L57N_YY	K2	

Table 14: BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin#	See Note
2	IO_L58P_Y	M5	
2	IO_L58N_Y	L3	
2	IO_L59P_Y	L1	
2	IO_L59N_Y	M4	
2	IO_VREF_L60P_Y	N5	3
2	IO_L60N_Y	M2	
2	IO_L61P_Y	N4	
2	IO_L61N_Y	N3	
2	IO_L62P_Y	N2	
2	IO_L62N_Y	P5	
2	IO_VREF_L63P_YY	P4	
2	IO_D3_L63N_YY	P3	
2	IO_L64P_Y	P2	
2	IO_L64N_Y	R5	
2	IO_L65P_Y	R4	
2	IO_L65N_Y	R3	
2	IO_VREF_L66P_Y	R1	
2	IO_L66N_Y	T4	
2	IO_L67P_Y	T5	
2	IO_VREF_L67N_Y	T3	2
2	IO_L68P_YY	T2	
2	IO_L68N_YY	U3	
3	IO	AE3	
3	IO	AF3	
3	IO	AH3	
3	IO	AK3	
3	IO_VREF_L69P_Y	U1	2
3	IO_L69N_Y	U2	
3	IO_L70P_Y	V2	
3	IO_VREF_L70N_Y	V4	
3	IO_L71P_Y	V5	
3	IO_L71N_Y	V3	
3	IO_L72P_Y	W1	
3	IO_L72N_Y	W3	

Table 18: FG456 — XCV200E and XCV300E

Bank	Pin Description	Pin #
5	IO_L76N_Y	W11
5	IO_L77P_YY	V11
5	IO_VREF_L77N_YY	Y10
5	IO_L78P_YY	AB10
5	IO_L78N_YY	W10
5	IO_L79P_Y	V10
5	IO_L79N_Y	Y9
5	IO_L80P_Y	AB9
5	IO_L80N_Y	W9
5	IO_L81P_YY	V9
5	IO_L81N_YY	AA8
5	IO_L82P_YY	Y8
5	IO_VREF_L82N_YY	W8
5	IO_L83P_Y	W7
5	IO_L83N_Y	AA7
5	IO_L84P_Y	AB6
5	IO_L84N_Y	AA6
5	IO_L85P_YY	AB5
5	IO_VREF_L85N_YY	AA5
5	IO_L86P_YY	Y7
5	IO_L86N_YY	W6
5	IO_L87P_YY	AA4
5	IO_VREF_L87N_YY	Y6
5	IO_L88P_YY	V7
5	IO_L88N_YY	AB3
6	IO	M2 ¹
6	IO	M5
6	IO	P4
6	IO	R3 ¹
6	IO	T2
6	IO	T4
6	IO	U3 ¹
6	IO	W2
6	IO	AA1 ¹
6	IO_L89N_YY	W3
6	IO_L89P_YY	Y2

Table 18: FG456 — XCV200E and XCV300E

Bank	Pin Description	Pin #
6	IO_L90N_YY	V4
6	IO_L90P_YY	V3
6	IO_VREF_L91N_YY	Y1
6	IO_L91P_YY	U4
6	IO_L92N_YY	V2
6	IO_L92P_YY	W1
6	IO_VREF_L93N_YY	T3
6	IO_L93P_YY	U2
6	IO_L94N_Y	T5
6	IO_L94P_Y	V1
6	IO_L95N_Y	R5
6	IO_L95P_Y	U1
6	IO_VREF_L96N_Y	R4
6	IO_L96P_Y	T1
6	IO_L97N_YY	R2
6	IO_L97P_YY	P3
6	IO_L98N_YY	P5
6	IO_L98P_YY	R1
6	IO_L99N_YY	P2
6	IO_L99P_YY	N5
6	IO_L100N_Y	P1
6	IO_L100P_Y	N4
6	IO_L101N	N3
6	IO_VREF_L101P	N2
6	IO_L102N_Y	N1
6	IO_L102P_Y	M4
6	IO_L103N_YY	M3
6	IO_L103P_YY	M6
6	IO	M1
7	IO	B1
7	IO	C2 ¹
7	IO	D1 ¹
7	IO	E4
7	IO	F4
7	IO	G2 ¹
7	IO	G4

Table 18: FG456 — XCV200E and XCV300E

Bank	Pin Description	Pin #
7	IO	J1
7	IO	J4
7	IO	L2 ¹
7	IO_L104N_YY	L3
7	IO_L104P_YY	L4
7	IO_L105N_YY	L5
7	IO_L105P_YY	L1
7	IO_L106N_Y	L6
7	IO_L106P_Y	K2
7	IO_L107N_Y	K4
7	IO_VREF_L107P_Y	K3
7	IO_L108N_YY	K1
7	IO_L108P_YY	K5
7	IO_L109N_YY	J3
7	IO_L109P_YY	J2
7	IO_L110N_YY	J5
7	IO_L110P_YY	H1
7	IO_L111N_YY	H2
7	IO_L111P_YY	H3
7	IO_L112N_Y	G1
7	IO_VREF_L112P_Y	H4
7	IO_L113N_Y	F1
7	IO_L113P_Y	F2
7	IO_L114N_YY	H5
7	IO_L114P_YY	G3
7	IO_L115N_YY	E1
7	IO_VREF_L115P_YY	E2
7	IO_L116N_YY	F3
7	IO_L116P_YY	G5
7	IO_L117N_YY	E3
7	IO_VREF_L117P_YY	D2
7	IO_L118N_YY	F5
7	IO_L118P_YY	C1
2	CCLK	B22
3	DONE	Y19
NA	DXN	Y5

Table 18: FG456 — XCV200E and XCV300E

Bank	Pin Description	Pin #
NA	DXP	V6
NA	M0	AB2
NA	M1	U5
NA	M2	Y4
NA	PROGRAM	W20
NA	TCK	C4
NA	TDI	B20
2	TDO	A21
NA	TMS	D3
NA	NC	W19
NA	NC	W4
NA	NC	D19
NA	NC	D4
NA	VCCINT	E5
NA	VCCINT	E18
NA	VCCINT	F6
NA	VCCINT	F17
NA	VCCINT	G7
NA	VCCINT	G8
NA	VCCINT	G9
NA	VCCINT	G14
NA	VCCINT	G15
NA	VCCINT	H7
NA	VCCINT	G16
NA	VCCINT	H16
NA	VCCINT	J7
NA	VCCINT	J16
NA	VCCINT	P7
NA	VCCINT	P16
NA	VCCINT	R7
NA	VCCINT	R16
NA	VCCINT	T7
NA	VCCINT	T8
NA	VCCINT	T9
NA	VCCINT	T14

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
7	IO	D2
7	IO	D3
7	IO	E1
7	IO	G1
7	IO	H2
7	IO	J1 ¹
7	IO	L1 ¹
7	IO	M1 ¹
7	IO	N1 ¹
7	IO_L160N_YY	N5
7	IO_L160P_YY	N8
7	IO_L161N_YY	N6
7	IO_L161P_YY	N3
7	IO_L162N_Y	N4
7	IO_VREF_L162P_Y	M2
7	IO_L163N_Y	N7
7	IO_L163P_Y	M7
7	IO_L164N_YY	M6
7	IO_L164P_YY	M3
7	IO_L165N_YY	M4
7	IO_VREF_L165P_YY	M5
7	IO_L166N_Y	L3
7	IO_L166P_Y	L7
7	IO_L167N_Y	L6
7	IO_L167P_Y	K2
7	IO_L168N_Y	L4
7	IO_L168P_Y	K1
7	IO_L169N_Y	K3
7	IO_L169P_Y	L5
7	IO_L170N_YY	K5
7	IO_L170P_YY	J3
7	IO_L171N_YY	K4
7	IO_L171P_YY	J4
7	IO_L172N_YY	H3
7	IO_VREF_L172P_YY	K6
7	IO_L173N_YY	K7
7	IO_L173P_YY	G3

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
7	IO_L174N_Y	J5
7	IO_VREF_L174P_Y	H1 ²
7	IO_L175N_Y	G2
7	IO_L175P_Y	J6
7	IO_L176N_YY	J7
7	IO_L176P_YY	F1
7	IO_L177N_YY	H4
7	IO_VREF_L177P_YY	G4
7	IO_L178N_Y	F3
7	IO_L178P_Y	H5
7	IO_L179N_Y	E2
7	IO_L179P_Y	H6
7	IO_L180N_Y	G5
7	IO_VREF_L180P_Y	F4
7	IO_L181N_Y	H7
7	IO_L181P_Y	G6
7	IO_L182N_YY	E3
7	IO_L182P_YY	E4
2	CCLK	D24
3	DONE	AB21
NA	DXN	AB7
NA	DXP	Y8
NA	M0	AD4
NA	M1	W7
NA	M2	AB6
NA	PROGRAM	AA22
NA	TCK	E6
NA	TDI	D22
2	TDO	C23
NA	TMS	F5
NA	NC	T25
NA	NC	T2
NA	NC	P2
NA	NC	N25
NA	NC	L25

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
NA	NC	L2
NA	NC	F6
NA	NC	F25
NA	NC	F21
NA	NC	F2
NA	NC	C26
NA	NC	C25
NA	NC	C2
NA	NC	C1
NA	NC	B6
NA	NC	B26
NA	NC	B24
NA	NC	B21
NA	NC	B16
NA	NC	B11
NA	NC	B1
NA	NC	AF25
NA	NC	AF24
NA	NC	AF2
NA	NC	AE6
NA	NC	AE3
NA	NC	AE26
NA	NC	AE24
NA	NC	AE21
NA	NC	AE16
NA	NC	AE14
NA	NC	AE11
NA	NC	AE1
NA	NC	AD25
NA	NC	AD2
NA	NC	AD1
NA	NC	AA6
NA	NC	AA25
NA	NC	AA21
NA	NC	AA2
NA	NC	A3
NA	NC	A25

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
NA	NC	A2
NA	NC	A15
NA	VCCINT	G7
NA	VCCINT	G20
NA	VCCINT	H8
NA	VCCINT	H19
NA	VCCINT	J9
NA	VCCINT	J10
NA	VCCINT	J11
NA	VCCINT	J16
NA	VCCINT	J17
NA	VCCINT	J18
NA	VCCINT	K9
NA	VCCINT	K18
NA	VCCINT	L9
NA	VCCINT	L18
NA	VCCINT	T9
NA	VCCINT	T18
NA	VCCINT	U9
NA	VCCINT	U18
NA	VCCINT	V9
NA	VCCINT	V10
NA	VCCINT	V11
NA	VCCINT	V16
NA	VCCINT	V17
NA	VCCINT	V18
NA	VCCINT	Y7
NA	VCCINT	Y20
NA	VCCINT	W8
NA	VCCINT	W19
0	VCCO	J13
0	VCCO	J12
0	VCCO	H9
0	VCCO	H12
0	VCCO	H11

FG680 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A ✓ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 23: FG680 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
GCLK LVDS					
3	0	A20	C22	NA	IO_DLL_L29N
2	1	D21	A19	NA	IO_DLL_L29P
1	5	AU22	AT22	NA	IO_DLL_L155N
0	4	AW19	AT21	NA	IO_DLL_L155P
IO LVDS					
Total Pairs: 247, Asynchronous Output Pairs: 111					
0	0	A36	C35	5	-
1	0	B35	D34	5	VREF
2	0	A35	C34	✓	-
3	0	B34	D33	✓	VREF
4	0	A34	C33	3	-
5	0	B33	D32	3	-
6	0	D31	C32	✓	-
7	0	C31	A33	✓	VREF
8	0	B31	B32	5	-
9	0	D30	A32	5	VREF
10	0	C30	A31	✓	-
11	0	D29	B30	✓	VREF
12	0	C29	A30	2	-
13	0	B29	A29	2	-
14	0	A28	B28	✓	VREF
15	0	B27	C28	✓	-
16	0	A27	D27	5	-
17	0	B26	C27	5	-

Table 23: FG680 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
18	0	C26	D26	✓	-
19	0	D25	A26	✓	VREF
20	0	C25	B25	3	-
21	0	D24	A25	3	-
22	0	B23	A24	✓	-
23	0	A23	C24	✓	VREF
24	0	B22	B24	5	-
25	0	A22	E23	5	-
26	0	B21	D23	✓	-
27	0	A21	C23	✓	VREF
28	0	B20	E22	2	-
29	1	A19	C22	NA	IO_LVDS_DLL
30	1	B19	C21	2	VREF
31	1	A18	C19	2	-
32	1	B18	D19	✓	VREF
33	1	A17	C18	✓	-
34	1	B17	D18	5	-
35	1	A16	E18	5	-
36	1	D17	C17	✓	VREF
37	1	E17	B16	✓	-
38	1	C16	A15	3	-
39	1	D16	B15	3	-
40	1	B14	A14	✓	VREF
41	1	A13	C15	✓	-
42	1	B13	D15	5	-
43	1	A12	C14	5	-
44	1	C13	D14	✓	-
45	1	D13	B12	✓	VREF
46	1	C12	A11	2	-
47	1	C11	B11	2	-
48	1	D11	A10	✓	VREF
49	1	C10	B10	✓	-
50	1	D10	A9	5	VREF
51	1	C9	B9	5	-

Table 25: FG860 Differential Pin Pair Summary
XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
188	5	AY27	AV28	√	-
189	5	BA27	AW29	5	-
190	5	BB28	AV29	1	-
191	5	AY28	AW30	1	-
192	5	BA28	AW31	2	-
193	5	BB29	AV31	√	-
194	5	AY29	AY32	√	VREF
195	5	AW32	BB30	2	-
196	5	AV32	AY30	2	-
197	5	BA30	AW33	√	VREF
198	5	BB31	AV33	√	-
199	5	AY34	BA31	1	VREF
200	5	AW34	BB32	1	-
201	5	BA32	AY35	√	VREF
202	5	BB33	AW35	√	-
203	5	AV35	BB34	5	-
204	5	AY36	BA34	5	-
205	5	BB35	AV36	√	VREF
206	5	BA35	AY37	√	-
207	5	BB36	BA36	5	-
208	5	AW37	BB37	1	VREF
209	5	BA37	AY38	1	-
210	5	BB38	AY39	2	-
211	6	AV42	AV41	√	-
212	6	AU41	AW40	3	-
213	6	AU42	AV39	1	-
214	6	AU38	AT41	2	VREF
215	6	AV40	AT42	4	-
216	6	AU39	AR41	2	-
217	6	AU40	AR42	1	VREF
218	6	AP42	AT38	√	-
219	6	AT39	AN41	2	-
220	6	AM40	AT40	1	-
221	6	AM41	AR38	√	VREF

Table 25: FG860 Differential Pin Pair Summary
XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
222	6	AR40	AM42	√	-
223	6	AP38	AL40	5	VREF
224	6	AL42	AP39	2	-
225	6	AK40	AP40	√	VREF
226	6	AN39	AK41	√	-
227	6	AN40	AK42	2	-
228	6	AJ41	AM38	√	VREF
229	6	AM39	AJ42	√	-
230	6	AH41	AH40	3	-
231	6	AH42	AL38	1	-
232	6	AG41	AL39	2	-
233	6	AG40	AK39	4	-
234	6	AG42	AJ38	2	-
235	6	AJ39	AF42	1	VREF
236	6	AH38	AF41	√	-
237	6	AH39	AE42	2	-
238	6	AE41	AG38	1	-
239	6	AD42	AG39	√	VREF
240	6	AF39	AD40	√	-
241	6	AE38	AD41	5	-
242	6	AC40	AE39	2	-
243	6	AC41	AD38	√	VREF
244	6	AC38	AB42	√	-
245	6	AC39	AB40	2	VREF
246	7	AB39	AA41	√	-
247	7	AA39	Y41	2	VREF
248	7	Y39	Y40	√	-
249	7	W41	Y38	√	VREF
250	7	W39	W40	2	-
251	7	V41	W38	5	-
252	7	V40	V39	√	-
253	7	U39	V42	√	VREF
254	7	U38	U41	1	-
255	7	T39	U42	2	-

Table 27: FG900 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
120	3	AA30	W24	4	-
121	3	AA29	V20	1	-
122	3	Y27	W23	NA	-
123	3	Y26	AB30	√	D5
124	3	V21	AA28	√	VREF
125	3	Y25	AA27	4	-
126	3	W22	Y23	4	-
127	3	Y24	AB28	4	VREF
128	3	AC30	AA25	√	-
129	3	W21	AA24	2	-
130	3	AB26	AD30	√	-
131	3	Y22	AC27	√	VREF
132	3	AD28	AB25	2	-
133	3	AC26	AE30	4	-
134	3	AD27	AF30	√	-
135	3	AF29	AB24	1	VREF
136	3	AB23	AE28	4	-
137	3	AG30	AC25	3	-
138	3	AE26	AG29	4	VREF
139	3	AH30	AC24	1	-
140	3	AF28	AD25	NA	-
141	3	AH29	AA22	√	INIT
142	4	AF27	AK28	√	-
143	4	AG26	AH27	4	-
144	4	AD23	AJ27	2	-
145	4	AB21	AF25	2	VREF
146	4	AC22	AH26	2	-
147	4	AA21	AG25	√	-
148	4	AJ26	AD22	√	VREF
149	4	AA20	AH25	1	-
150	4	AC21	AF24	1	-
151	4	AG24	AK26	√	-
152	4	AJ24	AF23	√	VREF
153	4	AE23	AB20	2	-

Table 27: FG900 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
154	4	AC20	AG23	2	-
155	4	AF22	AE22	√	-
156	4	AJ22	AG22	√	VREF
157	4	AK24	AD20	NA	-
158	4	AA19	AF21	4	-
159	4	AH22	AA18	NA	VREF
160	4	AG21	AK23	NA	-
161	4	AH21	AD19	4	-
162	4	AE20	AJ21	2	-
163	4	AG20	AF20	2	-
164	4	AC18	AF19	2	-
165	4	AJ20	AE19	√	-
166	4	AK22	AH20	√	VREF
167	4	AG19	AB17	1	-
168	4	AJ19	AD17	1	-
169	4	AA16	AA17	√	-
170	4	AK21	AB16	√	VREF
171	4	AG18	AK20	2	-
172	4	AK19	AD16	2	-
173	4	AE16	AE17	√	-
174	4	AG17	AJ17	√	VREF
175	4	AD15	AH17	NA	-
176	4	AG16	AK17	4	VREF
177	5	AF16	AH16	NA	IO_LVDS_DLL
178	5	AC15	AG15	4	VREF
179	5	AB15	AF15	√	-
180	5	AA15	AF14	√	VREF
181	5	AH15	AK15	√	-
182	5	AB14	AF13	2	-
183	5	AH14	AJ14	2	-
184	5	AE14	AG13	√	VREF
185	5	AK13	AD13	√	-
186	5	AE13	AF12	1	-
187	5	AC13	AA13	1	-

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
2	IO_L92N_Y	H29
2	IO_L93P_YY	J28 ⁴
2	IO_L93N_YY	E33 ⁵
2	IO_L94P_YY	H28
2	IO_L94N_YY	H30
2	IO_L95P_Y	H32
2	IO_L95N_Y	K28
2	IO_L96P_Y	L27 ⁴
2	IO_L96N_Y	F33 ⁵
2	IO_L97P_Y	M26
2	IO_L97N_Y	E34
2	IO_VREF_L98P_YY	H31
2	IO_L98N_YY	G32
2	IO_L99P_YY	N25 ⁴
2	IO_L99N_YY	J31 ⁵
2	IO_L100P_YY	J30
2	IO_L100N_YY	G33
2	IO_VREF_L101P_Y	H34 ²
2	IO_L101N_Y	J29
2	IO_L102P	M27 ⁴
2	IO_L102N	H33 ⁵
2	IO_L103P_Y	K29
2	IO_L103N_Y	J34
2	IO_VREF_L104P_YY	L29
2	IO_L104N_YY	J33
2	IO_L105P_YY	M28
2	IO_L105N_YY	K34
2	IO_L106P_Y	N27
2	IO_L106N_Y	L34
2	IO_VREF_L107P_YY	K33
2	IO_D1_L107N_YY	P26
2	IO_L108P_Y	R25
2	IO_L108N_Y	M34
2	IO_L109P_Y	L31

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
2	IO_L109N_Y	L33
2	IO_L110P_Y	P27
2	IO_L110N_Y	M33
2	IO_L111P	M31
2	IO_L111N	R26
2	IO_L112P_Y	N30
2	IO_L112N_Y	P28
2	IO_VREF_L113P_Y	N29
2	IO_L113N_Y	N33
2	IO_L114P_YY	T25 ⁴
2	IO_L114N_YY	N34 ⁵
2	IO_L115P_YY	P34
2	IO_L115N_YY	R27
2	IO_L116P_Y	P29
2	IO_L116N_Y	P31
2	IO_L117P_Y	P33 ⁴
2	IO_L117N_Y	T26 ⁵
2	IO_L118P_Y	R34
2	IO_L118N_Y	R28
2	IO_VREF_L119P_YY	N31
2	IO_D3_L119N_YY	N32
2	IO_L120P_YY	P30 ⁴
2	IO_L120N_YY	R33 ⁵
2	IO_L121P_YY	R29
2	IO_L121N_YY	T34
2	IO_L122P_Y	R30
2	IO_L122N_Y	T30
2	IO_L123P	T28 ⁴
2	IO_L123N	R31 ⁵
2	IO_L124P_Y	T29
2	IO_L124N_Y	U27
2	IO_VREF_L125P_YY	T31
2	IO_L125N_YY	T33
2	IO_L126P_YY	U28

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
6	IO_VREF_L265N_Y	AJ3
6	IO_L265P_Y	AG5
6	IO_L266N_YY	AD9 ⁴
6	IO_L266P_YY	AJ2 ⁵
6	IO_L267N_YY	AC10
6	IO_L267P_YY	AH2
6	IO_L268N_Y	AH3
6	IO_L268P_Y	AF5
6	IO_L269N_Y	AE8 ⁴
6	IO_L269P_Y	AG3 ⁵
6	IO_L270N_Y	AE7
6	IO_L270P_Y	AG2
6	IO_VREF_L271N_YY	AF6
6	IO_L271P_YY	AG1
6	IO_L272N_YY	AC9 ⁴
6	IO_L272P_YY	AG4 ⁵
6	IO_L273N_YY	AE6
6	IO_L273P_YY	AF3
6	IO_VREF_L274N_Y	AF1 ²
6	IO_L274P_Y	AF4
6	IO_L275N	AB10 ⁴
6	IO_L275P	AF2 ⁵
6	IO_L276N_Y	AC8
6	IO_L276P_Y	AE1
6	IO_VREF_L277N_YY	AD5
6	IO_L277P_YY	AE3
6	IO_L278N_YY	AC7
6	IO_L278P_YY	AD1
6	IO_L279N_Y	AD6
6	IO_L279P_Y	AD2
6	IO_VREF_L280N_YY	AB8
6	IO_L280P_YY	AC1
6	IO_L281N_YY	AC5
6	IO_L281P_YY	AC2

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
6	IO_L282N_Y	AA9
6	IO_L282P_Y	AC3
6	IO_L283N_Y	AC4
6	IO_L283P_Y	AD4
6	IO_L284N_Y	AA8
6	IO_L284P_Y	AB6
6	IO_L285N	AB1
6	IO_L285P	Y10
6	IO_L286N_Y	AB2
6	IO_L286P_Y	AA7
6	IO_VREF_L287N_Y	AA4
6	IO_L287P_Y	AA1
6	IO_L288N_YY	Y9 ⁴
6	IO_L288P_YY	AB4 ⁵
6	IO_L289N_YY	AA2
6	IO_L289P_YY	Y8
6	IO_L290N_Y	AA6
6	IO_L290P_Y	AA5
6	IO_L291N_Y	AB3 ⁴
6	IO_L291P_Y	Y7 ⁵
6	IO_L292N_Y	Y1
6	IO_L292P_Y	W10
6	IO_VREF_L293N_YY	Y5
6	IO_L293P_YY	Y2
6	IO_L294N_YY	W9 ⁴
6	IO_L294P_YY	W2 ⁵
6	IO_L295N_YY	W7
6	IO_L295P_YY	Y4
6	IO_L296N_Y	W1
6	IO_L296P_Y	Y6
6	IO_L297N_Y	W6 ⁴
6	IO_L297P_Y	W3 ⁵
6	IO_L298N_Y	V9
6	IO_L298P_Y	W4