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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	9600
Number of Logic Elements/Cells	43200
Total RAM Bits	655360
Number of I/O	804
Number of Gates	2541952
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1156-BBGA
Supplier Device Package	1156-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv2000e-8fg1156c

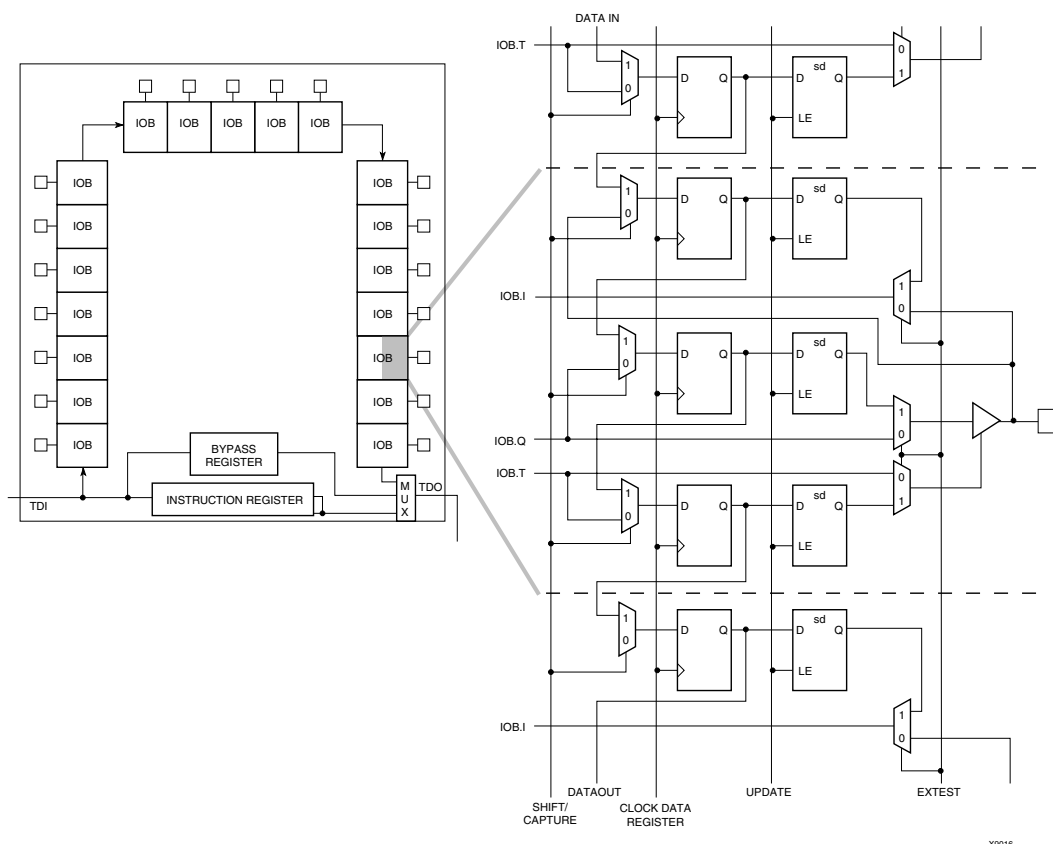


Figure 11: Virtex-E Family Boundary Scan Logic

Instruction Set

The Virtex-E series Boundary Scan instruction set also includes instructions to configure the device and read back configuration data (CFG_IN, CFG_OUT, and JSTART). The complete instruction set is coded as shown in Table 6..

Table 6: Boundary Scan Instructions

Boundary Scan Command	Binary Code(4:0)	Description
EXTEST	00000	Enables Boundary Scan EXTEST operation
SAMPLE/PRELOAD	00001	Enables Boundary Scan SAMPLE/PRELOAD operation
USER1	00010	Access user-defined register 1
USER2	00011	Access user-defined register 2
CFG_OUT	00100	Access the configuration bus for read operations.

Table 6: Boundary Scan Instructions (Continued)

Boundary Scan Command	Binary Code(4:0)	Description
CFG_IN	00101	Access the configuration bus for write operations.
INTEST	00111	Enables Boundary Scan INTEST operation
USERCODE	01000	Enables shifting out USER code
IDCODE	01001	Enables shifting out of ID Code
HIGHZ	01010	3-states output pins while enabling the Bypass Register
JSTART	01100	Clock the start-up sequence when StartupClk is TCK
BYPASS	11111	Enables BYPASS
RESERVED	All other codes	Xilinx reserved instructions

The voltage reference signal is “banked” within the Virtex-E device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 38 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

IBUF placement restrictions require that any differential amplifier input signals within a bank be of the same standard. How to specify a specific location for the IBUF via the LOC property is described below. Table 19 summarizes the Virtex-E input standards compatibility requirements.

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element by default activates to ensure a zero hold-time requirement. The NODELAY=TRUE property overrides this default.

When the IBUF does not drive a flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

Table 19: Xilinx Input Standards Compatibility Requirements

Rule 1	Standards with the same input V_{CCO} , output V_{CCO} , and V_{REF} can be placed within the same bank.
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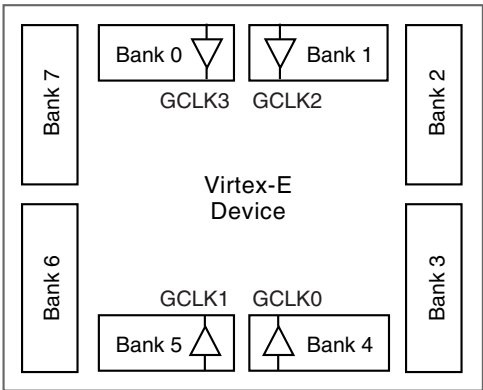


Figure 38: Virtex-E I/O Banks

IBUFG

Signals used as high fanout clock inputs to the Virtex-E device should drive a global clock input buffer (IBUFG) via an external input port in order to take advantage of one of the four dedicated global clock distribution networks. The output of the IBUFG should only drive a CLKDLL,

CLKDLLHF, or BUFG symbol. The generic Virtex-E IBUFG symbol appears in Figure 39.

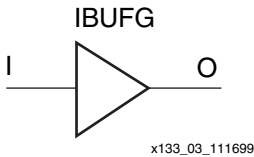


Figure 39: Virtex-E Global Clock Input Buffer (IBUFG) Symbol

The extension to the base name determines which I/O standard is used by the IBUFG. With no extension specified for the generic IBUFG symbol, the assumed standard is LVTTTL.

The following list details variations of the IBUFG symbol.

- IBUFG
- IBUFG_LVCMOS2
- IBUFG_PCI33_3
- IBUFG_PCI66_3
- IBUFG_GTL
- IBUFG_GTLP
- IBUFG_HSTL_I
- IBUFG_HSTL_III
- IBUFG_HSTL_IV
- IBUFG_SSTL3_I
- IBUFG_SSTL3_II
- IBUFG_SSTL2_I
- IBUFG_SSTL2_II
- IBUFG_CTT
- IBUFG_AGP
- IBUFG_LVCMOS18
- IBUFG_LVDS
- IBUFG_LVPECL

When the IBUFG symbol supports an I/O standard that requires a differential amplifier input, the IBUFG automatically configures as a differential amplifier input buffer. The low-voltage I/O standards with a differential amplifier input require an external reference voltage input V_{REF} .

The voltage reference signal is “banked” within the Virtex-E device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 38 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

IBUFG placement restrictions require any differential amplifier input signals within a bank be of the same standard. The LOC property can specify a location for the IBUFG.

As an added convenience, the BUFGP can be used to instantiate a high fanout clock input. The BUFGP symbol

represents a combination of the LVTTTL IBUFG and BUFG symbols, such that the output of the BUFGP can connect directly to the clock pins throughout the design.

Unlike previous architectures, the Virtex-E BUFGP symbol can only be placed in a global clock pad location. The LOC property can specify a location for the BUFGP.

OBUF

An OBUF must drive outputs through an external output port. The generic output buffer (OBUF) symbol appears in [Figure 40](#).

The extension to the base name defines which I/O standard the OBUF uses. With no extension specified for the generic OBUF symbol, the assumed standard is slew rate limited LVTTTL with 12 mA drive strength.

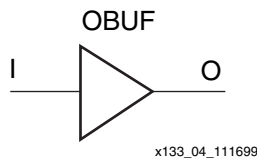


Figure 40: Virtex-E Output Buffer (OBUF) Symbol

The LVTTTL OBUF additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTTL output buffers have selectable drive strengths.

The format for LVTTTL OBUF symbol names is as follows:

OBUF_<slew_rate>_<drive_strength>

where <slew_rate> is either F (Fast) or S (Slow), and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

The following list details variations of the OBUF symbol.

- OBUF
- OBUF_S_2
- OBUF_S_4
- OBUF_S_6
- OBUF_S_8
- OBUF_S_12
- OBUF_S_16
- OBUF_S_24
- OBUF_F_2
- OBUF_F_4
- OBUF_F_6
- OBUF_F_8
- OBUF_F_12
- OBUF_F_16
- OBUF_F_24
- OBUF_LVCMOS2
- OBUF_PCI33_3

- OBUF_PCI66_3
- OBUF_GTL
- OBUF_GTLP
- OBUF_HSTL_I
- OBUF_HSTL_III
- OBUF_HSTL_IV
- OBUF_SSTL3_I
- OBUF_SSTL3_II
- OBUF_SSTL2_I
- OBUF_SSTL2_II
- OBUF_CTT
- OBUF_AGP
- OBUF_LVCMOS18
- OBUF_LVDS
- OBUF_LVPECL

The Virtex-E series supports eight banks for the HQ and PQ packages. The CS packages support four V_{CCO} banks.

OBUF placement restrictions require that within a given V_{CCO} bank each OBUF share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within any V_{CCO} bank. [Table 20](#) summarizes the Virtex-E output compatibility requirements. The LOC property can specify a location for the OBUF.

Table 20: Output Standards Compatibility Requirements

Rule 1	Only outputs with standards that share compatible V_{CCO} can be used within the same bank.
Rule 2	There are no placement restrictions for outputs with standards that do not require a V_{CCO} .
V_{CCO}	Compatible Standards
3.3	LVTTTL, SSTL3_I, SSTL3_II, CTT, AGP, GTL, GTL+, PCI33_3, PCI66_3
2.5	SSTL2_I, SSTL2_II, LVCMOS2, GTL, GTL+
1.5	HSTL_I, HSTL_III, HSTL_IV, GTL, GTL+

OBUFT

The generic 3-state output buffer OBUFT (see [Figure 41](#)) typically implements 3-state outputs or bidirectional I/O.

The extension to the base name defines which I/O standard OBUFT uses. With no extension specified for the generic OBUFT symbol, the assumed standard is slew rate limited LVTTTL with 12 mA drive strength.

The LVTTTL OBUFT additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

Application Examples

Creating a design with the SelectI/O features requires the instantiation of the desired library symbol within the design code. At the board level, designers need to know the termination techniques required for each I/O standard.

This section describes some common application examples illustrating the termination techniques recommended by each of the standards supported by the SelectI/O features.

Termination Examples

Circuit examples involving typical termination techniques for each of the SelectI/O standards follow. For a full range of accepted values for the DC voltage specifications for each standard, refer to the table associated with each figure.

The resistors used in each termination technique example and the transmission lines depicted represent board level components and are not meant to represent components on the device.

GTL

A sample circuit illustrating a valid termination technique for GTL is shown in Figure 44.

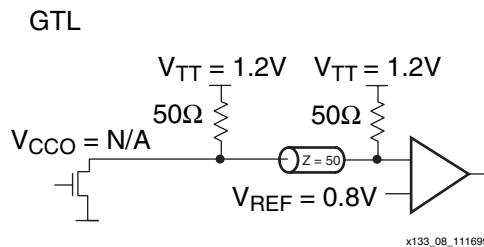


Figure 44: Terminated GTL

Table 23 lists DC voltage specifications.

Table 23: GTL Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	-	N/A	-
$V_{REF} = N \times V_{TT}^1$	0.74	0.8	0.86
V_{TT}	1.14	1.2	1.26
$V_{IH} = V_{REF} + 0.05$	0.79	0.85	-
$V_{IL} = V_{REF} - 0.05$	-	0.75	0.81
V_{OH}	-	-	-
V_{OL}	-	0.2	0.4
I_{OH} at V_{OH} (mA)	-	-	-
I_{OL} at V_{OL} (mA) at 0.4V	32	-	-
I_{OL} at V_{OL} (mA) at 0.2V	-	-	40

Notes:

1. N must be greater than or equal to 0.653 and less than or equal to 0.68.

GTL+

A sample circuit illustrating a valid termination technique for GTL+ appears in Figure 45. DC voltage specifications appear in Table 24.

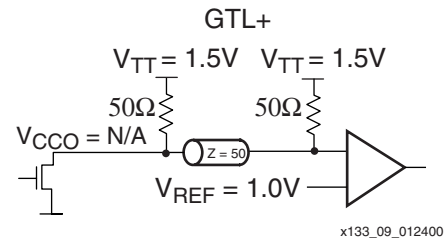


Figure 45: Terminated GTL+

Table 24: GTL+ Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	-	-	-
$V_{REF} = N \times V_{TT}^1$	0.88	1.0	1.12
V_{TT}	1.35	1.5	1.65
$V_{IH} = V_{REF} + 0.1$	0.98	1.1	-
$V_{IL} = V_{REF} - 0.1$	-	0.9	1.02
V_{OH}	-	-	-
V_{OL}	0.3	0.45	0.6
I_{OH} at V_{OH} (mA)	-	-	-
I_{OL} at V_{OL} (mA) at 0.6V	36	-	-
I_{OL} at V_{OL} (mA) at 0.3V	-	-	48

Notes:

1. N must be greater than or equal to 0.653 and less than or equal to 0.68.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
CTT	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.4$	$V_{REF} + 0.4$	8	-8
AGP	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2

Notes:

1. V_{OL} and V_{OH} for lower drive currents are sample tested.
2. Tested according to the relevant specifications.
3. DC input and output levels for HSTL18 (HSTL I/O standard with V_{CCO} of 1.8 V) are provided in an HSTL white paper on www.xilinx.com.

LVDS DC Specifications

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}		2.375	2.5	2.625	V
Output High Voltage for Q and $\bar{Q}$	V_{OH}	$R_T = 100 \Omega$ across Q and $\bar{Q}$ signals	1.25	1.425	1.6	V
Output Low Voltage for Q and $\bar{Q}$	V_{OL}	$R_T = 100 \Omega$ across Q and $\bar{Q}$ signals	0.9	1.075	1.25	V
Differential Output Voltage (Q - $\bar{Q}$), Q = High ($\bar{Q}$ - Q), $\bar{Q}$ = High	V_{ODIFF}	$R_T = 100 \Omega$ across Q and $\bar{Q}$ signals	250	350	450	mV
Output Common-Mode Voltage	V_{OCM}	$R_T = 100 \Omega$ across Q and $\bar{Q}$ signals	1.125	1.25	1.375	V
Differential Input Voltage (Q - $\bar{Q}$), Q = High ($\bar{Q}$ - Q), $\bar{Q}$ = High	V_{IDIFF}	Common-mode input voltage = 1.25 V	100	350	NA	mV
Input Common-Mode Voltage	V_{ICM}	Differential input voltage = ± 350 mV	0.2	1.25	2.2	V

Note: Refer to the Design Consideration section for termination schematics.

LVPECL DC Specifications

These values are valid at the output of the source termination pack shown under **LVPECL**, with a 100Ω differential load only. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. The following table summarizes the DC output specifications of LVPECL.

DC Parameter	Min	Max	Min	Max	Min	Max	Units
V_{CCO}	3.0		3.3		3.6		V
V_{OH}	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{IH}	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential Input Voltage	0.3	-	0.3	-	0.3	-	V

Low Voltage Differential Signals

The Virtex-E family incorporates low-voltage signalling (LVDS and LVPECL). Two pins are utilized for these signals to be connected to a Virtex-E device. These are known as differential pin pairs. Each differential pin pair has a Positive (P) and a Negative (N) pin. These pairs are labeled in the following manner.

IO_L#[P/N]

where

L = LVDS or LVPECL pin

= Pin Pair Number

P = Positive

N = Negative

I/O pins for differential signals can either be synchronous or asynchronous, input or output. The pin pairs can be used for synchronous input and output signals as well as asynchronous input signals. However, only some of the low-voltage pairs can be used for asynchronous output signals.

Differential signals require the pins of a pair to switch almost simultaneously. If the signals driving the pins are from IOB flip-flops, they are synchronous. If the signals driving the pins are from internal logic, they are asynchronous. [Table 2](#) defines the names and function of the different types of low-voltage pin pairs in the Virtex-E family.

Table 2: LVDS Pin Pairs

Pin Name	Description
IO_L#[P/N] Example: IO_L22N	Represents a general IO or a synchronous input/output differential signal. When used as a differential signal, N means Negative I/O and P means Positive I/O.
IO_L#[P/N]_Y Example: IO_L22N_Y	Represents a general IO or a synchronous input/output differential signal, or a part-dependent asynchronous output differential signal.
IO_L#[P/N]_YY Example: O_L22N_YY	Represents a general IO or a synchronous input/output differential signal, or an asynchronous output differential signal.
IO_LVDS_DLL_L#[P/N] Example: IO_LVDS_DLL_L16N	Represents a general IO or a synchronous input/output differential signal, a differential clock input signal, or a DLL input. When used as a differential clock input, this pin is paired with the adjacent GCK pin. The GCK pin is always the positive input in the differential clock input configuration.

Virtex-E Package Pinouts

The Virtex-E family of FPGAs is available in 12 popular packages, including chip-scale, plastic and high heat-dissipation quad flat packs, and ball grid and fine-pitch ball grid arrays. Family members have footprint compatibility across devices provided in the same package. The pinout tables in

this section indicate function, pin, and bank information for each package/device combination. Following each pinout table is an additional table summarizing information specific to differential pin pairs for all devices provided in that package.

BG352 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A check (✓) in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock

Table 11: BG352 Differential Pin Pair Summary
XCV100E, XCV200E, XCV300E

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	AE13	AC13	NA	IO LVDS 55
1	5	AF14	AD14	NA	IO LVDS 55
2	1	B14	A13	NA	IO LVDS 9
3	0	D14	A15	NA	IO LVDS 9
IO LVDS					
Total Outputs: 87, Asynchronous Output Pairs: 43					
0	0	B23	D21	✓	VREF_0
1	0	D20	A23	✓	-
2	0	B22	C21	✓	VREF_0
3	0	A21	B20	2	-
4	0	B19	C19	✓	VREF_0
5	0	C18	D17	✓	-
6	0	A18	C17	2	-
7	0	C16	B17	✓	-
8	0	D15	A16	✓	VREF_0
9	1	A13	A15	✓	GCLK LVDS 3/2
10	1	A12	C13	2	-
11	1	C12	B12	✓	VREF_1
12	1	B11	A11	✓	-
13	1	D11	C11	2	-
14	1	C10	B9	✓	-
15	1	C9	B8	✓	VREF_1
16	1	A7	D9	1	-
17	1	B6	A6	✓	VREF_1
18	1	A4	C7	✓	-

Table 11: BG352 Differential Pin Pair Summary
XCV100E, XCV200E, XCV300E

Pair	Bank	P Pin	N Pin	AO	Other Functions
19	1	D6	C6	✓	VREF_1
20	1	C4	D5	✓	CS
21	2	E4	D3	✓	DIN_D0
22	2	D2	C1	✓	VREF_2
23	2	G4	F3	✓	-
24	2	E2	F2	✓	VREF_2
25	2	F1	J4	2	-
26	2	H2	G1	✓	D1
27	2	J3	J2	✓	D2
28	2	J1	L4	1	-
29	2	L3	L2	✓	-
30	2	M4	M3	✓	D3
31	2	M2	M1	2	-
32	2	N4	N2	✓	-
33	3	R1	R2	2	-
34	3	R3	R4	✓	VREF_3
35	3	T2	U2	✓	-
36	3	T4	V1	1	-
37	3	U3	U4	✓	D5
38	3	V3	V4	✓	VREF_3
39	3	Y1	Y2	1	-
40	3	AA2	Y3	✓	VREF_3
41	3	AC1	AB2	✓	-
42	3	AA4	AC2	✓	VREF_3
43	3	AC3	AD2	✓	INIT
44	4	AC5	AD4	✓	-
45	4	AE4	AF3	✓	VREF_4
46	4	AC7	AD6	✓	-
47	4	AE5	AE6	✓	VREF_4
48	4	AF6	AC9	2	-
49	4	AE8	AF7	✓	VREF_4
50	4	AD9	AE9	✓	-
51	4	AF9	AC11	2	-
52	4	AD11	AE11	✓	-
53	4	AC12	AD12	✓	VREF_4
54	4	AE12	AF12	2	-

Table 16: FG256 Package — XCV50E, XCV100E, XCV200E, XCV300E

Bank	Pin Description	Pin #
1	IO_L11N_Y	A10
1	IO_L11P_Y	D10
1	IO_L12N_YY	C10
1	IO_L12P_YY	A11
1	IO_L13N_YY	B11
1	IO_VREF_L13P_YY	E11 ¹
1	IO_L14N_Y	A12
1	IO_L14P_Y	D11
1	IO_L15N_YY	A13
1	IO_VREF_L15P_YY	C11
1	IO_L16N_YY	B12
1	IO_L16P_YY	D12
1	IO_VREF_L17N_Y	A14 ²
1	IO_L17P_Y	C12
1	IO_WRITE_L18N_YY	C13
1	IO_CS_L18P_YY	B13
2	IO_DOUT_BUSY_L19P_YY	C15
2	IO_DIN_D0_L19N_YY	D14
2	IO_L20P	B16
2	IO_VREF_L20N	E13 ²
2	IO_L21P_YY	C16
2	IO_L21N_YY	E14
2	IO_VREF_L22P_Y	F13
2	IO_L22N_Y	E15
2	IO_L23P	F12
2	IO_L23N	D16
2	IO_VREF_L24P_Y	F14 ¹
2	IO_D1_L24N_Y	E16
2	IO_D2_L25P_YY	F15
2	IO_L25N_YY	G13
2	IO_L26P	F16
2	IO_L26N	G12
2	IO_L27P_YY	G15
2	IO_L27N_YY	G14

Table 16: FG256 Package — XCV50E, XCV100E, XCV200E, XCV300E

Bank	Pin Description	Pin #
2	IO_VREF_L28P_Y	H13
2	IO_D3_L28N_Y	G16
2	IO_L29P	J13
2	IO_L29N	H15
2	IO_L30P_YY	H14
2	IO_L30N_YY	H16
3	IO	J15
3	IO_L31P	K15
3	IO_L31N	J14
3	IO_D4_L32P_Y	J16
3	IO_VREF_L32N_Y	K16
3	IO_L33P_YY	K12
3	IO_L33N_YY	L15
3	IO_L34P	K13
3	IO_L34N	L16
3	IO_L35P_YY	K14
3	IO_D5_L35N_YY	M16
3	IO_D6_L36P_Y	N16
3	IO_VREF_L36N_Y	L13 ¹
3	IO_L37P	P16
3	IO_L37N	L12
3	IO_L38P_Y	M15
3	IO_VREF_L38N_Y	L14
3	IO_L39P_YY	M14
3	IO_L39N_YY	R16
3	IO_VREF_L40P	M13 ²
3	IO_L40N	T15
3	IO_D7_L41P_YY	N14
3	IO_INIT_L41N_YY	N15
4	GCK0	N8
4	IO	P10
4	IO_L42P_YY	T14
4	IO_L42N_YY	P13

FG456 Fine-Pitch Ball Grid Array Packages

XCV200E and XCV300E devices in FG456 fine-pitch Ball Grid Array packages have footprint compatibility. Pins labeled IO_VREF can be used as either in both devices provided in this package. If the pin is not used as V_{REF} it can be used as general I/O. Immediately following Table 18, see Table 19 for Differential Pair information.

Table 18: FG456 — XCV200E and XCV300E

Bank	Pin Description	Pin #
0	GCK3	C11
0	IO	A2 ¹
0	IO	A3
0	IO	A6 ¹
0	IO	A10
0	IO	B5
0	IO	B9
0	IO	C5
0	IO	D8
0	IO	D10
0	IO	E11 ¹
0	IO_L0N	D5
0	IO_L0P	B3
0	IO_VREF_L1N_YY	B4
0	IO_L1P_YY	E6
0	IO_L2N	A4
0	IO_L2P	E7
0	IO_VREF_L3N_YY	C6
0	IO_L3P_YY	D6
0	IO_L4N_Y	A5
0	IO_L4P_Y	B6
0	IO_L5N_Y	D7
0	IO_L5P_Y	C7
0	IO_VREF_L6N_YY	E8
0	IO_L6P_YY	B7
0	IO_L7N_YY	A7
0	IO_L7P_YY	E9
0	IO_L8N_Y	C8
0	IO_L8P_Y	B8
0	IO_L9N_Y	D9
0	IO_L9P_Y	A8

Table 18: FG456 — XCV200E and XCV300E

Bank	Pin Description	Pin #
0	IO_L10N	C9
0	IO_L10P	E10
0	IO_VREF_L11N_YY	A9
0	IO_L11P_YY	C10
0	IO_L12N_Y	F11
0	IO_L12P_Y	B10
0	IO_LVDS_DLL_L13N	B11
1	GCK2	A11
1	IO	A12 ¹
1	IO	A14
1	IO	B16 ¹
1	IO	B19
1	IO	E13
1	IO	E15
1	IO	E16
1	IO	E17 ¹
1	IO_LVDS_DLL_L13P	D11
1	IO_L14N_Y	C12
1	IO_L14P_Y	D12
1	IO_L15N_Y	B12
1	IO_L15P_Y	A13
1	IO_L16N_YY	E12
1	IO_VREF_L16P_YY	B13
1	IO_L17N_YY	C13
1	IO_L17P_YY	D13
1	IO_L18N_Y	B14
1	IO_L18P_Y	C14
1	IO_L19N_Y	F12
1	IO_L19P_Y	A15
1	IO_L20N_YY	B15
1	IO_L20P_YY	C15
1	IO_L21N_YY	A16
1	IO_VREF_L21P_YY	E14
1	IO_L22N_Y	D14
1	IO_L22P_Y	C16
1	IO_L23N_Y	D15

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
0	IO_L9N	A7
0	IO_L9P	D9
0	IO_L10N	B8
0	IO_VREF_L10P	G10
0	IO_L11N_YY	C9
0	IO_L11P_YY	F10
0	IO_L12N_Y	A8
0	IO_L12P_Y	E10
0	IO_L13N_YY	G11
0	IO_L13P_YY	D10
0	IO_L14N_YY	B10
0	IO_L14P_YY	F11
0	IO_L15N	C10
0	IO_L15P	E11
0	IO_L16N_YY	G12
0	IO_L16P_YY	D11
0	IO_VREF_L17N_YY	C11
0	IO_L17P_YY	F12
0	IO_L18N_YY	A11
0	IO_L18P_YY	E12
0	IO_L19N_Y	D12
0	IO_L19P_Y	C12
0	IO_VREF_L20N_Y	A12
0	IO_L20P_Y	H13
0	IO_LVDS_DLL_L21N	B13
1	GCK2	C13
1	IO	A13 ¹
1	IO	A16 ¹
1	IO	A19
1	IO	A20
1	IO	A22
1	IO	A24 ¹
1	IO	B15 ¹
1	IO	B17 ¹
1	IO	B23
1	IO_LVDS_DLL_L21P	F14

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
1	IO_L22N	E14
1	IO_L22P	F13
1	IO_L23N_Y	D14
1	IO_VREF_L23P_Y	A14
1	IO_L24N_Y	C14
1	IO_L24P_Y	H14
1	IO_L25N_YY	G14
1	IO_L25P_YY	C15
1	IO_L26N_YY	E15
1	IO_VREF_L26P_YY	D15
1	IO_L27N_YY	C16
1	IO_L27P_YY	F15
1	IO_L28N	G15
1	IO_L28P	D16
1	IO_L29N_YY	E16
1	IO_L29P_YY	A17
1	IO_L30N_YY	C17
1	IO_L30P_YY	E17
1	IO_L31N_Y	F16
1	IO_L31P_Y	D17
1	IO_L32N_YY	F17
1	IO_L32P_YY	C18
1	IO_L33N_YY	A18
1	IO_VREF_L33P_YY	G16
1	IO_L34N_YY	C19
1	IO_L34P_YY	G17
1	IO_L35N_Y	D18
1	IO_VREF_L35P_Y	B19 ²
1	IO_L36N_Y	D19
1	IO_L36P_Y	E18
1	IO_L37N_YY	F18
1	IO_L37P_YY	B20
1	IO_L38N_YY	G19
1	IO_VREF_L38P_YY	C20
1	IO_L39N_YY	G18
1	IO_L39P_YY	E19
1	IO_L40N_YY	A21

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
NA	GND	D20
NA	GND	D12
NA	GND	C39
NA	GND	C37
NA	GND	C3
NA	GND	C20
NA	GND	C1
NA	GND	B39
NA	GND	B38
NA	GND	B2
NA	GND	B1
NA	GND	AW39
NA	GND	AW38
NA	GND	AW37
NA	GND	AW3
NA	GND	AW2
NA	GND	AW1
NA	GND	AV39
NA	GND	AV38
NA	GND	AV2
NA	GND	AV1
NA	GND	AU39
NA	GND	AU37
NA	GND	AU3
NA	GND	AU20
NA	GND	AU1
NA	GND	AT4
NA	GND	AT36
NA	GND	AT28
NA	GND	AT20
NA	GND	AT12
NA	GND	AR5
NA	GND	AR35
NA	GND	AR28
NA	GND	AR21
NA	GND	AR20

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
NA	GND	AR19
NA	GND	AR12
NA	GND	AH5
NA	GND	AH4
NA	GND	AH36
NA	GND	AH35
NA	GND	AA5
NA	GND	AA35
NA	GND	A39
NA	GND	A38
NA	GND	A37
NA	GND	A3
NA	GND	A2
NA	GND	A1

Notes:

1. V_{REF} or I/O option only in the XCV1000E, 1600E, 2000E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV1600E, 2000E; otherwise, I/O option only.
3. V_{REF} or I/O option only in the XCV2000E; otherwise, I/O option only.

Table 26: FG900 — XCV600E, XCV1000E, XCV1600E

Bank	Pin Description	Pin #
NA	GND	AG27
NA	GND	D27
NA	GND	AF26
NA	GND	E26
NA	GND	F25
NA	GND	AE25
NA	GND	G24
NA	GND	AJ23
NA	GND	AD24
NA	GND	H23
NA	GND	B23
NA	GND	AC23
NA	GND	AB22
NA	GND	V22
NA	GND	N22
NA	GND	AH18
NA	GND	AB18
NA	GND	J18
NA	GND	C18
NA	GND	U17
NA	GND	T17
NA	GND	R17
NA	GND	P17
NA	GND	U16
NA	GND	T16
NA	GND	R16
NA	GND	P16
NA	GND	U15
NA	GND	T15
NA	GND	R15
NA	GND	P15
NA	GND	U14
NA	GND	T14
NA	GND	R14
NA	GND	P14
NA	GND	AH13
NA	GND	AB13

Table 26: FG900 — XCV600E, XCV1000E, XCV1600E

Bank	Pin Description	Pin #
NA	GND	J13
NA	GND	C13
NA	GND	V9
NA	GND	N9
NA	GND	J9
NA	GND	AJ8
NA	GND	AC8
NA	GND	H8
NA	GND	AD7
NA	GND	B8
NA	GND	AE6
NA	GND	G7
NA	GND	F6
NA	GND	AF5
NA	GND	E5
NA	GND	AG4
NA	GND	D4
NA	GND	V3
NA	GND	N3
NA	GND	C3
NA	GND	AK2
NA	GND	AH3
NA	GND	AC2
NA	GND	H2
NA	GND	B2
NA	GND	A2
NA	GND	AK1
NA	GND	AJ2
NA	GND	AJ1
NA	GND	A1
NA	GND	B1

Notes:

1. V_{REF} or I/O option only in the XCV1000E and XCV1600E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV1600E; otherwise, I/O option only.
3. I/O option only in the XCV600E.
4. No Connect in the XCV600E.
5. No Connect in the XCV600E, 1000E.

Table 27: FG900 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
120	3	AA30	W24	4	-
121	3	AA29	V20	1	-
122	3	Y27	W23	NA	-
123	3	Y26	AB30	√	D5
124	3	V21	AA28	√	VREF
125	3	Y25	AA27	4	-
126	3	W22	Y23	4	-
127	3	Y24	AB28	4	VREF
128	3	AC30	AA25	√	-
129	3	W21	AA24	2	-
130	3	AB26	AD30	√	-
131	3	Y22	AC27	√	VREF
132	3	AD28	AB25	2	-
133	3	AC26	AE30	4	-
134	3	AD27	AF30	√	-
135	3	AF29	AB24	1	VREF
136	3	AB23	AE28	4	-
137	3	AG30	AC25	3	-
138	3	AE26	AG29	4	VREF
139	3	AH30	AC24	1	-
140	3	AF28	AD25	NA	-
141	3	AH29	AA22	√	INIT
142	4	AF27	AK28	√	-
143	4	AG26	AH27	4	-
144	4	AD23	AJ27	2	-
145	4	AB21	AF25	2	VREF
146	4	AC22	AH26	2	-
147	4	AA21	AG25	√	-
148	4	AJ26	AD22	√	VREF
149	4	AA20	AH25	1	-
150	4	AC21	AF24	1	-
151	4	AG24	AK26	√	-
152	4	AJ24	AF23	√	VREF
153	4	AE23	AB20	2	-

Table 27: FG900 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
154	4	AC20	AG23	2	-
155	4	AF22	AE22	√	-
156	4	AJ22	AG22	√	VREF
157	4	AK24	AD20	NA	-
158	4	AA19	AF21	4	-
159	4	AH22	AA18	NA	VREF
160	4	AG21	AK23	NA	-
161	4	AH21	AD19	4	-
162	4	AE20	AJ21	2	-
163	4	AG20	AF20	2	-
164	4	AC18	AF19	2	-
165	4	AJ20	AE19	√	-
166	4	AK22	AH20	√	VREF
167	4	AG19	AB17	1	-
168	4	AJ19	AD17	1	-
169	4	AA16	AA17	√	-
170	4	AK21	AB16	√	VREF
171	4	AG18	AK20	2	-
172	4	AK19	AD16	2	-
173	4	AE16	AE17	√	-
174	4	AG17	AJ17	√	VREF
175	4	AD15	AH17	NA	-
176	4	AG16	AK17	4	VREF
177	5	AF16	AH16	NA	IO_LVDS_DLL
178	5	AC15	AG15	4	VREF
179	5	AB15	AF15	√	-
180	5	AA15	AF14	√	VREF
181	5	AH15	AK15	√	-
182	5	AB14	AF13	2	-
183	5	AH14	AJ14	2	-
184	5	AE14	AG13	√	VREF
185	5	AK13	AD13	√	-
186	5	AE13	AF12	1	-
187	5	AC13	AA13	1	-

Table 27: FG900 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
256	7	N6	M6	1	-
257	7	N1	N5	4	-
258	7	M5	M4	√	-
259	7	M1	M2	1	VREF
260	7	L2	L4	4	-
261	7	L5	M7	3	-
262	7	M8	L1	4	-
263	7	M9	K2	1	-
264	7	M10	L3	NA	-
265	7	K1	K5	√	-
266	7	K3	L6	√	VREF
267	7	K4	L7	4	-
268	7	J5	L8	4	-
269	7	H4	K6	4	VREF
270	7	K7	H1	4	-
271	7	J2	J7	2	-
272	7	G2	H5	√	-
273	7	G5	L9	√	VREF
274	7	K8	F3	1	-
275	7	E1	G3	4	-
276	7	E2	H6	√	-
277	7	K9	E4	1	VREF
278	7	F4	J8	4	-
279	7	H7	D1	3	-
280	7	C2	G6	4	VREF
281	7	F5	D2	1	-
282	7	K10	D3	4	-

Notes:

1. AO in the XCV600E, 1000E.
2. AO in the XCV1000E.
3. AO in the XCV1600E.
4. AO in the XCV1000E, XCV1600E.

FG1156 Fine-Pitch Ball Grid Array Package

XCV1000E, XCV1600E, XCV2000E, XCV2600E, and XCV3200E devices in the FG1156 fine-pitch Ball Grid Array package have footprint compatibility. Pins labeled IO_VREF can be used as either V_{REF} or general I/O, unless indicated in the footnotes. If the pin is not used as V_{REF} , it can be used as general I/O. Immediately following Table 28, see Table 29 for Differential Pair information.

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
0	GCK3	E17
0	IO	B4
0	IO	B9
0	IO	B10
0	IO	D9 ³
0	IO	D16
0	IO	E7 ³
0	IO	E11 ³
0	IO	E13 ³
0	IO	E16 ³
0	IO	F17 ³
0	IO	J12 ³
0	IO	J13 ³
0	IO	J14 ³
0	IO	K11 ³
0	IO_L0N_Y	F7
0	IO_L0P_Y	H9
0	IO_L1N_Y	C5
0	IO_L1P_Y	J10
0	IO_VREF_L2N_Y	E6
0	IO_L2P_Y	D6
0	IO_L3N_Y	A4
0	IO_L3P_Y	G8
0	IO_L4N_YY	C6
0	IO_L4P_YY	J11
0	IO_VREF_L5N_YY	G9
0	IO_L5P_YY	F8
0	IO_L6N_YY	A5 ⁴

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
2	IO_L92N_Y	H29
2	IO_L93P_YY	J28 ⁴
2	IO_L93N_YY	E33 ⁵
2	IO_L94P_YY	H28
2	IO_L94N_YY	H30
2	IO_L95P_Y	H32
2	IO_L95N_Y	K28
2	IO_L96P_Y	L27 ⁴
2	IO_L96N_Y	F33 ⁵
2	IO_L97P_Y	M26
2	IO_L97N_Y	E34
2	IO_VREF_L98P_YY	H31
2	IO_L98N_YY	G32
2	IO_L99P_YY	N25 ⁴
2	IO_L99N_YY	J31 ⁵
2	IO_L100P_YY	J30
2	IO_L100N_YY	G33
2	IO_VREF_L101P_Y	H34 ²
2	IO_L101N_Y	J29
2	IO_L102P	M27 ⁴
2	IO_L102N	H33 ⁵
2	IO_L103P_Y	K29
2	IO_L103N_Y	J34
2	IO_VREF_L104P_YY	L29
2	IO_L104N_YY	J33
2	IO_L105P_YY	M28
2	IO_L105N_YY	K34
2	IO_L106P_Y	N27
2	IO_L106N_Y	L34
2	IO_VREF_L107P_YY	K33
2	IO_D1_L107N_YY	P26
2	IO_L108P_Y	R25
2	IO_L108N_Y	M34
2	IO_L109P_Y	L31

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
2	IO_L109N_Y	L33
2	IO_L110P_Y	P27
2	IO_L110N_Y	M33
2	IO_L111P	M31
2	IO_L111N	R26
2	IO_L112P_Y	N30
2	IO_L112N_Y	P28
2	IO_VREF_L113P_Y	N29
2	IO_L113N_Y	N33
2	IO_L114P_YY	T25 ⁴
2	IO_L114N_YY	N34 ⁵
2	IO_L115P_YY	P34
2	IO_L115N_YY	R27
2	IO_L116P_Y	P29
2	IO_L116N_Y	P31
2	IO_L117P_Y	P33 ⁴
2	IO_L117N_Y	T26 ⁵
2	IO_L118P_Y	R34
2	IO_L118N_Y	R28
2	IO_VREF_L119P_YY	N31
2	IO_D3_L119N_YY	N32
2	IO_L120P_YY	P30 ⁴
2	IO_L120N_YY	R33 ⁵
2	IO_L121P_YY	R29
2	IO_L121N_YY	T34
2	IO_L122P_Y	R30
2	IO_L122N_Y	T30
2	IO_L123P	T28 ⁴
2	IO_L123N	R31 ⁵
2	IO_L124P_Y	T29
2	IO_L124N_Y	U27
2	IO_VREF_L125P_YY	T31
2	IO_L125N_YY	T33
2	IO_L126P_YY	U28

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
2	IO_L126N_YY	T32
2	IO_VREF_L127P_Y	U29 ¹
2	IO_L127N_Y	U33
2	IO_L128P_YY	V33
2	IO_L128N_YY	U31
3	IO	V27 ³
3	IO	V31
3	IO	V32 ³
3	IO	W33
3	IO	AB25 ³
3	IO	AB26 ³
3	IO	AB31 ³
3	IO	AC31 ³
3	IO	AF34
3	IO	AG31 ³
3	IO	AG33 ³
3	IO	AG34
3	IO	AH29 ³
3	IO	AJ30 ³
3	IO_L129P_Y	V26
3	IO_VREF_L129N_Y	V30 ¹
3	IO_L130P_YY	W34
3	IO_L130N_YY	V28
3	IO_L131P_YY	W32
3	IO_VREF_L131N_YY	W30
3	IO_L132P_Y	V29
3	IO_L132N_Y	Y34
3	IO_L133P	W29 ⁵
3	IO_L133N	Y33 ⁴
3	IO_L134P_Y	W26
3	IO_L134N_Y	W28
3	IO_L135P_YY	Y31
3	IO_L135N_YY	Y30

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
3	IO_L136P_YY	AA34 ⁵
3	IO_L136N_YY	W31 ⁴
3	IO_D4_L137P_YY	AA33
3	IO_VREF_L137N_YY	Y29
3	IO_L138P_Y	W25
3	IO_L138N_Y	AB34
3	IO_L139P_Y	Y28 ⁵
3	IO_L139N_Y	AB33 ⁴
3	IO_L140P_Y	AA30
3	IO_L140N_Y	Y26
3	IO_L141P_YY	Y27
3	IO_L141N_YY	AA31
3	IO_L142P_YY	AA27 ⁵
3	IO_L142N_YY	AA29 ⁴
3	IO_L143P_Y	AB32
3	IO_VREF_L143N_Y	AB29
3	IO_L144P_Y	AA28
3	IO_L144N_Y	AC34
3	IO_L145P	Y25
3	IO_L145N	AD34
3	IO_L146P_Y	AB30
3	IO_L146N_Y	AC33
3	IO_L147P_Y	AA26
3	IO_L147N_Y	AC32
3	IO_L148P_Y	AD33
3	IO_L148N_Y	AB28
3	IO_L149P_YY	AE34
3	IO_D5_L149N_YY	AB27
3	IO_D6_L150P_YY	AE33
3	IO_VREF_L150N_YY	AC30
3	IO_L151P_Y	AA25
3	IO_L151N_Y	AE32
3	IO_L152P_YY	AE31
3	IO_L152N_YY	AD29

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
4	IO_L212N_YY	AP18
4	IO_L213P_Y	AF18
4	IO_L213N_Y	AP17
4	IO_VREF_L214P_Y	AJ18 ¹
4	IO_L214N_Y	AL18
4	IO_LVDS_DLL_L215P	AM18
5	GCK1	AL19
5	IO	AF17 ³
5	IO	AG12 ³
5	IO	AH12
5	IO	AJ10 ³
5	IO	AJ11 ³
5	IO	AK7 ³
5	IO	AK13 ³
5	IO	AL13 ³
5	IO	AM4 ³
5	IO	AN9
5	IO	AN10 ³
5	IO	AN16
5	IO	AN17 ³
5	IO_LVDS_DLL_L215N	AL17
5	IO_L216P_Y	AH17
5	IO_VREF_L216N_Y	AM17 ¹
5	IO_L217P_Y	AJ17
5	IO_L217N_Y	AG17
5	IO_L218P_YY	AP16
5	IO_VREF_L218N_YY	AL16
5	IO_L219P_YY	AJ16
5	IO_L219N_YY	AM16
5	IO_L220P	AK16 ⁵
5	IO_L220N	AP15 ⁴
5	IO_L221P_Y	AL15
5	IO_L221N_Y	AH16

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
5	IO_L222P_Y	AN15
5	IO_L222N_Y	AF16
5	IO_L223P_Y	AP14 ⁵
5	IO_L223N_Y	AE16 ⁴
5	IO_L224P_YY	AK15
5	IO_VREF_L224N_YY	AJ15
5	IO_L225P_YY	AH15
5	IO_L225N_YY	AN14
5	IO_L226P	AK14 ⁵
5	IO_L226N	AG15 ⁴
5	IO_L227P_Y	AM13
5	IO_L227N_Y	AF15
5	IO_L228P_Y	AG14
5	IO_L228N_Y	AP13
5	IO_L229P_YY	AE14 ⁵
5	IO_L229N_YY	AE15 ⁴
5	IO_L230P_YY	AN13
5	IO_VREF_L230N_YY	AG13
5	IO_L231P_YY	AH14
5	IO_L231N_YY	AP12
5	IO_L232P_Y	AJ14
5	IO_L232N_Y	AL14
5	IO_L233P_Y	AF13
5	IO_L233N_Y	AN12
5	IO_L234P_Y	AF14
5	IO_L234N_Y	AP11
5	IO_L235P_Y	AN11
5	IO_L235N_Y	AH13
5	IO_L236P_YY	AM12
5	IO_L236N_YY	AL12
5	IO_L237P_YY	AJ13
5	IO_VREF_L237N_YY	AP10
5	IO_L238P_Y	AK12
5	IO_L238N_Y	AM10

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
NA	GND	AP2
NA	GND	AN3
NA	GND	AM20
NA	GND	AK30
NA	GND	AG8
NA	GND	AC29
NA	GND	Y3
NA	GND	Y32
NA	GND	W21
NA	GND	V21
NA	GND	T8
NA	GND	T27
NA	GND	R21
NA	GND	P21
NA	GND	H19
NA	GND	F29
NA	GND	C11
NA	GND	B3
NA	GND	A32
NA	GND	AP3
NA	GND	AN32
NA	GND	AM24
NA	GND	AJ6
NA	GND	AG16
NA	GND	AA14
NA	GND	Y14
NA	GND	W8
NA	GND	W27
NA	GND	U14
NA	GND	T14
NA	GND	R3
NA	GND	R32
NA	GND	M6
NA	GND	H27

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
NA	GND	E5
NA	GND	C15
NA	GND	B32
NA	GND	A33
NA	GND	AP7
NA	GND	AN33
NA	GND	AM32
NA	GND	AJ12
NA	GND	AG19
NA	GND	AA15
NA	GND	Y15
NA	GND	W14
NA	GND	V14
NA	GND	U15
NA	GND	T15
NA	GND	R14
NA	GND	P14
NA	GND	M29
NA	GND	G1
NA	GND	E18
NA	GND	C20
NA	GND	B33
NA	GND	A34
NA	GND	AP28
NA	GND	AN34
NA	GND	AM33
NA	GND	AJ23
NA	GND	AG27
NA	GND	AA16
NA	GND	Y16
NA	GND	W15
NA	GND	V15
NA	GND	U16
NA	GND	T16

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
111	2	M31	R26	2600 1600	-
112	2	N30	P28	3200 1600 1000	-
113	2	N29	N33	2600 2000 1000	VREF
114	2	T25	N34	3200 2600 2000 1600	-
115	2	P34	R27	3200 2600 2000 1600 1000	-
116	2	P29	P31	3200 2600 1600 1000	-
117	2	P33	T26	3200 2600 2000	-
118	2	R34	R28	2600 2000 1000	-
119	2	N31	N32	2000 1600 1000	D3
120	2	P30	R33	2000 1600	-
121	2	R29	T34	3200 2600 2000 1600 1000	-
122	2	R30	T30	1000	-
123	2	T28	R31	3200 1600	-
124	2	T29	U27	3200 2600 1600 1000	-
125	2	T31	T33	2000 1600 1000	VREF
126	2	U28	T32	2000 1600 1000	-
127	2	U29	U33	3200 2600 1600 1000	VREF
128	2	V33	U31	3200 2600 2000 1600 1000	-
129	3	V26	V30	3200 2600 1600 1000	VREF
130	3	W34	V28	2000 1600 1000	-
131	3	W32	W30	2000 1600 1000	VREF

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
132	3	V29	Y34	3200 2600 1600 1000	-
133	3	W29	Y33	3200 1600	-
134	3	W26	W28	1000	-
135	3	Y31	Y30	3200 2600 2000 1600 1000	-
136	3	AA34	W31	2000 1600	-
137	3	AA33	Y29	2000 1600 1000	VREF
138	3	W25	AB34	2600 2000 1000	-
139	3	Y28	AB33	3200 2600 2000	-
140	3	AA30	Y26	3200 2600 1600 1000	-
141	3	Y27	AA31	3200 2600 2000 1600 1000	-
142	3	AA27	AA29	3200 2600 2000 1600	-
143	3	AB32	AB29	2600 2000 1000	VREF
144	3	AA28	AC34	3200 1600 1000	-
145	3	Y25	AD34	2600 1600	-
146	3	AB30	AC33	3200 2600 1600 1000	-
147	3	AA26	AC32	2000 1000	-
148	3	AD33	AB28	3200 2600 2000	-
149	3	AE34	AB27	3200 2600 2000 1600 1000	D5
150	3	AE33	AC30	2000 1600 1000	VREF
151	3	AA25	AE32	3200 1600 1000	-
152	3	AE31	AD29	3200 2600 2000 1600 1000	-

Date	Version	Revision
4/2/01	2.0	- Updated numerous values in Virtex-E Switching Characteristics tables. - Changed pinout table footnotes from "V_{REF} option only" to "V_{REF} or I/O option only" to improve clarity. - Converted file to modularized format. See the Virtex-E Data Sheet section.
7/26/01	2.1	- Changed pinout table footnotes from "V_{REF} or I/O option only" to "V_{REF} or I/O option only; otherwise I/O only" to improve clarity. - Changed designation for pin pair 300 in Table 29 from AO to footnote 9.
10/25/01	2.2	- Changed Table 29 to clarify which devices in the FG1156 package can use each pin pair as an asynchronous output. - Updated references to the XCV3200E device in the FG1156 package.
11/15/01	2.3	Fixed cosmetic error.
07/17/02	2.4	- Added "VREF" to the description for pin B15 in Table 12. - Changed designation for pin pair 129 in Table 15 from AO to "AO in the XCV1000E, 1600E, 2000E". - Data sheet designation upgraded from Preliminary to Production.
03/14/03	2.5	Removed the Virtex-E XCV300E section under Pinout Differences Between Virtex and Virtex-E Families (and revised Table 1), since these differences do not exist.

Virtex-E Data Sheet

The Virtex-E Data Sheet contains the following modules:

- DS022-1, Virtex-E 1.8V FPGAs:
[Introduction and Ordering Information \(Module 1\)](#)
- DS022-2, Virtex-E 1.8V FPGAs:
[Functional Description \(Module 2\)](#)
- DS022-3, Virtex-E 1.8V FPGAs:
[DC and Switching Characteristics \(Module 3\)](#)
- DS022-4, Virtex-E 1.8V FPGAs:
[Pinout Tables \(Module 4\)](#)