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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	1176
Number of Logic Elements/Cells	5292
Total RAM Bits	114688
Number of I/O	94
Number of Gates	306393
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-TFBGA, CSPBGA
Supplier Device Package	144-LCSBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv200e-6cs144i

Initialization in Verilog and Synopsys

The block SelectRAM+ structures can be initialized in Verilog for both simulation and synthesis for inclusion in the EDIF output file. The simulation of the Verilog code uses a defparam to pass the initialization. The Synopsys FPGA compiler does not presently support defparam. The initialization values instead attach as attributes to the RAM by a built-in Synopsys dc_script. The translate_off statement stops synthesis translation of the defparam statements. The following code illustrates a module that employs these techniques.

Design Examples

Creating a 32-bit Single-Port RAM

The true dual-read/write port functionality of the block SelectRAM+ memory allows a single port, 128 deep by 32-bit wide RAM to be created using a single block SelectRAM+ cell as shown in **Figure 35**.

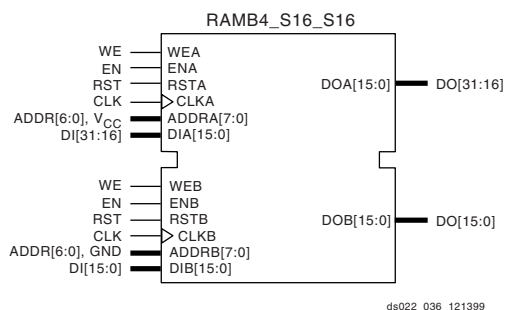


Figure 35: Single Port 128 x 32 RAM

Interleaving the memory space, setting the LSB of the address bus of Port A to 1 (V_{CC}), and the LSB of the

address bus of Port B to 0 (GND), allows a 32-bit wide single port RAM to be created.

Creating Two Single-Port RAMs

The true dual-read/write port functionality of the block SelectRAM+ memory allows a single RAM to be split into two single port memories of 2K bits each as shown in **Figure 36**.

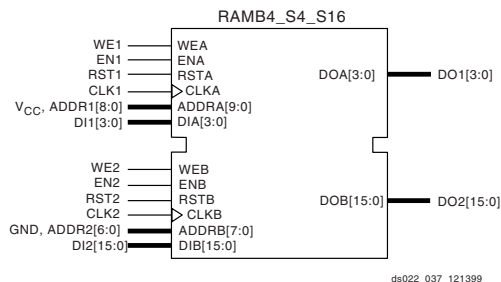


Figure 36: 512 x 4 RAM and 128 x 16 RAM

In this example, a 512K x 4 RAM (Port A) and a 128 x 16 RAM (Port B) are created out of a single block SelectRAM+. The address space for the RAM is split by fixing the MSB of Port A to 1 (V_{CC}) for the upper 2K bits and the MSB of Port B to 0 (GND) for the lower 2K bits.

Block Memory Generation

The CoreGen program generates memory structures using the block SelectRAM+ features. This program outputs VHDL or Verilog simulation code templates and an EDIF file for inclusion in a design.

Table 44: Bidirectional I/O Library Macros

Name	Inputs	Bidirectional	Outputs
IOBUFDS_FD_LVDS	D, T, C	IO, IOB	Q
IOBUFDS_FDE_LVDS	D, T, CE, C	IO, IOB	Q
IOBUFDS_FDC_LVDS	D, T, C, CLR	IO, IOB	Q
IOBUFDS_FDCE_LVDS	D, T, CE, C, CLR	IO, IOB	Q
IOBUFDS_FDP_LVDS	D, T, C, PRE	IO, IOB	Q
IOBUFDS_FDPE_LVDS	D, T, CE, C, PRE	IO, IOB	Q
IOBUFDS_FDR_LVDS	D, T, C, R	IO, IOB	Q
IOBUFDS_FDRE_LVDS	D, T, CE, C, R	IO, IOB	Q
IOBUFDS_FDS_LVDS	D, T, C, S	IO, IOB	Q
IOBUFDS_FDSE_LVDS	D, T, CE, C, S	IO, IOB	Q
IOBUFDS_LD_LVDS	D, T, G	IO, IOB	Q
IOBUFDS_LDE_LVDS	D, T, GE, G	IO, IOB	Q
IOBUFDS_LDC_LVDS	D, T, G, CLR	IO, IOB	Q
IOBUFDS_LDCE_LVDS	D, T, GE, G, CLR	IO, IOB	Q
IOBUFDS_LDP_LVDS	D, T, G, PRE	IO, IOB	Q
IOBUFDS_LDPE_LVDS	D, T, GE, G, PRE	IO, IOB	Q

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/7/99	1.0	Initial Xilinx release.
1/10/00	1.1	Re-released with spd.txt v. 1.18, FG860/900/1156 package information, and additional DLL, Select RAM and SelectI/O information.
1/28/00	1.2	Added Delay Measurement Methodology table, updated SelectI/O section, Figures 30, 54, & 55, text explaining Table 5, T_{BYP} values, buffered Hex Line info, p. 8, I/O Timing Measurement notes, notes for Tables 15, 16, and corrected F1156 pinout table footnote references.
2/29/00	1.3	Updated pinout tables, V_{CC} page 20, and corrected Figure 20.
5/23/00	1.4	Correction to table on p. 22.
7/10/00	1.5	- Numerous minor edits. - Data sheet upgraded to Preliminary. - Preview -8 numbers added to Virtex-E Electrical Characteristics tables.
8/1/00	1.6	- Reformatted entire document to follow new style guidelines. - Changed speed grade values in tables on pages 35-37.

Virtex-E Data Sheet

The Virtex-E Data Sheet contains the following modules:

- DS022-1, Virtex-E 1.8V FPGAs:
[Introduction and Ordering Information \(Module 1\)](#)
- DS022-2, Virtex-E 1.8V FPGAs:
Functional Description (Module 2)
- DS022-3, Virtex-E 1.8V FPGAs:
[DC and Switching Characteristics \(Module 3\)](#)
- DS022-4, Virtex-E 1.8V FPGAs:
[Pinout Tables \(Module 4\)](#)

Calculation of $T_{i\text{oop}}$ as a Function of Capacitance

$T_{i\text{oop}}$ is the propagation delay from the O Input of the IOB to the pad. The values for $T_{i\text{oop}}$ are based on the standard capacitive load (C_{sl}) for each I/O standard as listed in [Table 3](#).

Table 3: Constants for Use in Calculation of $T_{i\text{oop}}$

Standard	Csl (pF)	fl (ns/pF)
LVTTL Fast Slew Rate, 2mA drive	35	0.41
LVTTL Fast Slew Rate, 4mA drive	35	0.20
LVTTL Fast Slew Rate, 6mA drive	35	0.13
LVTTL Fast Slew Rate, 8mA drive	35	0.079
LVTTL Fast Slew Rate, 12mA drive	35	0.044
LVTTL Fast Slew Rate, 16mA drive	35	0.043
LVTTL Fast Slew Rate, 24mA drive	35	0.033
LVTTL Slow Slew Rate, 2mA drive	35	0.41
LVTTL Slow Slew Rate, 4mA drive	35	0.20
LVTTL Slow Slew Rate, 6mA drive	35	0.10
LVTTL Slow Slew Rate, 8mA drive	35	0.086
LVTTL Slow Slew Rate, 12mA drive	35	0.058
LVTTL Slow Slew Rate, 16mA drive	35	0.050
LVTTL Slow Slew Rate, 24mA drive	35	0.048
LVC MOS2	35	0.041
LVC MOS18	35	0.050
PCI 33 MHz 3.3 V	10	0.050
PCI 66 MHz 3.3 V	10	0.033
GTL	0	0.014
GTL+	0	0.017
HSTL Class I	20	0.022
HSTL Class III	20	0.016
HSTL Class IV	20	0.014
SSTL2 Class I	30	0.028
SSTL2 Class II	30	0.016
SSTL3 Class I	30	0.029
SSTL3 Class II	30	0.016
CTT	20	0.035
AGP	10	0.037

Notes:

- I/O parameter measurements are made with the capacitance values shown above. See the application examples (in Module 2 of this data sheet) for appropriate terminations.
- I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

For other capacitive loads, use the formulas below to calculate the corresponding $T_{i\text{oop}}$:

$$T_{i\text{oop}} = T_{i\text{oop}} + T_{\text{opadjust}} + (C_{\text{load}} - C_{sl}) * fl$$

where:

T_{opadjust} is reported above in the Output Delay Adjustment section.

C_{load} is the capacitive load for the design.

Table 4: Delay Measurement Methodology

Standard	V_L^1	V_H^1	Meas. Point	V_{REF} (Typ) ²
LVTTL	0	3	1.4	-
LVC MOS2	0	2.5	1.125	-
PCI33_3	Per PCI Spec			-
PCI66_3	Per PCI Spec			-
GTL	$V_{REF} - 0.2$	$V_{REF} + 0.2$	V_{REF}	0.80
GTL+	$V_{REF} - 0.2$	$V_{REF} + 0.2$	V_{REF}	1.0
HSTL Class I	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.75
HSTL Class III	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL Class IV	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
SSTL3 I & II	$V_{REF} - 1.0$	$V_{REF} + 1.0$	V_{REF}	1.5
SSTL2 I & II	$V_{REF} - 0.75$	$V_{REF} + 0.75$	V_{REF}	1.25
CTT	$V_{REF} - 0.2$	$V_{REF} + 0.2$	V_{REF}	1.5
AGP	$V_{REF} - (0.2 \times V_{CCO})$	$V_{REF} + (0.2 \times V_{CCO})$	V_{REF}	Per AGP Spec
LVDS	1.2 - 0.125	1.2 + 0.125	1.2	
LVPECL	1.6 - 0.3	1.6 + 0.3	1.6	

Notes:

- Input waveform switches between V_L and V_H .
- Measurements are made at V_{REF} (Typ), Maximum, and Minimum. Worst-case values are reported.
I/O parameter measurements are made with the capacitance values shown in [Table 3](#). See the application examples (in Module 2 of this data sheet) for appropriate terminations.
I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

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7/10/00	1.5	- Numerous minor edits. - Data sheet upgraded to Preliminary. - Preview -8 numbers added to Virtex-E Electrical Characteristics tables.
8/1/00	1.6	- Reformatted entire document to follow new style guidelines. - Changed speed grade values in tables on pages 35-37.
9/20/00	1.7	- Min values added to Virtex-E Electrical Characteristics tables. - XCV2600E and XCV3200E numbers added to Virtex-E Electrical Characteristics tables (Module 3). - Corrected user I/O count for XCV100E device in Table 1 (Module 1). - Changed several pins to "No Connect in the XCV100E" and removed duplicate V_{CCINT} pins in Table ~ (Module 4). - Changed pin J10 to "No connect in XCV600E" in Table 74 (Module 4). - Changed pin J30 to "VREF option only in the XCV600E" in Table 74 (Module 4). - Corrected pair 18 in Table 75 (Module 4) to be "AO in the XCV1000E, XCV1600E".
11/20/00	1.8	- Upgraded speed grade -8 numbers in Virtex-E Electrical Characteristics tables to Preliminary. - Updated minimums in Table 13 and added notes to Table 14. - Added to note 2 to Absolute Maximum Ratings. - Changed speed grade -8 numbers for $T_{SHCKO32}$, T_{REG}, T_{BCCS}, and T_{ICKOF}. - Changed all minimum hold times to -0.4 under Global Clock Set-Up and Hold for LVTTTL Standard, with DLL. - Revised maximum T_{DLLPW} in -6 speed grade for DLL Timing Parameters. - Changed GCLK0 to BA22 for FG860 package in Table 46.
2/12/01	1.9	- Revised footnote for Table 14. - Added numbers to Virtex-E Electrical Characteristics tables for XCV1000E and XCV2000E devices. - Updated Table 27 and Table 78 to include values for XCV400E and XCV600E devices. - Revised Table 62 to include pinout information for the XCV400E and XCV600E devices in the BG560 package. - Updated footnotes 1 and 2 for Table 76 to include XCV2600E and XCV3200E devices.
4/02/01	2.0	- Updated numerous values in Virtex-E Switching Characteristics tables. - Converted data sheet to modularized format. See the Virtex-E Data Sheet section.
4/19/01	2.1	Updated values in Virtex-E Switching Characteristics tables.

Table 7: PQ240 Differential Pin Pair Summary
XCV50E, XCV100E, XCV200E, XCV300E, XCV400E

Pair	Bank	P Pin	N Pin	AO	Other Functions
48	6	P56	P57	√	-
49	6	P52	P53	2	-
50	6	P49	P50	3	VREF
51	6	P46	P47	4	VREF
52	6	P41	P42	√	-
53	6	P38	P39	2	-
54	6	P35	P36	4	VREF
55	6	P33	P34	5	VREF
56	7	P27	P28	√	-
57	7	P23	P24	4	VREF
58	7	P20	P21	2	-
59	7	P17	P18	√	-
60	7	P12	P13	4	VREF
61	7	P9	P10	3	VREF
62	7	P6	P7	2	-
63	7	P4	P5	6	VREF

Notes:

1. AO in the XCV50E.
2. AO in the XCV50E, 100E, 200E, 300E.
3. AO in the XCV50E, 200E, 300E, 400E.
4. AO in the XCV50E, 300E, 400E.
5. AO in the XCV100E, 200E, 400E.
6. AO in the XCV100E, 400E.
7. AO in the XCV50E, 200E, 400E.
8. AO in the XCV100E.

HQ240 High-Heat Quad Flat-Pack Packages

XCV600E and XCV1000E devices in High-heat dissipation Quad Flat-pack packages have footprint compatibility. Pins labeled IO_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF} it can be used as general I/O. Immediately following Table 8, see Table 9 for Differential Pair information.

Table 8: HQ240 — XCV600E, XCV1000E

Pin #	Pin Description	Bank
P240	VCCO	7
P239	TCK	NA
P238	IO	0
P237	IO_L0N	0
P236	IO_VREF_L0P	0
P235	IO_L1N_YY	0
P234	IO_L1P_YY	0
P233	GND	NA
P232	VCCO	0
P231	IO_VREF	0
P230	IO_VREF	0
P229	IO_VREF_L2N_YY	0
P228	IO_L2P_YY	0
P227	GND	NA
P226	VCCO	0
P225	VCCINT	NA
P224	IO_L3N_YY	0
P223	IO_L3P_YY	0
P222	IO_VREF	0 ¹
P221	IO_L4N_Y	0
P220	IO_L4P_Y	0
P219	GND	NA
P218	IO_VREF_L5N_Y	0
P217	IO_L5P_Y	0
P216	IO_VREF	0
P215	IO_LVDS_DLL_L6N	0
P214	VCCINT	NA
P213	GCK3	0
P212	VCCO	0
P211	GND	NA

Table 8: HQ240 — XCV600E, XCV1000E

Pin #	Pin Description	Bank
P66	IO_VREF_L46P	5
P65	IO_L46N	5
P64	IO_L47P_YY	5
P63	IO_L47N_YY	5
P62	M2	NA
P61	VCCO	5
P60	M0	NA
P59	GND	NA
P58	M1	NA
P57	IO_L48N_YY	6
P56	IO_L48P_YY	6
P55	VCCO	6
P54	IO_VREF	6
P53	IO_L49N_Y	6
P52	IO_L49P_Y	6
P51	GND	NA
P50	IO_VREF_L50N_Y	6
P49	IO_L50P_Y	6
P48	IO_VREF	6
P47	IO_VREF_L51N_Y	6
P46	IO_L51P_Y	6
P45	GND	NA
P44	VCCO	6
P43	VCCINT	NA
P42	IO_L52N_YY	6
P41	IO_L52P_YY	6
P40 ¹	IO_VREF	6
P39	IO_L53N_Y	6
P38	IO_L53P_Y	6
P37	GND	NA
P36	IO_VREF_L54N_Y	6
P35	IO_L54P_Y	6
P34	IO_L55N_Y	6
P33	IO_VREF_L55P_Y	6
P32	VCCINT	NA
P31	IO	6

Table 8: HQ240 — XCV600E, XCV1000E

Pin #	Pin Description	Bank
P30	VCCO	6
P29	GND	NA
P28	IO_L56N_YY	7
P27	IO_L56P_YY	7
P26	IO_VREF	7
P25	VCCO	7
P24	IO_L57N_Y	7
P23	IO_VREF_L57P_Y	7
P22	GND	NA
P21	IO_L58N_Y	7
P20	IO_L58P_Y	7
P19 ¹	IO_VREF	7
P18	IO_L59N_YY	7
P17	IO_L59P_YY	7
P16	VCCINT	NA
P15	VCCO	7
P14	GND	NA
P13	IO_L60N_Y	7
P12	IO_VREF_L60P_Y	7
P11	IO_VREF	7
P10	IO_L61N_Y	7
P9	IO_VREF_L61P_Y	7
P8	GND	NA
P7	IO_L62N_Y	7
P6	IO_L62P_Y	7
P5	IO_VREF_L63N_Y	7
P4	IO_L63P_Y	7
P3	IO	7
P2	TMS	NA
P1	GND	NA

Notes:

1. V_{REF} or I/O option only in the XCV1000E; otherwise, I/O option only.

HQ240 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A ✓ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

**Table 9: HQ240 Differential Pin Pair Summary
XCV600E, XCV1000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	P92	P93	NA	IO_DLL_L40P
1	5	P89	P87	NA	IO_DLL_L40N
2	1	P210	P209	NA	IO_DLL_L6P
3	0	P213	P215	NA	IO_DLL_L6N
IO LVDS					
Total Pairs: 64, Asynchronous Output Pairs: 53					
0	0	P236	P237	NA	VREF
1	0	P234	P235	✓	-
2	0	P228	P229	✓	VREF
3	0	P223	P224	✓	-
4	0	P220	P221	✓	-
5	0	P217	P218	✓	VREF
6	1	P209	P215	NA	IO_LVDS_DLL
7	1	P205	P206	✓	VREF
8	1	P202	P203	✓	-
9	1	P199	P200	✓	-
10	1	P194	P195	✓	VREF
11	1	P191	P192	✓	VREF
12	1	P188	P189	✓	-
13	1	P186	P187	NA	VREF
14	1	P184	P185	✓	CS
15	2	P178	P177	✓	DIN, D0

**Table 9: HQ240 Differential Pin Pair Summary
XCV600E, XCV1000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
16	2	P174	P173	✓	-
17	2	P171	P170	✓	VREF
18	2	P168	P167	✓	D1
19	2	P163	P162	✓	D2
20	2	P160	P159	✓	-
21	2	P157	P156	✓	D3
22	2	P155	P154	1	VREF
23	2	P153	P152	✓	-
24	3	P145	P144	✓	D4, VREF
25	3	P142	P141	✓	-
26	3	P139	P138	✓	D5
27	3	P134	P133	✓	VREF
28	3	P131	P130	✓	VREF
29	3	P128	P127	✓	-
30	3	P126	P125	1	VREF
31	3	P124	P123	✓	INIT
32	4	P118	P117	✓	-
33	4	P114	P113	✓	-
34	4	P111	P110	✓	VREF
35	4	P108	P107	✓	VREF
36	4	P103	P102	✓	-
37	4	P100	P99	✓	-
38	4	P97	P96	✓	VREF
39	4	P95	P94	NA	VREF
40	5	P93	P87	NA	IO_LVDS_DLL
41	5	P84	P82	NA	VREF
42	5	P79	P78	✓	-
43	5	P74	P73	✓	VREF
44	5	P71	P70	✓	VREF
45	5	P68	P67	✓	-
46	5	P66	P65	NA	VREF
47	5	P64	P63	✓	-

Table 14: BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin#	See Note
7	IO_L165N_YY	P32	
7	IO_VREF_L165P_YY	P31	
7	IO_L166N_Y	P30	
7	IO_L166P_Y	P29	
7	IO_L167N_Y	M32	
7	IO_L167P_Y	N31	
7	IO_L168N_Y	N30	
7	IO_VREF_L168P_Y	L33	3
7	IO_L169N_Y	M31	
7	IO_L169P_Y	L32	
7	IO_L170N_Y	M30	
7	IO_L170P_Y	L31	
7	IO_L171N_YY	M29	
7	IO_L171P_YY	J33	
7	IO_L172N_YY	L30	
7	IO_VREF_L172P_YY	K31	
7	IO_L173N_Y	L29	
7	IO_L173P_Y	H33	
7	IO_L174N_Y	J31	
7	IO_VREF_L174P_Y	H32	4
7	IO_L175N_Y	K29	
7	IO_L175P_Y	H31	
7	IO_L176N_Y	J30	
7	IO_VREF_L176P_Y	G32	1
7	IO_L177N_YY	J29	
7	IO_VREF_L177P_YY	G31	
7	IO_L178N_Y	E33	
7	IO_L178P_Y	E32	
7	IO_L179N_Y	H29	
7	IO_L179P_Y	F31	
7	IO_L180N_Y	D32	
7	IO_VREF_L180P_Y	E31	
7	IO_L181N_Y	G29	
7	IO_L181P_Y	C33	
7	IO_L182N_Y	F30	

Table 14: BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin#	See Note
7	IO_VREF_L182P_Y	D31	3
2	CCLK	C4	
3	DONE	AJ5	
NA	DXN	AK29	
NA	DXP	AJ28	
NA	M0	AJ29	
NA	M1	AK30	
NA	M2	AN32	
NA	PROGRAM	AM1	
NA	TCK	E29	
NA	TDI	D5	
2	TDO	E6	
NA	TMS	B33	
NA	NC	C31	
NA	NC	AC2	
NA	NC	AK4	
NA	NC	AL3	
NA	VCCINT	A21	
NA	VCCINT	B12	
NA	VCCINT	B14	
NA	VCCINT	B18	
NA	VCCINT	B28	
NA	VCCINT	C22	
NA	VCCINT	C24	
NA	VCCINT	E9	
NA	VCCINT	E12	
NA	VCCINT	F2	
NA	VCCINT	H30	
NA	VCCINT	J1	
NA	VCCINT	K32	
NA	VCCINT	M3	
NA	VCCINT	N1	

Table 18: FG456 — XCV200E and XCV300E

Bank	Pin Description	Pin #
1	IO_L23P_Y	A17
1	IO_L24N_YY	B17
1	IO_VREF_L24P_YY	A18
1	IO_L25N_YY	D16
1	IO_L25P_YY	C17
1	IO_L26N_YY	B18
1	IO_VREF_L26P_YY	A19
1	IO_L27N_YY	D17
1	IO_L27P_YY	C18
1	IO_WRITE_L28N_YY	A20
1	IO_CS_L28P_YY	C19
2	IO	D18 ¹
2	IO	E19 ¹
2	IO	E20
2	IO	F20
2	IO	G21
2	IO	G22 ¹
2	IO	J22
2	IO	L19 ¹
2	IO_D3	K20
2	IO_DOUT_BUSY_L29P_YY	C21
2	IO_DIN_D0_L29N_YY	D20
2	IO_L30P_YY	C22
2	IO_L30N_YY	D21
2	IO_VREF_L31P_YY	D22
2	IO_L31N_YY	E21
2	IO_L32P_YY	E22
2	IO_L32N_YY	F18
2	IO_VREF_L33P_YY	F21
2	IO_L33N_YY	F19
2	IO_L34P_Y	F22
2	IO_L34N_Y	G19
2	IO_L35P_Y	G20
2	IO_L35N_Y	G18
2	IO_VREF_L36P_Y	H18
2	IO_D1_L36N_Y	H22

Table 18: FG456 — XCV200E and XCV300E

Bank	Pin Description	Pin #
2	IO_D2_L37P_YY	H20
2	IO_L37N_YY	H19
2	IO_L38P_YY	H21
2	IO_L38N_YY	J19
2	IO_L39P_YY	J18
2	IO_L39N_YY	J20
2	IO_L40P_Y	K18
2	IO_L40N_Y	J21
2	IO_L41P	K22
2	IO_VREF_L41N	K21
2	IO_L42P_Y	K19
2	IO_L42N_Y	L22
2	IO_L43P_YY	L21
2	IO_L43N_YY	L18
2	IO_L44P_YY	L17
2	IO_L44N_YY	L20
3	IO	M21 ¹
3	IO	P22
3	IO	R20 ¹
3	IO	R22
3	IO	T19
3	IO	U18 ¹
3	IO	V20
3	IO	V21
3	IO	Y22 ¹
3	IO_L45P_YY	M18
3	IO_L45N_YY	M20
3	IO_L46P_Y	M19
3	IO_L46N_Y	M17
3	IO_D4_L47P_Y	N22
3	IO_VREF_L47N_Y	N21
3	IO_L48P_YY	N20
3	IO_L48N_YY	N18
3	IO_L49P_YY	N19
3	IO_L49N_YY	P21
3	IO_L50P_YY	P20

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
7	IO	D2
7	IO	D3
7	IO	E1
7	IO	G1
7	IO	H2
7	IO	J1 ¹
7	IO	L1 ¹
7	IO	M1 ¹
7	IO	N1 ¹
7	IO_L160N_YY	N5
7	IO_L160P_YY	N8
7	IO_L161N_YY	N6
7	IO_L161P_YY	N3
7	IO_L162N_Y	N4
7	IO_VREF_L162P_Y	M2
7	IO_L163N_Y	N7
7	IO_L163P_Y	M7
7	IO_L164N_YY	M6
7	IO_L164P_YY	M3
7	IO_L165N_YY	M4
7	IO_VREF_L165P_YY	M5
7	IO_L166N_Y	L3
7	IO_L166P_Y	L7
7	IO_L167N_Y	L6
7	IO_L167P_Y	K2
7	IO_L168N_Y	L4
7	IO_L168P_Y	K1
7	IO_L169N_Y	K3
7	IO_L169P_Y	L5
7	IO_L170N_YY	K5
7	IO_L170P_YY	J3
7	IO_L171N_YY	K4
7	IO_L171P_YY	J4
7	IO_L172N_YY	H3
7	IO_VREF_L172P_YY	K6
7	IO_L173N_YY	K7
7	IO_L173P_YY	G3

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
7	IO_L174N_Y	J5
7	IO_VREF_L174P_Y	H1 ²
7	IO_L175N_Y	G2
7	IO_L175P_Y	J6
7	IO_L176N_YY	J7
7	IO_L176P_YY	F1
7	IO_L177N_YY	H4
7	IO_VREF_L177P_YY	G4
7	IO_L178N_Y	F3
7	IO_L178P_Y	H5
7	IO_L179N_Y	E2
7	IO_L179P_Y	H6
7	IO_L180N_Y	G5
7	IO_VREF_L180P_Y	F4
7	IO_L181N_Y	H7
7	IO_L181P_Y	G6
7	IO_L182N_YY	E3
7	IO_L182P_YY	E4
2	CCLK	D24
3	DONE	AB21
NA	DXN	AB7
NA	DXP	Y8
NA	M0	AD4
NA	M1	W7
NA	M2	AB6
NA	PROGRAM	AA22
NA	TCK	E6
NA	TDI	D22
2	TDO	C23
NA	TMS	F5
NA	NC	T25
NA	NC	T2
NA	NC	P2
NA	NC	N25
NA	NC	L25

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
4	IO_VREF_L132P_YY	AV8
4	IO_L132N_YY	AU9
4	IO_L133P_Y	AW8
4	IO_L133N_Y	AT10
4	IO_VREF_L134P_Y	AV9 ³
4	IO_L134N_Y	AU10
4	IO_L135P_YY	AW9
4	IO_L135N_YY	AT11
4	IO_VREF_L136P_YY	AV10
4	IO_L136N_YY	AU11
4	IO_L137P_Y	AW10
4	IO_L137N_Y	AU12
4	IO_L138P_Y	AV11
4	IO_L138N_Y	AT13
4	IO_VREF_L139P_YY	AW11
4	IO_L139N_YY	AU13
4	IO_L140P_YY	AT14
4	IO_L140N_YY	AV12
4	IO_L141P_Y	AU14
4	IO_L141N_Y	AW12
4	IO_L142P_Y	AT15
4	IO_L142N_Y	AV13
4	IO_L143P_YY	AU15
4	IO_L143N_YY	AW13
4	IO_VREF_L144P_YY	AV14 ¹
4	IO_L144N_YY	AT16
4	IO_L145P_Y	AW14
4	IO_L145N_Y	AU16
4	IO_L146P_Y	AV15
4	IO_L146N_Y	AR17
4	IO_L147P_YY	AW15
4	IO_L147N_YY	AT17
4	IO_VREF_L148P_YY	AU17
4	IO_L148N_YY	AV16
4	IO_L149P_Y	AR18
4	IO_L149N_Y	AW16

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
4	IO_L150P_Y	AT18
4	IO_L150N_Y	AV17
4	IO_L151P_YY	AU18
4	IO_L151N_YY	AW17
4	IO_VREF_L152P_YY	AT19
4	IO_L152N_YY	AV18
4	IO_L153P_Y	AU19
4	IO_L153N_Y	AW18
4	IO_VREF_L154P	AU21 ²
4	IO_L154N	AV19
4	IO_LVDS_DLL_L155P	AT21
5	GCK1	AU22
5	IO	AT34
5	IO	AW20
5	IO_LVDS_DLL_L155N	AT22
5	IO_VREF_L156P_Y	AV20 ²
5	IO_L156N_Y	AR22
5	IO_L157P_YY	AV23
5	IO_VREF_L157N_YY	AW21
5	IO_L158P_YY	AU23
5	IO_L158N_YY	AV21
5	IO_L159P_Y	AT23
5	IO_L159N_Y	AW22
5	IO_L160P_Y	AR23
5	IO_L160N_Y	AV22
5	IO_L161P_YY	AV24
5	IO_VREF_L161N_YY	AW23
5	IO_L162P_YY	AW24
5	IO_L162N_YY	AU24
5	IO_L163P_Y	AW25
5	IO_L163N_Y	AT24
5	IO_L164P_Y	AV25
5	IO_L164N_Y	AU25
5	IO_L165P_YY	AW26
5	IO_VREF_L165N_YY	AT25 ¹

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
5	IO_L166P_YY	AV26
5	IO_L166N_YY	AW27
5	IO_L167P_Y	AU26
5	IO_L167N_Y	AV27
5	IO_L168P_Y	AT26
5	IO_L168N_Y	AW28
5	IO_L169P_YY	AU27
5	IO_L169N_YY	AV28
5	IO_L170P_YY	AW29
5	IO_VREF_L170N_YY	AT27
5	IO_L171P_Y	AW30
5	IO_L171N_Y	AU28
5	IO_L172P_Y	AV30
5	IO_L172N_Y	AV29
5	IO_L173P_YY	AW31
5	IO_VREF_L173N_YY	AU29
5	IO_L174P_YY	AV31
5	IO_L174N_YY	AT29
5	IO_L175P_Y	AW32
5	IO_VREF_L175N_Y	AU30 ³
5	IO_L176P_Y	AW33
5	IO_L176N_Y	AT30
5	IO_L177P_YY	AV33
5	IO_VREF_L177N_YY	AU31
5	IO_L178P_YY	AT31
5	IO_L178N_YY	AW34
5	IO_L179P_Y	AV32
5	IO_L179N_Y	AV34
5	IO_L180P_Y	AU32
5	IO_L180N_Y	AW35
5	IO_L181P_YY	AT32
5	IO_VREF_L181N_YY	AV35
5	IO_L182P_YY	AU33
5	IO_L182N_YY	AW36
5	IO_L183P_Y	AT33
5	IO_VREF_L183N_Y	AV36 ¹

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
5	IO_L184P_Y	AU34
5	IO_L184N_Y	AU36
6	IO	W39
6	IO	AR37
6	IO	AR39
6	IO_L185N_YY	AR36
6	IO_L185P_YY	AT38
6	IO_L186N_Y	AR38
6	IO_L186P_Y	AP36
6	IO_VREF_L187N	AT39 ¹
6	IO_L187P	AP37
6	IO_L188N	AP38
6	IO_L188P	AP39
6	IO_VREF_L189N_Y	AN36
6	IO_L189P_Y	AN38
6	IO_L190N_YY	AN37
6	IO_L190P_YY	AN39
6	IO_L191N	AM36
6	IO_L191P	AM38
6	IO_L192N_Y	AM37
6	IO_L192P_Y	AL36
6	IO_VREF_L193N_YY	AM39
6	IO_L193P_YY	AL37
6	IO_L194N_YY	AL38
6	IO_L194P_YY	AK36
6	IO_VREF_L195N	AL39 ³
6	IO_L195P	AK37
6	IO_L196N	AK38
6	IO_L196P	AJ36
6	IO_VREF_L197N_YY	AK39
6	IO_L197P_YY	AJ37
6	IO_L198N_YY	AJ38
6	IO_L198P_YY	AH37
6	IO_L199N	AJ39
6	IO_L199P	AH38

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
2	IO_D1_L87N_YY	P2
2	IO_D2_L88P_YY	P3
2	IO_L88N_YY	L4
2	IO_L89P_Y	P1
2	IO_L89N_Y	R2
2	IO_L90P_Y	M5
2	IO_L90N_Y	R3
2	IO_L91P_Y	M4
2	IO_L91N_Y	R1
2	IO_L92P	N4
2	IO_L92N	T2
2	IO_L93P_Y	P5
2	IO_L93N_Y	T3
2	IO_VREF_L94P_Y	P4
2	IO_L94N_Y	T1
2	IO_L95P_YY	U2
2	IO_L95N_YY	R4
2	IO_L96P_Y	U3
2	IO_L96N_Y	T5
2	IO_L97P_Y	T4
2	IO_L97N_Y	V2
2	IO_VREF_L98P_YY	U5
2	IO_D3_L98N_YY	V3
2	IO_L99P_YY	V1
2	IO_L99N_YY	V5
2	IO_L100P_Y	W2
2	IO_L100N_Y	V4
2	IO_L101P_Y	W5
2	IO_L101N_Y	W1
2	IO_VREF_L102P_YY	Y2
2	IO_L102N_YY	W4
2	IO_L103P_YY	Y1
2	IO_L103N_YY	Y5
2	IO_VREF_L104P_Y	AA1 ¹
2	IO_L104N_Y	Y4
2	IO_L105P_YY	AA4
2	IO_L105N_YY	AA2

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
3	IO	AB4
3	IO	AC2
3	IO	AD1
3	IO	AE3
3	IO	AF4
3	IO	AH5
3	IO	AJ2
3	IO	AL1
3	IO	AM3
3	IO	AP3
3	IO	AR5
3	IO	AU4
3	IO	AB2
3	IO_L106P_Y	AB3
3	IO_VREF_L106N_Y	AC4 ¹
3	IO_L107P_YY	AB1
3	IO_L107N_YY	AC5
3	IO_L108P_YY	AD4
3	IO_VREF_L108N_YY	AC3
3	IO_L109P_Y	AC1
3	IO_L109N_Y	AD5
3	IO_L110P_Y	AE4
3	IO_L110N_Y	AD3
3	IO_L111P_YY	AE5
3	IO_L111N_YY	AD2
3	IO_D4_L112P_YY	AE1
3	IO_VREF_L112N_YY	AF5
3	IO_L113P_Y	AE2
3	IO_L113N_Y	AG4
3	IO_L114P_Y	AG5
3	IO_L114N_Y	AF1
3	IO_L115P_YY	AH4
3	IO_L115N_YY	AF2
3	IO_L116P_Y	AF3
3	IO_VREF_L116N_Y	AJ4
3	IO_L117P_Y	AG1

Table 26: FG900 — XCV600E, XCV1000E, XCV1600E

Bank	Pin Description	Pin #
6	IO	AC5 ⁴
6	IO	AD1 ⁴
6	IO	AE5 ⁵
6	IO_L212N_YY	AF3
6	IO_L212P_YY	AC6
6	IO_L213N	AH2 ⁴
6	IO_L213P	AG2 ³
6	IO_L214N	AB9
6	IO_L214P	AE4
6	IO_VREF_L215N_YY	AE3 ¹
6	IO_L215P_YY	AH1
6	IO_L216N_Y	AB8 ⁴
6	IO_L216P_Y	AD6 ³
6	IO_L217N_YY	AG1
6	IO_L217P_YY	AA10
6	IO_VREF_L218N	AA9
6	IO_L218P	AD4
6	IO_L219N_YY	AD5
6	IO_L219P_YY	AD2
6	IO_L220N_YY	AD3
6	IO_L220P_YY	AF2
6	IO_L221N	AA8
6	IO_L221P	AA7
6	IO_VREF_L222N_YY	AF1
6	IO_L222P_YY	Y9
6	IO_L223N_YY	AB6
6	IO_L223P_YY	AC4
6	IO_L224N	AE1
6	IO_L224P	W8
6	IO_L225N_YY	Y8
6	IO_L225P_YY	AB4
6	IO_VREF_L226N_YY	AB3
6	IO_L226P_YY	W9
6	IO_L227N_YY	AA5 ⁴
6	IO_L227P_YY	W10 ³
6	IO_L228N_YY	AB1
6	IO_L228P_YY	V10

Table 26: FG900 — XCV600E, XCV1000E, XCV1600E

Bank	Pin Description	Pin #
6	IO_L229N_YY	Y7 ⁴
6	IO_VREF_L229P_YY	AC1
6	IO_L230N	V11
6	IO_L230P	AA3
6	IO_L231N_YY	AA2 ³
6	IO_L231P_YY	U10 ⁴
6	IO_L232N	W7
6	IO_L232P	AA6
6	IO_L233N_YY	Y6
6	IO_L233P_YY	Y4
6	IO_L234N_Y	AA1 ⁴
6	IO_L234P_Y	V7 ⁴
6	IO_L235N_YY	Y3
6	IO_L235P_YY	Y2
6	IO_VREF_L236N	Y5 ¹
6	IO_L236P	W5
6	IO_L237N_YY	W4
6	IO_L237P_YY	W6
6	IO_L238N_YY	V6
6	IO_L238P_YY	W2
6	IO_L239N	U9
6	IO_L239P	V4
6	IO_VREF_L240N_YY	AB2
6	IO_L240P_YY	T8
6	IO_L241N_YY	U5
6	IO_L241P_YY	W1
6	IO_L242N	Y1
6	IO_L242P	T9
6	IO_L243N_YY	T7
6	IO_L243P_YY	U3
6	IO_VREF_L244N_YY	T5
6	IO_L244P_YY	V2
6	IO_L245N_YY	R9 ⁴
6	IO_L245P_YY	T6 ³
6	IO_VREF_L246N_YY	T4 ²
6	IO_L246P_YY	U2
6	IO_L247N	T1

Table 26: FG900 — XCV600E, XCV1000E, XCV1600E

Bank	Pin Description	Pin #
7	IO_L275N_YY	G3
7	IO_L275P_YY	E1
7	IO_L276N_YY	H6
7	IO_L276P_YY	E2
7	IO_L277N	E4
7	IO_VREF_L277P	K9
7	IO_L278N_YY	J8
7	IO_L278P_YY	F4
7	IO_L279N_Y	D1 ³
7	IO_L279P_Y	H7 ⁴
7	IO_L280N_YY	G6
7	IO_VREF_L280P_YY	C2 ¹
7	IO_L281N	D2
7	IO_L281P	F5
7	IO_L282N_YY	D3 ⁴
7	IO_L282P_YY	K10 ³
2	CCLK	F26
3	DONE	AJ28
NA	DXN	AJ3
NA	DXP	AH4
NA	M0	AF4
NA	M1	AC7
NA	M2	AK3
NA	PROGRAM	AG28
NA	TCK	B3
NA	TDI	H22
2	TDO	D26
NA	TMS	C1
NA	VCCINT	L11
NA	VCCINT	L12
NA	VCCINT	L19
NA	VCCINT	L20
NA	VCCINT	M11
NA	VCCINT	M12
NA	VCCINT	M19

Table 26: FG900 — XCV600E, XCV1000E, XCV1600E

Bank	Pin Description	Pin #
NA	VCCINT	M20
NA	VCCINT	N13
NA	VCCINT	N14
NA	VCCINT	N15
NA	VCCINT	N16
NA	VCCINT	N17
NA	VCCINT	N18
NA	VCCINT	P13
NA	VCCINT	P18
NA	VCCINT	R13
NA	VCCINT	R18
NA	VCCINT	T13
NA	VCCINT	T18
NA	VCCINT	U13
NA	VCCINT	U18
NA	VCCINT	V13
NA	VCCINT	V14
NA	VCCINT	V15
NA	VCCINT	V16
NA	VCCINT	V17
NA	VCCINT	V18
NA	VCCINT	W11
NA	VCCINT	W12
NA	VCCINT	W19
NA	VCCINT	W20
NA	VCCINT	Y11
NA	VCCINT	Y12
NA	VCCINT	Y19
NA	VCCINT	Y20
NA	VCCO_0	B6
NA	VCCO_0	M15
NA	VCCO_0	M14
NA	VCCO_0	L15
NA	VCCO_0	L14
NA	VCCO_0	H14
NA	VCCO_0	M13

Table 27: FG900 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
256	7	N6	M6	1	-
257	7	N1	N5	4	-
258	7	M5	M4	√	-
259	7	M1	M2	1	VREF
260	7	L2	L4	4	-
261	7	L5	M7	3	-
262	7	M8	L1	4	-
263	7	M9	K2	1	-
264	7	M10	L3	NA	-
265	7	K1	K5	√	-
266	7	K3	L6	√	VREF
267	7	K4	L7	4	-
268	7	J5	L8	4	-
269	7	H4	K6	4	VREF
270	7	K7	H1	4	-
271	7	J2	J7	2	-
272	7	G2	H5	√	-
273	7	G5	L9	√	VREF
274	7	K8	F3	1	-
275	7	E1	G3	4	-
276	7	E2	H6	√	-
277	7	K9	E4	1	VREF
278	7	F4	J8	4	-
279	7	H7	D1	3	-
280	7	C2	G6	4	VREF
281	7	F5	D2	1	-
282	7	K10	D3	4	-

Notes:

1. AO in the XCV600E, 1000E.
2. AO in the XCV1000E.
3. AO in the XCV1600E.
4. AO in the XCV1000E, XCV1600E.

FG1156 Fine-Pitch Ball Grid Array Package

XCV1000E, XCV1600E, XCV2000E, XCV2600E, and XCV3200E devices in the FG1156 fine-pitch Ball Grid Array package have footprint compatibility. Pins labeled IO_VREF can be used as either V_{REF} or general I/O, unless indicated in the footnotes. If the pin is not used as V_{REF} , it can be used as general I/O. Immediately following Table 28, see Table 29 for Differential Pair information.

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
0	GCK3	E17
0	IO	B4
0	IO	B9
0	IO	B10
0	IO	D9 ³
0	IO	D16
0	IO	E7 ³
0	IO	E11 ³
0	IO	E13 ³
0	IO	E16 ³
0	IO	F17 ³
0	IO	J12 ³
0	IO	J13 ³
0	IO	J14 ³
0	IO	K11 ³
0	IO_L0N_Y	F7
0	IO_L0P_Y	H9
0	IO_L1N_Y	C5
0	IO_L1P_Y	J10
0	IO_VREF_L2N_Y	E6
0	IO_L2P_Y	D6
0	IO_L3N_Y	A4
0	IO_L3P_Y	G8
0	IO_L4N_YY	C6
0	IO_L4P_YY	J11
0	IO_VREF_L5N_YY	G9
0	IO_L5P_YY	F8
0	IO_L6N_YY	A5 ⁴

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
4	IO_L212N_YY	AP18
4	IO_L213P_Y	AF18
4	IO_L213N_Y	AP17
4	IO_VREF_L214P_Y	AJ18 ¹
4	IO_L214N_Y	AL18
4	IO_LVDS_DLL_L215P	AM18
5	GCK1	AL19
5	IO	AF17 ³
5	IO	AG12 ³
5	IO	AH12
5	IO	AJ10 ³
5	IO	AJ11 ³
5	IO	AK7 ³
5	IO	AK13 ³
5	IO	AL13 ³
5	IO	AM4 ³
5	IO	AN9
5	IO	AN10 ³
5	IO	AN16
5	IO	AN17 ³
5	IO_LVDS_DLL_L215N	AL17
5	IO_L216P_Y	AH17
5	IO_VREF_L216N_Y	AM17 ¹
5	IO_L217P_Y	AJ17
5	IO_L217N_Y	AG17
5	IO_L218P_YY	AP16
5	IO_VREF_L218N_YY	AL16
5	IO_L219P_YY	AJ16
5	IO_L219N_YY	AM16
5	IO_L220P	AK16 ⁵
5	IO_L220N	AP15 ⁴
5	IO_L221P_Y	AL15
5	IO_L221N_Y	AH16

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
5	IO_L222P_Y	AN15
5	IO_L222N_Y	AF16
5	IO_L223P_Y	AP14 ⁵
5	IO_L223N_Y	AE16 ⁴
5	IO_L224P_YY	AK15
5	IO_VREF_L224N_YY	AJ15
5	IO_L225P_YY	AH15
5	IO_L225N_YY	AN14
5	IO_L226P	AK14 ⁵
5	IO_L226N	AG15 ⁴
5	IO_L227P_Y	AM13
5	IO_L227N_Y	AF15
5	IO_L228P_Y	AG14
5	IO_L228N_Y	AP13
5	IO_L229P_YY	AE14 ⁵
5	IO_L229N_YY	AE15 ⁴
5	IO_L230P_YY	AN13
5	IO_VREF_L230N_YY	AG13
5	IO_L231P_YY	AH14
5	IO_L231N_YY	AP12
5	IO_L232P_Y	AJ14
5	IO_L232N_Y	AL14
5	IO_L233P_Y	AF13
5	IO_L233N_Y	AN12
5	IO_L234P_Y	AF14
5	IO_L234N_Y	AP11
5	IO_L235P_Y	AN11
5	IO_L235N_Y	AH13
5	IO_L236P_YY	AM12
5	IO_L236N_YY	AL12
5	IO_L237P_YY	AJ13
5	IO_VREF_L237N_YY	AP10
5	IO_L238P_Y	AK12
5	IO_L238N_Y	AM10

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
32	0	B14	E14	3200 2600 2000 1600 1000	-
33	0	D14	G15	3200 2600 2000 1600 1000	VREF
34	0	D15	J16	3200 1600	-
35	0	B15	F15	3200 2000 1000	-
36	0	E15	A15	3200 2000 1000	-
37	0	A16	G16	3200 2600	-
38	0	J17	F16	3200 2600 2000 1600 1000	-
39	0	B16	C16	3200 2600 2000 1600 1000	VREF
40	0	A17	H17	2600 1600 1000	-
41	0	B17	G17	2600 1600 1000	VREF
42	1	J18	C17	None	IO_LVDS_DLL
43	1	C18	G18	2600 1600 1000	VREF
44	1	F18	H18	2600 1600 1000	-
45	1	A19	B19	3200 2600 2000 1600 1000	VREF
46	1	C19	K19	3200 2600 2000 1600 1000	-
47	1	E19	F19	3200 2600	-
48	1	J19	G19	3200 2000 1000	-
49	1	G20	A20	3200 2000 1000	-
50	1	F20	B20	3200 1600	-
51	1	E20	D20	3200 2600 2000 1600 1000	VREF

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
52	1	A21	H20	3200 2600 2000 1600 1000	-
53	1	J20	E21	3200	-
54	1	K20	D21	3200 2600 1000	-
55	1	H21	B21	3200 2600 1000	-
56	1	F21	G21	2000 1600	-
57	1	B22	A22	3200 2600 2000 1600 1000	VREF
58	1	C22	J21	3200 2600 2000 1600 1000	-
59	1	G22	D22	3200 2600 1000	-
60	1	A23	K21	3200 2000 1000	-
61	1	B23	F22	3200 2000 1000	-
62	1	H22	C23	3200 1600 1000	-
63	1	K22	D23	3200 2600 2000 1600 1000	-
64	1	J22	A24	3200 2600 2000 1600 1000	VREF
65	1	D24	H23	2600 1600 1000	-
66	1	E24	A25	2600 1600 1000	-
67	1	C25	A26	3200 2600 2000 1600 1000	VREF
68	1	B26	F24	3200 2600 2000 1600 1000	-
69	1	F25	K23	3200 2600	-
70	1	H24	C26	3200 2000 1000	VREF

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
153	3	AD31	AF33	3200 2600 2000 1600 1000	VREF
154	3	AC28	AF31	3200 2600 1600 1000	-
155	3	AC27	AF32	3200 2600 1600	-
156	3	AE29	AD28	2600 1000	VREF
157	3	AD30	AG32	3200 2600 2000 1600 1000	-
158	3	AC26	AH33	2000 1600	-
159	3	AD26	AF30	3200 2600 2000 1600 1000	VREF
160	3	AC25	AH32	2600 2000 1000	-
161	3	AE28	AL34	3200 2600 2000	-
162	3	AG30	AD27	3200 2600 1600 1000	-
163	3	AF29	AK34	3200 2600 2000 1600 1000	-
164	3	AD25	AE27	3200 2600 2000 1600	-
165	3	AJ33	AH31	2600 2000 1000	VREF
166	3	AE26	AL33	3200 2600 1600 1000	-
167	3	AF28	AL32	2600 1600	-
168	3	AJ31	AF27	3200 2600 1600 1000	VREF
169	3	AG29	AJ32	2600 2000 1000	-
170	3	AK33	AH30	3200 2600 2000	-
171	3	AK32	AK31	3200 2600 2000 1600 1000	INIT

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
172	4	AP31	AK29	3200 2600 2000 1600 1000	-
173	4	AP30	AN31	3200 1600 1000	-
174	4	AH27	AN30	3200 2000 1000	-
175	4	AM30	AK28	3200 2000 1000	VREF
176	4	AG26	AN29	3200 2600 1000	-
177	4	AF25	AM29	3200 2600 2000 1600 1000	-
178	4	AL29	AL28	3200 2600 2000 1600 1000	VREF
179	4	AE24	AN28	2000 1600	-
180	4	AJ27	AH26	3200 1000	-
181	4	AG25	AK27	3200 1000	-
182	4	AM28	AF24	3200 2600	-
183	4	AJ26	AP27	3200 2600 2000 1600 1000	-
184	4	AK26	AN27	3200 2600 2000 1600 1000	VREF
185	4	AE23	AM27	3200 1600	-
186	4	AL26	AP26	3200 2000 1000	-
187	4	AN26	AJ25	3200 2000 1000	VREF
188	4	AG24	AP25	3200 2600	-
189	4	AF23	AM26	3200 2600 2000 1600 1000	-
190	4	AJ24	AN25	3200 2600 2000 1600 1000	VREF
191	4	AE22	AM25	2600 1600 1000	-