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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	1176
Number of Logic Elements/Cells	5292
Total RAM Bits	114688
Number of I/O	176
Number of Gates	306393
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv200e-6fg256c

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Table 1: **Supported I/O Standards**

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Board Termination Voltage (V_{TT})
LVTTL	3.3	3.3	N/A	N/A
LVCMOS2	2.5	2.5	N/A	N/A
LVCMOS18	1.8	1.8	N/A	N/A
SSTL3 I & II	3.3	N/A	1.50	1.50
SSTL2 I & II	2.5	N/A	1.25	1.25
GTL	N/A	N/A	0.80	1.20
GTL+	N/A	N/A	1.0	1.50
HSTL I	1.5	N/A	0.75	0.75
HSTL III & IV	1.5	N/A	0.90	1.50
CTT	3.3	N/A	1.50	1.50
AGP-2X	3.3	N/A	1.32	N/A
PCI33_3	3.3	3.3	N/A	N/A
PCI66_3	3.3	3.3	N/A	N/A
BLVDS & LVDS	2.5	N/A	N/A	N/A
LVPECL	3.3	N/A	N/A	N/A

In addition to the CLK and CE control signals, the three flip-flops share a Set/Reset (SR). For each flip-flop, this signal can be independently configured as a synchronous Set, a synchronous Reset, an asynchronous Preset, or an asynchronous Clear.

The output buffer and all of the IOB control signals have independent polarity controls.

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. After configuration, clamping diodes are connected to V_{CCO} with the exception of LVCMOS18, LVCMOS25, GTL, GTL+, LVDS, and LVPECL.

Optional pull-up, pull-down and weak-keeper circuits are attached to each pad. Prior to configuration all outputs not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive, but I/Os can optionally be pulled up.

The activation of pull-up resistors prior to configuration is controlled on a global basis by the configuration mode pins. If the pull-up resistors are not activated, all the pins are in a high-impedance state. Consequently, external pull-up or pull-down resistors must be provided on pins required to be at a well-defined logic level prior to configuration.

All Virtex-E IOBs support IEEE 1149.1-compatible Boundary Scan testing.

Input Path

The Virtex-E IOB input path routes the input signal directly to internal logic and/ or through an optional input flip-flop.

An optional delay element at the D-input of this flip-flop eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the FPGA, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signalling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF}. The need to supply V_{REF} imposes constraints on which standards can be used in close proximity to each other. See **I/O Banking**.

There are optional pull-up and pull-down resistors at each user I/O input for use after configuration. Their value is in the range 50 – 100 kΩ.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output signal can be routed to the buffer directly from the internal logic or through an optional IOB output flip-flop.

The 3-state control of the output can also be routed directly from the internal logic or through a flip-flip that provides synchronous enable and disable.

Each output driver can be individually programmed for a wide range of low-voltage signalling standards. Each output buffer can source up to 24 mA and sink up to 48 mA. Drive strength and slew rate controls minimize bus transients.

In most signalling standards, the output High voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in close proximity to each other. See **I/O Banking**.

An optional weak-keeper circuit is connected to each output. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low to match the input signal. If the pin is connected to a multiple-source signal, the weak keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way eliminates bus chatter.

Since the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate V_{REF} voltage must be provided if the signalling standard requires one. The provision of this voltage must comply with the I/O banking rules.

I/O Banking

Some of the I/O standards described above require V_{CCO} and/or V_{REF} voltages. These voltages are externally supplied and connected to device pins that serve groups of IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

the internal storage elements to begin changing state in response to the logic and the user clock.

The relative timing of these events can be changed. In addition, the GTS, GSR, and GWE events can be made dependent on the DONE pins of multiple devices all going High, forcing the devices to start synchronously. The sequence can also be paused at any stage until lock has been achieved on any or all DLLs.

Readback

The configuration data stored in the Virtex-E configuration memory can be readback for verification. Along with the configuration data it is possible to readback the contents all flip-flops/latches, LUT RAMs, and block RAMs. This capability is used for real-time debugging. For more detailed information, see application note XAPP138 "Virtex FPGA Series Configuration and Readback".

Design Considerations

This section contains more detailed design information on the following features.

- Delay-Locked Loop . . . see page 19
- BlockRAM . . . see page 24
- SelectI/O . . . see page 31

Using DLLs

The Virtex-E FPGA series provides up to eight fully digital dedicated on-chip Delay-Locked Loop (DLL) circuits which provide zero propagation delay, low clock skew between output clock signals distributed throughout the device, and advanced clock domain control. These dedicated DLLs can be used to implement several circuits which improve and simplify system level design.

Introduction

As FPGAs grow in size, quality on-chip clock distribution becomes increasingly important. Clock skew and clock delay impact device performance and the task of managing clock skew and clock delay with conventional clock trees becomes more difficult in large devices. The Virtex-E series of devices resolve this potential problem by providing up to eight fully digital dedicated on-chip DLL circuits, which provide zero propagation delay and low clock skew between output clock signals distributed throughout the device.

Each DLL can drive up to two global clock routing networks within the device. The global clock distribution network minimizes clock skews due to loading differences. By monitoring a sample of the DLL output clock, the DLL can compensate for the delay on the routing network, effectively eliminating the delay from the external input port to the individual clock loads within the device.

In addition to providing zero delay with respect to a user source clock, the DLL can provide multiple phases of the source clock. The DLL can also act as a clock doubler or it can divide the user source clock by up to 16.

Clock multiplication gives the designer a number of design alternatives. For instance, a 50 MHz source clock doubled by the DLL can drive an FPGA design operating at 100 MHz. This technique can simplify board design because the clock path on the board no longer distributes such a high-speed signal. A multiplied clock also provides designers the option of time-domain-multiplexing, using one circuit twice per clock cycle, consuming less area than two copies of the same circuit. Two DLLs in can be connected in series to increase the effective clock multiplication factor to four.

The DLL can also act as a clock mirror. By driving the DLL output off-chip and then back in again, the DLL can be used to deskew a board level clock between multiple devices.

In order to guarantee the system clock establishes prior to the device "waking up," the DLL can delay the completion of the device configuration process until after the DLL achieves lock.

By taking advantage of the DLL to remove on-chip clock delay, the designer can greatly simplify and improve system level design involving high-fanout, high-performance clocks.

Library DLL Symbols

Figure 21 shows the simplified Xilinx library DLL macro symbol, BUFGDLL. This macro delivers a quick and efficient way to provide a system clock with zero propagation delay throughout the device. Figure 22 and Figure 23 show the two library DLL primitives. These symbols provide access to the complete set of DLL features when implementing more complex applications.

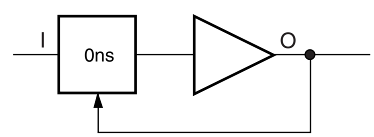

Figure 21: **Simplified DLL Macro Symbol BUFGDLL**

ground. As the DLL delay taps reset to zero, glitches can occur on the DLL clock output pins. Activation of the RST pin can also severely affect the duty cycle of the clock output pins. Furthermore, the DLL output clocks no longer deskew with respect to one another. For these reasons, rarely use the reset pin unless re-configuring the device or changing the input frequency.

2x Clock Output — CLK2X

The output pin CLK2X provides a frequency-doubled clock with an automatic 50/50 duty-cycle correction. Until the CLKDLL has achieved lock, the CLK2X output appears as a 1x version of the input clock with a 25/75 duty cycle. This behavior allows the DLL to lock on the correct edge with respect to source clock. This pin is not available on the CLKDLLHF primitive.

Clock Divide Output — CLKDV

The clock divide output pin CLKDV provides a lower frequency version of the source clock. The CLKDV_DIVIDE property controls CLKDV such that the source clock is divided by N where N is either 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

This feature provides automatic duty cycle correction such that the CLKDV output pin always has a 50/50 duty cycle, with the exception of noninteger divides in HF mode, where the duty cycle is 1/3 for N=1.5 and 2/5 for N=2.5.

1x Clock Outputs — CLK[0|90|180|270]

The 1x clock output pin CLK0 represents a delay-compensated version of the source clock (CLKIN) signal. The CLKDLL primitive provides three phase-shifted versions of the CLK0 signal while CLKDLLHF provides only the 180 phase-shifted version. The relationship between phase shift and the corresponding period shift appears in Table 13.

Table 13: **Relationship of Phase-Shifted Output Clock to Period Shift**

Phase (degrees)	Period Shift (percent)
0	0%
90	25%
180	50%
270	75%

The timing diagrams in Figure 25 illustrate the DLL clock output characteristics.

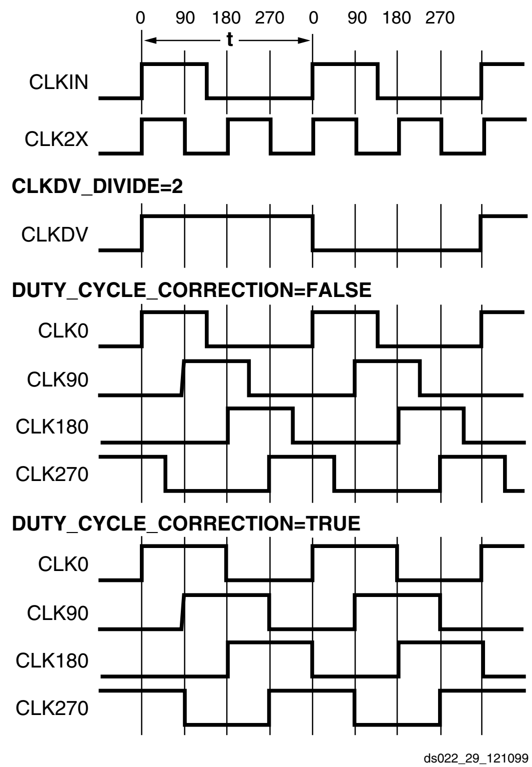

Figure 25: **DLL Output Characteristics**

The DLL provides duty cycle correction on all 1x clock outputs such that all 1x clock outputs by default have a 50/50 duty cycle. The DUTY_CYCLE_CORRECTION property (TRUE by default), controls this feature. In order to deactivate the DLL duty cycle correction, attach the DUTY_CYCLE_CORRECTION=FALSE property to the DLL symbol. When duty cycle correction deactivates, the output clock has the same duty cycle as the source clock.

The DLL clock outputs can drive an OBUF, a BUFG, or they can route directly to destination clock pins. The DLL clock outputs can only drive the BUFGs that reside on the same edge (top or bottom).

Locked Output — LOCKED

To achieve lock, the DLL might need to sample several thousand clock cycles. After the DLL achieves lock, the LOCKED signal activates. The DLL timing parameter section of the data sheet provides estimates for locking times.

To guarantee that the system clock is established prior to the device "waking up," the DLL can delay the completion of the device configuration process until after the DLL locks. The STARTUP_WAIT property activates this feature.

Until the LOCKED signal activates, the DLL output clocks are not valid and can exhibit glitches, spikes, or other spurious movement. In particular the CLK2X output appears as a 1x clock with a 25/75 duty cycle.

indicating that the block SelectRAM+ memory is now disabled. The DO bus retains the last value.

Dual Port Timing

Figure 34 shows a timing diagram for a true dual-port read/write block SelectRAM+ memory. The clock on port A has a longer period than the clock on Port B. The timing parameter T_{BCCS}, (clock-to-clock set-up) is shown on this diagram. The parameter, T_{BCCS} is violated once in the diagram. All other timing parameters are identical to the single port version shown in Figure 33.

T_{BCCS} is only of importance when the address of both ports are the same and at least one port is performing a write operation. When the clock-to-clock set-up parameter is violated for a WRITE-WRITE condition, the contents of the memory at that location are invalid. When the clock-to-clock set-up parameter is violated for a WRITE-READ condition, the contents of the memory are correct, but the read port has invalid data.

At the first rising edge of the CLKA, memory location 0x00 is to be written with the value 0xAAAA and is mirrored on the DOA bus. The last operation of Port B was a read to the same memory location 0x00. The DOB bus of Port B does not change with the new value on Port A, and retains the last read value. A short time later, Port B executes another read to memory location 0x00, and the DOB bus now reflects the new memory value written by Port A.

At the second rising edge of CLKA, memory location 0x7E is written with the value 0x9999 and is mirrored on the DOA bus. Port B then executes a read operation to the same memory location without violating the T_{BCCS} parameter and the DOB reflects the new memory values written by Port A.

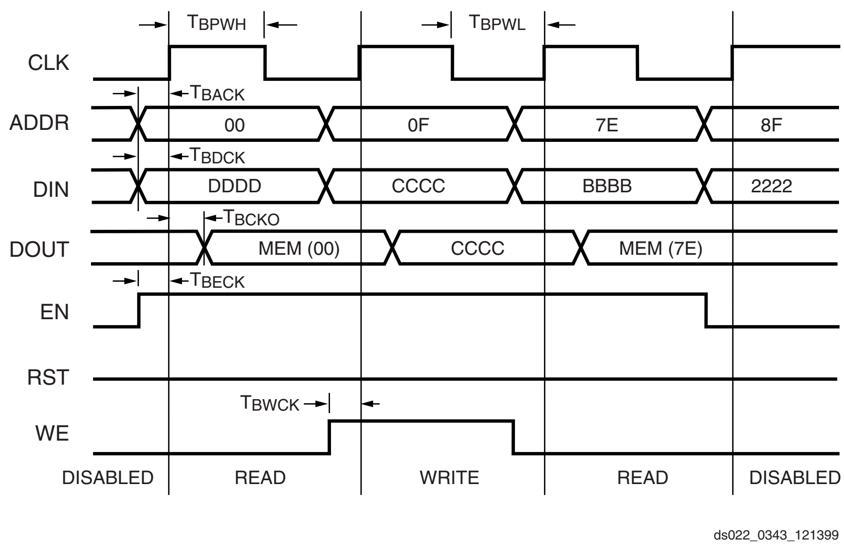

Figure 33: **Timing Diagram for Single Port Block SelectRAM+ Memory**

Verilog Initialization Example

```
module MYMEM (CLK, WE, ADDR, DIN, DOUT);
input CLK, WE;
input [8:0] ADDR;
input [7:0] DIN;
output [7:0] DOUT;

wire logic0, logic1;

//synopsys dc_script_begin
//set_attribute ram0 INIT_00
"0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF" -type string
//set_attribute ram0 INIT_01
"FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210" -type string
//synopsys dc_script_end

assign logic0 = 1'b0;
assign logic1 = 1'b1;

RAMB4_S8 ram0 (.WE(WE), .EN(logic1), .RST(logic0), .CLK(CLK), .ADDR(ADDR), .DI(DIN),
.DO(DOUT));
//synopsys translate_off
defparam ram0.INIT_00 =
256h'0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF;
defparam ram0.INIT_01 =
256h'FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210;
//synopsys translate_on
endmodule
```

Using SelectI/O

The Virtex-E FPGA series includes a highly configurable, high-performance I/O resource, called SelectI/O™ to provide support for a wide variety of I/O standards. The SelectI/O resource is a robust set of features including programmable control of output drive strength, slew rate, and input delay and hold time. Taking advantage of the flexibility and SelectI/O features and the design considerations described in this document can improve and simplify system level design.

Introduction

As FPGAs continue to grow in size and capacity, the larger and more complex systems designed for them demand an increased variety of I/O standards. Furthermore, as system clock speeds continue to increase, the need for high performance I/O becomes more important.

While chip-to-chip delays have an increasingly substantial impact on overall system speed, the task of achieving the desired system performance becomes more difficult with the proliferation of low-voltage I/O standards. SelectI/O, the revolutionary input/output resources of Virtex-E devices, resolve this potential problem by providing a highly configurable, high-performance alternative to the I/O resources of more conventional programmable devices. Virtex-E SelectI/O features combine the flexibility and time-to-market advantages of programmable logic with the high performance previously available only with ASICs and custom ICs.

Each SelectI/O block can support up to 20 I/O standards. Supporting such a variety of I/O standards allows the support of a wide variety of applications, from general purpose standard applications to high-speed low-voltage memory buses.

SelectI/O blocks also provide selectable output drive strengths and programmable slew rates for the LVTTL output buffers, as well as an optional, programmable weak pull-up, weak pull-down, or weak “keeper” circuit ideal for use in external bussing applications.

Each Input/Output Block (IOB) includes three registers, one each for the input, output, and 3-state signals within the IOB. These registers are optionally configurable as either a D-type flip-flop or as a level sensitive latch.

The input buffer has an optional delay element used to guarantee a zero hold time requirement for input signals registered within the IOB.

The Virtex-E SelectI/O features also provide dedicated resources for input reference voltage (V_{REF}) and output source voltage (V_{CCO}), along with a convenient banking system that simplifies board design.

By taking advantage of the built-in features and wide variety of I/O standards supported by the SelectI/O features, system-level design and board design can be greatly simplified and improved.

Fundamentals

Modern bus applications, pioneered by the largest and most influential companies in the digital electronics industry, are commonly introduced with a new I/O standard tailored specifically to the needs of that application. The bus I/O standards provide specifications to other vendors who create products designed to interface with these applications. Each standard often has its own specifications for current, voltage, I/O buffering, and termination techniques.

The ability to provide the flexibility and time-to-market advantages of programmable logic is increasingly dependent on the capability of the programmable logic device to support an ever increasing variety of I/O standards

The SelectI/O resources feature highly configurable input and output buffers which provide support for a wide variety of I/O standards. As shown in Table 18, each buffer type can support a variety of voltage requirements.

Table 18: **Virtex-E Supported I/O Standards**

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Board Termination Voltage (V_{TT})
LVTTL	3.3	3.3	N/A	N/A
LVCMOS2	2.5	2.5	N/A	N/A
LVCMOS18	1.8	1.8	N/A	N/A
SSTL3 I & II	3.3	N/A	1.50	1.50
SSTL2 I & II	2.5	N/A	1.25	1.25
GTL	N/A	N/A	0.80	1.20
GTL+	N/A	N/A	1.0	1.50
HSTL I	1.5	N/A	0.75	0.75
HSTL III & IV	1.5	N/A	0.90	1.50
CTT	3.3	N/A	1.50	1.50
AGP-2X	3.3	N/A	1.32	N/A
PCI33_3	3.3	3.3	N/A	N/A
PCI66_3	3.3	3.3	N/A	N/A
BLVDS & LVDS	2.5	N/A	N/A	N/A
LVPECL	3.3	N/A	N/A	N/A

Overview of Supported I/O Standards

This section provides a brief overview of the I/O standards supported by all Virtex-E devices.

While most I/O standards specify a range of allowed voltages, this document records typical voltage values only. Detailed information on each specification can be found on the Electronic Industry Alliance Jedec website at:

http://www.jedec.org

LVTTL — Low-Voltage TTL

The Low-Voltage TTL, or LVTTL standard is a general purpose EIA/JESDSA standard for 3.3V applications that uses an LVTTL input buffer and a Push-Pull output buffer. This standard requires a 3.3V output source voltage (V_{CCO}), but does not require the use of a reference voltage (V_{REF}) or a termination voltage (V_{TT}).

LVCMOS2 — Low-Voltage CMOS for 2.5 Volts

The Low-Voltage CMOS for 2.5 Volts or lower, or LVCMOS2 standard is an extension of the LVCMOS standard (JESD 8.-5) used for general purpose 2.5V applications. This standard requires a 2.5V output source voltage (V_{CCO}), but does not require the use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}).

LVCMOS18 — 1.8 V Low Voltage CMOS

This standard is an extension of the LVCMOS standard. It is used in general purpose 1.8 V applications. The use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}) is not required.

PCI — Peripheral Component Interface

The Peripheral Component Interface, or PCI standard specifies support for both 33 MHz and 66 MHz PCI bus applications. It uses a LVTTL input buffer and a Push-Pull output buffer. This standard does not require the use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}), however, it does require a 3.3V output source voltage (V_{CCO}).

GTL — Gunning Transceiver Logic Terminated

The Gunning Transceiver Logic, or GTL standard is a high-speed bus standard (JESD8.3) invented by Xerox. Xilinx has implemented the terminated variation for this standard. This standard requires a differential amplifier input buffer and a Open Drain output buffer.

GTL+ — Gunning Transceiver Logic Plus

The Gunning Transceiver Logic Plus, or GTL+ standard is a high-speed bus standard (JESD8.3) first used by the Pentium Pro processor.

HSTL — High-Speed Transceiver Logic

The High-Speed Transceiver Logic, or HSTL standard is a general purpose high-speed, 1.5V bus standard sponsored by IBM (EIA/JESD 8-6). This standard has four variations or classes. SelectI/O devices support Class I, III, and IV. This

Table 21: **Guidelines for Max Number of Simultaneously Switching Outputs per Power/Ground Pair *(Continued)***

Standard	Package		
	BGA, CS, FGA	HQ	PQ, TQ
HSTL Class I	18	13	9
HSTL Class III	9	7	5
HSTL Class IV	5	4	3
SSTL2 Class I	15	11	8
SSTL2 Class II	10	7	5
SSTL3 Class I	11	8	6
SSTL3 Class II	7	5	4
CTT	14	10	7
AGP	9	7	5

Note: This analysis assumes a 35 pF load for each output.

Table 22: **Virtex-E Equivalent Power/Ground Pairs**

Pkg/Part	XCV100E	XCV200E	XCV300E	XCV400E	XCV600E	XCV1000E	XCV1600E	XCV2000E
CS144	12	12						
PQ240	20	20	20	20				
HQ240					20	20		
BG352	20	32	32					
BG432			32	40	40			
BG560				40	40	56	58	60
FG256(1)	20	24	24					
FG456		40	40					
FG676				54	56			
FG680(2)					46	56	56	56
FG860						58	60	64
FG900					56	58		60
FG1156						96	104	120

Notes:
1. Virtex-E devices in FG256 packages have more V_{CCO} than Virtex series devices.
2. FG680 numbers are preliminary.

SSTL3_I

A sample circuit illustrating a valid termination technique for SSTL3_I appears in Figure 49. DC voltage specifications appear in Table 28.

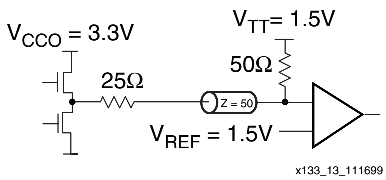

Figure 49: **Terminated SSTL3 Class I**

Table 28: **SSTL3_I Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	**3.0**	**3.3**	**3.6**
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} = V_{REF} + 0.2$	1.5	1.7	3.9(1)
$V_{IL} = V_{REF} – 0.2$	–0.3(2)	1.3	1.5
$V_{OH} = V_{REF} + 0.6$	1.9	-	-
$V_{OL} = V_{REF} – 0.6$	-	-	1.1
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL}at V_{OL} (mA)	8	-	-

Notes:
1. V_{IH} maximum is V_{CCO} + 0.3
2. V_{IL} minimum does not conform to the formula

SSTL3_II

A sample circuit illustrating a valid termination technique for SSTL3_II appears in Figure 50. DC voltage specifications appear in Table 29.

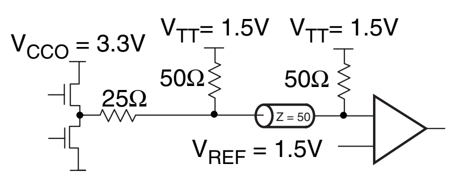

Figure 50: **Terminated SSTL3 Class II**

Table 29: **SSTL3_II Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} = V_{REF} + 0.2$	1.5	1.7	3.9(1)
$V_{IL}= V_{REF} – 0.2$	–0.3(2)	1.3	1.5
$V_{OH} = V_{REF} + 0.8$	2.1	-	-
$V_{OL}= V_{REF} – 0.8$	-	-	0.9
I_{OH} at V_{OH} (mA)	–16	-	-
I_{OL}at V_{OL} (mA)	16	-	-

Notes:
1. V_{IH} maximum is V_{CCO} + 0.3
2. V_{IL} minimum does not conform to the formula

SSTL2_I

A sample circuit illustrating a valid termination technique for SSTL2_I appears in Figure 51. DC voltage specifications appear in Table 30.

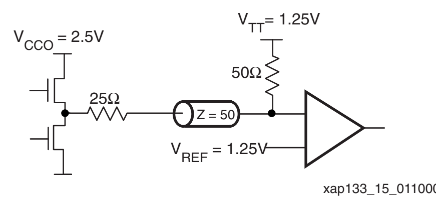

Figure 51: **Terminated SSTL2 Class I**

Table 30: **SSTL2_I Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
$V_{REF} = 0.5 \times V_{CCO}$	1.15	1.25	1.35
$V_{TT} = V_{REF} + N$(1)	1.11	1.25	1.39
$V_{IH} = V_{REF} + 0.18$	1.33	1.43	3.0(2)
$V_{IL} = V_{REF} – 0.18$	–0.3(3)	1.07	1.17
$V_{OH} = V_{REF} + 0.61$	1.76	-	-
$V_{OL}= V_{REF} – 0.61$	-	-	0.74
I_{OH} at V_{OH} (mA)	–7.6	-	-
I_{OL}at V_{OL} (mA)	7.6	-	-

Notes:
1. N must be greater than or equal to -0.04 and less than or equal to 0.04.
2. V_{IH} maximum is V_{CCO} + 0.3.
3. V_{IL} minimum does not conform to the formula.

DC Characteristics

Absolute Maximum Ratings

Symbol	Description[(1)]			Units
V_{CCINT}	Internal Supply voltage relative to GND		–0.5 to 2.0	V
V_{CCO}	Supply voltage relative to GND		–0.5 to 4.0	V
V_{REF}	Input Reference Voltage		–0.5 to 4.0	V
V_{IN} [(3)]	Input voltage relative to GND		–0.5 to V_{CCO} +0.5	V
V_{TS}	Voltage applied to 3-state output		–0.5 to 4.0	V
V_{CC}	Longest Supply Voltage Rise Time from 0 V - 1.71 V		50	ms
T_{STG}	Storage temperature (ambient)		–65 to +150	°C
T_J	Junction temperature [(2)]	Plastic packages	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time can affect device reliability.
2. For soldering guidelines and thermal considerations, see the device packaging information on www.xilinx.com.
3. Inputs configured as PCI are fully PCI compliant. This statement takes precedence over any specification that would imply that the device is not PCI compliant.

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CCINT}	Internal Supply voltage relative to GND, T_J = 0 °C to +85 °C	Commercial	1.8 – 5%	1.8 + 5%	V
	Internal Supply voltage relative to GND, T_J = –40 °C to +100 °C	Industrial	1.8 – 5%	1.8 + 5%	V
V_{CCO}	Supply voltage relative to GND, T_J = 0 °C to +85 °C	Commercial	1.2	3.6	V
	Supply voltage relative to GND, T_J = –40 °C to +100 °C	Industrial	1.2	3.6	V
T_{IN}	Input signal transition time			250	ns

DLL Timing Parameters

All devices are 100 percent functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

Description	Symbol	F_{CLKIN}	Speed Grade						Units
			-8		-7		-6		
			Min	Max	Min	Max	Min	Max	
Input Clock Frequency (CLKDLLHF)	FCLKINHF		60	350	60	320	60	275	MHz
Input Clock Frequency (CLKDLL)	FCLKINLF		25	160	25	160	25	135	MHz
Input Clock Low/High Pulse Width	T_{DLLPW}	≥25 MHz	5.0		5.0		5.0		ns
		≥50 MHz	3.0		3.0		3.0		ns
		≥100 MHz	2.4		2.4		2.4		ns
		≥150 MHz	2.0		2.0		2.0		ns
		≥200 MHz	1.8		1.8		1.8		ns
		≥250 MHz	1.5		1.5		1.5		ns
		≥300 MHz	1.3		1.3		NA		ns

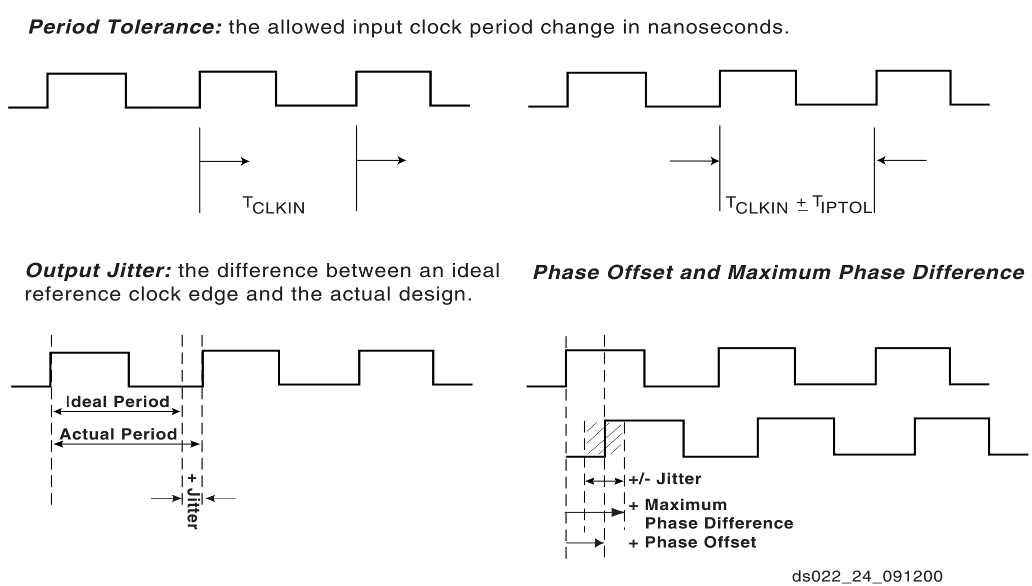

Figure 4: **DLL Timing Waveforms**

Pinout Differences Between Virtex and Virtex-E Families

The same device in the same package for the Virtex-E and Virtex families are pin-compatible with some minor exceptions, listed in Table 1.

XCV200E Device, FG456 Package

The Virtex-E XCV200E has two I/O pins swapped with the Virtex XCV200 to accommodate differential clock pairing.

XCV400E Device, FG676 Package

The Virtex-E XCV400E has two I/O pins swapped with the Virtex XCV400 to accommodate differential clock pairing.

All Devices, PQ240 and HQ240 Packages

The Virtex devices in PQ240 and HQ240 packages do not have V_{CCO} banking, but Virtex-E devices do. To achieve this, eight Virtex I/O pins (P232, P207, P176, P146, P116, P85, P55, and P25) are now VCCO pins in the Virtex-E family. This change also requires one Virtex I/O or VREF pin to be swapped with a standard I/O pin.

Additionally, accommodating differential clock input pairs in Virtex-E caused some IO_V_{REF} differences in the XCV400E and XCV600E devices only. Virtex IO_V_{REF} pins P215 and P87 are Virtex-E IO_V_{REF} pins P216 and P86, respectively. Virtex-E pins P215 and P87 are IO_DLL.

Table 1: **Pinout Differences Summary**

Part	Package	Pins	Virtex	Virtex-E
XCV200	FG456	E11, U11	I/O	No Connect
		B11, AA11	No Connect	IO_LVDS_DLL
XCV400	FG676	D13, Y13	I/O	No Connect
		B13, AF13	No Connect	IO_LVDS_DLL
XCV400/600	PQ240/HQ240	P215, P87	IO_V_{REF}	IO_LVDS_DLL
		P216, P86	I/O	IO_V_{REF}
All	PQ240/HQ240	P232, P207, P176, P146, P116, P85, P55, and P25	I/O	V_{CCO}
		P231	I/O	IO_V_{REF}

Table 6: **PQ240 — XCV50E, XCV100E, XCV200E, XCV300E, XCV400E**

Pin #	Pin Description	Bank
P173	IO_L16N_Y	2
P171	IO_VREF_L17P_Y	2
P170	IO_L17N_Y	2
P169	IO	2
P168[1]	IO_VREF_L18P_Y	2
P167	IO_D1_L18N_Y	2
P163	IO_D2_L19P_YY	2
P162	IO_L19N_YY	2
P161	IO	2
P160	IO_L20P_Y	2
P159	IO_L20N_Y	2
P157	IO_VREF_L21P_Y	2
P156	IO_D3_L21N_Y	2
P155	IO_L22P_Y	2
P154[3]	IO_VREF_L22N_Y	2
P153	IO_L23P_YY	2
P152	IO_L23N_YY	2
P149	IO	3
P147[3]	IO_VREF	3
P145	IO_D4_L24P_Y	3
P144	IO_VREF_L24N_Y	3
P142	IO_L25P_Y	3
P141	IO_L25N_Y	3
P140	IO	3
P139	IO_L26P_YY	3
P138	IO_D5_L26N_YY	3
P134	IO_D6_L27P_Y	3
P133[1]	IO_VREF_L27N_Y	3
P132	IO	3
P131	IO_L28P_Y	3
P130	IO_VREF_L28N_Y	3
P128	IO_L29P_Y	3
P127	IO_L29N_Y	3
P126[2]	IO_VREF_L30P_Y	3

Table 6: **PQ240 — XCV50E, XCV100E, XCV200E, XCV300E, XCV400E**

Pin #	Pin Description	Bank
P125	IO_L30N_Y	3
P124	IO_D7_L31P_YY	3
P123	IO_INIT_L31N_YY	3
P118	IO_L32P_YY	4
P117	IO_L32N_YY	4
P115[2]	IO_VREF	4
P114	IO_L33P_YY	4
P113	IO_L33N_YY	4
P111	IO_VREF_L34P_YY	4
P110	IO_L34N_YY	4
P109	IO	4
P108[1]	IO_VREF_L35P_YY	4
P107	IO_L35N_YY	4
P103	IO_L36P_YY	4
P102	IO_L36N_YY	4
P101	IO	4
P100	IO_L37P_Y	4
P99	IO_L37N_Y	4
P97	IO_VREF_L38P_Y	4
P96	IO_L38N_Y	4
P95	IO_L39P_Y	4
P94[3]	IO_VREF_L39N_Y	4
P93	IO_LVDS_DLL_L40P	4
P92	GCK0	4
P89	GCK1	5
P87	IO_LVDS_DLL_L40N	5
P86[3]	IO_VREF	5
P84	IO_VREF_L41P_Y	5
P82	IO_L41N_Y	5
P81	IO	5
P80	IO	5
P79	IO_L42P_YY	5
P78	IO_L42N_YY	5

Table 10: **BG352 — XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
2	IO_D3_L30N _Y	M3
2	IO_L31P	M2
2	IO_L31N	M1
2	IO	N3[1]
2	IO_L32P_YY	N4
2	IO_L32N_YY	N2
3	IO	P1
3	IO	P3[1]
3	IO_L33P	R1
3	IO_L33N	R2
3	IO_D4_L34P _Y	R3
3	IO_VREF_3_L34N _Y	R4
3	IO_L35P_YY	T2
3	IO_L35N_YY	U2
3	IO	T3[1]
3	IO_L36P	T4
3	IO_L36N	V1
3	IO	V2[1]
3	IO_L37P_YY	U3
3	IO_D5_L37N_YY	U4
3	IO_D6_L38P _Y	V3
3	IO_VREF_3_L38N _Y	V4
3	IO_L39P _Y	Y1
3	IO_L39N _Y	Y2
3	IO	W3
3	IO	W4[1]
3	IO	AA1[1]
3	IO_L40P_Y	AA2
3	IO_VREF_3_L40N_Y	Y3
3	IO_L41P_YY	AC1
3	IO_L41N_YY	AB2
3	IO	AA3[1]
3	IO_L42P_YY	AA4

Table 10: **BG352 — XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
3	IO_VREF_3_L42N_YY	AC2[2]
3	IO	AB3
3	IO	AD1[1]
3	IO	AB4[1]
3	IO_D7_L43P_YY	AC3
3	IO_INIT_L43N_YY	AD2
4	IO_L44P_YY	AC5
4	IO_L44N_YY	AD4
4	IO	AE3[1]
4	IO	AD5[1]
4	IO	AC6
4	IO_VREF_4_L45P_YY	AE4[2]
4	IO_L45N_YY	AF3
4	IO	AF4[1]
4	IO_L46P_YY	AC7
4	IO_L46N_YY	AD6
4	IO_VREF_4_L47P_YY	AE5
4	IO_L47N_YY	AE6
4	IO	AD7[1]
4	IO	AE7[1]
4	IO_L48P	AF6
4	IO_L48N	AC9
4	IO	AD8
4	IO_VREF_4_L49P_YY	AE8
4	IO_L49N_YY	AF7
4	IO_L50P_YY	AD9
4	IO_L50N_YY	AE9
4	IO	AD10[1]
4	IO_L51P	AF9
4	IO_L51N	AC11
4	IO	AE10[1]
4	IO_L52P_Y	AD11
4	IO_L52N_Y	AE11

Table 16: **FG256 Package — XCV50E, XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
NA	GND	K11
NA	GND	K10
NA	GND	K9
NA	GND	K8
NA	GND	K7
NA	GND	K6
NA	GND	J10
NA	GND	J9
NA	GND	J8
NA	GND	J7
NA	GND	H10
NA	GND	H9
NA	GND	H8
NA	GND	H7
NA	GND	G11
NA	GND	G10
NA	GND	G9
NA	GND	G8
NA	GND	G7
NA	GND	G6
NA	GND	F11
NA	GND	F10
NA	GND	F7
NA	GND	F6
NA	GND	B15
NA	GND	B2
NA	GND	A16
NA	GND	A1

Notes:
1. V_{REF} or I/O option only in the XCV100E, 200E, 300E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV200E, 300E; otherwise, I/O option only.

FG256 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 17: **FG256 Differential Pin Pair Summary XCV50E, XCV100E, XCV200E, XCV300E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	N8	N9	NA	IO_DLL_L52P
1	5	R8	T8	NA	IO_DLL_L52N
2	1	C9	A8	NA	IO_DLL_L8P
3	0	B8	A7	NA	IO_DLL_L8N
IO LVDS Total Pairs: 83, Asynchronous Outputs: 35					
0	0	A3	C5	7	VREF
1	0	E6	D5	√	-
2	0	A4	B4	√	VREF
3	0	B5	D6	2	-
4	0	A5	C6	√	VREF
5	0	C7	B6	√	-
6	0	C8	D7	1	-
7	0	A6	B7	1	VREF
8	1	A8	A7	NA	IO_LVDS_DLL
9	1	A9	D9	2	-
10	1	B9	E10	1	VREF
11	1	D10	A10	1	-
12	1	A11	C10	√	-
13	1	E11	B11	√	VREF
14	1	D11	A12	2	-
15	1	C11	A13	√	VREF
16	1	D12	B12	√	-
17	1	C12	A14	7	VREF
18	1	B13	C13	√	CS

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
3	IO_L50N_YY	P19
3	IO_L51P_YY	P18
3	IO_D5_L51N_YY	R21
3	IO_D6_L52P_Y	T22
3	IO_VREF_L52N_Y	R19
3	IO_L53P_Y	U22
3	IO_L53N_Y	R18
3	IO_L54P_YY	T21
3	IO_L54N_YY	V22
3	IO_L55P_YY	T20
3	IO_VREF_L55N_YY	U21
3	IO_L56P_YY	W22
3	IO_L56N_YY	T18
3	IO_L57P_YY	U19
3	IO_VREF_L57N_YY	U20
3	IO_L58P_YY	W21
3	IO_L58N_YY	AA22
3	IO_D7_L59P_YY	Y21
3	IO_INIT_L59N_YY	V19
3	IO	M22
4	GCK0	W12
4	IO	W14
4	IO	Y13
4	IO	Y17
4	IO	AA16[1]
4	IO	AA19
4	IO	AB12[1]
4	IO	AB17
4	IO	AB21[1]
4	IO_L60P_YY	W18
4	IO_L60N_YY	AA20
4	IO_L61P	Y18
4	IO_L61N	V17
4	IO_VREF_L62P_YY	AB20
4	IO_L62N_YY	W17
4	IO_L63P	AA18

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
4	IO_L63N	V16
4	IO_VREF_L64P_YY	AB19
4	IO_L64N_YY	AB18
4	IO_L65P_Y	W16
4	IO_L65N_Y	AA17
4	IO_L66P_Y	Y16
4	IO_L66N_Y	V15
4	IO_VREF_L67P_YY	AB16
4	IO_L67N_YY	Y15
4	IO_L68P_YY	AA15
4	IO_L68N_YY	AB15
4	IO_L69P_Y	W15
4	IO_L69N_Y	Y14
4	IO_L70P_Y	V14
4	IO_L70N_Y	AA14
4	IO_L71P	AB14
4	IO_L71N	V13
4	IO_VREF_L72P_YY	AA13
4	IO_L72N_YY	AB13
4	IO_L73P_Y	W13
4	IO_L73N_Y	AA12
4	IO_L74P_Y	Y12
4	IO_L74N_Y	V12
4	IO_LVDS_DLL_L75P	U12
5	IO	U11[1]
5	IO	V8
5	IO	W5
5	IO	AA3[1]
5	IO	AA9
5	IO	AA10
5	IO	AB4
5	IO	AB7[1]
5	IO	AB8
5	GCK1	Y11
5	IO_LVDS_DLL_L75N	AA11
5	IO_L76P_Y	AB11

Table 21: **FG676 Differential Pin Pair Summary XCV400E, XCV600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
52	2	G24	H22	√	-
53	2	J21	G25	2	-
54	2	G26	J22	1	VREF
55	2	H24	J23	√	-
56	2	J24	K20	√	VREF
57	2	K22	K21	√	D2
58	2	H25	K23	√	-
59	2	L20	J26	2	-
60	2	K25	L22	1	-
61	2	L21	L23	1	-
62	2	M20	L24	1	-
63	2	M23	M22	√	D3
64	2	L26	M21	√	-
65	2	N19	M24	2	-
66	2	M26	N20	1	VREF
67	2	N24	N21	√	-
68	2	N23	N22	√	-
69	3	P21	P23	√	-
70	3	P22	R25	1	VREF
71	3	P19	P20	2	-
72	3	R21	R22	√	-
73	3	R24	R23	√	VREF
74	3	T24	R20	1	-
75	3	T22	U24	1	-
76	3	T23	U25	1	-
77	3	T21	U20	2	-
78	3	U22	V26	√	-
79	3	T20	U23	√	D5
80	3	V24	U21	√	VREF
81	3	V23	W24	√	-
82	3	V22	W26	1	VREF
83	3	Y25	V21	2	-
84	3	V20	AA26	√	-
85	3	Y24	W23	√	VREF

Table 21: **FG676 Differential Pin Pair Summary XCV400E, XCV600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
86	3	AA24	Y23	1	-
87	3	AB26	W21	2	-
88	3	Y22	W22	1	VREF
89	3	AA23	AB24	2	-
90	3	W20	AC24	√	-
91	3	AB23	Y21	√	INIT
92	4	AC22	AD26	√	-
93	4	AD23	AA20	1	-
94	4	Y19	AC21	√	-
95	4	AD22	AB20	√	VREF
96	4	AE22	Y18	NA	-
97	4	AF22	AA19	NA	-
98	4	AD21	AB19	√	VREF
99	4	AC20	AA18	√	-
100	4	AC19	AD20	1	-
101	4	AF20	AB18	1	VREF
102	4	AD19	Y17	NA	-
103	4	AE19	AD18	NA	VREF
104	4	AF19	AA17	√	-
105	4	AC17	AB17	1	-
106	4	Y16	AE17	√	-
107	4	AF17	AA16	√	-
108	4	AD17	AB16	NA	-
109	4	AC16	AD16	√	-
110	4	AC15	Y15	√	VREF
111	4	AD15	AA15	√	-
112	4	W14	AB15	1	-
113	4	AF15	Y14	1	VREF
114	4	AD14	AB14	NA	-
115	5	AC14	AF13	NA	IO_LVDS_DLL
116	5	AA13	AF12	1	VREF
117	5	AC13	W13	1	-
118	5	AA12	AD12	√	-
119	5	AC12	AB12	√	VREF

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
4	IO_L147N_YY	AW7
4	IO_L148P_Y	AY7
4	IO_L148N_Y	BB8
4	IO_L149P_Y	BA9
4	IO_L149N_Y	AV8
4	IO_L150P_YY	AW8
4	IO_L150N_YY	BA10
4	IO_VREF_L151P_YY	BB10
4	IO_L151N_YY	AY8
4	IO_L152P_Y	AV9
4	IO_L152N_Y	BA11
4	IO_VREF_L153P_Y	BB11[2]
4	IO_L153N_Y	AW9
4	IO_L154P_YY	AY9
4	IO_L154N_YY	BA12
4	IO_VREF_L155P_YY	BB12
4	IO_L155N_YY	AV10
4	IO_L156P_Y	BA13
4	IO_L156N_Y	AW10
4	IO_L157P_Y	BB13
4	IO_L157N_Y	AY10
4	IO_VREF_L158P_YY	AV11
4	IO_L158N_YY	BA14
4	IO_L159P_YY	AW11
4	IO_L159N_YY	BB14
4	IO_L160P_Y	AV12
4	IO_L160N_Y	BA15
4	IO_L161P_Y	AW12
4	IO_L161N_Y	AY15
4	IO_L162P_Y	AW13
4	IO_L162N_Y	BB15
4	IO_L163P_Y	AV14
4	IO_L163N_Y	BA16
4	IO_L164P_YY	AW14
4	IO_L164N_YY	AY16
4	IO_VREF_L165P_YY	BB16
4	IO_L165N_YY	AV15

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
4	IO_L166P_Y	AY17
4	IO_L166N_Y	AW15
4	IO_L167P_Y	BB17
4	IO_L167N_Y	AU16
4	IO_L168P_YY	AV16
4	IO_L168N_YY	AY18
4	IO_VREF_L169P_YY	AW16
4	IO_L169N_YY	BA18
4	IO_L170P_Y	BB19
4	IO_L170N_Y	AW17
4	IO_L171P_Y	AY19
4	IO_L171N_Y	AV18
4	IO_L172P_YY	AW18
4	IO_L172N_YY	BB20
4	IO_VREF_L173P_YY	AY20
4	IO_L173N_YY	AV19
4	IO_L174P_Y	BB21
4	IO_L174N_Y	AW19
4	IO_VREF_L175P_Y	AY21[1]
4	IO_L175N_Y	AV20
4	IO_LVDS_DLL_L176P	AW20
5	GCK1	AY22
5	IO	AV24
5	IO	AV34
5	IO	AW27
5	IO	AW36
5	IO	AY23
5	IO	AY31
5	IO	AY33
5	IO	BA26
5	IO	BA29
5	IO	BA33
5	IO	BB25
5	IO_LVDS_DLL_L176N	AW21
5	IO_L177P_Y	BB22
5	IO_VREF_L177N_Y	AW22[1]

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
7	IO	E3
7	IO	F1[4]
7	IO	G1[5]
7	IO	G4[5]
7	IO	H3[5]
7	IO	J1[4]
7	IO	J3[4]
7	IO	J4[4]
7	IO	J6[4]
7	IO	L10[4]
7	IO	N2[4]
7	IO	N8[4]
7	IO	N10[4]
7	IO	P3[5]
7	IO	P9[4]
7	IO	R1[5]
7	IO	T3[4]
7	IO_L247P	R10
7	IO_L248N_YY	R5[3]
7	IO_L248P_YY	R6[4]
7	IO_L249N_YY	R8
7	IO_VREF_L249P_YY	R4[2]
7	IO_L250N_YY	R7
7	IO_L250P_YY	R3
7	IO_L251N_YY	P10
7	IO_VREF_L251P_YY	P6
7	IO_L252N_YY	P5
7	IO_L252P_YY	P2
7	IO_L253N	P7
7	IO_L253P	P4
7	IO_L254N_YY	N4
7	IO_L254P_YY	R2
7	IO_L255N_YY	N7
7	IO_VREF_L255P_YY	P1
7	IO_L256N	M6

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
7	IO_L256P	N6
7	IO_L257N_YY	N5
7	IO_L257P_YY	N1
7	IO_L258N_YY	M4
7	IO_L258P_YY	M5
7	IO_L259N	M2
7	IO_VREF_L259P	M1[1]
7	IO_L260N_YY	L4
7	IO_L260P_YY	L2
7	IO_L261N_Y	M7[4]
7	IO_L261P_Y	L5[4]
7	IO_L262N_YY	L1
7	IO_L262P_YY	M8
7	IO_L263N	K2
7	IO_L263P	M9
7	IO_L264N	L3[4]
7	IO_L264P	M10[4]
7	IO_L265N_YY	K5
7	IO_L265P_YY	K1
7	IO_L266N_YY	L6
7	IO_VREF_L266P_YY	K3
7	IO_L267N_YY	L7
7	IO_L267P_YY	K4
7	IO_L268N_YY	L8
7	IO_L268P_YY	J5
7	IO_L269N_YY	K6
7	IO_VREF_L269P_YY	H4
7	IO_L270N_YY	H1
7	IO_L270P_YY	K7
7	IO_L271N	J7
7	IO_L271P	J2
7	IO_L272N_YY	H5
7	IO_L272P_YY	G2
7	IO_L273N_YY	L9
7	IO_VREF_L273P_YY	G5
7	IO_L274N	F3
7	IO_L274P	K8

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
3	IO_L153P_YY	AD31
3	IO_VREF_L153N_YY	AF33
3	IO_L154P_Y	AC28
3	IO_L154N_Y	AF31
3	IO_L155P_Y	AC27[5]
3	IO_L155N_Y	AF32[4]
3	IO_L156P_Y	AE29
3	IO_VREF_L156N_Y	AD28[2]
3	IO_L157P_YY	AD30
3	IO_L157N_YY	AG32
3	IO_L158P_YY	AC26[5]
3	IO_L158N_YY	AH33[4]
3	IO_L159P_YY	AD26
3	IO_VREF_L159N_YY	AF30
3	IO_L160P_Y	AC25
3	IO_L160N_Y	AH32
3	IO_L161P_Y	AE28[5]
3	IO_L161N_Y	AL34[4]
3	IO_L162P_Y	AG30
3	IO_L162N_Y	AD27
3	IO_L163P_YY	AF29
3	IO_L163N_YY	AK34
3	IO_L164P_YY	AD25[5]
3	IO_L164N_YY	AE27[4]
3	IO_L165P_Y	AJ33
3	IO_VREF_L165N_Y	AH31
3	IO_L166P_Y	AE26
3	IO_L166N_Y	AL33
3	IO_L167P	AF28
3	IO_L167N	AL32
3	IO_L168P_Y	AJ31
3	IO_VREF_L168N_Y	AF27
3	IO_L169P_Y	AG29
3	IO_L169N_Y	AJ32

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
3	IO_L170P_Y	AK33
3	IO_L170N_Y	AH30
3	IO_D7_L171P_YY	AK32
3	IO_INIT_L171N_YY	AK31
3	IO	V34
4	GCK0	AH18
4	IO	AE21[3]
4	IO	AG18
4	IO	AG23
4	IO	AH24[3]
4	IO	AH25[3]
4	IO	AJ28[3]
4	IO	AK18[3]
4	IO	AK19[3]
4	IO	AL25
4	IO	AL27[3]
4	IO	AL30[3]
4	IO	AN18
4	IO	AN22[3]
4	IO	AN24[3]
4	IO_L172P_YY	AP31
4	IO_L172N_YY	AK29
4	IO_L173P_Y	AP30
4	IO_L173N_Y	AN31
4	IO_L174P_Y	AH27
4	IO_L174N_Y	AN30
4	IO_VREF_L175P_Y	AM30
4	IO_L175N_Y	AK28
4	IO_L176P_Y	AG26
4	IO_L176N_Y	AN29
4	IO_L177P_YY	AF25
4	IO_L177N_YY	AM29
4	IO_VREF_L178P_YY	AL29

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
NA	VCCINT	N22
NA	VCCINT	P13
NA	VCCINT	P22
NA	VCCINT	R13
NA	VCCINT	R22
NA	VCCINT	T13
NA	VCCINT	T22
NA	VCCINT	U10
NA	VCCINT	U25
NA	VCCINT	V10
NA	VCCINT	V25
NA	VCCINT	W13
NA	VCCINT	W22
NA	VCCINT	Y13
NA	VCCINT	Y22
NA	VCCINT	AA13
NA	VCCINT	AA22
NA	VCCINT	AB13
NA	VCCINT	AB14
NA	VCCINT	AB15
NA	VCCINT	AB16
NA	VCCINT	AB19
NA	VCCINT	AB20
NA	VCCINT	AB21
NA	VCCINT	AB22
NA	VCCINT	AC12
NA	VCCINT	AC23
NA	VCCINT	AD24
NA	VCCINT	AD11
NA	VCCINT	AE10
NA	VCCINT	AE17
NA	VCCINT	AE18
NA	VCCINT	AE25

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
NA	VCCO_0	M17
NA	VCCO_0	L17
NA	VCCO_0	L16
NA	VCCO_0	E10
NA	VCCO_0	C14
NA	VCCO_0	A6
NA	VCCO_0	M13
NA	VCCO_0	M14
NA	VCCO_0	M15
NA	VCCO_0	M16
NA	VCCO_0	L12
NA	VCCO_0	L13
NA	VCCO_0	L14
NA	VCCO_0	L15
NA	VCCO_1	M18
NA	VCCO_1	L18
NA	VCCO_1	L23
NA	VCCO_1	E25
NA	VCCO_1	C21
NA	VCCO_1	A29
NA	VCCO_1	M19
NA	VCCO_1	M20
NA	VCCO_1	M21
NA	VCCO_1	M22
NA	VCCO_1	L19
NA	VCCO_1	L20
NA	VCCO_1	L21
NA	VCCO_1	L22
NA	VCCO_2	U24
NA	VCCO_2	U23
NA	VCCO_2	N24
NA	VCCO_2	M24
NA	VCCO_2	K30
NA	VCCO_2	F34