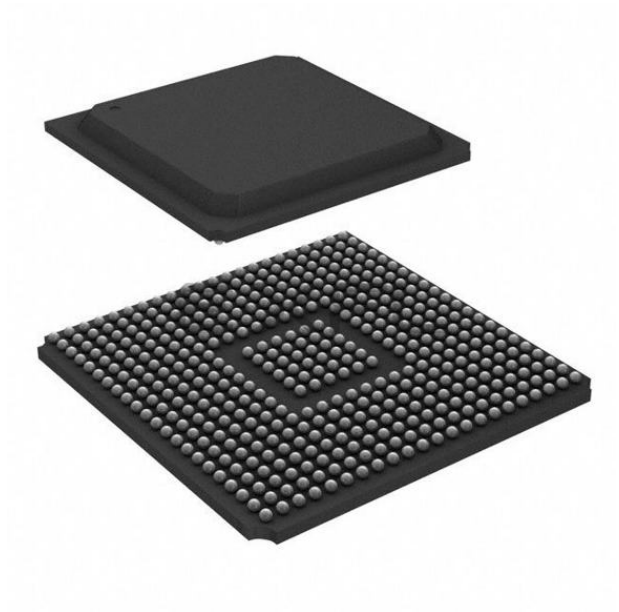

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1176
Number of Logic Elements/Cells	5292
Total RAM Bits	114688
Number of I/O	284
Number of Gates	306393
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv200e-6fg456i

Useful Application Examples

The Virtex-E DLL can be used in a variety of creative and useful applications. The following examples show some of the more common applications. The Verilog and VHDL example files are available at:

ftp://ftp.xilinx.com/pub/applications/xapp/xapp132.zip

Standard Usage

The circuit shown in Figure 27 resembles the BUFGDLL macro implemented to provide access to the RST and LOCKED pins of the CLKDLL.

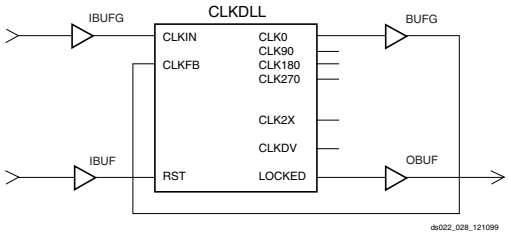

Figure 27: **Standard DLL Implementation**

Board Level Deskew of Multiple Non-Virtex-E Devices

The circuit shown in Figure 28 can be used to deskew a system clock between a Virtex-E chip and other non-Virtex-E chips on the same board. This application is commonly used when the Virtex-E device is used in conjunction with other standard products such as SRAM or DRAM devices. While designing the board level route, ensure that the return net delay to the source equals the delay to the other chips involved.

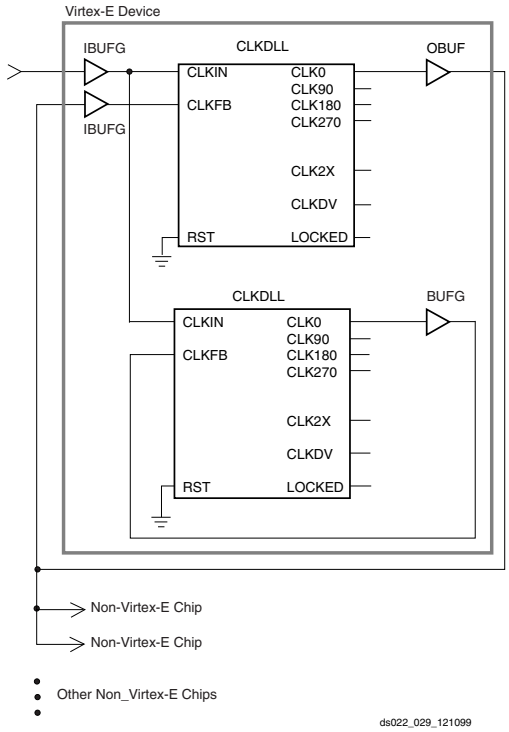

Figure 28: **DLL Deskew of Board Level Clock**

Board-level deskew is not required for low-fanout clock networks. It is recommended for systems that have fanout limitations on the clock network, or if the clock distribution chip cannot handle the load.

Do not use the DLL output clock signals until after activation of the LOCKED signal. Prior to the activation of the LOCKED signal, the DLL output clocks are not valid and can exhibit glitches, spikes, or other spurious movement.

The dll_mirror_1 files in the **xapp132.zip** file show the VHDL and Verilog implementation of this circuit.

Deskew of Clock and Its 2x Multiple

The circuit shown in Figure 29 implements a 2x clock multiplier and also uses the CLK0 clock output with a zero ns skew between registers on the same chip. Alternatively, a clock divider circuit can be implemented using similar connections.

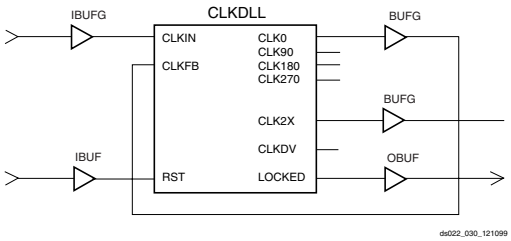

Figure 29: **DLL Deskew of Clock and 2x Multiple**

The voltage reference signal is “banked” within the Virtex-E device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 38 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

IBUF placement restrictions require that any differential amplifier input signals within a bank be of the same standard. How to specify a specific location for the IBUF via the LOC property is described below. Table 19 summarizes the Virtex-E input standards compatibility requirements.

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element by default activates to ensure a zero hold-time requirement. The NODELAY=TRUE property overrides this default.

When the IBUF does not drive a flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

Table 19: **Xilinx Input Standards Compatibility Requirements**

Rule 1	Standards with the same input V_{CCO}, output V_{CCO}, and V_{REF} can be placed within the same bank.

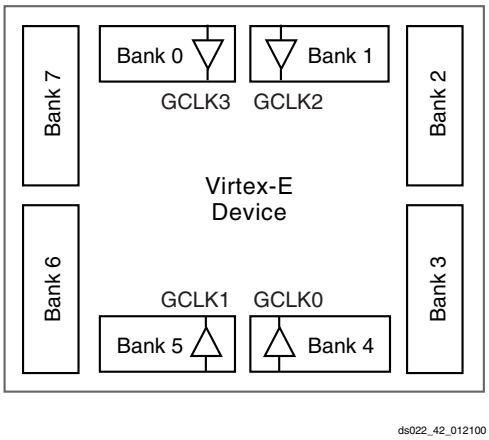

Figure 38: **Virtex-E I/O Banks**

IBUFG

Signals used as high fanout clock inputs to the Virtex-E device should drive a global clock input buffer (IBUFG) via an external input port in order to take advantage of one of the four dedicated global clock distribution networks. The output of the IBUFG should only drive a CLKDLL, CLKDLLHF, or BUFG symbol. The generic Virtex-E IBUFG symbol appears in Figure 39.

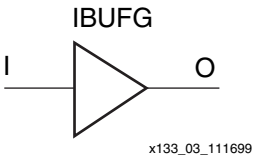

Figure 39: **Virtex-E Global Clock Input Buffer (IBUFG) Symbol**

The extension to the base name determines which I/O standard is used by the IBUFG. With no extension specified for the generic IBUFG symbol, the assumed standard is LVTTL.

The following list details variations of the IBUFG symbol.

- IBUFG
- IBUFG_LVCMOS2
- IBUFG_PCI33_3
- IBUFG_PCI66_3
- IBUFG_GTL
- IBUFG_GTLP
- IBUFG_HSTL_I
- IBUFG_HSTL_III
- IBUFG_HSTL_IV
- IBUFG_SSTL3_I
- IBUFG_SSTL3_II
- IBUFG_SSTL2_I
- IBUFG_SSTL2_II
- IBUFG_CTT
- IBUFG_AGP
- IBUFG_LVCMOS18
- IBUFG_LVDS
- IBUFG_LVPECL

When the IBUFG symbol supports an I/O standard that requires a differential amplifier input, the IBUFG automatically configures as a differential amplifier input buffer. The low-voltage I/O standards with a differential amplifier input require an external reference voltage input V_{REF}.

The voltage reference signal is “banked” within the Virtex-E device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 38 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

IBUFG placement restrictions require any differential amplifier input signals within a bank be of the same standard. The LOC property can specify a location for the IBUFG.

As an added convenience, the BUFGP can be used to instantiate a high fanout clock input. The BUFGP symbol

Input termination techniques include the following.

- None
- Parallel (Shunt)

These termination techniques can be applied in any combination. A generic example of each combination of termination methods appears in Figure 43.

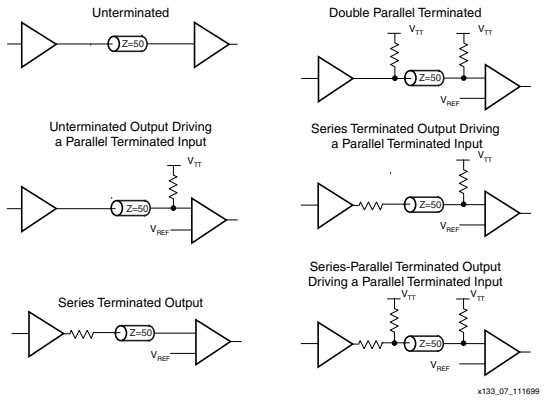

Figure 43: **Overview of Standard Input and Output Termination Methods**

Simultaneous Switching Guidelines

Ground bounce can occur with high-speed digital ICs when multiple outputs change states simultaneously, causing undesired transient behavior on an output, or in the internal logic. This problem is also referred to as the Simultaneous Switching Output (SSO) problem.

Ground bounce is primarily due to current changes in the combined inductance of ground pins, bond wires, and ground metallization. The IC internal ground level deviates from the external system ground level for a short duration (a few nanoseconds) after multiple outputs change state simultaneously.

Ground bounce affects stable Low outputs and all inputs because they interpret the incoming signal by comparing it to the internal ground. If the ground bounce amplitude exceeds the actual instantaneous noise margin, then a non-changing input can be interpreted as a short pulse with a polarity opposite to the ground bounce.

Table 21 provides guidelines for the maximum number of simultaneously switching outputs allowed per output power/ground pair to avoid the effects of ground bounce. See Table 22 for the number of effective output power/ground pairs for each Virtex-E device and package combination.

Table 21: **Guidelines for Max Number of Simultaneously Switching Outputs per Power/Ground Pair**

Standard	Package		
	BGA, CS, FGA	HQ	PQ, TQ
LVTTL Slow Slew Rate, 2 mA drive	68	49	36
LVTTL Slow Slew Rate, 4 mA drive	41	31	20
LVTTL Slow Slew Rate, 6 mA drive	29	22	15
LVTTL Slow Slew Rate, 8 mA drive	22	17	12
LVTTL Slow Slew Rate, 12 mA drive	17	12	9
LVTTL Slow Slew Rate, 16 mA drive	14	10	7
LVTTL Slow Slew Rate, 24 mA drive	9	7	5
LVTTL Fast Slew Rate, 2 mA drive	40	29	21
LVTTL Fast Slew Rate, 4 mA drive	24	18	12
LVTTL Fast Slew Rate, 6 mA drive	17	13	9
LVTTL Fast Slew Rate, 8 mA drive	13	10	7
LVTTL Fast Slew Rate, 12 mA drive	10	7	5
LVTTL Fast Slew Rate, 16 mA drive	8	6	4
LVTTL Fast Slew Rate, 24 mA drive	5	4	3
LVCMOS	10	7	5
PCI	8	6	4
GTL	4	4	4
GTL+	4	4	4

Date	Version	Revision
9/20/00	1.7	• Min values added to **Virtex-E Electrical Characteristics** tables. • XCV2600E and XCV3200E numbers added to **Virtex-E Electrical Characteristics** tables (Module 3). • Corrected user I/O count for XCV100E device in Table 1 (Module 1). • Changed several pins to “No Connect in the XCV100E“ and removed duplicate V_{CCINT} pins in Table ~ (Module 4). • Changed pin J10 to “No connect in XCV600E” in Table 74 (Module 4). • Changed pin J30 to “VREF option only in the XCV600E” in Table 74 (Module 4). • Corrected pair 18 in Table 75 (Module 4) to be “AO in the XCV1000E, XCV1600E“.
11/20/00	1.8	• Upgraded speed grade -8 numbers in **Virtex-E Electrical Characteristics** tables to Preliminary. • Updated minimums in Table 13 and added notes to Table 14. • Added to note 2 to **Absolute Maximum Ratings**. • Changed speed grade -8 numbers for $T_{SHCKO32}$, T_{REG}, T_{BCCS}, and T_{ICKOF}. • Changed all minimum hold times to –0.4 under **Global Clock Set-Up and Hold for LVTTL Standard, with DLL**. • Revised maximum T_{DLLPW} in -6 speed grade for **DLL Timing Parameters**. • Changed GCLK0 to BA22 for FG860 package in Table 46.
2/12/01	1.9	• Revised footnote for Table 14. • Added numbers to **Virtex-E Electrical Characteristics** tables for XCV1000E and XCV2000E devices. • Updated Table 27 and Table 78 to include values for XCV400E and XCV600E devices. • Revised Table 62 to include pinout information for the XCV400E and XCV600E devices in the BG560 package. • Updated footnotes 1 and 2 for Table 76 to include XCV2600E and XCV3200E devices.
4/02/01	2.0	• Updated numerous values in **Virtex-E Switching Characteristics** tables. • Converted data sheet to modularized format. See the **Virtex-E Data Sheet** section.
4/19/01	2.1	• Modified Figure 30 "DLL Generation of 4x Clock in Virtex-E Devices."
07/23/01	2.2	• Made minor edits to text under **Configuration**. • Added CLB column locations for XCV2600E anbd XCV3200E devices in Table 3.
11/09/01	2.3	• Added warning under **Configuration** section that attempting to load an incorrect bitstream causes configuration to fail and can damage the device.
07/17/02	2.4	• Data sheet designation upgraded from Preliminary to Production.
09/10/02	2.5	• Added clarification to the **Input/Output Block**, **Configuration**, **Boundary Scan Mode**, and **Block SelectRAM** sections. Revised Figure 18, Table 11, and Table 36.
11/19/02	2.6	• Added clarification in the **Boundary Scan** section. • Removed last sentence regarding deactivation of duty-cycle correction in **Duty Cycle Correction Property** section.
06/15/04	2.6.1	• Updated clickable web addresses.
01/12/06	2.7	• Updated the **Slave-Serial Mode** and the **Master-Serial Mode** sections.
01/16/06	2.8	• Made minor updates to Table 8.

DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Device	Min	Max	Units
V_{DRINT}	Data Retention V_{CCINT} Voltage (below which configuration data might be lost)		All	1.5		V
V_{DRIO}	Data Retention V_{CCO} Voltage (below which configuration data might be lost)		All	1.2		V
I_{CCINTQ}	Quiescent V_{CCINT} supply current (Note 1)		XCV50E		200	mA
			XCV100E		200	mA
			XCV200E		300	mA
			XCV300E		300	mA
			XCV400E		300	mA
			XCV600E		400	mA
			XCV1000E		500	mA
			XCV1600E		500	mA
			XCV2000E		500	mA
			XCV2600E		500	mA
			XCV3200E		500	mA
I_{CCOQ}	Quiescent V_{CCO} supply current (Note 1)		XCV50E		2	mA
			XCV100E		2	mA
			XCV200E		2	mA
			XCV300E		2	mA
			XCV400E		2	mA
			XCV600E		2	mA
			XCV1000E		2	mA
			XCV1600E		2	mA
			XCV2000E		2	mA
			XCV2600E		2	mA
			XCV3200E		2	mA
I_L	Input or output leakage current		All	–10	+10	µA
C_{IN}	Input capacitance (sample tested)	BGA, PQ, HQ, packages	All		8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0 V, V_{CCO} = 3.3 V (sample tested)		All	Note 2	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 3.6 V (sample tested)			Note 2	0.25	mA

Notes:
1. With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating.
2. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.

IOB Output Switching Characteristics, Figure 1

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 10.

Description[2]	Symbol	Speed Grade[1]				Units
		Min	-8	-7	-6	
Propagation Delays						
O input to Pad	T_{IOOP}	1.04	2.5	2.7	2.9	ns, max
O input to Pad via transparent latch	T_{IOOLP}	1.24	2.9	3.1	3.4	ns, max
3-State Delays						
T input to Pad high-impedance (Note 2)	T_{IOTHZ}	0.73	1.5	1.7	1.9	ns, max
T input to valid data on Pad	T_{IOTON}	1.13	2.7	2.9	3.1	ns, max
T input to Pad high-impedance via transparent latch (Note 2)	$T_{IOTLPHZ}$	0.86	1.8	2.0	2.2	ns, max
T input to valid data on Pad via transparent latch	$T_{IOTLPON}$	1.26	3.0	3.2	3.4	ns, max
GTS to Pad high impedance (Note 2)	T_{GTS}	1.94	4.1	4.6	4.9	ns, max
Sequential Delays						
Clock CLK						
Minimum Pulse Width, High	T_{CH}	0.56	1.2	1.3	1.4	ns, min
Minimum Pulse Width, Low	T_{CL}	0.56	1.2	1.3	1.4	ns, min
Clock CLK to Pad	T_{IOCKP}	0.97	2.4	2.8	2.9	ns, max
Clock CLK to Pad high-impedance (synchronous) (Note 2)	T_{IOCKHZ}	0.77	1.6	2.0	2.2	ns, max
Clock CLK to valid data on Pad (synchronous)	T_{IOCKON}	1.17	2.8	3.2	3.4	ns, max
Setup and Hold Times before/after Clock CLK						
O input	T_{IOOCK} / T_{IOCKO}	0.43 / 0	0.9 / 0	1.0 / 0	1.1 / 0	ns, min
OCE input	$T_{IOOCECK}$ / $T_{IOCKOCE}$	0.28 / 0	0.55 / 0.01	0.7 / 0	0.7 / 0	ns, min
SR input (OFF)	$T_{IOSRCKO}$ / $T_{IOCKOSR}$	0.40 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
3-State Setup Times, T input	T_{IOTCK} / T_{IOCKT}	0.26 / 0	0.51 / 0	0.6 / 0	0.7 / 0	ns, min
3-State Setup Times, TCE input	$T_{IOTCECK}$ / $T_{IOCKTCE}$	0.30 / 0	0.6 / 0	0.7 / 0	0.8 / 0	ns, min
3-State Setup Times, SR input (TFF)	$T_{IOSRCKT}$ / $T_{IOCKTSR}$	0.38 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
Set/Reset Delays						
SR input to Pad (asynchronous)	T_{IOSRP}	1.30	3.1	3.3	3.5	ns, max
SR input to Pad high-impedance (asynchronous) (Note 2)	T_{IOSRHZ}	1.08	2.2	2.4	2.7	ns, max
SR input to valid data on Pad (asynchronous)	T_{IOSRON}	1.48	3.4	3.7	3.9	ns, max
GSR to Pad	T_{IOGSRQ}	3.88	7.6	8.5	9.7	ns, max

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. 3-state turn-off delays should not be adjusted.

Global Clock Set-Up and Hold for LVTTL Standard, *without* DLL

Description[1]	Symbol	Device	Speed Grade[2, 3]				Units
			Min	-8	-7	-6	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in **IOB Input Switching Characteristics Standard Adjustments**, page 8.							
Full Delay	T_{PSFD}/T_{PHFD}	XCV50E	1.8 / 0	1.8 / 0	1.8 / 0	1.8 / 0	ns
Global Clock and IFF, without DLL		XCV100E	1.8 / 0	1.8 / 0	1.8 / 0	1.8 / 0	ns
		XCV200E	1.9 / 0	1.9 / 0	1.9 / 0	1.9 / 0	ns
		XCV300E	2.0 / 0	2.0 / 0	2.0 / 0	2.0 / 0	ns
		XCV400E	2.0 / 0	2.0 / 0	2.0 / 0	2.0 / 0	ns
		XCV600E	2.1 / 0	2.1 / 0	2.1 / 0	2.1 / 0	ns
		XCV1000E	2.3 / 0	2.3 / 0	2.3 / 0	2.3 / 0	ns
		XCV1600E	2.5 / 0	2.5 / 0	2.5 / 0	2.5 / 0	ns
		XCV2000E	2.5 / 0	2.5 / 0	2.5 / 0	2.5 / 0	ns
		XCV2600E	2.7 / 0	2.7 / 0	2.7 / 0	2.7 / 0	ns
		XCV3200E	2.8 / 0	2.8 / 0	2.8 / 0	2.8 / 0	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Pinout Differences Between Virtex and Virtex-E Families

The same device in the same package for the Virtex-E and Virtex families are pin-compatible with some minor exceptions, listed in Table 1.

XCV200E Device, FG456 Package

The Virtex-E XCV200E has two I/O pins swapped with the Virtex XCV200 to accommodate differential clock pairing.

XCV400E Device, FG676 Package

The Virtex-E XCV400E has two I/O pins swapped with the Virtex XCV400 to accommodate differential clock pairing.

All Devices, PQ240 and HQ240 Packages

The Virtex devices in PQ240 and HQ240 packages do not have V_{CCO} banking, but Virtex-E devices do. To achieve this, eight Virtex I/O pins (P232, P207, P176, P146, P116, P85, P55, and P25) are now VCCO pins in the Virtex-E family. This change also requires one Virtex I/O or VREF pin to be swapped with a standard I/O pin.

Additionally, accommodating differential clock input pairs in Virtex-E caused some IO_V_{REF} differences in the XCV400E and XCV600E devices only. Virtex IO_V_{REF} pins P215 and P87 are Virtex-E IO_V_{REF} pins P216 and P86, respectively. Virtex-E pins P215 and P87 are IO_DLL.

Table 1: **Pinout Differences Summary**

Part	Package	Pins	Virtex	Virtex-E
XCV200	FG456	E11, U11	I/O	No Connect
		B11, AA11	No Connect	IO_LVDS_DLL
XCV400	FG676	D13, Y13	I/O	No Connect
		B13, AF13	No Connect	IO_LVDS_DLL
XCV400/600	PQ240/HQ240	P215, P87	IO_V_{REF}	IO_LVDS_DLL
		P216, P86	I/O	IO_V_{REF}
All	PQ240/HQ240	P232, P207, P176, P146, P116, P85, P55, and P25	I/O	V_{CCO}
		P231	I/O	IO_V_{REF}

Table 12: **BG432 — XCV300E, XCV400E, XCV600E**

Bank	Pin Description	Pin #
6	IO	AA30
6	IO	AC30
6	IO	AD29
6	IO	U31
6	IO	W28
6	IO_L103N_YY	AJ30
6	IO_L103P_YY	AH30
6	IO_L104N	AG28
6	IO_L104P	AH31
6	IO_L105N_Y	AG29
6	IO_L105P_Y	AG30
6	IO_VREF_L106N_Y	AF28
6	IO_L106P_Y	AG31
6	IO_L107N	AF29
6	IO_L107P	AF30
6	IO_L108N_Y	AE28
6	IO_L108P_Y	AF31
6	IO_VREF_L109N_YY	AE30
6	IO_L109P_YY	AD28
6	IO_L110N_Y	AD30
6	IO_L110P_Y	AD31
6	IO_VREF_L111N_Y	AC28[1]
6	IO_L111P_Y	AC29
6	IO_VREF_L112N_YY	AB28
6	IO_L112P_YY	AB29
6	IO_L113N_YY	AB31
6	IO_L113P_YY	AA29
6	IO_L114N_Y	Y28
6	IO_L114P_Y	Y29
6	IO_L115N_Y	Y30
6	IO_L115P_Y	Y31
6	IO_L116N_Y	W29
6	IO_L116P_Y	W30
6	IO_VREF_L117N_YY	V28
6	IO_L117P_YY	V29
6	IO_L118N_Y	V30

Table 12: **BG432 — XCV300E, XCV400E, XCV600E**

Bank	Pin Description	Pin #
6	IO_L118P_Y	U29
6	IO_VREF_L119N_Y	U28[2]
6	IO_L119P_Y	U30
6	IO	T30
7	IO	C30
7	IO	H29
7	IO	H31
7	IO	L29
7	IO	M31
7	IO	R28
7	IO_L120N_YY	T31
7	IO_L120P_YY	R29
7	IO_L121N_Y	R30
7	IO_VREF_L121P_Y	R31[2]
7	IO_L122N_Y	P29
7	IO_L122P_Y	P28
7	IO_L123N_YY	P30
7	IO_VREF_L123P_YY	N30
7	IO_L124N_Y	N28
7	IO_L124P_Y	N31
7	IO_L125N_Y	M29
7	IO_L125P_Y	M28
7	IO_L126N_Y	M30
7	IO_L126P_Y	L30
7	IO_L127N_YY	K31
7	IO_L127P_YY	K30
7	IO_L128N_YY	K28
7	IO_VREF_L128P_YY	J30
7	IO_L129N_Y	J29
7	IO_VREF_L129P_Y	J28[1]
7	IO_L130N_Y	H30
7	IO_L130P_Y	G30
7	IO_L131N_YY	H28
7	IO_VREF_L131P_YY	F31
7	IO_L132N_Y	G29

Table 21: **FG676 Differential Pin Pair Summary XCV400E, XCV600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
52	2	G24	H22	√	-
53	2	J21	G25	2	-
54	2	G26	J22	1	VREF
55	2	H24	J23	√	-
56	2	J24	K20	√	VREF
57	2	K22	K21	√	D2
58	2	H25	K23	√	-
59	2	L20	J26	2	-
60	2	K25	L22	1	-
61	2	L21	L23	1	-
62	2	M20	L24	1	-
63	2	M23	M22	√	D3
64	2	L26	M21	√	-
65	2	N19	M24	2	-
66	2	M26	N20	1	VREF
67	2	N24	N21	√	-
68	2	N23	N22	√	-
69	3	P21	P23	√	-
70	3	P22	R25	1	VREF
71	3	P19	P20	2	-
72	3	R21	R22	√	-
73	3	R24	R23	√	VREF
74	3	T24	R20	1	-
75	3	T22	U24	1	-
76	3	T23	U25	1	-
77	3	T21	U20	2	-
78	3	U22	V26	√	-
79	3	T20	U23	√	D5
80	3	V24	U21	√	VREF
81	3	V23	W24	√	-
82	3	V22	W26	1	VREF
83	3	Y25	V21	2	-
84	3	V20	AA26	√	-
85	3	Y24	W23	√	VREF

Table 21: **FG676 Differential Pin Pair Summary XCV400E, XCV600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
86	3	AA24	Y23	1	-
87	3	AB26	W21	2	-
88	3	Y22	W22	1	VREF
89	3	AA23	AB24	2	-
90	3	W20	AC24	√	-
91	3	AB23	Y21	√	INIT
92	4	AC22	AD26	√	-
93	4	AD23	AA20	1	-
94	4	Y19	AC21	√	-
95	4	AD22	AB20	√	VREF
96	4	AE22	Y18	NA	-
97	4	AF22	AA19	NA	-
98	4	AD21	AB19	√	VREF
99	4	AC20	AA18	√	-
100	4	AC19	AD20	1	-
101	4	AF20	AB18	1	VREF
102	4	AD19	Y17	NA	-
103	4	AE19	AD18	NA	VREF
104	4	AF19	AA17	√	-
105	4	AC17	AB17	1	-
106	4	Y16	AE17	√	-
107	4	AF17	AA16	√	-
108	4	AD17	AB16	NA	-
109	4	AC16	AD16	√	-
110	4	AC15	Y15	√	VREF
111	4	AD15	AA15	√	-
112	4	W14	AB15	1	-
113	4	AF15	Y14	1	VREF
114	4	AD14	AB14	NA	-
115	5	AC14	AF13	NA	IO_LVDS_DLL
116	5	AA13	AF12	1	VREF
117	5	AC13	W13	1	-
118	5	AA12	AD12	√	-
119	5	AC12	AB12	√	VREF

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
2	IO_L63N	G4
2	IO_L64P	G3
2	IO_L64N	E2
2	IO_VREF_L65P_Y	H4
2	IO_L65N_Y	E1
2	IO_L66P_YY	H3
2	IO_L66N_YY	F2
2	IO_L67P	J4
2	IO_L67N	F1
2	IO_L68P_Y	J3
2	IO_L68N_Y	G2
2	IO_VREF_L69P_YY	G1
2	IO_L69N_YY	K4
2	IO_L70P_YY	H2
2	IO_L70N_YY	K3
2	IO_VREF_L71P	H1[3]
2	IO_L71N	L4
2	IO_L72P	J2
2	IO_L72N	L3
2	IO_VREF_L73P_YY	J1
2	IO_L73N_YY	M3
2	IO_L74P_YY	K2
2	IO_L74N_YY	N4
2	IO_L75P	K1
2	IO_L75N	N3
2	IO_VREF_L76P_YY	L2
2	IO_D1_L76N_YY	P4
2	IO_D2_L77P_YY	P3
2	IO_L77N_YY	L1
2	IO_L78P_Y	R4
2	IO_L78N_Y	M2
2	IO_L79P	R3
2	IO_L79N	M1
2	IO_L80P	T4
2	IO_L80N	N2
2	IO_VREF_L81P_Y	N1[1]

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
2	IO_L81N_Y	T3
2	IO_L82P_YY	P2
2	IO_L82N_YY	U5
2	IO_L83P	P1
2	IO_L83N	U4
2	IO_L84P_Y	R2
2	IO_L84N_Y	U3
2	IO_VREF_L85P_YY	V5
2	IO_D3_L85N_YY	R1
2	IO_L86P_YY	V4
2	IO_L86N_YY	T2
2	IO_L87P	V3
2	IO_L87N	T1
2	IO_L88P	W4
2	IO_L88N	U2
2	IO_VREF_L89P_YY	W3
2	IO_L89N_YY	U1
2	IO_L90P_YY	AA3
2	IO_L90N_YY	V2
2	IO_VREF_L91P	AA4[2]
2	IO_L91N	V1
2	IO_L92P_YY	AB2
2	IO_L92N_YY	W2
3	IO	AP3
3	IO	AT3
3	IO	AB3
3	IO_L93P	AB4
3	IO_VREF_L93N	W1[2]
3	IO_L94P_YY	AB5
3	IO_L94N_YY	Y2
3	IO_L95P_YY	AC2
3	IO_VREF_L95N_YY	Y1
3	IO_L96P	AC3
3	IO_L96N	AA1
3	IO_L97P	AC4

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
5	IO_L178P_Y	BB23
5	IO_L178N_Y	AW23
5	IO_L179P_YY	AV23
5	IO_VREF_L179N_YY	BA23
5	IO_L180P_YY	AW24
5	IO_L180N_YY	BB24
5	IO_L181P_Y	AY24
5	IO_L181N_Y	AW25
5	IO_L182P_Y	BA24
5	IO_L182N_Y	AV25
5	IO_L183P_YY	AW26
5	IO_VREF_L183N_YY	AY25
5	IO_L184P_YY	AV26
5	IO_L184N_YY	BA25
5	IO_L185P_Y	BB26
5	IO_L185N_Y	AV27
5	IO_L186P_Y	AY26
5	IO_L186N_Y	AU27
5	IO_L187P_YY	AW28
5	IO_VREF_L187N_YY	BB27
5	IO_L188P_YY	AY27
5	IO_L188N_YY	AV28
5	IO_L189P_Y	BA27
5	IO_L189N_Y	AW29
5	IO_L190P_Y	BB28
5	IO_L190N_Y	AV29
5	IO_L191P_Y	AY28
5	IO_L191N_Y	AW30
5	IO_L192P_Y	BA28
5	IO_L192N_Y	AW31
5	IO_L193P_YY	BB29
5	IO_L193N_YY	AV31
5	IO_L194P_YY	AY29
5	IO_VREF_L194N_YY	AY32
5	IO_L195P_Y	AW32
5	IO_L195N_Y	BB30
5	IO_L196P_Y	AV32

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
5	IO_L196N_Y	AY30
5	IO_L197P_YY	BA30
5	IO_VREF_L197N_YY	AW33
5	IO_L198P_YY	BB31
5	IO_L198N_YY	AV33
5	IO_L199P_Y	AY34
5	IO_VREF_L199N_Y	BA31[2]
5	IO_L200P_Y	AW34
5	IO_L200N_Y	BB32
5	IO_L201P_YY	BA32
5	IO_VREF_L201N_YY	AY35
5	IO_L202P_YY	BB33
5	IO_L202N_YY	AW35
5	IO_L203P_Y	AV35
5	IO_L203N_Y	BB34
5	IO_L204P_Y	AY36
5	IO_L204N_Y	BA34
5	IO_L205P_YY	BB35
5	IO_VREF_L205N_YY	AV36
5	IO_L206P_YY	BA35
5	IO_L206N_YY	AY37
5	IO_L207P_Y	BB36
5	IO_L207N_Y	BA36
5	IO_L208P_Y	AW37
5	IO_VREF_L208N_Y	BB37
5	IO_L209P_Y	BA37
5	IO_L209N_Y	AY38
5	IO_L210P_Y	BB38
5	IO_L210N_Y	AY39
6	IO	AA40
6	IO	AB41
6	IO	AC42
6	IO	AD39
6	IO	AE40
6	IO	AF38
6	IO	AF40

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
6	IO	AJ40
6	IO	AL41
6	IO	AN38
6	IO	AN42
6	IO	AP41
6	IO	AR39
6	IO_L211N_YY	AV41
6	IO_L211P_YY	AV42
6	IO_L212N_Y	AW40
6	IO_L212P_Y	AU41
6	IO_L213N_Y	AV39
6	IO_L213P_Y	AU42
6	IO_VREF_L214N_Y	AT41
6	IO_L214P_Y	AU38
6	IO_L215N	AT42
6	IO_L215P	AV40
6	IO_L216N_Y	AR41
6	IO_L216P_Y	AU39
6	IO_VREF_L217N_Y	AR42
6	IO_L217P_Y	AU40
6	IO_L218N_YY	AT38
6	IO_L218P_YY	AP42
6	IO_L219N_Y	AN41
6	IO_L219P_Y	AT39
6	IO_L220N_Y	AT40
6	IO_L220P_Y	AM40
6	IO_VREF_L221N_YY	AR38
6	IO_L221P_YY	AM41
6	IO_L222N_YY	AM42
6	IO_L222P_YY	AR40
6	IO_VREF_L223N_Y	AL40[2]
6	IO_L223P_Y	AP38
6	IO_L224N_Y	AP39
6	IO_L224P_Y	AL42
6	IO_VREF_L225N_YY	AP40
6	IO_L225P_YY	AK40
6	IO_L226N_YY	AK41

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
6	IO_L226P_YY	AN39
6	IO_L227N_Y	AK42
6	IO_L227P_Y	AN40
6	IO_VREF_L228N_YY	AM38
6	IO_L228P_YY	AJ41
6	IO_L229N_YY	AJ42
6	IO_L229P_YY	AM39
6	IO_L230N_Y	AH40
6	IO_L230P_Y	AH41
6	IO_L231N_Y	AL38
6	IO_L231P_Y	AH42
6	IO_L232N_Y	AL39
6	IO_L232P_Y	AG41
6	IO_L233N	AK39
6	IO_L233P	AG40
6	IO_L234N_Y	AJ38
6	IO_L234P_Y	AG42
6	IO_VREF_L235N_Y	AF42
6	IO_L235P_Y	AJ39
6	IO_L236N_YY	AF41
6	IO_L236P_YY	AH38
6	IO_L237N_Y	AE42
6	IO_L237P_Y	AH39
6	IO_L238N_Y	AG38
6	IO_L238P_Y	AE41
6	IO_VREF_L239N_YY	AG39
6	IO_L239P_YY	AD42
6	IO_L240N_YY	AD40
6	IO_L240P_YY	AF39
6	IO_L241N_Y	AD41
6	IO_L241P_Y	AE38
6	IO_L242N_Y	AE39
6	IO_L242P_Y	AC40
6	IO_VREF_L243N_YY	AD38
6	IO_L243P_YY	AC41
6	IO_L244N_YY	AB42
6	IO_L244P_YY	AC38

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
NA	VCCO_1	F15
NA	VCCO_1	F19
NA	VCCO_1	F20
NA	VCCO_1	F7
NA	VCCO_1	F8
NA	VCCO_2	G6
NA	VCCO_2	H6
NA	VCCO_2	L6
NA	VCCO_2	M6
NA	VCCO_2	P6
NA	VCCO_2	R6
NA	VCCO_2	W6
NA	VCCO_2	Y6
NA	VCCO_3	AC6
NA	VCCO_3	AD6
NA	VCCO_3	AH6
NA	VCCO_3	AJ6
NA	VCCO_3	AL6
NA	VCCO_3	AM6
NA	VCCO_3	AR6
NA	VCCO_3	AT6
NA	VCCO_4	AU11
NA	VCCO_4	AU12
NA	VCCO_4	AU14
NA	VCCO_4	AU15
NA	VCCO_4	AU19
NA	VCCO_4	AU20
NA	VCCO_4	AU7
NA	VCCO_4	AU8
NA	VCCO_5	AU23
NA	VCCO_5	AU24
NA	VCCO_5	AU28
NA	VCCO_5	AU29
NA	VCCO_5	AU31
NA	VCCO_5	AU32
NA	VCCO_5	AU35
NA	VCCO_5	AU36

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
NA	VCCO_6	AC37
NA	VCCO_6	AD37
NA	VCCO_6	AH37
NA	VCCO_6	AJ37
NA	VCCO_6	AL37
NA	VCCO_6	AM37
NA	VCCO_6	AR37
NA	VCCO_6	AT37
NA	VCCO_7	G37
NA	VCCO_7	H37
NA	VCCO_7	L37
NA	VCCO_7	M37
NA	VCCO_7	P37
NA	VCCO_7	R37
NA	VCCO_7	W37
NA	VCCO_7	Y37
NA	GND	N6
NA	GND	N5
NA	GND	N38
NA	GND	N37
NA	GND	F6
NA	GND	F37
NA	GND	F30
NA	GND	F22
NA	GND	F21
NA	GND	F13
NA	GND	E5
NA	GND	E38
NA	GND	E30
NA	GND	E22
NA	GND	E21
NA	GND	E13
NA	GND	D42
NA	GND	D4
NA	GND	D39
NA	GND	D1

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
7	IO	E3
7	IO	F1[4]
7	IO	G1[5]
7	IO	G4[5]
7	IO	H3[5]
7	IO	J1[4]
7	IO	J3[4]
7	IO	J4[4]
7	IO	J6[4]
7	IO	L10[4]
7	IO	N2[4]
7	IO	N8[4]
7	IO	N10[4]
7	IO	P3[5]
7	IO	P9[4]
7	IO	R1[5]
7	IO	T3[4]
7	IO_L247P	R10
7	IO_L248N_YY	R5[3]
7	IO_L248P_YY	R6[4]
7	IO_L249N_YY	R8
7	IO_VREF_L249P_YY	R4[2]
7	IO_L250N_YY	R7
7	IO_L250P_YY	R3
7	IO_L251N_YY	P10
7	IO_VREF_L251P_YY	P6
7	IO_L252N_YY	P5
7	IO_L252P_YY	P2
7	IO_L253N	P7
7	IO_L253P	P4
7	IO_L254N_YY	N4
7	IO_L254P_YY	R2
7	IO_L255N_YY	N7
7	IO_VREF_L255P_YY	P1
7	IO_L256N	M6

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
7	IO_L256P	N6
7	IO_L257N_YY	N5
7	IO_L257P_YY	N1
7	IO_L258N_YY	M4
7	IO_L258P_YY	M5
7	IO_L259N	M2
7	IO_VREF_L259P	M1[1]
7	IO_L260N_YY	L4
7	IO_L260P_YY	L2
7	IO_L261N_Y	M7[4]
7	IO_L261P_Y	L5[4]
7	IO_L262N_YY	L1
7	IO_L262P_YY	M8
7	IO_L263N	K2
7	IO_L263P	M9
7	IO_L264N	L3[4]
7	IO_L264P	M10[4]
7	IO_L265N_YY	K5
7	IO_L265P_YY	K1
7	IO_L266N_YY	L6
7	IO_VREF_L266P_YY	K3
7	IO_L267N_YY	L7
7	IO_L267P_YY	K4
7	IO_L268N_YY	L8
7	IO_L268P_YY	J5
7	IO_L269N_YY	K6
7	IO_VREF_L269P_YY	H4
7	IO_L270N_YY	H1
7	IO_L270P_YY	K7
7	IO_L271N	J7
7	IO_L271P	J2
7	IO_L272N_YY	H5
7	IO_L272P_YY	G2
7	IO_L273N_YY	L9
7	IO_VREF_L273P_YY	G5
7	IO_L274N	F3
7	IO_L274P	K8

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
NA	GND	AG27
NA	GND	D27
NA	GND	AF26
NA	GND	E26
NA	GND	F25
NA	GND	AE25
NA	GND	G24
NA	GND	AJ23
NA	GND	AD24
NA	GND	H23
NA	GND	B23
NA	GND	AC23
NA	GND	AB22
NA	GND	V22
NA	GND	N22
NA	GND	AH18
NA	GND	AB18
NA	GND	J18
NA	GND	C18
NA	GND	U17
NA	GND	T17
NA	GND	R17
NA	GND	P17
NA	GND	U16
NA	GND	T16
NA	GND	R16
NA	GND	P16
NA	GND	U15
NA	GND	T15
NA	GND	R15
NA	GND	P15
NA	GND	U14
NA	GND	T14
NA	GND	R14
NA	GND	P14
NA	GND	AH13
NA	GND	AB13

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
NA	GND	J13
NA	GND	C13
NA	GND	V9
NA	GND	N9
NA	GND	J9
NA	GND	AJ8
NA	GND	AC8
NA	GND	H8
NA	GND	AD7
NA	GND	B8
NA	GND	AE6
NA	GND	G7
NA	GND	F6
NA	GND	AF5
NA	GND	E5
NA	GND	AG4
NA	GND	D4
NA	GND	V3
NA	GND	N3
NA	GND	C3
NA	GND	AK2
NA	GND	AH3
NA	GND	AC2
NA	GND	H2
NA	GND	B2
NA	GND	A2
NA	GND	AK1
NA	GND	AJ2
NA	GND	AJ1
NA	GND	A1
NA	GND	B1

Notes:

1. V_{REF} or I/O option only in the XCV1000E and XCV1600E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV1600E; otherwise, I/O option only.
3. I/O option only in the XCV600E.
4. No Connect in the XCV600E.
5. No Connect in the XCV600E, 1000E.

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
4	IO_L178N_YY	AL28
4	IO_L179P_YY	AE24[4]
4	IO_L179N_YY	AN28[5]
4	IO_L180P_Y	AJ27
4	IO_L180N_Y	AH26
4	IO_L181P_Y	AG25
4	IO_L181N_Y	AK27
4	IO_L182P	AM28[4]
4	IO_L182N	AF24[5]
4	IO_L183P_YY	AJ26
4	IO_L183N_YY	AP27
4	IO_VREF_L184P_YY	AK26
4	IO_L184N_YY	AN27
4	IO_L185P	AE23[4]
4	IO_L185N	AM27[5]
4	IO_L186P_Y	AL26
4	IO_L186N_Y	AP26
4	IO_VREF_L187P_Y	AN26[2]
4	IO_L187N_Y	AJ25
4	IO_L188P	AG24[4]
4	IO_L188N	AP25[5]
4	IO_L189P_YY	AF23
4	IO_L189N_YY	AM26
4	IO_VREF_L190P_YY	AJ24
4	IO_L190N_YY	AN25
4	IO_L191P_Y	AE22
4	IO_L191N_Y	AM25
4	IO_L192P_Y	AK24
4	IO_L192N_Y	AH23
4	IO_VREF_L193P_YY	AF22
4	IO_L193N_YY	AP24
4	IO_L194P_YY	AL24
4	IO_L194N_YY	AK23
4	IO_L195P_Y	AG22

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
4	IO_L195N_Y	AN23
4	IO_L196P_Y	AP23
4	IO_L196N_Y	AM23
4	IO_L197P_Y	AH22
4	IO_L197N_Y	AP22
4	IO_L198P_Y	AL23
4	IO_L198N_Y	AF21
4	IO_L199P_YY	AL22
4	IO_L199N_YY	AJ22
4	IO_VREF_L200P_YY	AK22
4	IO_L200N_YY	AM22
4	IO_L201P_YY	AG21[4]
4	IO_L201N_YY	AJ21[5]
4	IO_L202P_Y	AP21
4	IO_L202N_Y	AE20
4	IO_L203P_Y	AH21
4	IO_L203N_Y	AL21
4	IO_L204P	AN21[4]
4	IO_L204N	AF20[5]
4	IO_L205P_YY	AK21
4	IO_L205N_YY	AP20
4	IO_VREF_L206P_YY	AE19
4	IO_L206N_YY	AN20
4	IO_L207P_Y	AG20[4]
4	IO_L207N_Y	AL20[5]
4	IO_L208P_Y	AH20
4	IO_L208N_Y	AK20
4	IO_L209P_Y	AN19
4	IO_L209N_Y	AJ20
4	IO_L210P	AF19[4]
4	IO_L210N	AP19[5]
4	IO_L211P_YY	AM19
4	IO_L211N_YY	AH19
4	IO_VREF_L212P_YY	AJ19

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
6	IO_VREF_L265N_Y	AJ3
6	IO_L265P_Y	AG5
6	IO_L266N_YY	AD9[4]
6	IO_L266P_YY	AJ2[5]
6	IO_L267N_YY	AC10
6	IO_L267P_YY	AH2
6	IO_L268N_Y	AH3
6	IO_L268P_Y	AF5
6	IO_L269N_Y	AE8[4]
6	IO_L269P_Y	AG3[5]
6	IO_L270N_Y	AE7
6	IO_L270P_Y	AG2
6	IO_VREF_L271N_YY	AF6
6	IO_L271P_YY	AG1
6	IO_L272N_YY	AC9[4]
6	IO_L272P_YY	AG4[5]
6	IO_L273N_YY	AE6
6	IO_L273P_YY	AF3
6	IO_VREF_L274N_Y	AF1[2]
6	IO_L274P_Y	AF4
6	IO_L275N	AB10[4]
6	IO_L275P	AF2[5]
6	IO_L276N_Y	AC8
6	IO_L276P_Y	AE1
6	IO_VREF_L277N_YY	AD5
6	IO_L277P_YY	AE3
6	IO_L278N_YY	AC7
6	IO_L278P_YY	AD1
6	IO_L279N_Y	AD6
6	IO_L279P_Y	AD2
6	IO_VREF_L280N_YY	AB8
6	IO_L280P_YY	AC1
6	IO_L281N_YY	AC5
6	IO_L281P_YY	AC2

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
6	IO_L282N_Y	AA9
6	IO_L282P_Y	AC3
6	IO_L283N_Y	AC4
6	IO_L283P_Y	AD4
6	IO_L284N_Y	AA8
6	IO_L284P_Y	AB6
6	IO_L285N	AB1
6	IO_L285P	Y10
6	IO_L286N_Y	AB2
6	IO_L286P_Y	AA7
6	IO_VREF_L287N_Y	AA4
6	IO_L287P_Y	AA1
6	IO_L288N_YY	Y9[4]
6	IO_L288P_YY	AB4[5]
6	IO_L289N_YY	AA2
6	IO_L289P_YY	Y8
6	IO_L290N_Y	AA6
6	IO_L290P_Y	AA5
6	IO_L291N_Y	AB3[4]
6	IO_L291P_Y	Y7[5]
6	IO_L292N_Y	Y1
6	IO_L292P_Y	W10
6	IO_VREF_L293N_YY	Y5
6	IO_L293P_YY	Y2
6	IO_L294N_YY	W9[4]
6	IO_L294P_YY	W2[5]
6	IO_L295N_YY	W7
6	IO_L295P_YY	Y4
6	IO_L296N_Y	W1
6	IO_L296P_Y	Y6
6	IO_L297N_Y	W6[4]
6	IO_L297P_Y	W3[5]
6	IO_L298N_Y	V9
6	IO_L298P_Y	W4

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
NA	GND	R15
NA	GND	P15
NA	GND	L3
NA	GND	G7
NA	GND	E30
NA	GND	C24
NA	GND	B34
NA	GND	AP32
NA	GND	AM1
NA	GND	AM34
NA	GND	AJ29
NA	GND	AF9
NA	GND	AA17
NA	GND	Y17
NA	GND	W16
NA	GND	V16
NA	GND	U17
NA	GND	T17
NA	GND	R16
NA	GND	P16
NA	GND	L32
NA	GND	G28
NA	GND	D4
NA	GND	C32
NA	GND	A1
NA	GND	AP33
NA	GND	AM2
NA	GND	AL4
NA	GND	AH1
NA	GND	AF26
NA	GND	AA18
NA	GND	Y18
NA	GND	W17
NA	GND	V17

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
NA	GND	U18
NA	GND	T18
NA	GND	R17
NA	GND	P17
NA	GND	J9
NA	GND	G34
NA	GND	D31
NA	GND	C33
NA	GND	A2
NA	GND	AB17
NA	GND	AB18
NA	GND	N17
NA	GND	N18
NA	GND	U13
NA	GND	V13
NA	GND	U22
NA	GND	V22

Notes:

1. V_{REF} or I/O option only in the XCV1600E, XCV2000E, XCV2600E, and XCV3200E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV2000E, XCV2600E, and XCV3200E; otherwise, I/O option only.
3. No Connect in the XCV1000E, XCV1600E.
4. No Connect in the XCV1000E.
5. I/O in the XCV1000E.