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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1176
Number of Logic Elements/Cells	5292
Total RAM Bits	114688
Number of I/O	158
Number of Gates	306393
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	240-BFQFP
Supplier Device Package	240-PQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv200e-6pq240c

Table 1: **Virtex-E Field-Programmable Gate Array Family Members**

Device	System Gates	Logic Gates	CLB Array	Logic Cells	Differential I/O Pairs	User I/O	BlockRAM Bits	Distributed RAM Bits
XCV50E	71,693	20,736	16 x 24	1,728	83	176	65,536	24,576
XCV100E	128,236	32,400	20 x 30	2,700	83	196	81,920	38,400
XCV200E	306,393	63,504	28 x 42	5,292	119	284	114,688	75,264
XCV300E	411,955	82,944	32 x 48	6,912	137	316	131,072	98,304
XCV400E	569,952	129,600	40 x 60	10,800	183	404	163,840	153,600
XCV600E	985,882	186,624	48 x 72	15,552	247	512	294,912	221,184
XCV1000E	1,569,178	331,776	64 x 96	27,648	281	660	393,216	393,216
XCV1600E	2,188,742	419,904	72 x 108	34,992	344	724	589,824	497,664
XCV2000E	2,541,952	518,400	80 x 120	43,200	344	804	655,360	614,400
XCV2600E	3,263,755	685,584	92 x 138	57,132	344	804	753,664	812,544
XCV3200E	4,074,387	876,096	104 x 156	73,008	344	804	851,968	1,038,336

Virtex-E Compared to Virtex Devices

The Virtex-E family offers up to 43,200 logic cells in devices up to 30% faster than the Virtex family.

I/O performance is increased to 622 Mb/s using Source Synchronous data transmission architectures and synchronous system performance up to 240 MHz using singled-ended SelectI/O technology. Additional I/O standards are supported, notably LVPECL, LVDS, and BLVDS, which use two pins per signal. Almost all signal pins can be used for these new standards.

Virtex-E devices have up to 640 Kb of faster (250 MHz) block SelectRAM, but the individual RAMs are the same size and structure as in the Virtex family. They also have eight DLLs instead of the four in Virtex devices. Each individual DLL is slightly improved with easier clock mirroring and 4x frequency multiplication.

V_{CCINT}, the supply voltage for the internal logic and memory, is 1.8 V, instead of 2.5 V for Virtex devices. Advanced processing and 0.18 µm design rules have resulted in smaller dice, faster speed, and lower power consumption.

I/O pins are 3 V tolerant, and can be 5 V tolerant with an external 100 Ω resistor. PCI 5 V is not supported. With the addition of appropriate external resistors, any pin can tolerate any voltage desired.

Banking rules are different. With Virtex devices, all input buffers are powered by V_{CCINT}. With Virtex-E devices, the LVTTL, LVCMOS2, and PCI input buffers are powered by the I/O supply voltage V_{CCO}.

The Virtex-E family is not bitstream-compatible with the Virtex family, but Virtex designs can be compiled into equivalent Virtex-E devices.

The same device in the same package for the Virtex-E and Virtex families are pin-compatible with some minor exceptions. See the data sheet pinout section for details.

General Description

The Virtex-E FPGA family delivers high-performance, high-capacity programmable logic solutions. Dramatic increases in silicon efficiency result from optimizing the new architecture for place-and-route efficiency and exploiting an aggressive 6-layer metal 0.18 µm CMOS process. These advances make Virtex-E FPGAs powerful and flexible alternatives to mask-programmed gate arrays. The Virtex-E family includes the nine members in Table 1.

Building on experience gained from Virtex FPGAs, the Virtex-E family is an evolutionary step forward in programmable logic design. Combining a wide variety of programmable system features, a rich hierarchy of fast, flexible interconnect resources, and advanced process technology, the Virtex-E family delivers a high-speed and high-capacity programmable logic solution that enhances design flexibility while reducing time-to-market.

Virtex-E Architecture

Virtex-E devices feature a flexible, regular architecture that comprises an array of configurable logic blocks (CLBs) surrounded by programmable input/output blocks (IOBs), all interconnected by a rich hierarchy of fast, versatile routing

HSTL

A sample circuit illustrating a valid termination technique for HSTL_I appears in Figure 46. A sample circuit illustrating a valid termination technique for HSTL_III appears in Figure 47.

Table 25: **HSTL Class I Voltage Specification**

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF}	0.68	0.75	0.90
V_{TT}	-	$V_{CCO} \times 0.5$	-
V_{IH}	$V_{REF} + 0.1$	-	-
V_{IL}	-	-	$V_{REF} - 0.1$
V_{OH}	$V_{CCO} - 0.4$	-	-
V_{OL}			0.4
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL} at V_{OL} (mA)	8	-	-

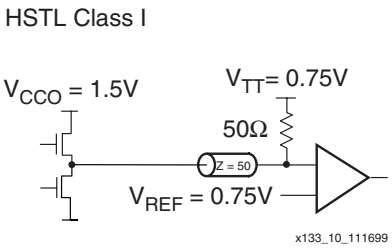

Figure 46: **Terminated HSTL Class I**

Table 26: **HSTL Class III Voltage Specification**

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF} (1)	-	0.90	-
V_{TT}	-	V_{CCO}	-
V_{IH}	$V_{REF} + 0.1$	-	-
V_{IL}	-	-	$V_{REF} - 0.1$
V_{OH}	$V_{CCO} - 0.4$	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL} at V_{OL} (mA)	24	-	-

Note: Per EIA/JESD8-6, "The value of V_{REF} is to be selected by the user to provide optimum noise margin in the use conditions specified by the user."

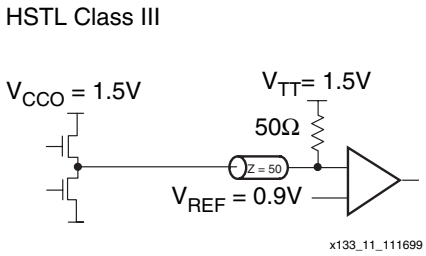

Figure 47: **Terminated HSTL Class III**

A sample circuit illustrating a valid termination technique for HSTL_IV appears in Figure 48.

Table 27: **HSTL Class IV Voltage Specification**

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF}	-	0.90	-
V_{TT}	-	V_{CCO}	-
V_{IH}	$V_{REF} + 0.1$	-	-
V_{IL}	-	-	$V_{REF} - 0.1$
V_{OH}	$V_{CCO} - 0.4$	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL} at V_{OL} (mA)	48	-	-

Note: Per EIA/JESD8-6, "The value of V_{REF} is to be selected by the user to provide optimum noise margin in the use conditions specified by the user.

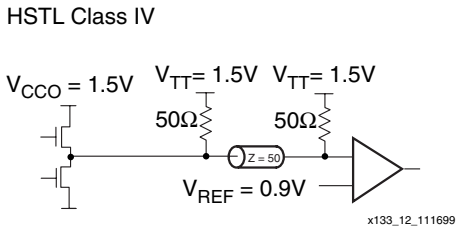

Figure 48: **Terminated HSTL Class IV**

SSTL2_II

A sample circuit illustrating a valid termination technique for SSTL2_II appears in Figure 52. DC voltage specifications appear in Table 31.

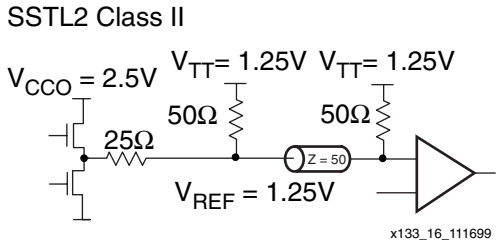

Figure 52: **Terminated SSTL2 Class II**

Table 31: **SSTL2_II Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
$V_{REF} = 0.5 \times V_{CCO}$	1.15	1.25	1.35
$V_{TT} = V_{REF} + N$(1)	1.11	1.25	1.39
$V_{IH} = V_{REF} + 0.18$	1.33	1.43	3.0(2)
$V_{IL} = V_{REF} - 0.18$	–0.3(3)	1.07	1.17
$V_{OH} = V_{REF} + 0.8$	1.95	-	-
$V_{OL} = V_{REF} - 0.8$	-	-	0.55
I_{OH} at V_{OH} (mA)	–15.2	-	-
I_{OL} at V_{OL} (mA)	15.2	-	-

Notes:
1. N must be greater than or equal to -0.04 and less than or equal to 0.04.
2. V_{IH} maximum is V_{CCO} + 0.3.
3. V_{IL} minimum does not conform to the formula.

CTT

A sample circuit illustrating a valid termination technique for CTT appear in Figure 53. DC voltage specifications appear in Table 32.

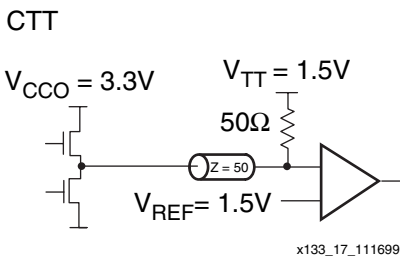

Figure 53: **Terminated CTT**

Table 32: **CTT Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	2.05(1)	3.3	3.6
V_{REF}	1.35	1.5	1.65
V_{TT}	1.35	1.5	1.65
$V_{IH} = V_{REF} + 0.2$	1.55	1.7	-
$V_{IL} = V_{REF} - 0.2$	-	1.3	1.45
$V_{OH} = V_{REF} + 0.4$	1.75	1.9	-
$V_{OL}= V_{REF} - 0.4$	-	1.1	1.25
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL} at V_{OL} (mA)	8	-	-

Notes:
1. Timing delays are calculated based on V_{CCO} min of 3.0V.

PCI33_3 & PCI66_3

PCI33_3 or PCI66_3 require no termination. DC voltage specifications appear in Table 33.

Table 33: **PCI33_3 and PCI66_3 Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
V_{REF}	-	-	-
V_{TT}	-	-	-
$V_{IH} = 0.5 \times V_{CCO}$	1.5	1.65	V_{CCO} + 0.5
$V_{IL} = 0.3 \times V_{CCO}$	–0.5	0.99	1.08
$V_{OH} = 0.9 \times V_{CCO}$	2.7	-	-
$V_{OL}= 0.1 \times V_{CCO}$	-	-	0.36
I_{OH} at V_{OH} (mA)	Note 1	-	-
I_{OL} at V_{OL} (mA)	Note 1	-	-

Notes:
1. Tested according to the relevant specification.

DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Device	Min	Max	Units
V_{DRINT}	Data Retention V_{CCINT} Voltage (below which configuration data might be lost)		All	1.5		V
V_{DRIO}	Data Retention V_{CCO} Voltage (below which configuration data might be lost)		All	1.2		V
I_{CCINTQ}	Quiescent V_{CCINT} supply current (Note 1)		XCV50E		200	mA
			XCV100E		200	mA
			XCV200E		300	mA
			XCV300E		300	mA
			XCV400E		300	mA
			XCV600E		400	mA
			XCV1000E		500	mA
			XCV1600E		500	mA
			XCV2000E		500	mA
			XCV2600E		500	mA
			XCV3200E		500	mA
I_{CCOQ}	Quiescent V_{CCO} supply current (Note 1)		XCV50E		2	mA
			XCV100E		2	mA
			XCV200E		2	mA
			XCV300E		2	mA
			XCV400E		2	mA
			XCV600E		2	mA
			XCV1000E		2	mA
			XCV1600E		2	mA
			XCV2000E		2	mA
			XCV2600E		2	mA
			XCV3200E		2	mA
I_L	Input or output leakage current		All	–10	+10	µA
C_{IN}	Input capacitance (sample tested)	BGA, PQ, HQ, packages	All		8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0 V, V_{CCO} = 3.3 V (sample tested)		All	Note 2	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 3.6 V (sample tested)			Note 2	0.25	mA

Notes:
1. With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating.
2. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.

Table 2: **IOB Input Switching Characteristics *(Continued)***

Description[2]	Symbol	Device	Speed Grade[1] Min	-8	-7	-6	Units
Sequential Delays							
Clock CLK							
Minimum Pulse Width, High	T_{CH}	All	0.56	1.2	1.3	1.4	ns, min
Minimum Pulse Width, Low	T_{CL}		0.56	1.2	1.3	1.4	ns, min
Clock CLK to output IQ	T_{IOCKIQ}		0.18	0.4	0.7	0.7	ns, max
Setup and Hold Times with respect to Clock at IOB Input Register							
Pad, no delay	T_{IOPICK}/ T_{IOICKP}	All	0.69 / 0	1.3 / 0	1.4 / 0	1.5 / 0	ns, min
Pad, with delay	$T_{IOPICKD}$/ $T_{IOICKPD}$	XCV50E	1.25 / 0	2.8 / 0	2.9 / 0	2.9 / 0	ns, min
		XCV100E	1.25 / 0	2.8 / 0	2.9 / 0	2.9 / 0	ns, min
		XCV200E	1.33 / 0	3.0 / 0	3.1 / 0	3.1 / 0	ns, min
		XCV300E	1.33 / 0	3.0 / 0	3.1 / 0	3.1 / 0	ns, min
		XCV400E	1.37 / 0	3.1 / 0	3.2 / 0	3.2 / 0	ns, min
		XCV600E	1.49 / 0	3.4 / 0	3.5 / 0	3.5 / 0	ns, min
		XCV1000E	1.49 / 0	3.4 / 0	3.5 / 0	3.5 / 0	ns, min
		XCV1600E	1.53 / 0	3.5 / 0	3.6 / 0	3.6 / 0	ns, min
		XCV2000E	1.53 / 0	3.5 / 0	3.6 / 0	3.6 / 0	ns, min
		XCV2600E	1.53 / 0	3.5 / 0	3.6 / 0	3.6 / 0	ns, min
		XCV3200E	1.53 / 0	3.5 / 0	3.6 / 0	3.6 / 0	ns, min
ICE input	$T_{IOICECK}$/ $T_{IOCKICE}$	All	0.28 / 0.0	0.55 / 0.01	0.7 / 0.01	0.7 / 0.01	ns, min
SR input (IFF, synchronous)	$T_{IOSRCKI}$	All	0.38	0.8	0.9	1.0	ns, min
Set/Reset Delays							
SR input to IQ (asynchronous)	T_{IOSRIQ}	All	0.54	1.1	1.2	1.4	ns, max
GSR to output IQ	T_{GSRQ}	All	3.88	7.6	8.5	9.7	ns, max

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. Input timing i for LVTTL is measured at 1.4 V. For other I/O standards, see Table 4.

DLL Clock Tolerance, Jitter, and Phase Information

All DLL output jitter and phase specifications determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers.

			CLKDLLHF		CLKDLL		
Description	**Symbol**	**F_{CLKIN}**	**Min**	**Max**	**Min**	**Max**	**Units**
Input Clock Period Tolerance	T_{IPTOL}		-	1.0	-	1.0	ns
Input Clock Jitter Tolerance (Cycle to Cycle)	T_{IJITCC}		-	± 150	-	± 300	ps
Time Required for DLL to Acquire Lock(6)	T_{LOCK}	> 60 MHz	-	20	-	20	µs
		50 - 60 MHz	-	-	-	25	µs
		40 - 50 MHz	-	-	-	50	µs
		30 - 40 MHz	-	-	-	90	µs
		25 - 30 MHz	-	-	-	120	µs
Output Jitter (cycle-to-cycle) for any DLL Clock Output(1)	T_{OJITCC}			± 60		± 60	ps
Phase Offset between CLKIN and CLKO(2)	T_{PHIO}			± 100		± 100	ps
Phase Offset between Clock Outputs on the DLL(3)	T_{PHOO}			± 140		± 140	ps
Maximum Phase Difference between CLKIN and CLKO(4)	T_{PHIOM}			± 160		± 160	ps
Maximum Phase Difference between Clock Outputs on the DLL(5)	T_{PHOOM}			± 200		± 200	ps

Notes:

1. **Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock and is based on a maximum tap delay resolution, *excluding* input clock jitter.
2. **Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* Output Jitter and input clock jitter.
3. **Phase Offset between Clock Outputs on the DLL** is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* Output Jitter and input clock jitter.
4. **Maximum Phase Difference between CLKIN an CLKO** is the sum of Output Jitter and Phase Offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).
5. **Maximum Phase DIfference between Clock Outputs on the DLL** is the sum of Output JItter and Phase Offset between any DLL clock outputs, or the greatest difference between any two DLL output rising edges sue to DLL alone (*excluding* input clock jitter).
6. Add 30% to the value for industrial grade parts.

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P210	GCK2	1
P209	IO_LVDS_DLL_L6P	1
P208	IO_VREF	1
P207	VCCO	1
P206	IO_L7N_Y	1
P205	IO_VREF_L7P_Y	1
P204	GND	NA
P203	IO_L8N_Y	1
P202	IO_L8P_Y	1
P201[1]	IO_VREF	1
P200	IO_L9N_YY	1
P199	IO_L9P_YY	1
P198	VCCINT	NA
P197	VCCO	1
P196	GND	NA
P195	IO_L10N_YY	1
P194	IO_VREF_L10P_YY	1
P193	IO_VREF	1
P192	IO_L11N_YY	1
P191	IO_VREF_L11P_YY	1
P190	GND	NA
P189	IO_L12N_YY	1
P188	IO_L12P_YY	1
P187	IO_VREF_L13N	1
P186	IO_L13P	1
P185	IO_WRITE_L14N_YY	1
P184	IO_CS_L14P_YY	1
P183	TDI	NA
P182	GND	NA
P181	TDO	2
P180	VCCO	1
P179	CCLK	2
P178	IO_DOUT_BUSY_L15P_YY	2
P177	IO_DIN_D0_L15N_YY	2
P176	VCCO	2
P175	IO_VREF	2

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P174	IO_L16P_Y	2
P173	IO_L16N_Y	2
P172	GND	NA
P171	IO_VREF_L17P_Y	2
P170	IO_L17N_Y	2
P169	IO_VREF	2
P168	IO_VREF_L18P_Y	2
P167	IO_D1_L18N_Y	2
P166	GND	NA
P165	VCCO	2
P164	VCCINT	NA
P163	IO_D2_L19P_YY	2
P162	IO_L19N_YY	2
P161[1]	IO_VREF	2
P160	IO_L20P_Y	2
P159	IO_L20N_Y	2
P158	GND	NA
P157	IO_VREF_L21P_Y	2
P156	IO_D3_L21N_Y	2
P155	IO_L22P_Y	2
P154	IO_VREF_L22N_Y	2
P153	IO_L23P_YY	2
P152	IO_L23N_YY	2
P151	GND	NA
P150	VCCO	2
P149	IO	3
P148	VCCINT	NA
P147	IO_VREF	3
P146	VCCO	3
P145	IO_D4_L24P_Y	3
P144	IO_VREF_L24N_Y	3
P143	GND	NA
P142	IO_L25P_Y	3
P141	IO_L25N_Y	3
P140[1]	IO_VREF	3
P139	IO_L26P_YY	3

Table 12: **BG432 — XCV300E, XCV400E, XCV600E**

Bank	Pin Description	Pin #
0	IO_L12N_YY	A20
0	IO_L12P_YY	D19
0	IO_VREF_L13N_YY	B19
0	IO_L13P_YY	A19
0	IO_L14N_Y	B18
0	IO_L14P_Y	D18
0	IO_VREF_L15N_Y	C18[2]
0	IO_L15P_Y	B17
0	IO_LVDS_DLL_L16N	C17
1	GCK2	A16
1	IO	A12
1	IO	B9
1	IO	B11
1	IO	C16
1	IO	D9
1	IO_LVDS_DLL_L16P	B16
1	IO_L17N_Y	A15
1	IO_VREF_L17P_Y	B15[2]
1	IO_L18N_Y	C15
1	IO_L18P_Y	D15
1	IO_L19N_YY	B14
1	IO_VREF_L19P_YY	A13
1	IO_L20N_YY	B13
1	IO_L20P_YY	D14
1	IO_L21N_YY	C13
1	IO_L21P_YY	B12
1	IO_L22N_YY	D13
1	IO_L22P_YY	C12
1	IO_L23N_YY	D12
1	IO_L23P_YY	C11
1	IO_L24N_YY	B10
1	IO_VREF_L24P_YY	C10
1	IO_L25N_Y	C9
1	IO_VREF_L25P_Y	D10[1]
1	IO_L26N_Y	A8

Table 12: **BG432 — XCV300E, XCV400E, XCV600E**

Bank	Pin Description	Pin #
1	IO_L26P_Y	B8
1	IO_L27N_YY	C8
1	IO_VREF_L27P_YY	B7
1	IO_L28N_YY	D8
1	IO_L28P_YY	A6
1	IO_L29N_Y	B6
1	IO_L29P_Y	D7
1	IO_L30N_YY	A5
1	IO_VREF_L30P_YY	C6
1	IO_L31N_YY	B5
1	IO_L31P_YY	D6
1	IO_L32N_Y	A4
1	IO_L32P_Y	C5
1	IO_WRITE_L33N_YY	B4
1	IO_CS_L33P_YY	D5
2	IO	H4
2	IO	J3
2	IO	L3
2	IO	M1
2	IO	R2
2	IO_DOUT_BUSY_L34P_YY	D3
2	IO_DIN_D0_L34N_YY	C2
2	IO_L35P	D2
2	IO_L35N	E4
2	IO_L36P_Y	D1
2	IO_L36N_Y	E3
2	IO_VREF_L37P_Y	E2
2	IO_L37N_Y	F4
2	IO_L38P	E1
2	IO_L38N	F3
2	IO_L39P_Y	F2
2	IO_L39N_Y	G4
2	IO_VREF_L40P_YY	G3
2	IO_L40N_YY	G2
2	IO_L41P_Y	H3

Table 16: **FG256 Package — XCV50E, XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
4	IO_L43P_Y	P12
4	IO_VREF_L43N_Y	R13[2]
4	IO_L44P_YY	N12
4	IO_L44N_YY	T13
4	IO_VREF_L45P_YY	T12
4	IO_L45N_YY	P11
4	IO_L46P_Y	R12
4	IO_L46N_Y	N11
4	IO_VREF_L47P_YY	T11[1]
4	IO_L47N_YY	M11
4	IO_L48P_YY	R11
4	IO_L48N_YY	T10
4	IO_L49P_Y	R10
4	IO_L49N_Y	M10
4	IO_VREF_L50P_Y	P9
4	IO_L50N_Y	T9
4	IO_L51P_Y	N10
4	IO_L51N_Y	R9
4	IO_LVDS_DLL_L52P	N9
5	GCK1	R8
5	IO	N7
5	IO	T7
5	IO_LVDS_DLL_L52N	T8
5	IO_L53P_Y	R7
5	IO_VREF_L53N_Y	P8
5	IO_L54P_Y	P7
5	IO_L54N_Y	T6
5	IO_L55P_YY	M7
5	IO_L55N_YY	R6
5	IO_L56P_YY	P6
5	IO_VREF_L56N_YY	R5[1]
5	IO_L57P_Y	N6
5	IO_L57N_Y	T5
5	IO_L58P_YY	M6

Table 16: **FG256 Package — XCV50E, XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
5	IO_VREF_L58N_YY	T4
5	IO_L59P_YY	T3
5	IO_L59N_YY	P5
5	IO_VREF_L60P_Y	T2[2]
5	IO_L60N_Y	N5
6	IO_L61N_YY	M3
6	IO_L61P_YY	R1
6	IO_L62N	M4
6	IO_VREF_L62P	N2[2]
6	IO_L63N_YY	L5
6	IO_L63P_YY	P1
6	IO_VREF_L64N_Y	N1
6	IO_L64P_Y	L3
6	IO_L65N	M2
6	IO_L65P	L4
6	IO_VREF_L66N_Y	M1[1]
6	IO_L66P_Y	K4
6	IO_L67N_YY	L2
6	IO_L67P_YY	L1
6	IO_L68N	K3
6	IO_L68P	K1
6	IO_L69N_YY	K2
6	IO_L69P_YY	K5
6	IO_VREF_L70N_Y	J3
6	IO_L70P_Y	J1
6	IO_L71N	J4
6	IO_L71P	H1
6	IO	J2
7	IO	C2
7	IO_L72N_YY	G1
7	IO_L72P_YY	H4
7	IO_L73N	G5
7	IO_L73P	H2

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
NA	VCCINT	T15
NA	VCCINT	T16
NA	VCCINT	U6
NA	VCCINT	U17
NA	VCCINT	V5
NA	VCCINT	V18
NA	VCCO_7	L7
NA	VCCO_7	K7
NA	VCCO_7	K6
NA	VCCO_7	J6
NA	VCCO_7	H6
NA	VCCO_7	G6
NA	VCCO_6	N7
NA	VCCO_6	M7
NA	VCCO_6	T6
NA	VCCO_6	R6
NA	VCCO_6	P6
NA	VCCO_6	N6
NA	VCCO_5	U10
NA	VCCO_5	U9
NA	VCCO_5	U8
NA	VCCO_5	U7
NA	VCCO_5	T11
NA	VCCO_5	T10
NA	VCCO_4	U16
NA	VCCO_4	U15
NA	VCCO_4	U14
NA	VCCO_4	U13
NA	VCCO_4	T13
NA	VCCO_4	T12
NA	VCCO_3	T17
NA	VCCO_3	R17
NA	VCCO_3	P17
NA	VCCO_3	N17
NA	VCCO_3	N16
NA	VCCO_3	M16

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
NA	VCCO_2	K17
NA	VCCO_2	J17
NA	VCCO_2	H17
NA	VCCO_2	G17
NA	VCCO_2	L16
NA	VCCO_2	K16
NA	VCCO_1	G13
NA	VCCO_1	G12
NA	VCCO_1	F16
NA	VCCO_1	F15
NA	VCCO_1	F14
NA	VCCO_1	F13
NA	VCCO_0	G11
NA	VCCO_0	G10
NA	VCCO_0	F10
NA	VCCO_0	F9
NA	VCCO_0	F8
NA	VCCO_0	F7
NA	GND	AB22
NA	GND	AB1
NA	GND	AA21
NA	GND	AA2
NA	GND	Y20
NA	GND	Y3
NA	GND	P14
NA	GND	P13
NA	GND	P12
NA	GND	P11
NA	GND	P10
NA	GND	P9
NA	GND	N14
NA	GND	N13
NA	GND	N12
NA	GND	N11
NA	GND	N10
NA	GND	N9

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
0	IO_VREF_L27N_YY	D27
0	IO_L27P_YY	B25
0	IO_L28N_Y	A25
0	IO_L28P_Y	D26
0	IO_L29N_Y	A24
0	IO_L29P_Y	E25
0	IO_L30N_YY	D25
0	IO_L30P_YY	B24
0	IO_VREF_L31N_YY	E24
0	IO_L31P_YY	A23
0	IO_L32N_Y	C23
0	IO_L32P_Y	E23
0	IO_VREF_L33N_Y	B23[1]
0	IO_L33P_Y	D23
0	IO_LVDS_DLL_L34N	A22
1	GCK2	B22
1	IO	A14
1	IO	A20
1	IO	B11
1	IO	B13
1	IO	C8
1	IO	C18
1	IO	C21
1	IO	D7
1	IO	D10
1	IO	D15
1	IO	D17
1	IO	E20
1	IO_LVDS_DLL_L34P	D22
1	IO_L35N_Y	D21
1	IO_VREF_L35P_Y	B21[1]
1	IO_L36N_Y	D20
1	IO_L36P_Y	A21
1	IO_L37N_YY	C20
1	IO_VREF_L37P_YY	D19
1	IO_L38N_YY	B20

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
1	IO_L38P_YY	E19
1	IO_L39N_Y	D18
1	IO_L39P_Y	A19
1	IO_L40N_Y	E18
1	IO_L40P_Y	C19
1	IO_L41N_YY	B19
1	IO_VREF_L41P_YY	E17
1	IO_L42N_YY	A18
1	IO_L42P_YY	D16
1	IO_L43N_Y	E16
1	IO_L43P_Y	B18
1	IO_L44N_Y	F16
1	IO_L44P_Y	A17
1	IO_L45N_YY	C17
1	IO_VREF_L45P_YY	E15
1	IO_L46N_YY	B17
1	IO_L46P_YY	D14
1	IO_L47N_Y	A16
1	IO_L47P_Y	E14
1	IO_L48N_Y	C16
1	IO_L48P_Y	D13
1	IO_L49N_Y	B16
1	IO_L49P_Y	D12
1	IO_L50N_Y	A15
1	IO_L50P_Y	E12
1	IO_L51N_YY	C15
1	IO_L51P_YY	C11
1	IO_L52N_YY	B15
1	IO_VREF_L52P_YY	D11
1	IO_L53N_Y	E11
1	IO_L53P_Y	C14
1	IO_L54N_Y	C10
1	IO_L54P_Y	B14
1	IO_L55N_YY	A13
1	IO_VREF_L55P_YY	E10
1	IO_L56N_YY	C13
1	IO_L56P_YY	C9

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
1	IO_L57N_Y	D9
1	IO_VREF_L57P_Y	A12[2]
1	IO_L58N_Y	E9
1	IO_L58P_Y	C12
1	IO_L59N_YY	B12
1	IO_VREF_L59P_YY	D8
1	IO_L60N_YY	A11
1	IO_L60P_YY	E8
1	IO_L61N_Y	C7
1	IO_L61P_Y	A10
1	IO_L62N_Y	C6
1	IO_L62P_Y	B10
1	IO_L63N_YY	A9
1	IO_VREF_L63P_YY	B9
1	IO_L64N_YY	A8
1	IO_L64P_YY	E7
1	IO_L65N_Y	B8
1	IO_L65P_Y	C5
1	IO_L66N_Y	A7
1	IO_VREF_L66P_Y	A6
1	IO_L67N_Y	B7
1	IO_L67P_Y	D6
1	IO_L68N_Y	A5
1	IO_L68P_Y	C4
1	IO_WRITE_L69N_YY	B6
1	IO_CS_L69P_YY	E6
2	IO	H2
2	IO	H3
2	IO	J1
2	IO	K5
2	IO	M2
2	IO	N1
2	IO	R5
2	IO	U1
2	IO	U4
2	IO	W3
2	IO	Y3
2	IO	AA3
2	IO_DOUT_BUSY_L70P_YY	F5
2	IO_DIN_D0_L70N_YY	D2
2	IO_L71P_Y	E4
2	IO_L71N_Y	E2
2	IO_L72P_Y	D3
2	IO_L72N_Y	F2
2	IO_VREF_L73P_Y	E1
2	IO_L73N_Y	F4
2	IO_L74P	G2
2	IO_L74N	E3
2	IO_L75P_Y	F1
2	IO_L75N_Y	G5
2	IO_VREF_L76P_Y	G1
2	IO_L76N_Y	F3
2	IO_L77P_YY	G4
2	IO_L77N_YY	H1
2	IO_L78P_Y	J2
2	IO_L78N_Y	G3
2	IO_L79P_Y	H5
2	IO_L79N_Y	K2
2	IO_VREF_L80P_YY	H4
2	IO_L80N_YY	K1
2	IO_L81P_YY	L2
2	IO_L81N_YY	L3
2	IO_VREF_L82P_Y	L1[2]
2	IO_L82N_Y	J5
2	IO_L83P_Y	J4
2	IO_L83N_Y	M3
2	IO_VREF_L84P_YY	J3
2	IO_L84N_YY	M1
2	IO_L85P_YY	N2
2	IO_L85N_YY	K4
2	IO_L86P_Y	N3
2	IO_L86N_Y	K3
2	IO_VREF_L87P_YY	L5

FG860 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 25: **FG860 Differential Pin Pair Summary XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
3	0	C22	A22	NA	IO_DLL_L34N
2	1	B22	D22	NA	IO_DLL_L34P
1	5	AY22	AW21	NA	IO_DLL_L176N
0	4	BA22	AW20	NA	IO_DLL_L176P
IO LVDS Total Pairs: 281, Asynchronous Output Pairs: 111					
0	0	D38	A38	2	-
1	0	E37	B37	1	-
2	0	C39	A37	1	VREF
3	0	C38	B36	1	-
4	0	B35	A36	√	-
5	0	D37	A35	√	VREF
6	0	A34	C37	5	-
7	0	B33	E36	5	-
8	0	C32	A33	√	-
9	0	B32	C36	√	VREF
10	0	D35	A32	1	-
11	0	C35	C31	1	VREF
12	0	A31	E34	√	-
13	0	C30	D34	√	VREF
14	0	E33	B30	2	-
15	0	D33	A30	2	-
16	0	B29	C33	√	VREF
17	0	A29	E32	√	-

Table 25: **FG860 Differential Pin Pair Summary XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
18	0	C28	D32	2	-
19	0	B28	E31	1	-
20	0	A28	D31	1	-
21	0	C27	D30	5	-
22	0	B27	E29	√	-
23	0	A27	D29	√	VREF
24	0	D28	C26	5	-
25	0	F27	B26	5	-
26	0	C25	E27	√	-
27	0	B25	D27	√	VREF
28	0	D26	A25	1	-
29	0	E25	A24	1	-
30	0	B24	D25	√	-
31	0	A23	E24	√	VREF
32	0	E23	C23	2	-
33	0	D23	B23	2	VREF
34	1	D22	A22	NA	IO_LVDS_DLL
35	1	B21	D21	2	VREF
36	1	A21	D20	2	-
37	1	D19	C20	√	VREF
38	1	E19	B20	√	-
39	1	A19	D18	1	-
40	1	C19	E18	1	-
41	1	E17	B19	√	VREF
42	1	D16	A18	√	-
43	1	B18	E16	5	-
44	1	A17	F16	5	-
45	1	E15	C17	√	VREF
46	1	D14	B17	√	-
47	1	E14	A16	5	-
48	1	D13	C16	1	-
49	1	D12	B16	1	-
50	1	E12	A15	2	-
51	1	C11	C15	√	-

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
2	IO_L99P_YY	N26
2	IO_L99N_YY	P28
2	IO_L100P	P29
2	IO_L100N	N24
2	IO_L101P_YY	P22
2	IO_L101N_YY	R26
2	IO_VREF_L102P_YY	P25
2	IO_L102N_YY	R29
2	IO_L103P_YY	R21[4]
2	IO_L103N_YY	R28[3]
2	IO_VREF_L104P_YY	R25[2]
2	IO_L104N_YY	T30
2	IO_L105P_YY	P24[4]
2	IO_L105N_YY	R27[3]
2	IO_L106P	R24
3	IO	T22[4]
3	IO	T24[4]
3	IO	T26[4]
3	IO	T29[4]
3	IO	U26[5]
3	IO	V23[4]
3	IO	V25[4]
3	IO	V30[5]
3	IO	Y21[4]
3	IO	AA26[4]
3	IO	AA23[4]
3	IO	AB27[4]
3	IO	AB29[4]
3	IO	AC28[5]
3	IO	AD26[4]
3	IO	AD29[5]
3	IO	AE27[5]
3	IO_L106N	U29
3	IO_L107P_YY	R22
3	IO_VREF_L107N_YY	T27[2]
3	IO_L108P_YY	R23

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
3	IO_L108N_YY	T28
3	IO_L109P_YY	T21
3	IO_VREF_L109N_YY	T25
3	IO_L110P_YY	U28
3	IO_L110N_YY	U30
3	IO_L111P	T23
3	IO_L111N	U27
3	IO_L112P_YY	U25
3	IO_L112N_YY	V27
3	IO_D4_L113P_YY	U24
3	IO_VREF_L113N_YY	V29
3	IO_L114P	W30
3	IO_L114N	U22
3	IO_L115P_YY	U21
3	IO_L115N_YY	W29
3	IO_L116P_YY	V26
3	IO_L116N_YY	W27
3	IO_L117P	W26
3	IO_VREF_L117N	Y29[1]
3	IO_L118P_YY	W25
3	IO_L118N_YY	Y30
3	IO_L119P_Y	V24[4]
3	IO_L119N_Y	Y28[4]
3	IO_L120P_YY	AA30
3	IO_L120N_YY	W24
3	IO_L121P	AA29
3	IO_L121N	V20
3	IO_L122P	Y27[4]
3	IO_L122N	W23[4]
3	IO_L123P_YY	Y26
3	IO_D5_L123N_YY	AB30
3	IO_D6_L124P_YY	V21
3	IO_VREF_L124N_YY	AA28
3	IO_L125P_YY	Y25
3	IO_L125N_YY	AA27
3	IO_L126P_YY	W22
3	IO_L126N_YY	Y23

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
0	IO_L40P_Y	A17
0	IO_VREF_L41N_Y	G17[1]
0	IO_L41P_Y	B17
0	IO_LVDS_DLL_L42N	C17
1	GCK2	D17
1	IO	A18
1	IO	B18[3]
1	IO	B24
1	IO	B25
1	IO	E22[3]
1	IO	E23[3]
1	IO	D18[3]
1	IO	D19
1	IO	D25[3]
1	IO	D26[3]
1	IO	D28[3]
1	IO	D29[3]
1	IO	G23[3]
1	IO	J23[3]
1	IO_LVDS_DLL_L42P	J18
1	IO_L43N_Y	G18
1	IO_VREF_L43P_Y	C18[1]
1	IO_L44N_Y	H18
1	IO_L44P_Y	F18
1	IO_L45N_YY	B19
1	IO_VREF_L45P_YY	A19
1	IO_L46N_YY	K19
1	IO_L46P_YY	C19
1	IO_L47N	F19[5]
1	IO_L47P	E19[4]
1	IO_L48N_Y	G19
1	IO_L48P_Y	J19
1	IO_L49N_Y	A20

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
1	IO_L49P_Y	G20
1	IO_L50N	B20[5]
1	IO_L50P	F20[4]
1	IO_L51N_YY	D20
1	IO_VREF_L51P_YY	E20
1	IO_L52N_YY	H20
1	IO_L52P_YY	A21
1	IO_L53N	E21[5]
1	IO_L53P	J20[4]
1	IO_L54N_Y	D21
1	IO_L54P_Y	K20
1	IO_L55N_Y	B21
1	IO_L55P_Y	H21
1	IO_L56N_YY	G21[5]
1	IO_L56P_YY	F21[4]
1	IO_L57N_YY	A22
1	IO_VREF_L57P_YY	B22
1	IO_L58N_YY	J21
1	IO_L58P_YY	C22
1	IO_L59N_Y	D22
1	IO_L59P_Y	G22
1	IO_L60N_Y	K21
1	IO_L60P_Y	A23
1	IO_L61N_Y	F22
1	IO_L61P_Y	B23
1	IO_L62N_Y	C23
1	IO_L62P_Y	H22
1	IO_L63N_YY	D23
1	IO_L63P_YY	K22
1	IO_L64N_YY	A24
1	IO_VREF_L64P_YY	J22
1	IO_L65N_Y	H23
1	IO_L65P_Y	D24
1	IO_L66N_Y	A25

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
2	IO_L92N_Y	H29
2	IO_L93P_YY	J28[4]
2	IO_L93N_YY	E33[5]
2	IO_L94P_YY	H28
2	IO_L94N_YY	H30
2	IO_L95P_Y	H32
2	IO_L95N_Y	K28
2	IO_L96P_Y	L27[4]
2	IO_L96N_Y	F33[5]
2	IO_L97P_Y	M26
2	IO_L97N_Y	E34
2	IO_VREF_L98P_YY	H31
2	IO_L98N_YY	G32
2	IO_L99P_YY	N25[4]
2	IO_L99N_YY	J31[5]
2	IO_L100P_YY	J30
2	IO_L100N_YY	G33
2	IO_VREF_L101P_Y	H34[2]
2	IO_L101N_Y	J29
2	IO_L102P	M27[4]
2	IO_L102N	H33[5]
2	IO_L103P_Y	K29
2	IO_L103N_Y	J34
2	IO_VREF_L104P_YY	L29
2	IO_L104N_YY	J33
2	IO_L105P_YY	M28
2	IO_L105N_YY	K34
2	IO_L106P_Y	N27
2	IO_L106N_Y	L34
2	IO_VREF_L107P_YY	K33
2	IO_D1_L107N_YY	P26
2	IO_L108P_Y	R25
2	IO_L108N_Y	M34
2	IO_L109P_Y	L31

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
2	IO_L109N_Y	L33
2	IO_L110P_Y	P27
2	IO_L110N_Y	M33
2	IO_L111P	M31
2	IO_L111N	R26
2	IO_L112P_Y	N30
2	IO_L112N_Y	P28
2	IO_VREF_L113P_Y	N29
2	IO_L113N_Y	N33
2	IO_L114P_YY	T25[4]
2	IO_L114N_YY	N34[5]
2	IO_L115P_YY	P34
2	IO_L115N_YY	R27
2	IO_L116P_Y	P29
2	IO_L116N_Y	P31
2	IO_L117P_Y	P33[4]
2	IO_L117N_Y	T26[5]
2	IO_L118P_Y	R34
2	IO_L118N_Y	R28
2	IO_VREF_L119P_YY	N31
2	IO_D3_L119N_YY	N32
2	IO_L120P_YY	P30[4]
2	IO_L120N_YY	R33[5]
2	IO_L121P_YY	R29
2	IO_L121N_YY	T34
2	IO_L122P_Y	R30
2	IO_L122N_Y	T30
2	IO_L123P	T28[4]
2	IO_L123N	R31[5]
2	IO_L124P_Y	T29
2	IO_L124N_Y	U27
2	IO_VREF_L125P_YY	T31
2	IO_L125N_YY	T33
2	IO_L126P_YY	U28

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
2	IO_L126N_YY	T32
2	IO_VREF_L127P_Y	U29[1]
2	IO_L127N_Y	U33
2	IO_L128P_YY	V33
2	IO_L128N_YY	U31
3	IO	V27[3]
3	IO	V31
3	IO	V32[3]
3	IO	W33
3	IO	AB25[3]
3	IO	AB26[3]
3	IO	AB31[3]
3	IO	AC31[3]
3	IO	AF34
3	IO	AG31[3]
3	IO	AG33[3]
3	IO	AG34
3	IO	AH29[3]
3	IO	AJ30[3]
3	IO_L129P_Y	V26
3	IO_VREF_L129N_Y	V30[1]
3	IO_L130P_YY	W34
3	IO_L130N_YY	V28
3	IO_L131P_YY	W32
3	IO_VREF_L131N_YY	W30
3	IO_L132P_Y	V29
3	IO_L132N_Y	Y34
3	IO_L133P	W29[5]
3	IO_L133N	Y33[4]
3	IO_L134P_Y	W26
3	IO_L134N_Y	W28
3	IO_L135P_YY	Y31
3	IO_L135N_YY	Y30

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
3	IO_L136P_YY	AA34[5]
3	IO_L136N_YY	W31[4]
3	IO_D4_L137P_YY	AA33
3	IO_VREF_L137N_YY	Y29
3	IO_L138P_Y	W25
3	IO_L138N_Y	AB34
3	IO_L139P_Y	Y28[5]
3	IO_L139N_Y	AB33[4]
3	IO_L140P_Y	AA30
3	IO_L140N_Y	Y26
3	IO_L141P_YY	Y27
3	IO_L141N_YY	AA31
3	IO_L142P_YY	AA27[5]
3	IO_L142N_YY	AA29[4]
3	IO_L143P_Y	AB32
3	IO_VREF_L143N_Y	AB29
3	IO_L144P_Y	AA28
3	IO_L144N_Y	AC34
3	IO_L145P	Y25
3	IO_L145N	AD34
3	IO_L146P_Y	AB30
3	IO_L146N_Y	AC33
3	IO_L147P_Y	AA26
3	IO_L147N_Y	AC32
3	IO_L148P_Y	AD33
3	IO_L148N_Y	AB28
3	IO_L149P_YY	AE34
3	IO_D5_L149N_YY	AB27
3	IO_D6_L150P_YY	AE33
3	IO_VREF_L150N_YY	AC30
3	IO_L151P_Y	AA25
3	IO_L151N_Y	AE32
3	IO_L152P_YY	AE31
3	IO_L152N_YY	AD29

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
3	IO_L153P_YY	AD31
3	IO_VREF_L153N_YY	AF33
3	IO_L154P_Y	AC28
3	IO_L154N_Y	AF31
3	IO_L155P_Y	AC27[5]
3	IO_L155N_Y	AF32[4]
3	IO_L156P_Y	AE29
3	IO_VREF_L156N_Y	AD28[2]
3	IO_L157P_YY	AD30
3	IO_L157N_YY	AG32
3	IO_L158P_YY	AC26[5]
3	IO_L158N_YY	AH33[4]
3	IO_L159P_YY	AD26
3	IO_VREF_L159N_YY	AF30
3	IO_L160P_Y	AC25
3	IO_L160N_Y	AH32
3	IO_L161P_Y	AE28[5]
3	IO_L161N_Y	AL34[4]
3	IO_L162P_Y	AG30
3	IO_L162N_Y	AD27
3	IO_L163P_YY	AF29
3	IO_L163N_YY	AK34
3	IO_L164P_YY	AD25[5]
3	IO_L164N_YY	AE27[4]
3	IO_L165P_Y	AJ33
3	IO_VREF_L165N_Y	AH31
3	IO_L166P_Y	AE26
3	IO_L166N_Y	AL33
3	IO_L167P	AF28
3	IO_L167N	AL32
3	IO_L168P_Y	AJ31
3	IO_VREF_L168N_Y	AF27
3	IO_L169P_Y	AG29
3	IO_L169N_Y	AJ32

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
3	IO_L170P_Y	AK33
3	IO_L170N_Y	AH30
3	IO_D7_L171P_YY	AK32
3	IO_INIT_L171N_YY	AK31
3	IO	V34
4	GCK0	AH18
4	IO	AE21[3]
4	IO	AG18
4	IO	AG23
4	IO	AH24[3]
4	IO	AH25[3]
4	IO	AJ28[3]
4	IO	AK18[3]
4	IO	AK19[3]
4	IO	AL25
4	IO	AL27[3]
4	IO	AL30[3]
4	IO	AN18
4	IO	AN22[3]
4	IO	AN24[3]
4	IO_L172P_YY	AP31
4	IO_L172N_YY	AK29
4	IO_L173P_Y	AP30
4	IO_L173N_Y	AN31
4	IO_L174P_Y	AH27
4	IO_L174N_Y	AN30
4	IO_VREF_L175P_Y	AM30
4	IO_L175N_Y	AK28
4	IO_L176P_Y	AG26
4	IO_L176N_Y	AN29
4	IO_L177P_YY	AF25
4	IO_L177N_YY	AM29
4	IO_VREF_L178P_YY	AL29

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
6	IO_VREF_L299N_YY	W5
6	IO_L299P_YY	V1
6	IO_L300N_YY	V7
6	IO_L300P_YY	U2
6	IO_VREF_L301N_Y	V6[1]
6	IO_L301P_Y	U1
7	IO	F5
7	IO	G6[3]
7	IO	H1
7	IO	H7[3]
7	IO	K2[3]
7	IO	K4[3]
7	IO	L6[3]
7	IO	M5[3]
7	IO	M10[3]
7	IO	N5[3]
7	IO	N10
7	IO	R7[4]
7	IO	T2
7	IO	T7[3]
7	IO	U8
7	IO	V4[3]
7	IO_L302N_YY	U9
7	IO_L302P_YY	U4
7	IO_L303N_Y	U7
7	IO_VREF_L303P_Y	U5[1]
7	IO_L304N_YY	U3
7	IO_L304P_YY	U6
7	IO_L305N_YY	T3
7	IO_VREF_L305P_YY	T6
7	IO_L306N_Y	T9
7	IO_L306P_Y	T4
7	IO_L307N_Y	T5[5]

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
7	IO_L307P_Y	R1[4]
7	IO_L308N_Y	R6
7	IO_L308P_Y	T10
7	IO_L309N_YY	R2
7	IO_L309P_YY	R5
7	IO_L310N_YY	P1
7	IO_VREF_L310P_YY	P5
7	IO_L311N_Y	R8
7	IO_L311P_Y	P2
7	IO_L312N_Y	R9[5]
7	IO_L312P_Y	N1[4]
7	IO_L313N_Y	P4
7	IO_L313P_Y	R10
7	IO_L314N_YY	P8
7	IO_L314P_YY	N2
7	IO_L315N_YY	P6[5]
7	IO_L315P_YY	P7[4]
7	IO_L316N_Y	M1
7	IO_VREF_L316P_Y	N4
7	IO_L317N_Y	N6
7	IO_L317P_Y	N3
7	IO_L318N	P9
7	IO_L318P	M2
7	IO_L319N_Y	N7
7	IO_L319P_Y	M3
7	IO_L320N_Y	P10
7	IO_L320P_Y	M4
7	IO_L321N_Y	L1
7	IO_L321P_Y	N8
7	IO_L322N_YY	L2
7	IO_L322P_YY	N9
7	IO_L323N_YY	M7
7	IO_VREF_L323P_YY	K1
7	IO_L324N_Y	M8

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/7/99	1.0	Initial Xilinx release.
1/10/00	1.1	Re-released with spd.txt v. 1.18, FG860/900/1156 package information, and additional DLL, Select RAM and SelectI/O information.
1/28/00	1.2	Added Delay Measurement Methodology table, updated SelectI/O section, Figures 30, 54, & 55, text explaining Table 5, T_{BYP} values, buffered Hex Line info, p. 8, I/O Timing Measurement notes, notes for Tables 15, 16, and corrected F1156 pinout table footnote references.
2/29/00	1.3	Updated pinout tables, V_{CC} page 20, and corrected Figure 20.
5/23/00	1.4	Correction to table on p. 22.
7/10/00	1.5	• Numerous minor edits. • Data sheet upgraded to Preliminary. • Preview -8 numbers added to **Virtex-E Electrical Characteristics** tables.
8/1/00	1.6	• Reformatted entire document to follow new style guidelines. • Changed speed grade values in tables on pages 35-37.
9/20/00	1.7	• Min values added to **Virtex-E Electrical Characteristics** tables. • XCV2600E and XCV3200E numbers added to **Virtex-E Electrical Characteristics** tables (Module 3). • Corrected user I/O count for XCV100E device in Table 1 (Module 1). • Changed several pins to “No Connect in the XCV100E“ and removed duplicate V_{CCINT} pins in Table ~ (Module 4). • Changed pin J10 to “No connect in XCV600E” in Table 74 (Module 4). • Changed pin J30 to “V_{REF} or I/O option only in the XCV600E” in Table 74 (Module 4). • Corrected pair 18 in Table 75 (Module 4) to be “AO in the XCV1000E, XCV1600E“.
11/20/00	1.8	• Upgraded speed grade -8 numbers in **Virtex-E Electrical Characteristics** tables to Preliminary. • Updated minimums in Table 13 and added notes to Table 14. • Added to note 2 to **Absolute Maximum Ratings**. • Changed speed grade -8 numbers for $T_{SHCKO32}$, T_{REG}, T_{BCCS}, and T_{ICKOF}. • Changed all minimum hold times to –0.4 under **Global Clock Set-Up and Hold for LVTTL Standard, with DLL**. • Revised maximum T_{DLLPW} in -6 speed grade for **DLL Timing Parameters**. • Changed GCLK0 to BA22 for FG860 package in Table 46.
2/12/01	1.9	• Revised footnote for Table 14. • Added numbers to **Virtex-E Electrical Characteristics** tables for XCV1000E and XCV2000E devices. • Updated Table 27 and Table 78 to include values for XCV400E and XCV600E devices. • Revised Table 62 to include pinout information for the XCV400E and XCV600E devices in the BG560 package. • Updated footnotes 1 and 2 for Table 76 to include XCV2600E and XCV3200E devices.