AMD Xilinx - XCV200E-7BG352I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	1176
Number of Logic Elements/Cells	5292
Total RAM Bits	114688
Number of I/O	260
Number of Gates	306393
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	352-LBGA Exposed Pad, Metal
Supplier Device Package	352-MBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv200e-7bg352i

Table 1: **Virtex-E Field-Programmable Gate Array Family Members**

Device	System Gates	Logic Gates	CLB Array	Logic Cells	Differential I/O Pairs	User I/O	BlockRAM Bits	Distributed RAM Bits
XCV50E	71,693	20,736	16 x 24	1,728	83	176	65,536	24,576
XCV100E	128,236	32,400	20 x 30	2,700	83	196	81,920	38,400
XCV200E	306,393	63,504	28 x 42	5,292	119	284	114,688	75,264
XCV300E	411,955	82,944	32 x 48	6,912	137	316	131,072	98,304
XCV400E	569,952	129,600	40 x 60	10,800	183	404	163,840	153,600
XCV600E	985,882	186,624	48 x 72	15,552	247	512	294,912	221,184
XCV1000E	1,569,178	331,776	64 x 96	27,648	281	660	393,216	393,216
XCV1600E	2,188,742	419,904	72 x 108	34,992	344	724	589,824	497,664
XCV2000E	2,541,952	518,400	80 x 120	43,200	344	804	655,360	614,400
XCV2600E	3,263,755	685,584	92 x 138	57,132	344	804	753,664	812,544
XCV3200E	4,074,387	876,096	104 x 156	73,008	344	804	851,968	1,038,336

Virtex-E Compared to Virtex Devices

The Virtex-E family offers up to 43,200 logic cells in devices up to 30% faster than the Virtex family.

I/O performance is increased to 622 Mb/s using Source Synchronous data transmission architectures and synchronous system performance up to 240 MHz using singled-ended SelectI/O technology. Additional I/O standards are supported, notably LVPECL, LVDS, and BLVDS, which use two pins per signal. Almost all signal pins can be used for these new standards.

Virtex-E devices have up to 640 Kb of faster (250 MHz) block SelectRAM, but the individual RAMs are the same size and structure as in the Virtex family. They also have eight DLLs instead of the four in Virtex devices. Each individual DLL is slightly improved with easier clock mirroring and 4x frequency multiplication.

V_{CCINT}, the supply voltage for the internal logic and memory, is 1.8 V, instead of 2.5 V for Virtex devices. Advanced processing and 0.18 μm design rules have resulted in smaller dice, faster speed, and lower power consumption.

I/O pins are 3 V tolerant, and can be 5 V tolerant with an external 100 Ω resistor. PCI 5 V is not supported. With the addition of appropriate external resistors, any pin can tolerate any voltage desired.

Banking rules are different. With Virtex devices, all input buffers are powered by V_{CCINT}. With Virtex-E devices, the LVTTL, LVCMOS2, and PCI input buffers are powered by the I/O supply voltage V_{CCO}.

The Virtex-E family is not bitstream-compatible with the Virtex family, but Virtex designs can be compiled into equivalent Virtex-E devices.

The same device in the same package for the Virtex-E and Virtex families are pin-compatible with some minor exceptions. See the data sheet pinout section for details.

General Description

The Virtex-E FPGA family delivers high-performance, high-capacity programmable logic solutions. Dramatic increases in silicon efficiency result from optimizing the new architecture for place-and-route efficiency and exploiting an aggressive 6-layer metal 0.18 μm CMOS process. These advances make Virtex-E FPGAs powerful and flexible alternatives to mask-programmed gate arrays. The Virtex-E family includes the nine members in Table 1.

Building on experience gained from Virtex FPGAs, the Virtex-E family is an evolutionary step forward in programmable logic design. Combining a wide variety of programmable system features, a rich hierarchy of fast, flexible interconnect resources, and advanced process technology, the Virtex-E family delivers a high-speed and high-capacity programmable logic solution that enhances design flexibility while reducing time-to-market.

Virtex-E Architecture

Virtex-E devices feature a flexible, regular architecture that comprises an array of configurable logic blocks (CLBs) surrounded by programmable input/output blocks (IOBs), all interconnected by a rich hierarchy of fast, versatile routing

Dedicated Routing

Some classes of signal require dedicated routing resources to maximize performance. In the Virtex-E architecture, dedicated routing resources are provided for two classes of signal.

- Horizontal routing resources are provided for on-chip 3-state buses. Four partitionable bus lines are provided per CLB row, permitting multiple buses within a row, as shown in Figure 8.
- Two dedicated nets per CLB propagate carry signals vertically to the adjacent CLB.Global Clock Distribution Network
- DLL Location

Clock Routing

Clock Routing resources distribute clocks and other signals with very high fanout throughout the device. Virtex-E devices include two tiers of clock routing resources referred to as global and local clock routing resources.

- The global routing resources are four dedicated global nets with dedicated input pins that are designed to distribute high-fanout clock signals with minimal skew. Each global clock net can drive all CLB, IOB, and block RAM clock pins. The global nets can be driven only by global buffers. There are four global buffers, one for each global net.
- The local clock routing resources consist of 24 backbone lines, 12 across the top of the chip and 12 across bottom. From these lines, up to 12 unique signals per column can be distributed via the 12 longlines in the column. These local resources are more flexible than the global resources since they are not restricted to routing only to clock pins.

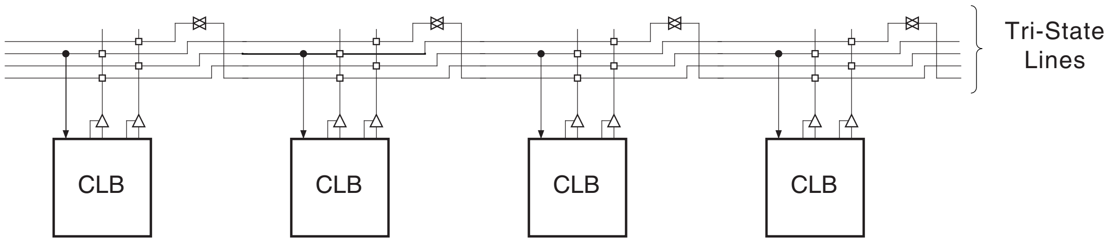

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Figure 8: **BUFT Connections to Dedicated Horizontal Bus LInes**

Global Clock Distribution

Virtex-E provides high-speed, low-skew clock distribution through the global routing resources described above. A typical clock distribution net is shown in Figure 9.

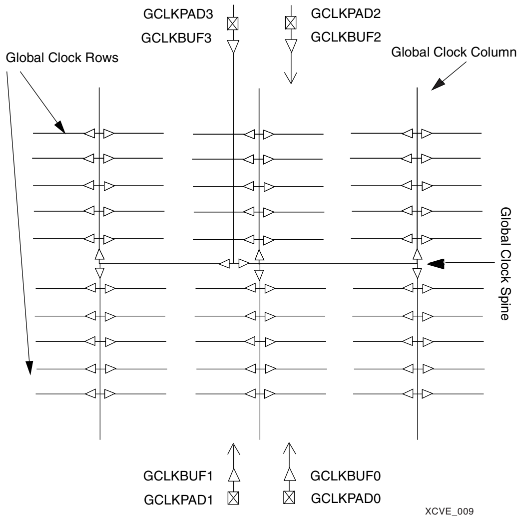

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Figure 9: **Global Clock Distribution Network**

Four global buffers are provided, two at the top center of the device and two at the bottom center. These drive the four global nets that in turn drive any clock pin.

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is selected either from these pads or from signals in the general purpose routing.

Digital Delay-Locked Loops

There are eight DLLs (Delay-Locked Loops) per device, with four located at the top and four at the bottom, Figure 10. The DLLs can be used to eliminate skew between the clock input pad and the internal clock input pins throughout the device. Each DLL can drive two global clock networks.The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element. Additional delay is introduced such that clock edges arrive at internal flip-flops synchronized with clock edges arriving at the input.

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock, and can double the clock or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

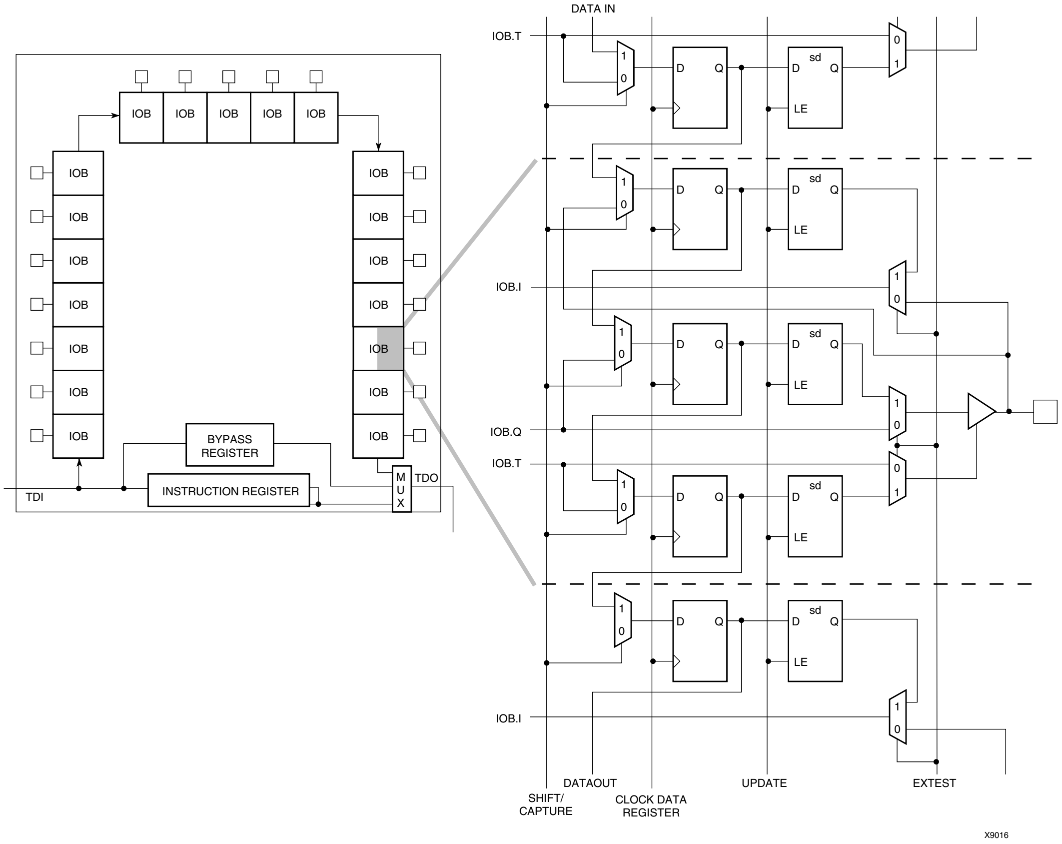


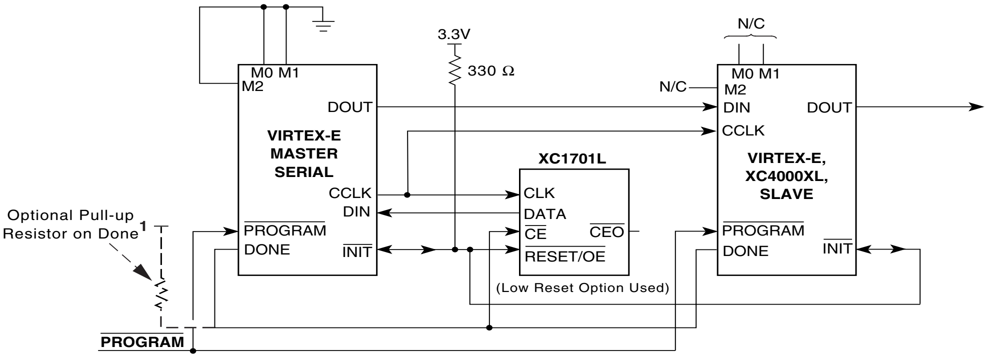
Figure 11: **Virtex-E Family Boundary Scan Logic**

Instruction Set

The Virtex-E series Boundary Scan instruction set also includes instructions to configure the device and read back configuration data (CFG_IN, CFG_OUT, and JSTART). The complete instruction set is coded as shown in Table 6..

Table 6: **Boundary Scan Instructions**

Boundary Scan Command	Binary Code(4:0)	Description
EXTEST	00000	Enables Boundary Scan EXTEST operation
SAMPLE/ PRELOAD	00001	Enables Boundary Scan SAMPLE/PRELOAD operation
USER1	00010	Access user-defined register 1
USER2	00011	Access user-defined register 2
CFG_OUT	00100	Access the configuration bus for read operations.
CFG_IN	00101	Access the configuration bus for write operations.
INTEST	00111	Enables Boundary Scan INTEST operation
USERCODE	01000	Enables shifting out USER code
IDCODE	01001	Enables shifting out of ID Code
HIGHZ	01010	3-states output pins while enabling the Bypass Register
JSTART	01100	Clock the start-up sequence when StartupClk is TCK
BYPASS	11111	Enables BYPASS
RESERVED	All other codes	Xilinx reserved instructions



Note 1: If none of the Virtex FPGAs have been selected to drive DONE, an external pull-up resistor of 330 Ω should be added to the common DONE line. (For Spartan-XL devices, add a 4.7K Ω pull-up resistor.) This pull-up is not needed if the DriveDONE attribute is set. If used, DriveDONE should be selected only for the last device in the configuration chain.

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Figure 13: **Master/Slave Serial Mode Circuit Diagram**

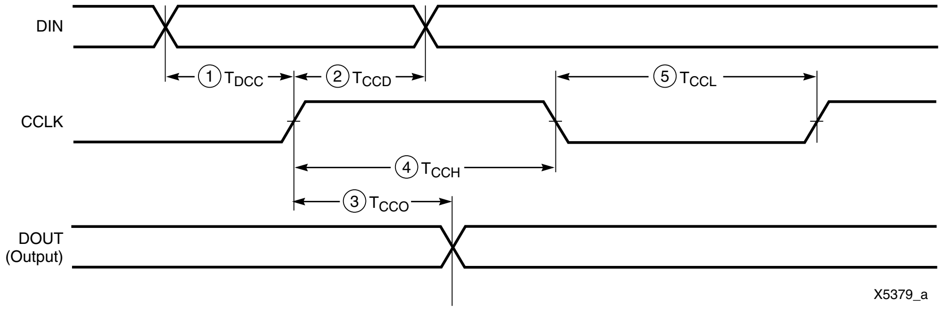

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Figure 14: **Slave-Serial Mode Programming Switching Characteristics**

Master-Serial Mode

In master-serial mode, the CCLK output of the FPGA drives a Xilinx Serial PROM that feeds bit-serial data to the DIN input. The FPGA accepts this data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge. The maximum capacity for a single LOUT/DOUT write is 2^{20}-1 (1,048,575) 32-bit words, or 33,554,4000 bits.

The interface is identical to slave-serial except that an internal oscillator is used to generate the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK, which always starts at a slow default frequency. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration. Switching to a lower frequency is prohibited.

The CCLK frequency is set using the ConfigRate option in the bitstream generation software. The maximum CCLK frequency that can be selected is 60 MHz. When selecting a CCLK frequency, ensure that the serial PROM and any daisy-chained FPGAs are fast enough to support the clock rate.

On power-up, the CCLK frequency is approximately 2.5 MHz. This frequency is used until the ConfigRate bits have been loaded when the frequency changes to the selected ConfigRate. Unless a different frequency is specified in the design, the default ConfigRate is 4 MHz.

In a full master/slave system (Figure 13), the left-most device operates in master-serial mode. The remaining devices operate in slave-serial mode. The SPROM RESET pin is driven by INIT, and the CE input is driven by DONE. There is the potential for contention on the DONE pin, depending on the start-up sequence options chosen.

The sequence of operations necessary to configure a Virtex-E FPGA serially appears in Figure 15.

Input termination techniques include the following.

- None
- Parallel (Shunt)

These termination techniques can be applied in any combination. A generic example of each combination of termination methods appears in Figure 43.

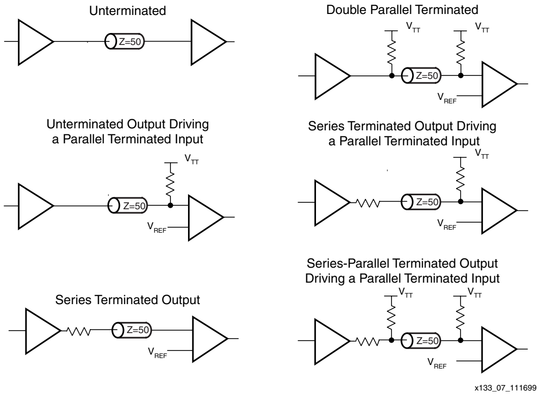

Figure 43: **Overview of Standard Input and Output Termination Methods**

Simultaneous Switching Guidelines

Ground bounce can occur with high-speed digital ICs when multiple outputs change states simultaneously, causing undesired transient behavior on an output, or in the internal logic. This problem is also referred to as the Simultaneous Switching Output (SSO) problem.

Ground bounce is primarily due to current changes in the combined inductance of ground pins, bond wires, and ground metallization. The IC internal ground level deviates from the external system ground level for a short duration (a few nanoseconds) after multiple outputs change state simultaneously.

Ground bounce affects stable Low outputs and all inputs because they interpret the incoming signal by comparing it to the internal ground. If the ground bounce amplitude exceeds the actual instantaneous noise margin, then a non-changing input can be interpreted as a short pulse with a polarity opposite to the ground bounce.

Table 21 provides guidelines for the maximum number of simultaneously switching outputs allowed per output power/ground pair to avoid the effects of ground bounce. See Table 22 for the number of effective output power/ground pairs for each Virtex-E device and package combination.

Table 21: **Guidelines for Max Number of Simultaneously Switching Outputs per Power/Ground Pair**

Standard	Package		
	BGA, CS, FGA	**HQ**	**PQ, TQ**
LVTTL Slow Slew Rate, 2 mA drive	68	49	36
LVTTL Slow Slew Rate, 4 mA drive	41	31	20
LVTTL Slow Slew Rate, 6 mA drive	29	22	15
LVTTL Slow Slew Rate, 8 mA drive	22	17	12
LVTTL Slow Slew Rate, 12 mA drive	17	12	9
LVTTL Slow Slew Rate, 16 mA drive	14	10	7
LVTTL Slow Slew Rate, 24 mA drive	9	7	5
LVTTL Fast Slew Rate, 2 mA drive	40	29	21
LVTTL Fast Slew Rate, 4 mA drive	24	18	12
LVTTL Fast Slew Rate, 6 mA drive	17	13	9
LVTTL Fast Slew Rate, 8 mA drive	13	10	7
LVTTL Fast Slew Rate, 12 mA drive	10	7	5
LVTTL Fast Slew Rate, 16 mA drive	8	6	4
LVTTL Fast Slew Rate, 24 mA drive	5	4	3
LVCMOS	10	7	5
PCI	8	6	4
GTL	4	4	4
GTL+	4	4	4

LVDS

Depending on whether the device is transmitting an LVDS signal or receiving an LVDS signal, there are two different circuits used for LVDS termination. A sample circuit illustrating a valid termination technique for transmitting LVDS signals appears in Figure 54. A sample circuit illustrating a valid termination for receiving LVDS signals appears in Figure 55. Table 38 lists DC voltage specifications. Further information on the specific termination resistor packs shown can be found on Table 40.

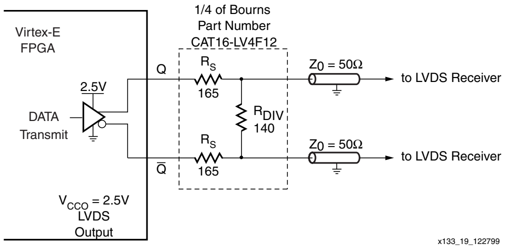

Figure 54: **Transmitting LVDS Signal Circuit**

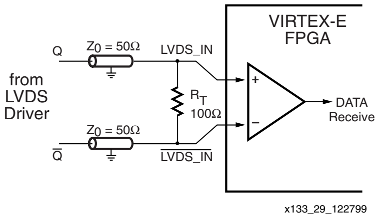

Figure 55: **Receiving LVDS Signal Circuit**

Table 38: **LVDS Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	2.375	2.5	2.625
$V_{ICM}^{(2)}$	0.2	1.25	2.2
$V_{OCM}^{(1)}$	1.125	1.25	1.375
V_{IDIFF} $^{(1)}$	0.1	0.35	-
V_{ODIFF} $^{(1)}$	0.25	0.35	0.45
$V_{OH}^{(1)}$	1.25	-	-
$V_{OL}^{(1)}$	-	-	1.25

Notes:

1. Measured with a 100 Ω resistor across Q and $\overline{Q}$.
2. Measured with a differential input voltage = +/− 350 mV.

LVPECL

Depending on whether the device is transmitting or receiving an LVPECL signal, two different circuits are used for LVPECL termination. A sample circuit illustrating a valid termination technique for transmitting LVPECL signals appears in Figure 56. A sample circuit illustrating a valid termination for receiving LVPECL signals appears in Figure 57. Table 39 lists DC voltage specifications. Further information on the specific termination resistor packs shown can be found on Table 40.

Table 39: **LVPECL Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
V_{REF}	-	-	-
V_{TT}	-	-	-
V_{IH}	1.49	-	2.72
V_{IL}	0.86	-	2.125
V_{OH}	1.8	-	-
V_{OL}	-	-	1.57

Notes:

1. For more detailed information, see DS022-3: *Virtex-E 1.8V FPGA DC and Switching Characteristics*, Module 3, LVPECL DC Specifications section.

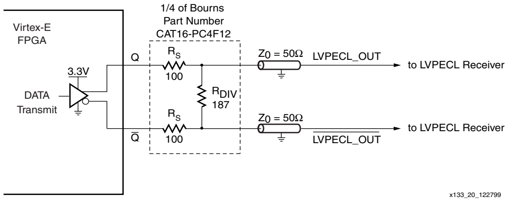

Figure 56: **Transmitting LVPECL Signal Circuit**

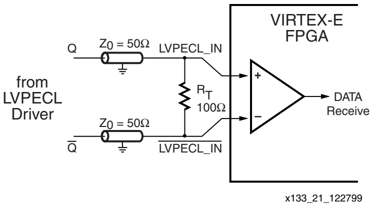

Figure 57: **Receiving LVPECL Signal Circuit**

DC Characteristics

Absolute Maximum Ratings

Symbol	Description[1]			Units
V_{CCINT}	Internal Supply voltage relative to GND		–0.5 to 2.0	V
V_{CCO}	Supply voltage relative to GND		–0.5 to 4.0	V
V_{REF}	Input Reference Voltage		–0.5 to 4.0	V
V_{IN} [3]	Input voltage relative to GND		–0.5 to V_{CCO} +0.5	V
V_{TS}	Voltage applied to 3-state output		–0.5 to 4.0	V
V_{CC}	Longest Supply Voltage Rise Time from 0 V - 1.71 V		50	ms
T_{STG}	Storage temperature (ambient)		–65 to +150	°C
T_J	Junction temperature [2]	Plastic packages	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time can affect device reliability.
2. For soldering guidelines and thermal considerations, see the device packaging information on www.xilinx.com.
3. Inputs configured as PCI are fully PCI compliant. This statement takes precedence over any specification that would imply that the device is not PCI compliant.

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CCINT}	Internal Supply voltage relative to GND, T_J = 0 °C to +85 °C	Commercial	1.8 – 5%	1.8 + 5%	V
	Internal Supply voltage relative to GND, T_J = –40 °C to +100 °C	Industrial	1.8 – 5%	1.8 + 5%	V
V_{CCO}	Supply voltage relative to GND, T_J = 0 °C to +85 °C	Commercial	1.2	3.6	V
	Supply voltage relative to GND, T_J = –40 °C to +100 °C	Industrial	1.2	3.6	V
T_{IN}	Input signal transition time			250	ns

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used, see Figure 2. The values listed below are worst-case. Precise values are provided by the timing analyzer.

		Speed Grade(1)				
Description	**Symbol**	**Min**	**-8**	**-7**	**-6**	**Units**
Combinatorial Delays						
4-input function: F/G inputs to X/Y outputs	T_{ILO}	0.19	0.40	0.42	0.47	ns, max
5-input function: F/G inputs to F5 output	T_{IF5}	0.36	0.76	0.8	0.9	ns, max
5-input function: F/G inputs to X output	T_{IF5X}	0.35	0.74	0.8	0.9	ns, max
6-input function: F/G inputs to Y output via F6 MUX	T_{IF6Y}	0.35	0.74	0.9	1.0	ns, max
6-input function: F5IN input to Y output	T_{F5INY}	0.04	0.11	0.20	0.22	ns, max
Incremental delay routing through transparent latch to XQ/YQ outputs	T_{IFNCTL}	0.27	0.63	0.7	0.8	ns, max
BY input to YB output	T_{BYYB}	0.19	0.38	0.46	0.51	ns, max
Sequential Delays						
FF Clock CLK to XQ/YQ outputs	T_{CKO}	0.34	0.78	0.9	1.0	ns, max
Latch Clock CLK to XQ/YQ outputs	T_{CKLO}	0.40	0.77	0.9	1.0	ns, max
Setup and Hold Times before/after Clock CLK						
4-input function: F/G Inputs	T_{ICK} / T_{CKI}	0.39 / 0	0.9 / 0	1.0 / 0	1.1 / 0	ns, min
5-input function: F/G inputs	T_{IF5CK} / T_{CKIF5}	0.55 / 0	1.3 / 0	1.4 / 0	1.5 / 0	ns, min
6-input function: F5IN input	T_{F5INCK} / T_{CKF5IN}	0.27 / 0	0.6 / 0	0.8 / 0	0.8 / 0	ns, min
6-input function: F/G inputs via F6 MUX	T_{IF6CK} / T_{CKIF6}	0.58 / 0	1.3 / 0	1.5 / 0	1.6 / 0	ns, min
BX/BY inputs	T_{DICK} / T_{CKDI}	0.25 / 0	0.6 / 0	0.7 / 0	0.8 / 0	ns, min
CE input	T_{CECK} / T_{CKCE}	0.28 / 0	0.55 / 0	0.7 / 0	0.7 / 0	ns, min
SR/BY inputs (synchronous)	T_{RCK} / T_{CKR}	0.24 / 0	0.46 / 0	0.52 / 0	0.6 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T_{CH}	0.56	1.2	1.3	1.4	ns, min
Minimum Pulse Width, Low	T_{CL}	0.56	1.2	1.3	1.4	ns, min
Set/Reset						
Minimum Pulse Width, SR/BY inputs	T_{RPW}	0.94	1.9	2.1	2.4	ns, min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T_{RQ}	0.39	0.8	0.9	1.0	ns, max
Toggle Frequency (MHz) (for export control)	F_{TOG}	-	416	400	357	MHz

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

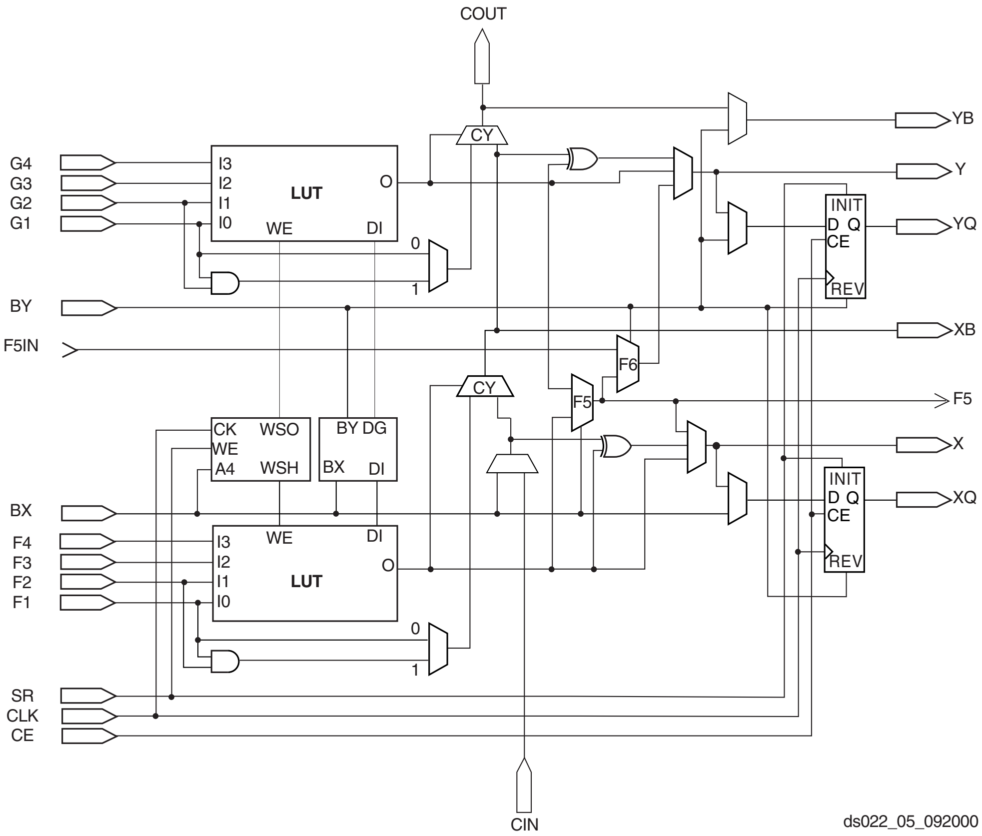

Figure 2: **Detailed View of Virtex-E Slice**

CLB Arithmetic Switching Characteristics

Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer.

		Speed Grade(1)				Units
Description	**Symbol**	**Min**	**-8**	**-7**	**-6**	
Combinatorial Delays						
F operand inputs to X via XOR	T_{OPX}	0.32	0.68	0.8	0.8	ns, max
F operand input to XB output	T_{OPXB}	0.35	0.65	0.8	0.9	ns, max
F operand input to Y via XOR	T_{OPY}	0.59	1.07	1.4	1.5	ns, max
F operand input to YB output	T_{OPYB}	0.48	0.89	1.1	1.3	ns, max
F operand input to COUT output	T_{OPCYF}	0.37	0.71	0.9	1.0	ns, max
G operand inputs to Y via XOR	T_{OPGY}	0.34	0.72	0.8	0.9	ns, max
G operand input to YB output	T_{OPGYB}	0.47	0.78	1.2	1.3	ns, max
G operand input to COUT output	T_{OPCYG}	0.36	0.60	0.9	1.0	ns, max
BX initialization input to COUT	T_{BXCY}	0.19	0.36	0.51	0.57	ns, max
CIN input to X output via XOR	T_{CINX}	0.27	0.50	0.6	0.7	ns, max
CIN input to XB	T_{CINXB}	0.02	0.04	0.07	0.08	ns, max
CIN input to Y via XOR	T_{CINY}	0.26	0.45	0.7	0.7	ns, max
CIN input to YB	T_{CINYB}	0.16	0.28	0.38	0.43	ns, max
CIN input to COUT output	T_{BYP}	0.05	0.10	0.14	0.15	ns, max
Multiplier Operation						
F1/2 operand inputs to XB output via AND	T_{FANDXB}	0.10	0.30	0.35	0.39	ns, max
F1/2 operand inputs to YB output via AND	T_{FANDYB}	0.28	0.56	0.7	0.8	ns, max
F1/2 operand inputs to COUT output via AND	T_{FANDCY}	0.17	0.38	0.46	0.51	ns, max
G1/2 operand inputs to YB output via AND	T_{GANDYB}	0.20	0.46	0.55	0.7	ns, max
G1/2 operand inputs to COUT output via AND	T_{GANDCY}	0.09	0.28	0.30	0.34	ns, max
Setup and Hold Times before/after Clock CLK						
CIN input to FFX	T_{CCKX}/T_{CKCX}	0.47 / 0	1.0 / 0	1.2 / 0	1.3 / 0	ns, min
CIN input to FFY	T_{CCKY}/T_{CKCY}	0.49 / 0	0.92 / 0	1.2 / 0	1.3 / 0	ns, min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Block RAM Switching Characteristics

		Speed Grade[1]				
Description	**Symbol**	**Min**	**-8**	**-7**	**-6**	**Units**
Sequential Delays						
Clock CLK to DOUT output	T_{BCKO}	0.63	2.46	3.1	3.5	ns, max
Setup and Hold Times before Clock CLK						
ADDR inputs	T_{BACK}/T_{BCKA}	0.42 / 0	0.9 / 0	1.0 / 0	1.1 / 0	ns, min
DIN inputs	T_{BDCK}/T_{BCKD}	0.42 / 0	0.9 / 0	1.0 / 0	1.1 / 0	ns, min
EN input	T_{BECK}/T_{BCKE}	0.97 / 0	2.0 / 0	2.2 / 0	2.5 / 0	ns, min
RST input	T_{BRCK}/T_{BCKR}	0.9 / 0	1.8 / 0	2.1 / 0	2.3 / 0	ns, min
WEN input	T_{BWCK}/T_{BCKW}	0.86 / 0	1.7 / 0	2.0 / 0	2.2 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T_{BPWH}	0.6	1.2	1.35	1.5	ns, min
Minimum Pulse Width, Low	T_{BPWL}	0.6	1.2	1.35	1.5	ns, min
CLKA -> CLKB setup time for different ports	T_{BCCS}	1.2	2.4	2.7	3.0	ns, min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

TBUF Switching Characteristics

		Speed Grade				
Description	**Symbol**	**Min**	**-8**	**-7**	**-6**	**Units**
Combinatorial Delays						
IN input to OUT output	T_{IO}	0.0	0.0	0.0	0 .0	ns, max
TRI input to OUT output high-impedance	T_{OFF}	0.05	0.092	0.10	0.11	ns, max
TRI input to valid data on OUT output	T_{ON}	0.05	0.092	0.10	0.11	ns, max

JTAG Test Access Port Switching Characteristics

Description	Symbol	Value	Units
TMS and TDI Setup times before TCK	T_{TAPTK}	4.0	ns, min
TMS and TDI Hold times after TCK	T_{TCKTAP}	2.0	ns, min
Output delay from clock TCK to output TDO	T_{TCKTDO}	11.0	ns, max
Maximum TCK clock frequency	F_{TCK}	33	MHz, max

Table 13: **BG432 Differential Pin Pair Summary XCV300E, XCV400E, XC600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
48	2	N1	P4	√	D3
49	2	P3	P2	4	-
50	2	R3	R4	1	VREF
51	2	R1	T3	√	-
52	3	U4	U2	1	VREF
53	3	U1	V3	4	-
54	3	V4	V2	√	VREF
55	3	W3	W4	1	-
56	3	Y1	Y3	1	-
57	3	Y4	Y2	4	-
58	3	AA3	AB1	√	D5
59	3	AB3	AB4	√	VREF
60	3	AD1	AC3	1	VREF
61	3	AC4	AD2	4	-
62	3	AD3	AD4	√	VREF
63	3	AF2	AE3	1	-
64	3	AE4	AG1	5	-
65	3	AG2	AF3	1	VREF
66	3	AF4	AH1	4	-
67	3	AH2	AG3	3	-
68	3	AG4	AJ2	√	INIT
69	4	AJ4	AK3	√	-
70	4	AH5	AK4	1	-
71	4	AJ5	AH6	√	-
72	4	AL4	AK5	√	VREF
73	4	AJ6	AH7	2	-
74	4	AL5	AK6	√	-
75	4	AJ7	AL6	√	VREF
76	4	AH9	AJ8	1	-
77	4	AK8	AJ9	1	VREF
78	4	AL8	AK9	√	VREF
79	4	AK10	AL10	√	-
80	4	AH12	AK11	√	-
81	4	AJ12	AK12	√	-
82	4	AH13	AJ13	√	-
83	4	AL13	AK14	√	VREF
84	4	AH14	AJ14	1	-
85	4	AK15	AJ15	1	VREF
86	5	AH15	AL17	NA	IO_LVDS_DLL
87	5	AK17	AJ17	1	VREF
88	5	AH17	AK18	1	-
89	5	AL19	AJ18	√	VREF
90	5	AH18	AL20	√	-
91	5	AK20	AH19	√	-
92	5	AJ20	AK21	√	-
93	5	AJ21	AL22	√	-
94	5	AJ22	AK23	√	VREF
95	5	AH22	AL24	1	VREF
96	5	AK24	AH23	1	-
97	5	AK25	AJ25	√	VREF
98	5	AL26	AK26	√	-
99	5	AH25	AL27	2	-
100	5	AJ26	AK27	√	VREF
101	5	AH26	AL28	√	-
102	5	AJ27	AK28	1	-
103	6	AH30	AJ30	√	-
104	6	AH31	AG28	3	-
105	6	AG30	AG29	4	-
106	6	AG31	AF28	1	VREF
107	6	AF30	AF29	5	-
108	6	AF31	AE28	1	-
109	6	AD28	AE30	√	VREF
110	6	AD31	AD30	4	-
111	6	AC29	AC28	1	VREF

Table 16: **FG256 Package — XCV50E, XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
NA	GND	K11
NA	GND	K10
NA	GND	K9
NA	GND	K8
NA	GND	K7
NA	GND	K6
NA	GND	J10
NA	GND	J9
NA	GND	J8
NA	GND	J7
NA	GND	H10
NA	GND	H9
NA	GND	H8
NA	GND	H7
NA	GND	G11
NA	GND	G10
NA	GND	G9
NA	GND	G8
NA	GND	G7
NA	GND	G6
NA	GND	F11
NA	GND	F10
NA	GND	F7
NA	GND	F6
NA	GND	B15
NA	GND	B2
NA	GND	A16
NA	GND	A1

Notes:

1. V_{REF} or I/O option only in the XCV100E, 200E, 300E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV200E, 300E; otherwise, I/O option only.

FG256 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 17: **FG256 Differential Pin Pair Summary XCV50E, XCV100E, XCV200E, XCV300E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	N8	N9	NA	IO_DLL_L52P
1	5	R8	T8	NA	IO_DLL_L52N
2	1	C9	A8	NA	IO_DLL_L8P
3	0	B8	A7	NA	IO_DLL_L8N
IO LVDS Total Pairs: 83, Asynchronous Outputs: 35					
0	0	A3	C5	7	VREF
1	0	E6	D5	√	-
2	0	A4	B4	√	VREF
3	0	B5	D6	2	-
4	0	A5	C6	√	VREF
5	0	C7	B6	√	-
6	0	C8	D7	1	-
7	0	A6	B7	1	VREF
8	1	A8	A7	NA	IO_LVDS_DLL
9	1	A9	D9	2	-
10	1	B9	E10	1	VREF
11	1	D10	A10	1	-
12	1	A11	C10	√	-
13	1	E11	B11	√	VREF
14	1	D11	A12	2	-
15	1	C11	A13	√	VREF
16	1	D12	B12	√	-
17	1	C12	A14	7	VREF
18	1	B13	C13	√	CS

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
1	IO_L40P_YY	D20
1	IO_L41N_YY	F19
1	IO_VREF_L41P_YY	C21
1	IO_L42N_YY	B22
1	IO_L42P_YY	E20
1	IO_L43N_Y	A23
1	IO_L43P_Y	D21
1	IO_WRITE_L44N_YY	C22
1	IO_CS_L44P_YY	E21
2	IO	D25[1]
2	IO	D26
2	IO	E26
2	IO	F26
2	IO	H26[1]
2	IO	K26[1]
2	IO	M25[1]
2	IO	N26[1]
2	IO_D1	K24
2	IO_DOUT_BUSY_L45P_YY	E23
2	IO_DIN_D0_L45N_YY	F22
2	IO_L46P_YY	E24
2	IO_L46N_YY	F20
2	IO_L47P_Y	G21
2	IO_L47N_Y	G22
2	IO_VREF_L48P_Y	F24
2	IO_L48N_Y	H20
2	IO_L49P_Y	E25
2	IO_L49N_Y	H21
2	IO_L50P_YY	F23
2	IO_L50N_YY	G23
2	IO_VREF_L51P_YY	H23
2	IO_L51N_YY	J20
2	IO_L52P_YY	G24
2	IO_L52N_YY	H22
2	IO_L53P_Y	J21
2	IO_L53N_Y	G25
2	IO_VREF_L54P_Y	G26[2]
2	IO_L54N_Y	J22
2	IO_L55P_YY	H24
2	IO_L55N_YY	J23
2	IO_L56P_YY	J24
2	IO_VREF_L56N_YY	K20
2	IO_D2_L57P_YY	K22
2	IO_L57N_YY	K21
2	IO_L58P_YY	H25
2	IO_L58N_YY	K23
2	IO_L59P_Y	L20
2	IO_L59N_Y	J26
2	IO_L60P_Y	K25
2	IO_L60N_Y	L22
2	IO_L61P_Y	L21
2	IO_L61N_Y	L23
2	IO_L62P_Y	M20
2	IO_L62N_Y	L24
2	IO_VREF_L63P_YY	M23
2	IO_D3_L63N_YY	M22
2	IO_L64P_YY	L26
2	IO_L64N_YY	M21
2	IO_L65P_Y	N19
2	IO_L65N_Y	M24
2	IO_VREF_L66P_Y	M26
2	IO_L66N_Y	N20
2	IO_L67P_YY	N24
2	IO_L67N_YY	N21
2	IO_L68P_YY	N23
2	IO_L68N_YY	N22
3	IO	P24
3	IO	P26[1]
3	IO	R26[1]
3	IO	T26[1]
3	IO	U26[1]
3	IO	W25

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
5	IO_L129N_Y	AB9
5	IO_L130P_YY	AA9
5	IO_L130N_YY	AF6
5	IO_L131P_YY	AC8
5	IO_VREF_L131N_YY	AC7
5	IO_L132P_YY	AD6
5	IO_L132N_YY	Y9
5	IO_L133P_YY	AE5
5	IO_L133N_YY	AA8
5	IO_L134P_YY	AC6
5	IO_VREF_L134N_YY	AB8
5	IO_L135P_YY	AD5
5	IO_L135N_YY	AA7
5	IO_L136P_Y	AF4
5	IO_L136N_Y	AC5
6	IO	P3
6	IO	AA3
6	IO	AC1[1]
6	IO	P1[1]
6	IO	R2[1]
6	IO	T1[1]
6	IO	V1[1]
6	IO	W3
6	IO	Y2
6	IO	Y6
6	IO_L137N_YY	AA5
6	IO_L137P_YY	AC3
6	IO_L138N_YY	AC2
6	IO_L138P_YY	AB4
6	IO_L139N_Y	W6
6	IO_L139P_Y	AA4
6	IO_VREF_L140N_Y	AB3
6	IO_L140P_Y	Y5
6	IO_L141N_Y	AB2
6	IO_L141P_Y	V7
6	IO_L142N_YY	AB1
6	IO_L142P_YY	Y4
6	IO_VREF_L143N_YY	V5
6	IO_L143P_YY	W5
6	IO_L144N_YY	AA1
6	IO_L144P_YY	V6
6	IO_L145N_Y	W4
6	IO_L145P_Y	Y3
6	IO_VREF_L146N_Y	Y1[2]
6	IO_L146P_Y	U7
6	IO_L147N_YY	W1
6	IO_L147P_YY	V4
6	IO_L148N_YY	W2
6	IO_VREF_L148P_YY	U6
6	IO_L149N_YY	V3
6	IO_L149P_YY	T5
6	IO_L150N_YY	U5
6	IO_L150P_YY	U4
6	IO_L151N_Y	T7
6	IO_L151P_Y	U3
6	IO_L152N_Y	U2
6	IO_L152P_Y	T6
6	IO_L153N_Y	U1
6	IO_L153P_Y	T4
6	IO_L154N_Y	R7
6	IO_L154P_Y	T3
6	IO_VREF_L155N_YY	R4
6	IO_L155P_YY	R6
6	IO_L156N_YY	R3
6	IO_L156P_YY	R5
6	IO_L157N_Y	P8
6	IO_L157P_Y	P7
6	IO_VREF_L158N_Y	R1
6	IO_L158P_Y	P6
6	IO_L159N_YY	P5
6	IO_L159P_YY	P4
7	IO	D1[1]

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
NA	GND	P14
NA	GND	P13
NA	GND	P12
NA	GND	P11
NA	GND	P10
NA	GND	N2
NA	GND	N17
NA	GND	N16
NA	GND	N15
NA	GND	N14
NA	GND	N13
NA	GND	N12
NA	GND	N11
NA	GND	N10
NA	GND	M17
NA	GND	M16
NA	GND	M15
NA	GND	M14
NA	GND	M13
NA	GND	M12
NA	GND	M11
NA	GND	M10
NA	GND	L17
NA	GND	L16
NA	GND	L15
NA	GND	L14
NA	GND	L13
NA	GND	L12
NA	GND	L11
NA	GND	L10
NA	GND	K17
NA	GND	K16
NA	GND	K15
NA	GND	K14
NA	GND	K13
NA	GND	K12
NA	GND	K11
NA	GND	K10
NA	GND	J25
NA	GND	J2
NA	GND	E5
NA	GND	E22
NA	GND	D4
NA	GND	D23
NA	GND	C3
NA	GND	C24
NA	GND	B9
NA	GND	B25
NA	GND	B2
NA	GND	B18
NA	GND	B14
NA	GND	AF26
NA	GND	AF1
NA	GND	AE9
NA	GND	AE25
NA	GND	AE2
NA	GND	AE18
NA	GND	AE13
NA	GND	AD3
NA	GND	AD24
NA	GND	AC4
NA	GND	AC23
NA	GND	AB5
NA	GND	AB22
NA	GND	A26
NA	GND	A1

Notes:
1. NC in the XCV400E.
2. V_{REF} or I/O option only in the XCV600E; otherwise, I/O option only.

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
6	IO	AJ40
6	IO	AL41
6	IO	AN38
6	IO	AN42
6	IO	AP41
6	IO	AR39
6	IO_L211N_YY	AV41
6	IO_L211P_YY	AV42
6	IO_L212N_Y	AW40
6	IO_L212P_Y	AU41
6	IO_L213N_Y	AV39
6	IO_L213P_Y	AU42
6	IO_VREF_L214N_Y	AT41
6	IO_L214P_Y	AU38
6	IO_L215N	AT42
6	IO_L215P	AV40
6	IO_L216N_Y	AR41
6	IO_L216P_Y	AU39
6	IO_VREF_L217N_Y	AR42
6	IO_L217P_Y	AU40
6	IO_L218N_YY	AT38
6	IO_L218P_YY	AP42
6	IO_L219N_Y	AN41
6	IO_L219P_Y	AT39
6	IO_L220N_Y	AT40
6	IO_L220P_Y	AM40
6	IO_VREF_L221N_YY	AR38
6	IO_L221P_YY	AM41
6	IO_L222N_YY	AM42
6	IO_L222P_YY	AR40
6	IO_VREF_L223N_Y	AL40[2]
6	IO_L223P_Y	AP38
6	IO_L224N_Y	AP39
6	IO_L224P_Y	AL42
6	IO_VREF_L225N_YY	AP40
6	IO_L225P_YY	AK40
6	IO_L226N_YY	AK41
6	IO_L226P_YY	AN39
6	IO_L227N_Y	AK42
6	IO_L227P_Y	AN40
6	IO_VREF_L228N_YY	AM38
6	IO_L228P_YY	AJ41
6	IO_L229N_YY	AJ42
6	IO_L229P_YY	AM39
6	IO_L230N_Y	AH40
6	IO_L230P_Y	AH41
6	IO_L231N_Y	AL38
6	IO_L231P_Y	AH42
6	IO_L232N_Y	AL39
6	IO_L232P_Y	AG41
6	IO_L233N	AK39
6	IO_L233P	AG40
6	IO_L234N_Y	AJ38
6	IO_L234P_Y	AG42
6	IO_VREF_L235N_Y	AF42
6	IO_L235P_Y	AJ39
6	IO_L236N_YY	AF41
6	IO_L236P_YY	AH38
6	IO_L237N_Y	AE42
6	IO_L237P_Y	AH39
6	IO_L238N_Y	AG38
6	IO_L238P_Y	AE41
6	IO_VREF_L239N_YY	AG39
6	IO_L239P_YY	AD42
6	IO_L240N_YY	AD40
6	IO_L240P_YY	AF39
6	IO_L241N_Y	AD41
6	IO_L241P_Y	AE38
6	IO_L242N_Y	AE39
6	IO_L242P_Y	AC40
6	IO_VREF_L243N_YY	AD38
6	IO_L243P_YY	AC41
6	IO_L244N_YY	AB42
6	IO_L244P_YY	AC38

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
0	IO_L6P_YY	H10[5]
0	IO_L7N_Y	D7
0	IO_L7P_Y	B5
0	IO_L8N_Y	K12
0	IO_L8P_Y	E8
0	IO_L9N	B6[4]
0	IO_L9P	F9[5]
0	IO_L10N_YY	G10
0	IO_L10P_YY	C7
0	IO_VREF_L11N_YY	D8
0	IO_L11P_YY	B7
0	IO_L12N	H11[4]
0	IO_L12P	C8[5]
0	IO_L13N_Y	E9
0	IO_L13P_Y	B8
0	IO_VREF_L14N_Y	K13[2]
0	IO_L14P_Y	G11
0	IO_L15N	A8[4]
0	IO_L15P	F10[5]
0	IO_L16N_YY	C9
0	IO_L16P_YY	H12
0	IO_VREF_L17N_YY	D10
0	IO_L17P_YY	A9
0	IO_L18N_Y	F11
0	IO_L18P_Y	A10
0	IO_L19N_Y	K14
0	IO_L19P_Y	C10
0	IO_VREF_L20N_YY	H13
0	IO_L20P_YY	G12
0	IO_L21N_YY	A11
0	IO_L21P_YY	B11
0	IO_L22N_Y	E12
0	IO_L22P_Y	D11
0	IO_L23N_Y	G13
0	IO_L23P_Y	C12
0	IO_L24N_Y	K15
0	IO_L24P_Y	A12
0	IO_L25N_Y	B12
0	IO_L25P_Y	H14
0	IO_L26N_YY	D12
0	IO_L26P_YY	F13
0	IO_VREF_L27N_YY	A13
0	IO_L27P_YY	B13
0	IO_L28N_YY	J15[4]
0	IO_L28P_YY	G14[5]
0	IO_L29N_Y	C13
0	IO_L29P_Y	F14
0	IO_L30N_Y	H15
0	IO_L30P_Y	D13
0	IO_L31N	A14[4]
0	IO_L31P	K16[5]
0	IO_L32N_YY	E14
0	IO_L32P_YY	B14
0	IO_VREF_L33N_YY	G15
0	IO_L33P_YY	D14
0	IO_L34N	J16[4]
0	IO_L34P	D15[5]
0	IO_L35N_Y	F15
0	IO_L35P_Y	B15
0	IO_L36N_Y	A15
0	IO_L36P_Y	E15
0	IO_L37N	G16[4]
0	IO_L37P	A16[5]
0	IO_L38N_YY	F16
0	IO_L38P_YY	J17
0	IO_VREF_L39N_YY	C16
0	IO_L39P_YY	B16
0	IO_L40N_Y	H17

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
6	IO_VREF_L265N_Y	AJ3
6	IO_L265P_Y	AG5
6	IO_L266N_YY	AD9[4]
6	IO_L266P_YY	AJ2[5]
6	IO_L267N_YY	AC10
6	IO_L267P_YY	AH2
6	IO_L268N_Y	AH3
6	IO_L268P_Y	AF5
6	IO_L269N_Y	AE8[4]
6	IO_L269P_Y	AG3[5]
6	IO_L270N_Y	AE7
6	IO_L270P_Y	AG2
6	IO_VREF_L271N_YY	AF6
6	IO_L271P_YY	AG1
6	IO_L272N_YY	AC9[4]
6	IO_L272P_YY	AG4[5]
6	IO_L273N_YY	AE6
6	IO_L273P_YY	AF3
6	IO_VREF_L274N_Y	AF1[2]
6	IO_L274P_Y	AF4
6	IO_L275N	AB10[4]
6	IO_L275P	AF2[5]
6	IO_L276N_Y	AC8
6	IO_L276P_Y	AE1
6	IO_VREF_L277N_YY	AD5
6	IO_L277P_YY	AE3
6	IO_L278N_YY	AC7
6	IO_L278P_YY	AD1
6	IO_L279N_Y	AD6
6	IO_L279P_Y	AD2
6	IO_VREF_L280N_YY	AB8
6	IO_L280P_YY	AC1
6	IO_L281N_YY	AC5
6	IO_L281P_YY	AC2
6	IO_L282N_Y	AA9
6	IO_L282P_Y	AC3
6	IO_L283N_Y	AC4
6	IO_L283P_Y	AD4
6	IO_L284N_Y	AA8
6	IO_L284P_Y	AB6
6	IO_L285N	AB1
6	IO_L285P	Y10
6	IO_L286N_Y	AB2
6	IO_L286P_Y	AA7
6	IO_VREF_L287N_Y	AA4
6	IO_L287P_Y	AA1
6	IO_L288N_YY	Y9[4]
6	IO_L288P_YY	AB4[5]
6	IO_L289N_YY	AA2
6	IO_L289P_YY	Y8
6	IO_L290N_Y	AA6
6	IO_L290P_Y	AA5
6	IO_L291N_Y	AB3[4]
6	IO_L291P_Y	Y7[5]
6	IO_L292N_Y	Y1
6	IO_L292P_Y	W10
6	IO_VREF_L293N_YY	Y5
6	IO_L293P_YY	Y2
6	IO_L294N_YY	W9[4]
6	IO_L294P_YY	W2[5]
6	IO_L295N_YY	W7
6	IO_L295P_YY	Y4
6	IO_L296N_Y	W1
6	IO_L296P_Y	Y6
6	IO_L297N_Y	W6[4]
6	IO_L297P_Y	W3[5]
6	IO_L298N_Y	V9
6	IO_L298P_Y	W4

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
32	0	B14	E14	3200 2600 2000 1600 1000	-
33	0	D14	G15	3200 2600 2000 1600 1000	VREF
34	0	D15	J16	3200 1600	-
35	0	B15	F15	3200 2000 1000	-
36	0	E15	A15	3200 2000 1000	-
37	0	A16	G16	3200 2600	-
38	0	J17	F16	3200 2600 2000 1600 1000	-
39	0	B16	C16	3200 2600 2000 1600 1000	VREF
40	0	A17	H17	2600 1600 1000	-
41	0	B17	G17	2600 1600 1000	VREF
42	1	J18	C17	None	IO_LVDS_DLL
43	1	C18	G18	2600 1600 1000	VREF
44	1	F18	H18	2600 1600 1000	-
45	1	A19	B19	3200 2600 2000 1600 1000	VREF
46	1	C19	K19	3200 2600 2000 1600 1000	-
47	1	E19	F19	3200 2600	-
48	1	J19	G19	3200 2000 1000	-
49	1	G20	A20	3200 2000 1000	-
50	1	F20	B20	3200 1600	-
51	1	E20	D20	3200 2600 2000 1600 1000	VREF
52	1	A21	H20	3200 2600 2000 1600 1000	-
53	1	J20	E21	3200	-
54	1	K20	D21	3200 2600 1000	-
55	1	H21	B21	3200 2600 1000	-
56	1	F21	G21	2000 1600	-
57	1	B22	A22	3200 2600 2000 1600 1000	VREF
58	1	C22	J21	3200 2600 2000 1600 1000	-
59	1	G22	D22	3200 2600 1000	-
60	1	A23	K21	3200 2000 1000	-
61	1	B23	F22	3200 2000 1000	-
62	1	H22	C23	3200 1600 1000	-
63	1	K22	D23	3200 2600 2000 1600 1000	-
64	1	J22	A24	3200 2600 2000 1600 1000	VREF
65	1	D24	H23	2600 1600 1000	-
66	1	E24	A25	2600 1600 1000	-
67	1	C25	A26	3200 2600 2000 1600 1000	VREF
68	1	B26	F24	3200 2600 2000 1600 1000	-
69	1	F25	K23	3200 2600	-
70	1	H24	C26	3200 2000 1000	VREF