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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1176
Number of Logic Elements/Cells	5292
Total RAM Bits	114688
Number of I/O	94
Number of Gates	306393
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-TFBGA, CSPBGA
Supplier Device Package	144-LCSBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv200e-7cs144c

For in-circuit debugging, an optional download and readback cable is available. This cable connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can single-step the logic, readback the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.

Configuration

Virtex-E devices are configured by loading configuration data into the internal configuration memory. Note that attempting to load an incorrect bitstream causes configuration to fail and can damage the device.

Some of the pins used for configuration are dedicated pins, while others can be re-used as general purpose inputs and outputs once configuration is complete.

The following are dedicated pins:

- Mode pins (M2, M1, M0)
- Configuration clock pin (CCLK)
- $\overline{\text{PROGRAM}}$ pin
- DONE pin
- Boundary Scan pins (TDI, TDO, TMS, TCK)

Depending on the configuration mode chosen, CCLK can be an output generated by the FPGA, or can be generated externally and provided to the FPGA as an input. The $\overline{\text{PROGRAM}}$ pin must be pulled High prior to reconfiguration.

Note that some configuration pins can act as outputs. For correct operation, these pins require a V_{CCO} of 3.3 V or 2.5 V. At 3.3 V the pins operate as LVTTL, and at 2.5 V they operate as LVCMOS. All affected pins fall in banks 2 or 3. The configuration pins needed for SelectMap (CS, Write) are located in bank 1.

Configuration Modes

Virtex-E supports the following four configuration modes.

- Slave-serial mode
- Master-serial mode
- SelectMAP mode
- Boundary Scan mode (JTAG)

The Configuration mode pins (M2, M1, M0) select among these configuration modes with the option in each case of having the IOB pins either pulled up or left floating prior to configuration. The selection codes are listed in Table 8.

Configuration through the Boundary Scan port is always available, independent of the mode selection. Selecting the Boundary Scan mode simply turns off the other modes. The three mode pins have internal pull-up resistors, and default to a logic High if left unconnected. However, it is recommended to drive the configuration mode pins externally.

Table 8: **Configuration Codes**

Configuration Mode	M2[1]	M1	M0	CCLK Direction	Data Width	Serial D_{out}	Configuration Pull-ups[1]
Master-serial mode	0	0	0	Out	1	Yes	No
Boundary Scan mode	1	0	1	N/A	1	No	No
SelectMAP mode	1	1	0	In	8	No	No
Slave-serial mode	1	1	1	In	1	Yes	No
Master-serial mode	1	0	0	Out	1	Yes	Yes
Boundary Scan mode	0	0	1	N/A	1	No	Yes
SelectMAP mode	0	1	0	In	8	No	Yes
Slave-serial mode	0	1	1	In	1	Yes	Yes

Notes:
1. M2 is sampled continuously from power up until the end of the configuration. Toggling M2 while INIT is being held externally Low can cause the configuration pull-up settings to change.

Initialization in Verilog and Synopsys

The block SelectRAM+ structures can be initialized in Verilog for both simulation and synthesis for inclusion in the EDIF output file. The simulation of the Verilog code uses a defparam to pass the initialization. The Synopsys FPGA compiler does not presently support defparam. The initialization values instead attach as attributes to the RAM by a built-in Synopsys dc_script. The translate_off statement stops synthesis translation of the defparam statements. The following code illustrates a module that employs these techniques.

Design Examples

Creating a 32-bit Single-Port RAM

The true dual-read/write port functionality of the block SelectRAM+ memory allows a single port, 128 deep by 32-bit wide RAM to be created using a single block SelectRAM+ cell as shown in Figure 35.

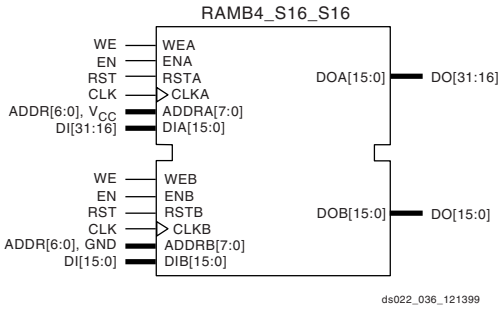

Figure 35: **Single Port 128 x 32 RAM**

Interleaving the memory space, setting the LSB of the address bus of Port A to 1 (V_{CC}), and the LSB of the address bus of Port B to 0 (GND), allows a 32-bit wide single port RAM to be created.

Creating Two Single-Port RAMs

The true dual-read/write port functionality of the block SelectRAM+ memory allows a single RAM to be split into two single port memories of 2K bits each as shown in Figure 36.

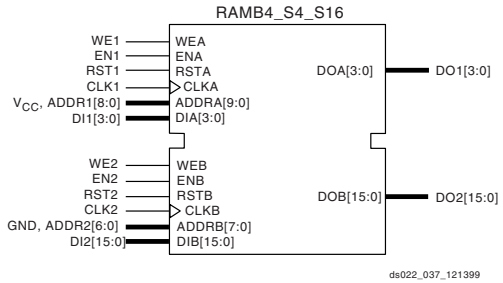

Figure 36: **512 x 4 RAM and 128 x 16 RAM**

In this example, a 512K x 4 RAM (Port A) and a 128 x 16 RAM (Port B) are created out of a single block SelectRAM+. The address space for the RAM is split by fixing the MSB of Port A to 1 (V_{CC}) for the upper 2K bits and the MSB of Port B to 0 (GND) for the lower 2K bits.

Block Memory Generation

The CoreGen program generates memory structures using the block SelectRAM+ features. This program outputs VHDL or Verilog simulation code templates and an EDIF file for inclusion in a design.

VHDL Initialization Example

```
library IEEE;
use IEEE.std_logic_1164.all;

entity MYMEM is
port (CLK, WE:in std_logic;
ADDR: in std_logic_vector(8 downto 0);
DIN: in std_logic_vector(7 downto 0);
DOUT: out std_logic_vector(7 downto 0));
end MYMEM;

architecture BEHAVE of MYMEM is
signal logic0, logic1: std_logic;

component RAMB4_S8
--synopsys translate_off
generic( INIT_00,INIT_01, INIT_02, INIT_03, INIT_04, INIT_05, INIT_06, INIT_07,
INIT_08, INIT_09, INIT_0a, INIT_0b, INIT_0c, INIT_0d, INIT_0e, INIT_0f : BIT_VECTOR(255
downto 0)
:= X"0000000000000000000000000000000000000000000000000000000000000000");
--synopsys translate_on
port (WE, EN, RST, CLK: in STD_LOGIC;
ADDR: in STD_LOGIC_VECTOR(8 downto 0);
DI: in STD_LOGIC_VECTOR(7 downto 0);
DO: out STD_LOGIC_VECTOR(7 downto 0));
end component;

--synopsys dc_script_begin
--set_attribute ram0 INIT_00
"0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF" -type string
--set_attribute ram0 INIT_01
"FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210" -type string
--synopsys dc_script_end

begin
logic0 <='0';
logic1 <='1';

ram0: RAMB4_S8
--synopsys translate_off
generic map (

INIT_00 => X"0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF",
INIT_01 => X"FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210")
--synopsys translate_on
port map (WE=>WE, EN=>logic1, RST=>logic0, CLK=>CLK,ADDR=>ADDR, DI=>DIN, DO=>DOUT);

end BEHAVE;
```

standard requires a Differential Amplifier input buffer and a Push-Pull output buffer.

SSTL3 — Stub Series Terminated Logic for 3.3V

The Stub Series Terminated Logic for 3.3V, or SSTL3 standard is a general purpose 3.3V memory bus standard also sponsored by Hitachi and IBM (JESD8-8). This standard has two classes, I and II. SelectI/O devices support both classes for the SSTL3 standard. This standard requires a Differential Amplifier input buffer and an Push-Pull output buffer.

SSTL2 — Stub Series Terminated Logic for 2.5V

The Stub Series Terminated Logic for 2.5V, or SSTL2 standard is a general purpose 2.5V memory bus standard sponsored by Hitachi and IBM (JESD8-9). This standard has two classes, I and II. SelectI/O devices support both classes for the SSTL2 standard. This standard requires a Differential Amplifier input buffer and an Push-Pull output buffer.

CTT — Center Tap Terminated

The Center Tap Terminated, or CTT standard is a 3.3V memory bus standard sponsored by Fujitsu (JESD8-4). This standard requires a Differential Amplifier input buffer and a Push-Pull output buffer.

AGP-2X — Advanced Graphics Port

The Intel AGP standard is a 3.3V Advanced Graphics Port-2X bus standard used with the Pentium II processor for graphics applications. This standard requires a Push-Pull output buffer and a Differential Amplifier input buffer.

LVDS — Low Voltage Differential Signal

LVDS is a differential I/O standard. It requires that one data bit is carried through two signal lines. As with all differential signaling standards, LVDS has an inherent noise immunity over single-ended I/O standards. The voltage swing between two signal lines is approximately 350mV. The use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}) is not required. LVDS requires the use of two pins per input or output. LVDS requires external resistor termination.

BLVDS — Bus LVDS

This standard allows for bidirectional LVDS communication between two or more devices. The external resistor termination is different than the one for standard LVDS.

LVPECL — Low Voltage Positive Emitter Coupled Logic

LVPECL is another differential I/O standard. It requires two signal lines for transmitting one data bit. This standard specifies two pins per input or output. The voltage swing between these two signal lines is approximately 850 mV. The use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}) is not required. The LVPECL standard requires external resistor termination.

Library Symbols

The Xilinx library includes an extensive list of symbols designed to provide support for the variety of SelectI/O features. Most of these symbols represent variations of the five generic SelectI/O symbols.

- IBUF (input buffer)
- IBUFG (global clock input buffer)
- OBUF (output buffer)
- OBUFT (3-state output buffer)
- IOBUF (input/output buffer)

IBUF

Signals used as inputs to the Virtex-E device must source an input buffer (IBUF) via an external input port. The generic Virtex-E IBUF symbol appears in Figure 37. The extension

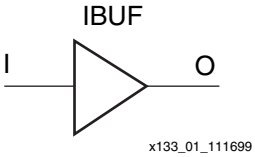

Figure 37: **Input Buffer (IBUF) Symbols**

to the base name defines which I/O standard the IBUF uses. The assumed standard is LVTTL when the generic IBUF has no specified extension.

The following list details the variations of the IBUF symbol:

- IBUF
- IBUF_LVCMOS2
- IBUF_PCI33_3
- IBUF_PCI66_3
- IBUF_GTL
- IBUF_GTLP
- IBUF_HSTL_I
- IBUF_HSTL_III
- IBUF_HSTL_IV
- IBUF_SSTL3_I
- IBUF_SSTL3_II
- IBUF_SSTL2_I
- IBUF_SSTL2_II
- IBUF_CTT
- IBUF_AGP
- IBUF_LVCMOS18
- IBUF_LVDS
- IBUF_LVPECL

When the IBUF symbol supports an I/O standard that requires a V_{REF}, the IBUF automatically configures as a differential amplifier input buffer. The V_{REF} voltage must be supplied on the V_{REF} pins. In the case of LVDS, LVPECL, and BLVDS, V_{REF} is not required.

Table 42: **Input Library Macros**

Name	Inputs	Outputs
IBUFDS_FD_LVDS	I, IB, C	Q
IBUFDS_FDE_LVDS	I, IB, CE, C	Q
IBUFDS_FDC_LVDS	I, IB, C, CLR	Q
IBUFDS_FDCE_LVDS	I, IB, CE, C, CLR	Q
IBUFDS_FDP_LVDS	I, IB, C, PRE	Q
IBUFDS_FDPE_LVDS	I, IB, CE, C, PRE	Q
IBUFDS_FDR_LVDS	I, IB, C, R	Q
IBUFDS_FDRE_LVDS	I, IB, CE, C, R	Q
IBUFDS_FDS_LVDS	I, IB, C, S	Q
IBUFDS_FDSE_LVDS	I, IB, CE, C, S	Q
IBUFDS_LD_LVDS	I, IB, G	Q
IBUFDS_LDE_LVDS	I, IB, GE, G	Q
IBUFDS_LDC_LVDS	I, IB, G, CLR	Q
IBUFDS_LDCE_LVDS	I, IB, GE, G, CLR	Q
IBUFDS_LDP_LVDS	I, IB, G, PRE	Q
IBUFDS_LDPE_LVDS	I, IB, GE, G, PRE	Q

Creating LVDS Output Buffers

LVDS output buffers can be placed in a wide number of IOB locations. The exact locations are dependent on the package used. The Virtex-E package information lists the possible locations as IO_L#P for the P-side and IO_L#N for the N-side, where # is the pair number.

HDL Instantiation

Both output buffers are required to be instantiated in the design and placed on the correct IO_L#P and IO_L#N locations. The IOB must have the same net source the following pins, clock (C), set/reset (SR), output (O), output clock enable (OCE). In addition, the output (O) pins must be inverted with respect to each other, and if output registers are used, the INIT states must be opposite values (one HIGH and one LOW). Failure to follow these rules leads to DRC errors in software.

VHDL Instantiation

```
data0_p  : OBUF_LVDS port map
(I=>data_int(0),   O=>data_p(0));

data0_inv: INV       port map
(I=>data_int(0),   O=>data_n_int(0));

data0_n  : OBUF_LVDS port map
(I=>data_n_int(0), O=>data_n(0));
```

Verilog Instantiation

```
OBUF_LVDS data0_p   (.I(data_int[0]),
.O(data_p[0]));

INV       data0_inv (.I(data_int[0],
.O(data_n_int[0]);

OBUF_LVDS data0_n   (.I(data_n_int[0]),
.O(data_n[0]));
```

Location Constraints

All LVDS buffers must be explicitly placed on a device. For the output buffers this can be done with the following constraint in the .ucf or .ncf file.

```
NET data_p<0> LOC = D28; # IO_L0P

NET data_n<0> LOC = B29; # IO_L0N
```

Synchronous vs. Asynchronous Outputs

If the outputs are synchronous (registered in the IOB) then any IO_L#P|N pair can be used. If the outputs are asynchronous (no output register), then they must use one of the pairs that are part of the same IOB group at the end of a ROW or COLUMN in the device.

The LVDS pairs that can be used as asynchronous outputs are listed in the Virtex-E pinout tables. Some pairs are marked as asynchronous-capable for all devices in that package, and others are marked as available only for that device in the package. If the device size might change at some point in the product lifetime, then only the common pairs for all packages should be used.

Adding an Output Register

All LVDS buffers can have an output register in the IOB. The output registers must be in both the P-side and N-side IOBs. All the normal IOB register options are available (FD, FDE, FDC, FDCE, FDP, FDPE, FDR, FDRE, FDS, FDSE, LD, LDE, LDC, LDCE, LDP, LDPE). The register elements can be inferred or explicitly instantiated in the HDL code.

Special care must be taken to insure that the D pins of the registers are inverted and that the INIT states of the registers are opposite. The clock pin (C), clock enable (CE) and set/reset (CLR/PRE or S/R) pins must connect to the same source. Failure to do this leads to a DRC error in the software.

The register elements can be packed in the IOB using the IOB property to TRUE on the register or by using the “map -pr [i|o|b]” where “i” is inputs only, “o” is outputs only and “b” is both inputs and outputs.

To improve design coding times VHDL and Verilog synthesis macro libraries have been developed to explicitly create these structures. The output library macros are listed in Table 43. The O and OB inputs to the macros are the external net connections.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply. This is the time required to reach the nominal power supply voltage of the device[1] from 0V. The fastest ramp rate is 0V to nominal voltage in 2 ms, and the slowest allowed ramp rate is 0V to nominal voltage in 50 ms. For more details on power supply requirements, see XAPP158 on www.xilinx.com.

Product (Commercial Grade)	Description(2)	Current Requirement(3)
XCV50E - XCV600E	Minimum required current supply	500 mA
XCV812E - XCV2000E	Minimum required current supply	1 A
XCV2600E - XCV3200E	Minimum required current supply	1.2 A
Virtex-E Family, Industrial Grade	Minimum required current supply	2 A

Notes:
1. Ramp rate used for this specification is from 0 - 1.8 V DC. Peak current occurs on or near the internal power-on reset threshold and lasts for less than 3 ms.
2. Devices are guaranteed to initialize properly with the minimum current available from the power supply as noted above.
3. Larger currents might result if ramp rates are forced to be faster.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTL(1)	– 0.5	0.8	2.0	3.6	0.4	2.4	24	– 24
LVCMOS2	– 0.5	0.7	1.7	2.7	0.4	1.9	12	– 12
LVCMOS18	– 0.5	35% V_{CCO}	65% V_{CCO}	1.95	0.4	V_{CCO} – 0.4	8	– 8
PCI, 3.3 V	– 0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
GTL	– 0.5	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	n/a	40	n/a
GTL+	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	n/a	36	n/a
HSTL I(3)	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	8	–8
HSTL III	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	24	–8
HSTL IV	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	48	–8
SSTL3 I	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.6	V_{REF} + 0.6	8	–8
SSTL3 II	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.8	V_{REF} + 0.8	16	–16
SSTL2 I	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.61	V_{REF} + 0.61	7.6	–7.6
SSTL2 II	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.80	V_{REF} + 0.80	15.2	–15.2

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used, see Figure 2. The values listed below are worst-case. Precise values are provided by the timing analyzer.

Description	Symbol	Speed Grade(1)				Units
		Min	-8	-7	-6	
Combinatorial Delays						
4-input function: F/G inputs to X/Y outputs	T_{ILO}	0.19	0.40	0.42	0.47	ns, max
5-input function: F/G inputs to F5 output	T_{IF5}	0.36	0.76	0.8	0.9	ns, max
5-input function: F/G inputs to X output	T_{IF5X}	0.35	0.74	0.8	0.9	ns, max
6-input function: F/G inputs to Y output via F6 MUX	T_{IF6Y}	0.35	0.74	0.9	1.0	ns, max
6-input function: F5IN input to Y output	T_{F5INY}	0.04	0.11	0.20	0.22	ns, max
Incremental delay routing through transparent latch to XQ/YQ outputs	T_{IFNCTL}	0.27	0.63	0.7	0.8	ns, max
BY input to YB output	T_{BYYB}	0.19	0.38	0.46	0.51	ns, max
Sequential Delays						
FF Clock CLK to XQ/YQ outputs	T_{CKO}	0.34	0.78	0.9	1.0	ns, max
Latch Clock CLK to XQ/YQ outputs	T_{CKLO}	0.40	0.77	0.9	1.0	ns, max
Setup and Hold Times before/after Clock CLK						
4-input function: F/G Inputs	T_{ICK} / T_{CKI}	0.39 / 0	0.9 / 0	1.0 / 0	1.1 / 0	ns, min
5-input function: F/G inputs	T_{IF5CK} / T_{CKIF5}	0.55 / 0	1.3 / 0	1.4 / 0	1.5 / 0	ns, min
6-input function: F5IN input	T_{F5INCK} / T_{CKF5IN}	0.27 / 0	0.6 / 0	0.8 / 0	0.8 / 0	ns, min
6-input function: F/G inputs via F6 MUX	T_{IF6CK} / T_{CKIF6}	0.58 / 0	1.3 / 0	1.5 / 0	1.6 / 0	ns, min
BX/BY inputs	T_{DICK} / T_{CKDI}	0.25 / 0	0.6 / 0	0.7 / 0	0.8 / 0	ns, min
CE input	T_{CECK} / T_{CKCE}	0.28 / 0	0.55 / 0	0.7 / 0	0.7 / 0	ns, min
SR/BY inputs (synchronous)	T_{RCK} / T_{CKR}	0.24 / 0	0.46 / 0	0.52 / 0	0.6 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T_{CH}	0.56	1.2	1.3	1.4	ns, min
Minimum Pulse Width, Low	T_{CL}	0.56	1.2	1.3	1.4	ns, min
Set/Reset						
Minimum Pulse Width, SR/BY inputs	T_{RPW}	0.94	1.9	2.1	2.4	ns, min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T_{RQ}	0.39	0.8	0.9	1.0	ns, max
Toggle Frequency (MHz) (for export control)	F_{TOG}	-	416	400	357	MHz

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Block RAM Switching Characteristics

Description	Symbol	Speed Grade(1)				Units
		Min	-8	-7	-6	
Sequential Delays						
Clock CLK to DOUT output	T_{BCKO}	0.63	2.46	3.1	3.5	ns, max
Setup and Hold Times before Clock CLK						
ADDR inputs	T_{BACK}/T_{BCKA}	0.42 / 0	0.9 / 0	1.0 / 0	1.1 / 0	ns, min
DIN inputs	T_{BDCK}/T_{BCKD}	0.42 / 0	0.9 / 0	1.0 / 0	1.1 / 0	ns, min
EN input	T_{BECK}/T_{BCKE}	0.97 / 0	2.0 / 0	2.2 / 0	2.5 / 0	ns, min
RST input	T_{BRCK}/T_{BCKR}	0.9 / 0	1.8 / 0	2.1 / 0	2.3 / 0	ns, min
WEN input	T_{BWCK}/T_{BCKW}	0.86 / 0	1.7 / 0	2.0 / 0	2.2 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T_{BPWH}	0.6	1.2	1.35	1.5	ns, min
Minimum Pulse Width, Low	T_{BPWL}	0.6	1.2	1.35	1.5	ns, min
CLKA -> CLKB setup time for different ports	T_{BCCS}	1.2	2.4	2.7	3.0	ns, min

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

TBUF Switching Characteristics

Description	Symbol	Speed Grade				Units
		Min	-8	-7	-6	
Combinatorial Delays						
IN input to OUT output	T_{IO}	0.0	0.0	0.0	0 .0	ns, max
TRI input to OUT output high-impedance	T_{OFF}	0.05	0.092	0.10	0.11	ns, max
TRI input to valid data on OUT output	T_{ON}	0.05	0.092	0.10	0.11	ns, max

JTAG Test Access Port Switching Characteristics

Description	Symbol	Value	Units
TMS and TDI Setup times before TCK	T_{TAPTK}	4.0	ns, min
TMS and TDI Hold times after TCK	T_{TCKTAP}	2.0	ns, min
Output delay from clock TCK to output TDO	T_{TCKTDO}	11.0	ns, max
Maximum TCK clock frequency	F_{TCK}	33	MHz, max

Date	Version	Revision
07/23/01	2.2	• Under **Absolute Maximum Ratings**, changed (T_{SOL}) to 220 °C. • Changes made to SSTL symbol names in **IOB Input Switching Characteristics Standard Adjustments** table.
07/26/01	2.3	• Removed T_{SOL} parameter and added footnote to **Absolute Maximum Ratings** table.
9/18/01	2.4	• Reworded power supplies footnote to **Absolute Maximum Ratings** table.
10/25/01	2.5	• Updated the speed grade designations used in data sheets, and added Table 1, which shows the current speed grade designation for each device. • Added XCV2600E and XCV3200E values to **DC Characteristics Over Recommended Operating Conditions** and **Power-On Power Supply Requirements** tables.
11/09/01	2.6	• Updated the **Power-On Power Supply Requirements** table.
02/01/02	2.7	• Updated footnotes to the **DC Input and Output Levels** and **DLL Clock Tolerance, Jitter, and Phase Information** tables.
07/17/02	2.8	• Data sheet designation upgraded from Preliminary to Production. • Removed mention of MIL-M-38510/605 specification. • Added link to XAPP158 from the **Power-On Power Supply Requirements** section.
09/10/02	2.9	• Revised V_{IN} in **Absolute Maximum Ratings** table. • Added Clock CLK switching characteristics to Table **2, "IOB Input Switching Characteristics," on page 6** and **IOB Output Switching Characteristics, Figure 1**.
12/22/02	2.9.1	• Added footnote regarding V_{IN} PCI compliance to **Absolute Maximum Ratings** table. • The fastest ramp rate is 0V to nominal voltage in 2 ms
03/14/03	2.9.2	• Under **Power-On Power Supply Requirements**, the fastest ramp rate is no longer a "suggested" rate.

Virtex-E Data Sheet

The Virtex-E Data Sheet contains the following modules:

- DS022-1, Virtex-E 1.8V FPGAs:
  Introduction and Ordering Information (Module 1)
- DS022-2, Virtex-E 1.8V FPGAs:
  Functional Description (Module 2)
- DS022-3, Virtex-E 1.8V FPGAs:
  DC and Switching Characteristics (Module 3)
- DS022-4, Virtex-E 1.8V FPGAs:
  Pinout Tables (Module 4)

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
7	IO_L165N_YY	P32	
7	IO_VREF_L165P_YY	P31	
7	IO_L166N_Y	P30	
7	IO_L166P_Y	P29	
7	IO_L167N_Y	M32	
7	IO_L167P_Y	N31	
7	IO_L168N_Y	N30	
7	IO_VREF_L168P_Y	L33	3
7	IO_L169N_Y	M31	
7	IO_L169P_Y	L32	
7	IO_L170N_Y	M30	
7	IO_L170P_Y	L31	
7	IO_L171N_YY	M29	
7	IO_L171P_YY	J33	
7	IO_L172N_YY	L30	
7	IO_VREF_L172P_YY	K31	
7	IO_L173N_Y	L29	
7	IO_L173P_Y	H33	
7	IO_L174N_Y	J31	
7	IO_VREF_L174P_Y	H32	4
7	IO_L175N_Y	K29	
7	IO_L175P_Y	H31	
7	IO_L176N_Y	J30	
7	IO_VREF_L176P_Y	G32	1
7	IO_L177N_YY	J29	
7	IO_VREF_L177P_YY	G31	
7	IO_L178N_Y	E33	
7	IO_L178P_Y	E32	
7	IO_L179N_Y	H29	
7	IO_L179P_Y	F31	
7	IO_L180N_Y	D32	
7	IO_VREF_L180P_Y	E31	
7	IO_L181N_Y	G29	
7	IO_L181P_Y	C33	
7	IO_L182N_Y	F30	

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
7	IO_VREF_L182P_Y	D31	3
2	CCLK	C4	
3	DONE	AJ5	
NA	DXN	AK29	
NA	DXP	AJ28	
NA	M0	AJ29	
NA	M1	AK30	
NA	M2	AN32	
NA	PROGRAM	AM1	
NA	TCK	E29	
NA	TDI	D5	
2	TDO	E6	
NA	TMS	B33	
NA	NC	C31	
NA	NC	AC2	
NA	NC	AK4	
NA	NC	AL3	
NA	VCCINT	A21	
NA	VCCINT	B12	
NA	VCCINT	B14	
NA	VCCINT	B18	
NA	VCCINT	B28	
NA	VCCINT	C22	
NA	VCCINT	C24	
NA	VCCINT	E9	
NA	VCCINT	E12	
NA	VCCINT	F2	
NA	VCCINT	H30	
NA	VCCINT	J1	
NA	VCCINT	K32	
NA	VCCINT	M3	
NA	VCCINT	N1	

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
NA	VCCINT	N29	
NA	VCCINT	N33	
NA	VCCINT	U5	
NA	VCCINT	U30	
NA	VCCINT	Y2	
NA	VCCINT	Y31	
NA	VCCINT	AB2	
NA	VCCINT	AB32	
NA	VCCINT	AD2	
NA	VCCINT	AD32	
NA	VCCINT	AG3	
NA	VCCINT	AG31	
NA	VCCINT	AJ13	
NA	VCCINT	AK8	
NA	VCCINT	AK11	
NA	VCCINT	AK17	
NA	VCCINT	AK20	
NA	VCCINT	AL14	
NA	VCCINT	AL22	
NA	VCCINT	AL27	
NA	VCCINT	AN25	
0	VCCO	A22	
0	VCCO	A26	
0	VCCO	A30	
0	VCCO	B19	
0	VCCO	B32	
1	VCCO	A10	
1	VCCO	A16	
1	VCCO	B13	
1	VCCO	C3	
1	VCCO	E5	
2	VCCO	B2	
2	VCCO	D1	
2	VCCO	H1	

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
2	VCCO	M1	
2	VCCO	R2	
3	VCCO	V1	
3	VCCO	AA2	
3	VCCO	AD1	
3	VCCO	AK1	
3	VCCO	AL2	
4	VCCO	AN4	
4	VCCO	AN8	
4	VCCO	AN12	
4	VCCO	AM2	
4	VCCO	AM15	
5	VCCO	AL31	
5	VCCO	AM21	
5	VCCO	AN18	
5	VCCO	AN24	
5	VCCO	AN30	
6	VCCO	W32	
6	VCCO	AB33	
6	VCCO	AF33	
6	VCCO	AK33	
6	VCCO	AM32	
7	VCCO	C32	
7	VCCO	D33	
7	VCCO	K33	
7	VCCO	N32	
7	VCCO	T33	
NA	GND	A1	
NA	GND	A7	
NA	GND	A12	
NA	GND	A14	
NA	GND	A18	
NA	GND	A20	
NA	GND	A24	

Table 15: **BG560 Differential Pin Pair Summary**
XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
47	2	F4	C1	14	-
48	2	G5	E3	15	VREF
49	2	D2	G4	16	-
50	2	H5	E2	15	-
51	2	H4	G3	√	VREF
52	2	J5	F1	17	VREF
53	2	J4	H3	14	-
54	2	K5	H2	18	VREF
55	2	J3	K4	19	-
56	2	L5	K3	√	D1
57	2	L4	K2	√	D2
58	2	M5	L3	17	-
59	2	L1	M4	14	-
60	2	N5	M2	15	VREF
61	2	N4	N3	16	-
62	2	N2	P5	15	-
63	2	P4	P3	√	D3
64	2	P2	R5	17	-
65	2	R4	R3	14	-
66	2	R1	T4	18	VREF
67	2	T5	T3	19	VREF
68	2	T2	U3	√	-
69	3	U1	U2	19	VREF
70	3	V2	V4	18	VREF
71	3	V5	V3	14	-
72	3	W1	W3	17	-
73	3	W4	W5	√	VREF
74	3	Y3	Y4	15	-
75	3	AA1	Y5	16	-
76	3	AA3	AA4	15	VREF
77	3	AB3	AA5	14	-

Table 15: **BG560 Differential Pin Pair Summary**
XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
78	3	AC1	AB4	17	-
79	3	AC3	AB5	√	D5
80	3	AC4	AD3	√	VREF
81	3	AE1	AC5	4	-
82	3	AD4	AF1	18	VREF
83	3	AF2	AD5	14	-
84	3	AG2	AE4	20	VREF
85	3	AH1	AE5	√	VREF
86	3	AF4	AJ1	15	-
87	3	AJ2	AF5	14	-
88	3	AG4	AK2	15	VREF
89	3	AJ3	AG5	14	-
90	3	AL1	AH4	14	VREF
91	3	AJ4	AH5	√	INIT
92	4	AL4	AJ6	√	-
93	4	AK5	AN3	8	VREF
94	4	AL5	AJ7	√	-
95	4	AM4	AM5	√	VREF
96	4	AK7	AL6	3	-
97	4	AM6	AN6	√	-
98	4	AL7	AJ9	√	VREF
99	4	AN7	AL8	9	VREF
100	4	AM8	AJ10	7	-
101	4	AL9	AM9	7	VREF
102	4	AK10	AN9	2	-
103	4	AL10	AM10	√	VREF
104	4	AL11	AJ12	√	-
105	4	AN11	AK12	8	-
106	4	AL12	AM12	√	-
107	4	AK13	AL13	√	VREF
108	4	AM13	AN13	3	-

Table 25: **FG860 Differential Pin Pair Summary XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
120	3	AH1	AL5	1	-
121	3	AH2	AM4	3	-
122	3	AH3	AM5	√	D5
123	3	AJ1	AN3	√	VREF
124	3	AN4	AJ3	2	-
125	3	AN5	AK1	√	-
126	3	AK2	AP4	√	VREF
127	3	AK3	AP5	2	-
128	3	AR3	AL2	5	VREF
129	3	AR4	AL3	√	-
130	3	AM1	AT3	√	VREF
131	3	AM2	AT4	1	-
132	3	AT5	AN1	2	-
133	3	AU3	AN2	√	-
134	3	AP1	AP2	1	VREF
135	3	AR1	AV3	2	-
136	3	AR2	AT1	4	-
137	3	AV4	AT2	2	VREF
138	3	AU1	AU5	1	-
139	3	AU2	AW3	3	-
140	3	AV1	AW5	√	INIT
141	4	AV6	BA4	√	-
142	4	AY4	BA5	2	-
143	4	AW6	BB5	1	-
144	4	BA6	AY5	1	VREF
145	4	BB6	AY6	5	-
146	4	BA7	AV7	√	-
147	4	BB7	AW7	√	VREF
148	4	AY7	BB8	5	-
149	4	BA9	AV8	5	-
150	4	AW8	BA10	√	-
151	4	BB10	AY8	√	VREF
152	4	AV9	BA11	1	-
153	4	BB11	AW9	1	VREF

Table 25: **FG860 Differential Pin Pair Summary XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
154	4	AY9	BA12	√	-
155	4	BB12	AV10	√	VREF
156	4	BA13	AW10	2	-
157	4	BB13	AY10	2	-
158	4	AV11	BA14	√	VREF
159	4	AW11	BB14	√	-
160	4	AV12	BA15	2	-
161	4	AW12	AY15	1	-
162	4	AW13	BB15	1	-
163	4	AV14	BA16	5	-
164	4	AW14	AY16	√	-
165	4	BB16	AV15	√	VREF
166	4	AY17	AW15	5	-
167	4	BB17	AU16	5	-
168	4	AV16	AY18	√	-
169	4	AW16	BA18	√	VREF
170	4	BB19	AW17	1	-
171	4	AY19	AV18	1	-
172	4	AW18	BB20	√	-
173	4	AY20	AV19	√	VREF
174	4	BB21	AW19	2	-
175	4	AY21	AV20	2	VREF
176	5	AW20	AW21	NA	IO_LVDS_DLL
177	5	BB22	AW22	2	VREF
178	5	BB23	AW23	2	-
179	5	AV23	BA23	√	VREF
180	5	AW24	BB24	√	-
181	5	AY24	AW25	1	-
182	5	BA24	AV25	1	-
183	5	AW26	AY25	√	VREF
184	5	AV26	BA25	√	-
185	5	BB26	AV27	5	-
186	5	AY26	AU27	5	-
187	5	AW28	BB27	√	VREF

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
4	IO_L154N	AG23
4	IO_L155P_YY	AF22
4	IO_L155N_YY	AE22
4	IO_VREF_L156P_YY	AJ22
4	IO_L156N_YY	AG22
4	IO_L157P	AK24[4]
4	IO_L157N	AD20[3]
4	IO_L158P_YY	AA19
4	IO_L158N_YY	AF21
4	IO_L159P	AH22[4]
4	IO_VREF_L159N	AA18
4	IO_L160P	AG21
4	IO_L160N	AK23
4	IO_L161P_YY	AH21[4]
4	IO_L161N_YY	AD19[4]
4	IO_L162P	AE20
4	IO_L162N	AJ21
4	IO_L163P	AG20
4	IO_L163N	AF20
4	IO_L164P	AC18[4]
4	IO_L164N	AF19[4]
4	IO_L165P_YY	AJ20
4	IO_L165N_YY	AE19
4	IO_VREF_L166P_YY	AK22[1]
4	IO_L166N_YY	AH20
4	IO_L167P	AG19
4	IO_L167N	AB17
4	IO_L168P	AJ19
4	IO_L168N	AD17
4	IO_L169P_YY	AA16
4	IO_L169N_YY	AA17
4	IO_VREF_L170P_YY	AK21
4	IO_L170N_YY	AB16
4	IO_L171P	AG18
4	IO_L171N	AK20
4	IO_L172P	AK19
4	IO_L172N	AD16

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
4	IO_L173P_YY	AE16
4	IO_L173N_YY	AE17
4	IO_VREF_L174P_YY	AG17
4	IO_L174N_YY	AJ17
4	IO_L175P	AD15[4]
4	IO_L175N	AH17[3]
4	IO_VREF_L176P_YY	AG16[2]
4	IO_L176N_YY	AK17
4	IO_LVDS_DLL_L177P	AF16
5	GCK1	AK16
5	IO	AA11[4]
5	IO	AA14[4]
5	IO	AD14[4]
5	IO	AE7[5]
5	IO	AE8[5]
5	IO	AE10[4]
5	IO	AF6[4]
5	IO	AF10[4]
5	IO	AG9[4]
5	IO	AG12[4]
5	IO	AG14[5]
5	IO	AH8[4]
5	IO	AK6[5]
5	IO	AK14[5]
5	IO	AJ13[4]
5	IO	AJ15[4]
5	IO_LVDS_DLL_L177N	AH16
5	IO_L178P_YY	AC15[4]
5	IO_VREF_L178N_YY	AG15[2,3]
5	IO_L179P_YY	AB15
5	IO_L179N_YY	AF15
5	IO_L180P_YY	AA15
5	IO_VREF_L180N_YY	AF14
5	IO_L181P_YY	AH15
5	IO_L181N_YY	AK15
5	IO_L182P	AB14

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
6	IO	AC5[4]
6	IO	AD1[4]
6	IO	AE5[5]
6	IO_L212N_YY	AF3
6	IO_L212P_YY	AC6
6	IO_L213N	AH2[4]
6	IO_L213P	AG2[3]
6	IO_L214N	AB9
6	IO_L214P	AE4
6	IO_VREF_L215N_YY	AE3[1]
6	IO_L215P_YY	AH1
6	IO_L216N_Y	AB8[4]
6	IO_L216P_Y	AD6[3]
6	IO_L217N_YY	AG1
6	IO_L217P_YY	AA10
6	IO_VREF_L218N	AA9
6	IO_L218P	AD4
6	IO_L219N_YY	AD5
6	IO_L219P_YY	AD2
6	IO_L220N_YY	AD3
6	IO_L220P_YY	AF2
6	IO_L221N	AA8
6	IO_L221P	AA7
6	IO_VREF_L222N_YY	AF1
6	IO_L222P_YY	Y9
6	IO_L223N_YY	AB6
6	IO_L223P_YY	AC4
6	IO_L224N	AE1
6	IO_L224P	W8
6	IO_L225N_YY	Y8
6	IO_L225P_YY	AB4
6	IO_VREF_L226N_YY	AB3
6	IO_L226P_YY	W9
6	IO_L227N_YY	AA5[4]
6	IO_L227P_YY	W10[3]
6	IO_L228N_YY	AB1
6	IO_L228P_YY	V10

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
6	IO_L229N_YY	Y7[4]
6	IO_VREF_L229P_YY	AC1
6	IO_L230N	V11
6	IO_L230P	AA3
6	IO_L231N_YY	AA2[3]
6	IO_L231P_YY	U10[4]
6	IO_L232N	W7
6	IO_L232P	AA6
6	IO_L233N_YY	Y6
6	IO_L233P_YY	Y4
6	IO_L234N_Y	AA1[4]
6	IO_L234P_Y	V7[4]
6	IO_L235N_YY	Y3
6	IO_L235P_YY	Y2
6	IO_VREF_L236N	Y5[1]
6	IO_L236P	W5
6	IO_L237N_YY	W4
6	IO_L237P_YY	W6
6	IO_L238N_YY	V6
6	IO_L238P_YY	W2
6	IO_L239N	U9
6	IO_L239P	V4
6	IO_VREF_L240N_YY	AB2
6	IO_L240P_YY	T8
6	IO_L241N_YY	U5
6	IO_L241P_YY	W1
6	IO_L242N	Y1
6	IO_L242P	T9
6	IO_L243N_YY	T7
6	IO_L243P_YY	U3
6	IO_VREF_L244N_YY	T5
6	IO_L244P_YY	V2
6	IO_L245N_YY	R9[4]
6	IO_L245P_YY	T6[3]
6	IO_VREF_L246N_YY	T4[2]
6	IO_L246P_YY	U2
6	IO_L247N	T1

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
7	IO_L275N_YY	G3
7	IO_L275P_YY	E1
7	IO_L276N_YY	H6
7	IO_L276P_YY	E2
7	IO_L277N	E4
7	IO_VREF_L277P	K9
7	IO_L278N_YY	J8
7	IO_L278P_YY	F4
7	IO_L279N_Y	D1[3]
7	IO_L279P_Y	H7[4]
7	IO_L280N_YY	G6
7	IO_VREF_L280P_YY	C2[1]
7	IO_L281N	D2
7	IO_L281P	F5
7	IO_L282N_YY	D3[4]
7	IO_L282P_YY	K10[3]
2	CCLK	F26
3	DONE	AJ28
NA	DXN	AJ3
NA	DXP	AH4
NA	M0	AF4
NA	M1	AC7
NA	M2	AK3
NA	PROGRAM	AG28
NA	TCK	B3
NA	TDI	H22
2	TDO	D26
NA	TMS	C1
NA	VCCINT	L11
NA	VCCINT	L12
NA	VCCINT	L19
NA	VCCINT	L20
NA	VCCINT	M11
NA	VCCINT	M12
NA	VCCINT	M19

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
NA	VCCINT	M20
NA	VCCINT	N13
NA	VCCINT	N14
NA	VCCINT	N15
NA	VCCINT	N16
NA	VCCINT	N17
NA	VCCINT	N18
NA	VCCINT	P13
NA	VCCINT	P18
NA	VCCINT	R13
NA	VCCINT	R18
NA	VCCINT	T13
NA	VCCINT	T18
NA	VCCINT	U13
NA	VCCINT	U18
NA	VCCINT	V13
NA	VCCINT	V14
NA	VCCINT	V15
NA	VCCINT	V16
NA	VCCINT	V17
NA	VCCINT	V18
NA	VCCINT	W11
NA	VCCINT	W12
NA	VCCINT	W19
NA	VCCINT	W20
NA	VCCINT	Y11
NA	VCCINT	Y12
NA	VCCINT	Y19
NA	VCCINT	Y20
NA	VCCO_0	B6
NA	VCCO_0	M15
NA	VCCO_0	M14
NA	VCCO_0	L15
NA	VCCO_0	L14
NA	VCCO_0	H14
NA	VCCO_0	M13

Table 27: **FG900 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
52	1	A22	C21	√	VREF
53	1	B22	H19	4	-
54	1	D22	E21	4	-
55	1	C22	F21	√	VREF
56	1	E22	H20	√	-
57	1	A23	G21	2	-
58	1	K19	A24	2	-
59	1	B24	C24	√	VREF
60	1	G22	H21	√	-
61	1	C25	E23	1	-
62	1	A26	D24	1	-
63	1	K20	B26	√	VREF
64	1	J21	D25	√	-
65	1	F23	C26	2	-
66	1	G23	B27	2	VREF
67	1	F24	A27	2	-
68	1	A28	B28	4	-
69	1	C27	K21	√	CS
70	2	J22	E27	√	DIN, D0
71	2	C29	D28	NA	-
72	2	G25	E25	1	-
73	2	E28	C30	4	VREF
74	2	K22	F27	3	-
75	2	D30	J23	4	-
76	2	L21	F28	1	VREF
77	2	G28	E30	√	-
78	2	G27	E29	4	-
79	2	K23	H26	1	-
80	2	F30	L22	√	VREF
81	2	H27	G29	√	-
82	2	G30	M21	2	-
83	2	J24	J26	4	-
84	2	H30	L23	4	VREF
85	2	K26	J28	4	-

Table 27: **FG900 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
86	2	J29	K24	4	-
87	2	K27	J30	4	VREF
88	2	M22	K29	NA	D2
89	2	K28	L25	4	-
90	2	N21	K25	1	-
91	2	L24	L27	4	-
92	2	L29	M23	3	-
93	2	L26	L28	4	-
94	2	L30	M27	1	VREF
95	2	M26	M29	√	-
96	2	N29	M30	4	-
97	2	N25	N27	1	-
98	2	N30	P21	√	D3
99	2	N26	P28	√	-
100	2	P29	N24	2	-
101	2	P22	R26	√	-
102	2	P25	R29	4	VREF
103	2	R21	R28	4	-
104	2	R25	T30	4	VREF
105	2	P24	R27	4	-
106	3	R24	U29	NA	
107	3	R22	T27	4	VREF
108	3	R23	T28	4	-
109	3	T21	T25	4	VREF
110	3	U28	U30	4	-
111	3	T23	U27	2	-
112	3	U25	V27	√	-
113	3	U24	V29	√	VREF
114	3	W30	U22	1	-
115	3	U21	W29	4	-
116	3	V26	W27	√	-
117	3	W26	Y29	1	VREF
118	3	W25	Y30	4	-
119	3	V24	Y28	3	-

Table 27: **FG900 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
256	7	N6	M6	1	-
257	7	N1	N5	4	-
258	7	M5	M4	√	-
259	7	M1	M2	1	VREF
260	7	L2	L4	4	-
261	7	L5	M7	3	-
262	7	M8	L1	4	-
263	7	M9	K2	1	-
264	7	M10	L3	NA	-
265	7	K1	K5	√	-
266	7	K3	L6	√	VREF
267	7	K4	L7	4	-
268	7	J5	L8	4	-
269	7	H4	K6	4	VREF
270	7	K7	H1	4	-
271	7	J2	J7	2	-
272	7	G2	H5	√	-
273	7	G5	L9	√	VREF
274	7	K8	F3	1	-
275	7	E1	G3	4	-
276	7	E2	H6	√	-
277	7	K9	E4	1	VREF
278	7	F4	J8	4	-
279	7	H7	D1	3	-
280	7	C2	G6	4	VREF
281	7	F5	D2	1	-
282	7	K10	D3	4	-

Notes:
1. AO in the XCV600E, 1000E.
2. AO in the XCV1000E.
3. AO in the XCV1600E.
4. AO in the XCV1000E, XCV1600E.

FG1156 Fine-Pitch Ball Grid Array Package

XCV1000E, XCV1600E, XCV2000E, XCV2600E, and XCV3200E devices in the FG1156 fine-pitch Ball Grid Array package have footprint compatibility. Pins labeled IO_VREF can be used as either V_{REF} or general I/O, unless indicated in the footnotes. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 28, see Table 29 for Differential Pair information.

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
0	GCK3	E17
0	IO	B4
0	IO	B9
0	IO	B10
0	IO	D9[3]
0	IO	D16
0	IO	E7[3]
0	IO	E11[3]
0	IO	E13[3]
0	IO	E16[3]
0	IO	F17[3]
0	IO	J12[3]
0	IO	J13[3]
0	IO	J14[3]
0	IO	K11[3]
0	IO_L0N_Y	F7
0	IO_L0P_Y	H9
0	IO_L1N_Y	C5
0	IO_L1P_Y	J10
0	IO_VREF_L2N_Y	E6
0	IO_L2P_Y	D6
0	IO_L3N_Y	A4
0	IO_L3P_Y	G8
0	IO_L4N_YY	C6
0	IO_L4P_YY	J11
0	IO_VREF_L5N_YY	G9
0	IO_L5P_YY	F8
0	IO_L6N_YY	A5[4]

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
2	IO_L126N_YY	T32
2	IO_VREF_L127P_Y	U29[1]
2	IO_L127N_Y	U33
2	IO_L128P_YY	V33
2	IO_L128N_YY	U31
3	IO	V27[3]
3	IO	V31
3	IO	V32[3]
3	IO	W33
3	IO	AB25[3]
3	IO	AB26[3]
3	IO	AB31[3]
3	IO	AC31[3]
3	IO	AF34
3	IO	AG31[3]
3	IO	AG33[3]
3	IO	AG34
3	IO	AH29[3]
3	IO	AJ30[3]
3	IO_L129P_Y	V26
3	IO_VREF_L129N_Y	V30[1]
3	IO_L130P_YY	W34
3	IO_L130N_YY	V28
3	IO_L131P_YY	W32
3	IO_VREF_L131N_YY	W30
3	IO_L132P_Y	V29
3	IO_L132N_Y	Y34
3	IO_L133P	W29[5]
3	IO_L133N	Y33[4]
3	IO_L134P_Y	W26
3	IO_L134N_Y	W28
3	IO_L135P_YY	Y31
3	IO_L135N_YY	Y30

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
3	IO_L136P_YY	AA34[5]
3	IO_L136N_YY	W31[4]
3	IO_D4_L137P_YY	AA33
3	IO_VREF_L137N_YY	Y29
3	IO_L138P_Y	W25
3	IO_L138N_Y	AB34
3	IO_L139P_Y	Y28[5]
3	IO_L139N_Y	AB33[4]
3	IO_L140P_Y	AA30
3	IO_L140N_Y	Y26
3	IO_L141P_YY	Y27
3	IO_L141N_YY	AA31
3	IO_L142P_YY	AA27[5]
3	IO_L142N_YY	AA29[4]
3	IO_L143P_Y	AB32
3	IO_VREF_L143N_Y	AB29
3	IO_L144P_Y	AA28
3	IO_L144N_Y	AC34
3	IO_L145P	Y25
3	IO_L145N	AD34
3	IO_L146P_Y	AB30
3	IO_L146N_Y	AC33
3	IO_L147P_Y	AA26
3	IO_L147N_Y	AC32
3	IO_L148P_Y	AD33
3	IO_L148N_Y	AB28
3	IO_L149P_YY	AE34
3	IO_D5_L149N_YY	AB27
3	IO_D6_L150P_YY	AE33
3	IO_VREF_L150N_YY	AC30
3	IO_L151P_Y	AA25
3	IO_L151N_Y	AE32
3	IO_L152P_YY	AE31
3	IO_L152N_YY	AD29

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
32	0	B14	E14	3200 2600 2000 1600 1000	-
33	0	D14	G15	3200 2600 2000 1600 1000	VREF
34	0	D15	J16	3200 1600	-
35	0	B15	F15	3200 2000 1000	-
36	0	E15	A15	3200 2000 1000	-
37	0	A16	G16	3200 2600	-
38	0	J17	F16	3200 2600 2000 1600 1000	-
39	0	B16	C16	3200 2600 2000 1600 1000	VREF
40	0	A17	H17	2600 1600 1000	-
41	0	B17	G17	2600 1600 1000	VREF
42	1	J18	C17	None	IO_LVDS_DLL
43	1	C18	G18	2600 1600 1000	VREF
44	1	F18	H18	2600 1600 1000	-
45	1	A19	B19	3200 2600 2000 1600 1000	VREF
46	1	C19	K19	3200 2600 2000 1600 1000	-
47	1	E19	F19	3200 2600	-
48	1	J19	G19	3200 2000 1000	-
49	1	G20	A20	3200 2000 1000	-
50	1	F20	B20	3200 1600	-
51	1	E20	D20	3200 2600 2000 1600 1000	VREF

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
52	1	A21	H20	3200 2600 2000 1600 1000	-
53	1	J20	E21	3200	-
54	1	K20	D21	3200 2600 1000	-
55	1	H21	B21	3200 2600 1000	-
56	1	F21	G21	2000 1600	-
57	1	B22	A22	3200 2600 2000 1600 1000	VREF
58	1	C22	J21	3200 2600 2000 1600 1000	-
59	1	G22	D22	3200 2600 1000	-
60	1	A23	K21	3200 2000 1000	-
61	1	B23	F22	3200 2000 1000	-
62	1	H22	C23	3200 1600 1000	-
63	1	K22	D23	3200 2600 2000 1600 1000	-
64	1	J22	A24	3200 2600 2000 1600 1000	VREF
65	1	D24	H23	2600 1600 1000	-
66	1	E24	A25	2600 1600 1000	-
67	1	C25	A26	3200 2600 2000 1600 1000	VREF
68	1	B26	F24	3200 2600 2000 1600 1000	-
69	1	F25	K23	3200 2600	-
70	1	H24	C26	3200 2000 1000	VREF