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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	1176
Number of Logic Elements/Cells	5292
Total RAM Bits	114688
Number of I/O	94
Number of Gates	306393
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-TFBGA, CSPBGA
Supplier Device Package	144-LCSBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv200e-7cs144i

Table 1: Virtex-E Field-Programmable Gate Array Family Members

Device	System Gates	Logic Gates	CLB Array	Logic Cells	Differential I/O Pairs	User I/O	BlockRAM Bits	Distributed RAM Bits
XCV50E	71,693	20,736	16 x 24	1,728	83	176	65,536	24,576
XCV100E	128,236	32,400	20 x 30	2,700	83	196	81,920	38,400
XCV200E	306,393	63,504	28 x 42	5,292	119	284	114,688	75,264
XCV300E	411,955	82,944	32 x 48	6,912	137	316	131,072	98,304
XCV400E	569,952	129,600	40 x 60	10,800	183	404	163,840	153,600
XCV600E	985,882	186,624	48 x 72	15,552	247	512	294,912	221,184
XCV1000E	1,569,178	331,776	64 x 96	27,648	281	660	393,216	393,216
XCV1600E	2,188,742	419,904	72 x 108	34,992	344	724	589,824	497,664
XCV2000E	2,541,952	518,400	80 x 120	43,200	344	804	655,360	614,400
XCV2600E	3,263,755	685,584	92 x 138	57,132	344	804	753,664	812,544
XCV3200E	4,074,387	876,096	104 x 156	73,008	344	804	851,968	1,038,336

Virtex-E Compared to Virtex Devices

The Virtex-E family offers up to 43,200 logic cells in devices up to 30% faster than the Virtex family.

I/O performance is increased to 622 Mb/s using Source Synchronous data transmission architectures and synchronous system performance up to 240 MHz using singled-ended SelectI/O technology. Additional I/O standards are supported, notably LVPECL, LVDS, and BLVDS, which use two pins per signal. Almost all signal pins can be used for these new standards.

Virtex-E devices have up to 640 Kb of faster (250 MHz) block SelectRAM, but the individual RAMs are the same size and structure as in the Virtex family. They also have eight DLLs instead of the four in Virtex devices. Each individual DLL is slightly improved with easier clock mirroring and 4x frequency multiplication.

V_{CCINT} , the supply voltage for the internal logic and memory, is 1.8 V, instead of 2.5 V for Virtex devices. Advanced processing and 0.18 μ m design rules have resulted in smaller dice, faster speed, and lower power consumption.

I/O pins are 3 V tolerant, and can be 5 V tolerant with an external 100 Ω resistor. PCI 5 V is not supported. With the addition of appropriate external resistors, any pin can tolerate any voltage desired.

Banking rules are different. With Virtex devices, all input buffers are powered by V_{CCINT} . With Virtex-E devices, the LVTTTL, LVCMOS2, and PCI input buffers are powered by the I/O supply voltage V_{CCO} .

The Virtex-E family is not bitstream-compatible with the Virtex family, but Virtex designs can be compiled into equivalent Virtex-E devices.

The same device in the same package for the Virtex-E and Virtex families are pin-compatible with some minor exceptions. See the data sheet pinout section for details.

General Description

The Virtex-E FPGA family delivers high-performance, high-capacity programmable logic solutions. Dramatic increases in silicon efficiency result from optimizing the new architecture for place-and-route efficiency and exploiting an aggressive 6-layer metal 0.18 μ m CMOS process. These advances make Virtex-E FPGAs powerful and flexible alternatives to mask-programmed gate arrays. The Virtex-E family includes the nine members in Table 1.

Building on experience gained from Virtex FPGAs, the Virtex-E family is an evolutionary step forward in programmable logic design. Combining a wide variety of programmable system features, a rich hierarchy of fast, flexible interconnect resources, and advanced process technology, the Virtex-E family delivers a high-speed and high-capacity programmable logic solution that enhances design flexibility while reducing time-to-market.

Virtex-E Architecture

Virtex-E devices feature a flexible, regular architecture that comprises an array of configurable logic blocks (CLBs) surrounded by programmable input/output blocks (IOBs), all interconnected by a rich hierarchy of fast, versatile routing

Table 1: Supported I/O Standards

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Board Termination Voltage (V_{TT})
LVTTTL	3.3	3.3	N/A	N/A
LVC MOS2	2.5	2.5	N/A	N/A
LVC MOS18	1.8	1.8	N/A	N/A
SSTL3 I & II	3.3	N/A	1.50	1.50
SSTL2 I & II	2.5	N/A	1.25	1.25
GTL	N/A	N/A	0.80	1.20
GTL+	N/A	N/A	1.0	1.50
HSTL I	1.5	N/A	0.75	0.75
HSTL III & IV	1.5	N/A	0.90	1.50
CTT	3.3	N/A	1.50	1.50
AGP-2X	3.3	N/A	1.32	N/A
PCI33_3	3.3	3.3	N/A	N/A
PCI66_3	3.3	3.3	N/A	N/A
BLVDS & LVDS	2.5	N/A	N/A	N/A
LVPECL	3.3	N/A	N/A	N/A

In addition to the CLK and CE control signals, the three flip-flops share a Set/Reset (SR). For each flip-flop, this signal can be independently configured as a synchronous Set, a synchronous Reset, an asynchronous Preset, or an asynchronous Clear.

The output buffer and all of the IOB control signals have independent polarity controls.

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. After configuration, clamping diodes are connected to V_{CCO} with the exception of LVC MOS18, LVC MOS25, GTL, GTL+, LVDS, and LVPECL.

Optional pull-up, pull-down and weak-keeper circuits are attached to each pad. Prior to configuration all outputs not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive, but I/Os can optionally be pulled up.

The activation of pull-up resistors prior to configuration is controlled on a global basis by the configuration mode pins. If the pull-up resistors are not activated, all the pins are in a high-impedance state. Consequently, external pull-up or pull-down resistors must be provided on pins required to be at a well-defined logic level prior to configuration.

All Virtex-E IOBs support IEEE 1149.1-compatible Boundary Scan testing.

Input Path

The Virtex-E IOB input path routes the input signal directly to internal logic and/ or through an optional input flip-flop.

An optional delay element at the D-input of this flip-flop eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the FPGA, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signalling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF} . The need to supply V_{REF} imposes constraints on which standards can be used in close proximity to each other. See **I/O Banking**.

There are optional pull-up and pull-down resistors at each user I/O input for use after configuration. Their value is in the range 50 – 100 k Ω .

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output signal can be routed to the buffer directly from the internal logic or through an optional IOB output flip-flop.

The 3-state control of the output can also be routed directly from the internal logic or through a flip-flop that provides synchronous enable and disable.

Each output driver can be individually programmed for a wide range of low-voltage signalling standards. Each output buffer can source up to 24 mA and sink up to 48 mA. Drive strength and slew rate controls minimize bus transients.

In most signalling standards, the output High voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in close proximity to each other. See **I/O Banking**.

An optional weak-keeper circuit is connected to each output. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low to match the input signal. If the pin is connected to a multiple-source signal, the weak keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way eliminates bus chatter.

Since the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate V_{REF} voltage must be provided if the signalling standard requires one. The provision of this voltage must comply with the I/O banking rules.

I/O Banking

Some of the I/O standards described above require V_{CCO} and/or V_{REF} voltages. These voltages are externally supplied and connected to device pins that serve groups of IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Because any single DLL can access only two BUFGs at most, any additional output clock signals must be routed from the DLL in this example on the high speed backbone routing.

The dll_2x files in the [xapp132.zip](#) file show the VHDL and Verilog implementation of this circuit.

Virtex-E 4x Clock

Two DLLs located in the same half-edge (top-left, top-right, bottom-right, bottom-left) can be connected together, without using a BUFG between the CLKDLLs, to generate a 4x clock as shown in [Figure 30](#). Virtex-E devices, like the Virtex devices, have four clock networks that are available for internal deskewing of the clock. Each of the eight DLLs have access to two of the four clock networks. Although all the DLLs can be used for internal deskewing, the presence of two GCLKBUFs on the top and two on the bottom indicate that only two of the four DLLs on the top (and two of the four DLLs on the bottom) can be used for this purpose.

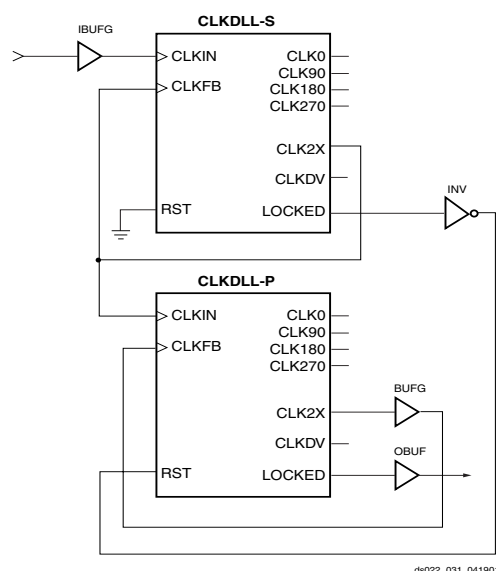


Figure 30: DLL Generation of 4x Clock in Virtex-E Devices

The dll_4xe files in the xapp132.zip file show the DLL implementation in Verilog for Virtex-E devices. These files can be found at:

<ftp://ftp.xilinx.com/pub/applications/xapp/xapp132.zip>

Using Block SelectRAM+ Features

The Virtex FPGA Series provides dedicated blocks of on-chip, true dual-read/write port synchronous RAM, with 4096 memory cells. Each port of the block SelectRAM+ memory can be independently configured as a read/write port, a read port, a write port, and can be configured to a specific data width. The block SelectRAM+ memory offers

new capabilities allowing the FPGA designer to simplify designs.

Operating Modes

Virtex-E block SelectRAM+ memory supports two operating modes:

- Read Through
- Write Back

Read Through (one clock edge)

The read address is registered on the read port clock edge and data appears on the output after the RAM access time. Some memories might place the latch/register at the outputs, depending on whether a faster clock-to-out versus set-up time is desired. This is generally considered to be an inferior solution, since it changes the read operation to an asynchronous function with the possibility of missing an address/control line transition during the generation of the read pulse clock.

Write Back (one clock edge)

The write address is registered on the write port clock edge and the data input is written to the memory and mirrored on the output.

Block SelectRAM+ Characteristics

- All inputs are registered with the port clock and have a set-up to clock timing specification.
- All outputs have a read through or write back function depending on the state of the port WE pin. The outputs relative to the port clock are available after the clock-to-out timing specification.
- The block SelectRAMs are true SRAM memories and do not have a combinatorial path from the address to the output. The LUT SelectRAM+ cells in the CLBs are still available with this function.
- The ports are completely independent from each other (*i.e.*, clocking, control, address, read/write function, and data width) without arbitration.
- A write operation requires only one clock edge.
- A read operation requires only one clock edge.

The output ports are latched with a self timed circuit to guarantee a glitch free read. The state of the output port does not change until the port executes another read or write operation.

Library Primitives

Figure 31 and Figure 32 show the two generic library block SelectRAM+ primitives. Table 14 describes all of the available primitives for synthesis and simulation.

Data Output Bus—DO[AIB]<#:0>

The data out bus reflects the contents of the memory cells referenced by the address bus at the last active clock edge. During a write operation, the data out bus reflects the data in bus. The width of this bus equals the width of the port. The allowed widths appear in [Table 15](#).

Inverting Control Pins

The four control pins (CLK, EN, WE and RST) for each port have independent inversion control as a configuration option.

Address Mapping

Each port accesses the same set of 4096 memory cells using an addressing scheme dependent on the width of the port.

The physical RAM location addressed for a particular width are described in the following formula (of interest only when the two ports use different aspect ratios).

$$\text{Start} = ((\text{ADDR}_{\text{port}} + 1) * \text{Width}_{\text{port}}) - 1$$

$$\text{End} = \text{ADDR}_{\text{port}} * \text{Width}_{\text{port}}$$

Conflict Resolution

The block SelectRAM+ memory is a true dual-read/write port RAM that allows simultaneous access of the same memory cell from both ports. When one port writes to a given memory cell, the other port must not address that memory cell (for a write or a read) within the clock-to-clock setup window. The following lists specifics of port and memory cell write conflict resolution.

- If both ports write to the same memory cell simultaneously, violating the clock-to-clock setup requirement, consider the data stored as invalid.
- If one port attempts a read of the same memory cell the other simultaneously writes, violating the clock-to-clock setup requirement, the following occurs.
 - The write succeeds
 - The data out on the writing port accurately reflects the data written.
 - The data out on the reading port is invalid.

Conflicts do not cause any physical damage.

[Table 16](#) shows low order address mapping for each port width.

Table 16: Port Address Mapping

Port Width	Port Addresses																
1	4095...	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2	2047...	07		06		05		04		03		02		01		00	
4	1023...	03				02				01				00			
8	511...	01								00							
16	255...	00															

Creating Larger RAM Structures

The block SelectRAM+ columns have specialized routing to allow cascading blocks together with minimal routing delays. This achieves wider or deeper RAM structures with a smaller timing penalty than when using normal routing channels.

Location Constraints

Block SelectRAM+ instances can have LOC properties attached to them to constrain the placement. The block SelectRAM+ placement locations are separate from the CLB location naming convention, allowing the LOC properties to transfer easily from array to array.

The LOC properties use the following form.

$$\text{LOC} = \text{RAMB4_R\#C\#}$$

RAMB4_R0C0 is the upper left RAMB4 location on the device.

Single Port Timing

[Figure 33](#) shows a timing diagram for a single port of a block SelectRAM+ memory. The block SelectRAM+ AC switching characteristics are specified in the data sheet. The block SelectRAM+ memory is initially disabled.

At the first rising edge of the CLK pin, the ADDR, DI, EN, WE, and RST pins are sampled. The EN pin is High and the WE pin is Low indicating a read operation. The DO bus contains the contents of the memory location, 0x00, as indicated by the ADDR bus.

At the second rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN and WE pins are High indicating a write operation. The DO bus mirrors the DI bus. The DI bus is written to the memory location 0x0F.

At the third rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN pin is High and the WE pin is Low indicating a read operation. The DO bus contains the contents of the memory location 0x7E as indicated by the ADDR bus.

At the fourth rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN pin is Low

HSTL

A sample circuit illustrating a valid termination technique for HSTL_I appears in [Figure 46](#). A sample circuit illustrating a valid termination technique for HSTL_III appears in [Figure 47](#).

Table 25: HSTL Class I Voltage Specification

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF}	0.68	0.75	0.90
V_{TT}	-	$V_{CCO} \times 0.5$	-
V_{IH}	$V_{REF} + 0.1$	-	-
V_{IL}	-	-	$V_{REF} - 0.1$
V_{OH}	$V_{CCO} - 0.4$	-	-
V_{OL}			0.4
I_{OH} at V_{OH} (mA)	-8	-	-
I_{OL} at V_{OL} (mA)	8	-	-

HSTL Class I

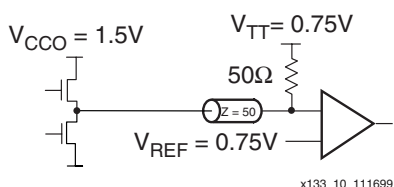


Figure 46: Terminated HSTL Class I

Table 26: HSTL Class III Voltage Specification

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
$V_{REF}^{(1)}$	-	0.90	-
V_{TT}	-	V_{CCO}	-
V_{IH}	$V_{REF} + 0.1$	-	-
V_{IL}	-	-	$V_{REF} - 0.1$
V_{OH}	$V_{CCO} - 0.4$	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	-8	-	-
I_{OL} at V_{OL} (mA)	24	-	-

Note: Per EIA/JESD8-6, "The value of V_{REF} is to be selected by the user to provide optimum noise margin in the use conditions specified by the user."

HSTL Class III

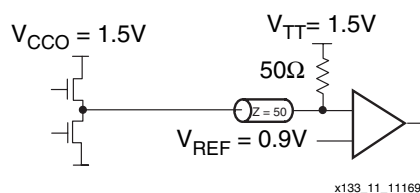


Figure 47: Terminated HSTL Class III

A sample circuit illustrating a valid termination technique for HSTL_IV appears in [Figure 48](#).

Table 27: HSTL Class IV Voltage Specification

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF}	-	0.90	-
V_{TT}	-	V_{CCO}	-
V_{IH}	$V_{REF} + 0.1$	-	-
V_{IL}	-	-	$V_{REF} - 0.1$
V_{OH}	$V_{CCO} - 0.4$	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	-8	-	-
I_{OL} at V_{OL} (mA)	48	-	-

Note: Per EIA/JESD8-6, "The value of V_{REF} is to be selected by the user to provide optimum noise margin in the use conditions specified by the user."

HSTL Class IV

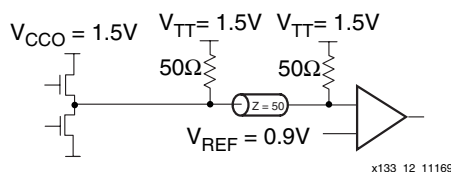


Figure 48: Terminated HSTL Class IV

Table 6: PQ240 — XCV50E, XCV100E, XCV200E, XCV300E, XCV400E

Pin #	Pin Description	Bank
P173	IO_L16N_Y	2
P171	IO_VREF_L17P_Y	2
P170	IO_L17N_Y	2
P169	IO	2
P168 ¹	IO_VREF_L18P_Y	2
P167	IO_D1_L18N_Y	2
P163	IO_D2_L19P_YY	2
P162	IO_L19N_YY	2
P161	IO	2
P160	IO_L20P_Y	2
P159	IO_L20N_Y	2
P157	IO_VREF_L21P_Y	2
P156	IO_D3_L21N_Y	2
P155	IO_L22P_Y	2
P154 ³	IO_VREF_L22N_Y	2
P153	IO_L23P_YY	2
P152	IO_L23N_YY	2
P149	IO	3
P147 ³	IO_VREF	3
P145	IO_D4_L24P_Y	3
P144	IO_VREF_L24N_Y	3
P142	IO_L25P_Y	3
P141	IO_L25N_Y	3
P140	IO	3
P139	IO_L26P_YY	3
P138	IO_D5_L26N_YY	3
P134	IO_D6_L27P_Y	3
P133 ¹	IO_VREF_L27N_Y	3
P132	IO	3
P131	IO_L28P_Y	3
P130	IO_VREF_L28N_Y	3
P128	IO_L29P_Y	3
P127	IO_L29N_Y	3
P126 ²	IO_VREF_L30P_Y	3

Table 6: PQ240 — XCV50E, XCV100E, XCV200E, XCV300E, XCV400E

Pin #	Pin Description	Bank
P125	IO_L30N_Y	3
P124	IO_D7_L31P_YY	3
P123	IO_INIT_L31N_YY	3
P118	IO_L32P_YY	4
P117	IO_L32N_YY	4
P115 ²	IO_VREF	4
P114	IO_L33P_YY	4
P113	IO_L33N_YY	4
P111	IO_VREF_L34P_YY	4
P110	IO_L34N_YY	4
P109	IO	4
P108 ¹	IO_VREF_L35P_YY	4
P107	IO_L35N_YY	4
P103	IO_L36P_YY	4
P102	IO_L36N_YY	4
P101	IO	4
P100	IO_L37P_Y	4
P99	IO_L37N_Y	4
P97	IO_VREF_L38P_Y	4
P96	IO_L38N_Y	4
P95	IO_L39P_Y	4
P94 ³	IO_VREF_L39N_Y	4
P93	IO_LVDS_DLL_L40P	4
P92	GCK0	4
P89	GCK1	5
P87	IO_LVDS_DLL_L40N	5
P86 ³	IO_VREF	5
P84	IO_VREF_L41P_Y	5
P82	IO_L41N_Y	5
P81	IO	5
P80	IO	5
P79	IO_L42P_YY	5
P78	IO_L42N_YY	5

Table 7: PQ240 Differential Pin Pair Summary
XCV50E, XCV100E, XCV200E, XCV300E, XCV400E

Pair	Bank	P Pin	N Pin	AO	Other Functions
48	6	P56	P57	√	-
49	6	P52	P53	2	-
50	6	P49	P50	3	VREF
51	6	P46	P47	4	VREF
52	6	P41	P42	√	-
53	6	P38	P39	2	-
54	6	P35	P36	4	VREF
55	6	P33	P34	5	VREF
56	7	P27	P28	√	-
57	7	P23	P24	4	VREF
58	7	P20	P21	2	-
59	7	P17	P18	√	-
60	7	P12	P13	4	VREF
61	7	P9	P10	3	VREF
62	7	P6	P7	2	-
63	7	P4	P5	6	VREF

Notes:

1. AO in the XCV50E.
2. AO in the XCV50E, 100E, 200E, 300E.
3. AO in the XCV50E, 200E, 300E, 400E.
4. AO in the XCV50E, 300E, 400E.
5. AO in the XCV100E, 200E, 400E.
6. AO in the XCV100E, 400E.
7. AO in the XCV50E, 200E, 400E.
8. AO in the XCV100E.

HQ240 High-Heat Quad Flat-Pack Packages

XCV600E and XCV1000E devices in High-heat dissipation Quad Flat-pack packages have footprint compatibility. Pins labeled IO_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF} it can be used as general I/O. Immediately following Table 8, see Table 9 for Differential Pair information.

Table 8: HQ240 — XCV600E, XCV1000E

Pin #	Pin Description	Bank
P240	VCCO	7
P239	TCK	NA
P238	IO	0
P237	IO_L0N	0
P236	IO_VREF_L0P	0
P235	IO_L1N_YY	0
P234	IO_L1P_YY	0
P233	GND	NA
P232	VCCO	0
P231	IO_VREF	0
P230	IO_VREF	0
P229	IO_VREF_L2N_YY	0
P228	IO_L2P_YY	0
P227	GND	NA
P226	VCCO	0
P225	VCCINT	NA
P224	IO_L3N_YY	0
P223	IO_L3P_YY	0
P222	IO_VREF	0 ¹
P221	IO_L4N_Y	0
P220	IO_L4P_Y	0
P219	GND	NA
P218	IO_VREF_L5N_Y	0
P217	IO_L5P_Y	0
P216	IO_VREF	0
P215	IO_LVDS_DLL_L6N	0
P214	VCCINT	NA
P213	GCK3	0
P212	VCCO	0
P211	GND	NA

Table 11: BG352 Differential Pin Pair Summary
XCV100E, XCV200E, XCV300E

Pair	Bank	P Pin	N Pin	AO	Other Functions
55	5	AC13	AD14	✓	GCLK LVDS 1/0
56	5	AD15	AC15	✓	VREF_5
57	5	AE16	AE17	✓	-
58	5	AC16	AF18	2	-
59	5	AD17	AC17	✓	-
60	5	AD18	AC18	✓	VREF_5
61	5	AF20	AE20	1	-
62	5	AE21	AD20	✓	VREF_5
63	5	AF23	AE22	✓	-
64	5	AC21	AE23	✓	VREF_5
65	6	AD25	AC24	✓	-
66	6	AC26	AD26	✓	VREF_6
67	6	AB25	AA24	✓	-
68	6	Y24	AA25	✓	VREF_6
69	6	W24	V23	2	-
70	6	U23	Y26	✓	VREF_6
71	6	U24	V25	✓	-
72	6	U25	T23	1	-
73	6	T26	T25	✓	-
74	6	R25	R24	✓	VREF_6
75	6	P24	R26	2	-
76	7	N24	N25	✓	-
77	7	M24	M25	2	-
78	7	L26	M23	✓	VREF_7
79	7	L24	K25	✓	-
80	7	J25	J26	1	-
81	7	H25	K23	✓	-
82	7	G26	J23	✓	VREF_7
83	7	H24	G25	1	-
84	7	D26	G24	✓	VREF_7
85	7	F24	E25	✓	-
86	7	E24	D25	✓	VREF_7

Notes:

1. AO in the XCV100E.
2. AO in the XCV200E.

BG432 Ball Grid Array Packages

XCV300E, XCV400E, and XCV600E devices in BG432 Ball Grid Array packages have footprint compatibility. Pins labeled IO_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF} it can be used as general I/O. Immediately following Table 12, see Table 13 for Differential Pair information.

Table 12: BG432 — XCV300E, XCV400E, XCV600E

Bank	Pin Description	Pin #
0	GCK3	D17
0	IO	A22
0	IO	A26
0	IO	B20
0	IO	C23
0	IO	C28
0	IO_L0N_Y	B29
0	IO_L0P_Y	D27
0	IO_L1N_YY	B28
0	IO_L1P_YY	C27
0	IO_VREF_L2N_YY	D26
0	IO_L2P_YY	A28
0	IO_L3N_Y	B27
0	IO_L3P_Y	C26
0	IO_L4N_YY	D25
0	IO_L4P_YY	A27
0	IO_VREF_L5N_YY	D24
0	IO_L5P_YY	C25
0	IO_L6N_Y	B25
0	IO_L6P_Y	D23
0	IO_VREF_L7N_Y	C24 ¹
0	IO_L7P_Y	B24
0	IO_VREF_L8N_YY	D22
0	IO_L8P_YY	A24
0	IO_L9N_YY	C22
0	IO_L9P_YY	B22
0	IO_L10N_YY	C21
0	IO_L10P_YY	D20
0	IO_L11N_YY	B21
0	IO_L11P_YY	C20

Table 14: BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin#	See Note
0	IO_L11P_YY	B24	
0	IO_L12N_Y	E22	
0	IO_L12P_Y	C23	
0	IO_L13N_YY	A23	
0	IO_L13P_YY	D22	
0	IO_VREF_L14N_YY	E21	3
0	IO_L14P_YY	B22	
0	IO_L15N_Y	D21	
0	IO_L15P_Y	C21	
0	IO_L16N_YY	B21	
0	IO_L16P_YY	E20	
0	IO_VREF_L17N_YY	D20	
0	IO_L17P_YY	C20	
0	IO_L18N_Y	B20	
0	IO_L18P_Y	E19	
0	IO_L19N_Y	D19	
0	IO_L19P_Y	C19	
0	IO_VREF_L20N_Y	A19	
0	IO_L20P_Y	D18	
0	IO_LVDS_DLL_L21N	C18	
0	IO_VREF	E18	2
1	GCK2	D17	
1	IO	A3	
1	IO	D9	
1	IO	E8	
1	IO	E11	
1	IO_LVDS_DLL_L21P	E17	
1	IO_VREF_L22N_Y	C17	2
1	IO_L22P_Y	B17	
1	IO_L23N_Y	B16	
1	IO_VREF_L23P_Y	D16	
1	IO_L24N_Y	E16	
1	IO_L24P_Y	C16	
1	IO_L25N_Y	A15	

Table 14: BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin#	See Note
1	IO_L25P_Y	C15	
1	IO_L26N_YY	D15	
1	IO_VREF_L26P_YY	E15	
1	IO_L27N_YY	C14	
1	IO_L27P_YY	D14	
1	IO_L28N_Y	A13	
1	IO_L28P_Y	E14	
1	IO_L29N_YY	C13	
1	IO_VREF_L29P_YY	D13	3
1	IO_L30N_YY	C12	
1	IO_L30P_YY	E13	
1	IO_L31N_Y	A11	
1	IO_L31P_Y	D12	
1	IO_L32N_YY	B11	
1	IO_L32P_YY	C11	
1	IO_L33N_YY	B10	
1	IO_VREF_L33P_YY	D11	
1	IO_L34N_Y	C10	
1	IO_L34P_Y	A9	
1	IO_L35N_Y	C9	
1	IO_VREF_L35P_Y	D10	4
1	IO_L36N_Y	A8	
1	IO_L36P_Y	B8	
1	IO_L37N_Y	E10	
1	IO_VREF_L37P_Y	C8	1
1	IO_L38N_YY	B7	
1	IO_VREF_L38P_YY	A6	
1	IO_L39N_YY	C7	
1	IO_L39P_YY	D8	
1	IO_L40N_Y	A5	
1	IO_L40P_Y	B5	
1	IO_L41N_YY	C6	
1	IO_VREF_L41P_YY	D7	
1	IO_L42N_YY	A4	
1	IO_L42P_YY	B4	

Table 14: BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin#	See Note
4	IO_L104N_YY	AJ12	
4	IO_L105P_Y	AN11	
4	IO_L105N_Y	AK12	
4	IO_L106P_YY	AL12	
4	IO_L106N_YY	AM12	
4	IO_VREF_L107P_YY	AK13	3
4	IO_L107N_YY	AL13	
4	IO_L108P_Y	AM13	
4	IO_L108N_Y	AN13	
4	IO_L109P_YY	AJ14	
4	IO_L109N_YY	AK14	
4	IO_VREF_L110P_YY	AM14	
4	IO_L110N_YY	AN15	
4	IO_L111P_Y	AJ15	
4	IO_L111N_Y	AK15	
4	IO_L112P_Y	AL15	
4	IO_L112N_Y	AM16	
4	IO_VREF_L113P_Y	AL16	
4	IO_L113N_Y	AJ16	
4	IO_L114P_Y	AK16	
4	IO_VREF_L114N_Y	AN17	2
4	IO_LVDS_DLL_L115P	AM17	
5	GCK1	AJ17	
5	IO	AL25	
5	IO	AL28	
5	IO	AL30	
5	IO	AN28	
5	IO_LVDS_DLL_L115N	AM18	
5	IO_VREF	AL18	2
5	IO_L116P_Y	AK18	
5	IO_VREF_L116N_Y	AJ18	
5	IO_L117P_Y	AN19	
5	IO_L117N_Y	AL19	
5	IO_L118P_Y	AK19	

Table 14: BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin#	See Note
5	IO_L118N_Y	AM20	
5	IO_L119P_YY	AJ19	
5	IO_VREF_L119N_YY	AL20	
5	IO_L120P_YY	AN21	
5	IO_L120N_YY	AL21	
5	IO_L121P_Y	AJ20	
5	IO_L121N_Y	AM22	
5	IO_L122P_YY	AK21	
5	IO_VREF_L122N_YY	AN23	3
5	IO_L123P_YY	AJ21	
5	IO_L123N_YY	AM23	
5	IO_L124P_Y	AK22	
5	IO_L124N_Y	AM24	
5	IO_L125P_YY	AL23	
5	IO_L125N_YY	AJ22	
5	IO_L126P_YY	AK23	
5	IO_VREF_L126N_YY	AL24	
5	IO_L127P_Y	AN26	
5	IO_L127N_Y	AJ23	
5	IO_L128P_Y	AK24	
5	IO_VREF_L128N_Y	AM26	4
5	IO_L129P_Y	AM27	
5	IO_L129N_Y	AJ24	
5	IO_L130P_Y	AL26	
5	IO_VREF_L130N_Y	AK25	1
5	IO_L131P_YY	AN29	
5	IO_VREF_L131N_YY	AJ25	
5	IO_L132P_YY	AK26	
5	IO_L132N_YY	AM29	
5	IO_L133P_Y	AM30	
5	IO_L133N_Y	AJ26	
5	IO_L134P_YY	AK27	
5	IO_VREF_L134N_YY	AL29	
5	IO_L135P_YY	AN31	
5	IO_L135N_YY	AJ27	

Table 21: FG676 Differential Pin Pair Summary
XCV400E, XCV600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
52	2	G24	H22	√	-
53	2	J21	G25	2	-
54	2	G26	J22	1	VREF
55	2	H24	J23	√	-
56	2	J24	K20	√	VREF
57	2	K22	K21	√	D2
58	2	H25	K23	√	-
59	2	L20	J26	2	-
60	2	K25	L22	1	-
61	2	L21	L23	1	-
62	2	M20	L24	1	-
63	2	M23	M22	√	D3
64	2	L26	M21	√	-
65	2	N19	M24	2	-
66	2	M26	N20	1	VREF
67	2	N24	N21	√	-
68	2	N23	N22	√	-
69	3	P21	P23	√	-
70	3	P22	R25	1	VREF
71	3	P19	P20	2	-
72	3	R21	R22	√	-
73	3	R24	R23	√	VREF
74	3	T24	R20	1	-
75	3	T22	U24	1	-
76	3	T23	U25	1	-
77	3	T21	U20	2	-
78	3	U22	V26	√	-
79	3	T20	U23	√	D5
80	3	V24	U21	√	VREF
81	3	V23	W24	√	-
82	3	V22	W26	1	VREF
83	3	Y25	V21	2	-
84	3	V20	AA26	√	-
85	3	Y24	W23	√	VREF

Table 21: FG676 Differential Pin Pair Summary
XCV400E, XCV600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
86	3	AA24	Y23	1	-
87	3	AB26	W21	2	-
88	3	Y22	W22	1	VREF
89	3	AA23	AB24	2	-
90	3	W20	AC24	√	-
91	3	AB23	Y21	√	INIT
92	4	AC22	AD26	√	-
93	4	AD23	AA20	1	-
94	4	Y19	AC21	√	-
95	4	AD22	AB20	√	VREF
96	4	AE22	Y18	NA	-
97	4	AF22	AA19	NA	-
98	4	AD21	AB19	√	VREF
99	4	AC20	AA18	√	-
100	4	AC19	AD20	1	-
101	4	AF20	AB18	1	VREF
102	4	AD19	Y17	NA	-
103	4	AE19	AD18	NA	VREF
104	4	AF19	AA17	√	-
105	4	AC17	AB17	1	-
106	4	Y16	AE17	√	-
107	4	AF17	AA16	√	-
108	4	AD17	AB16	NA	-
109	4	AC16	AD16	√	-
110	4	AC15	Y15	√	VREF
111	4	AD15	AA15	√	-
112	4	W14	AB15	1	-
113	4	AF15	Y14	1	VREF
114	4	AD14	AB14	NA	-
115	5	AC14	AF13	NA	IO_LVDS_DLL
116	5	AA13	AF12	1	VREF
117	5	AC13	W13	1	-
118	5	AA12	AD12	√	-
119	5	AC12	AB12	√	VREF

FG680 Fine-Pitch Ball Grid Array Package

XCV600E, XCV1000E, XCV1600E, and XCV2000E devices in the FG680 fine-pitch Ball Grid Array package have footprint compatibility. Pins labeled IO_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF} , it can be used as general I/O. Immediately following Table 22, see Table 23 for Differential Pair information.

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
0	GCK3	A20
0	IO	D35
0	IO	B36
0	IO_L0N_Y	C35
0	IO_L0P_Y	A36
0	IO_VREF_L1N_Y	D34 ¹
0	IO_L1P_Y	B35
0	IO_L2N_YY	C34
0	IO_L2P_YY	A35
0	IO_VREF_L3N_YY	D33
0	IO_L3P_YY	B34
0	IO_L4N	C33
0	IO_L4P	A34
0	IO_L5N_Y	D32
0	IO_L5P_Y	B33
0	IO_L6N_YY	C32
0	IO_L6P_YY	D31
0	IO_VREF_L7N_YY	A33
0	IO_L7P_YY	C31
0	IO_L8N_Y	B32
0	IO_L8P_Y	B31
0	IO_VREF_L9N_Y	A32 ³
0	IO_L9P_Y	D30
0	IO_L10N_YY	A31
0	IO_L10P_YY	C30
0	IO_VREF_L11N_YY	B30
0	IO_L11P_YY	D29
0	IO_L12N_Y	A30
0	IO_L12P_Y	C29

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
0	IO_L13N_Y	A29
0	IO_L13P_Y	B29
0	IO_VREF_L14N_YY	B28
0	IO_L14P_YY	A28
0	IO_L15N_YY	C28
0	IO_L15P_YY	B27
0	IO_L16N_Y	D27
0	IO_L16P_Y	A27
0	IO_L17N_Y	C27
0	IO_L17P_Y	B26
0	IO_L18N_YY	D26
0	IO_L18P_YY	C26
0	IO_VREF_L19N_YY	A26 ¹
0	IO_L19P_YY	D25
0	IO_L20N_Y	B25
0	IO_L20P_Y	C25
0	IO_L21N_Y	A25
0	IO_L21P_Y	D24
0	IO_L22N_YY	A24
0	IO_L22P_YY	B23
0	IO_VREF_L23N_YY	C24
0	IO_L23P_YY	A23
0	IO_L24N_Y	B24
0	IO_L24P_Y	B22
0	IO_L25N_Y	E23
0	IO_L25P_Y	A22
0	IO_L26N_YY	D23
0	IO_L26P_YY	B21
0	IO_VREF_L27N_YY	C23
0	IO_L27P_YY	A21
0	IO_L28N_Y	E22
0	IO_L28P_Y	B20
0	IO_LVDS_DLL_L29N	C22
0	IO_VREF	D22 ²
1	GCK2	D21

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
0	VCCO	E34
0	VCCO	E33
0	VCCO	E30
0	VCCO	E29
0	VCCO	E27
0	VCCO	E26
1	VCCO	E10
1	VCCO	E11
1	VCCO	E13
1	VCCO	E14
1	VCCO	E6
1	VCCO	E7
2	VCCO	P5
2	VCCO	N5
2	VCCO	L5
2	VCCO	K5
2	VCCO	G5
2	VCCO	F5
3	VCCO	AP5
3	VCCO	AN5
3	VCCO	AK5
3	VCCO	AJ5
3	VCCO	AG5
3	VCCO	AF5
4	VCCO	AR10
4	VCCO	AR11
4	VCCO	AR13
4	VCCO	AR14
4	VCCO	AR6
4	VCCO	AR7
5	VCCO	AR34
5	VCCO	AR33
5	VCCO	AR30
5	VCCO	AR29
5	VCCO	AR27

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
5	VCCO	AR26
6	VCCO	AP35
6	VCCO	AN35
6	VCCO	AK35
6	VCCO	AJ35
6	VCCO	AG35
6	VCCO	AF35
7	VCCO	P35
7	VCCO	N35
7	VCCO	L35
7	VCCO	K35
7	VCCO	G35
7	VCCO	F35
NA	GND	Y5
NA	GND	Y4
NA	GND	Y37
NA	GND	Y36
NA	GND	Y35
NA	GND	Y3
NA	GND	W5
NA	GND	W35
NA	GND	M5
NA	GND	M4
NA	GND	M36
NA	GND	M35
NA	GND	E5
NA	GND	E35
NA	GND	E28
NA	GND	E21
NA	GND	E20
NA	GND	E19
NA	GND	E12
NA	GND	D4
NA	GND	D36
NA	GND	D28

FG680 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A ✓ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 23: FG680 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
GCLK LVDS					
3	0	A20	C22	NA	IO_DLL_L29N
2	1	D21	A19	NA	IO_DLL_L29P
1	5	AU22	AT22	NA	IO_DLL_L155N
0	4	AW19	AT21	NA	IO_DLL_L155P
IO LVDS					
Total Pairs: 247, Asynchronous Output Pairs: 111					
0	0	A36	C35	5	-
1	0	B35	D34	5	VREF
2	0	A35	C34	✓	-
3	0	B34	D33	✓	VREF
4	0	A34	C33	3	-
5	0	B33	D32	3	-
6	0	D31	C32	✓	-
7	0	C31	A33	✓	VREF
8	0	B31	B32	5	-
9	0	D30	A32	5	VREF
10	0	C30	A31	✓	-
11	0	D29	B30	✓	VREF
12	0	C29	A30	2	-
13	0	B29	A29	2	-
14	0	A28	B28	✓	VREF
15	0	B27	C28	✓	-
16	0	A27	D27	5	-
17	0	B26	C27	5	-

Table 23: FG680 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
18	0	C26	D26	✓	-
19	0	D25	A26	✓	VREF
20	0	C25	B25	3	-
21	0	D24	A25	3	-
22	0	B23	A24	✓	-
23	0	A23	C24	✓	VREF
24	0	B22	B24	5	-
25	0	A22	E23	5	-
26	0	B21	D23	✓	-
27	0	A21	C23	✓	VREF
28	0	B20	E22	2	-
29	1	A19	C22	NA	IO_LVDS_DLL
30	1	B19	C21	2	VREF
31	1	A18	C19	2	-
32	1	B18	D19	✓	VREF
33	1	A17	C18	✓	-
34	1	B17	D18	5	-
35	1	A16	E18	5	-
36	1	D17	C17	✓	VREF
37	1	E17	B16	✓	-
38	1	C16	A15	3	-
39	1	D16	B15	3	-
40	1	B14	A14	✓	VREF
41	1	A13	C15	✓	-
42	1	B13	D15	5	-
43	1	A12	C14	5	-
44	1	C13	D14	✓	-
45	1	D13	B12	✓	VREF
46	1	C12	A11	2	-
47	1	C11	B11	2	-
48	1	D11	A10	✓	VREF
49	1	C10	B10	✓	-
50	1	D10	A9	5	VREF
51	1	C9	B9	5	-

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
NA	VCCO_1	F15
NA	VCCO_1	F19
NA	VCCO_1	F20
NA	VCCO_1	F7
NA	VCCO_1	F8
NA	VCCO_2	G6
NA	VCCO_2	H6
NA	VCCO_2	L6
NA	VCCO_2	M6
NA	VCCO_2	P6
NA	VCCO_2	R6
NA	VCCO_2	W6
NA	VCCO_2	Y6
NA	VCCO_3	AC6
NA	VCCO_3	AD6
NA	VCCO_3	AH6
NA	VCCO_3	AJ6
NA	VCCO_3	AL6
NA	VCCO_3	AM6
NA	VCCO_3	AR6
NA	VCCO_3	AT6
NA	VCCO_4	AU11
NA	VCCO_4	AU12
NA	VCCO_4	AU14
NA	VCCO_4	AU15
NA	VCCO_4	AU19
NA	VCCO_4	AU20
NA	VCCO_4	AU7
NA	VCCO_4	AU8
NA	VCCO_5	AU23
NA	VCCO_5	AU24
NA	VCCO_5	AU28
NA	VCCO_5	AU29
NA	VCCO_5	AU31
NA	VCCO_5	AU32
NA	VCCO_5	AU35
NA	VCCO_5	AU36

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
NA	VCCO_6	AC37
NA	VCCO_6	AD37
NA	VCCO_6	AH37
NA	VCCO_6	AJ37
NA	VCCO_6	AL37
NA	VCCO_6	AM37
NA	VCCO_6	AR37
NA	VCCO_6	AT37
NA	VCCO_7	G37
NA	VCCO_7	H37
NA	VCCO_7	L37
NA	VCCO_7	M37
NA	VCCO_7	P37
NA	VCCO_7	R37
NA	VCCO_7	W37
NA	VCCO_7	Y37
NA	GND	N6
NA	GND	N5
NA	GND	N38
NA	GND	N37
NA	GND	F6
NA	GND	F37
NA	GND	F30
NA	GND	F22
NA	GND	F21
NA	GND	F13
NA	GND	E5
NA	GND	E38
NA	GND	E30
NA	GND	E22
NA	GND	E21
NA	GND	E13
NA	GND	D42
NA	GND	D4
NA	GND	D39
NA	GND	D1

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
0	IO_L6P_YY	H10 ⁵
0	IO_L7N_Y	D7
0	IO_L7P_Y	B5
0	IO_L8N_Y	K12
0	IO_L8P_Y	E8
0	IO_L9N	B6 ⁴
0	IO_L9P	F9 ⁵
0	IO_L10N_YY	G10
0	IO_L10P_YY	C7
0	IO_VREF_L11N_YY	D8
0	IO_L11P_YY	B7
0	IO_L12N	H11 ⁴
0	IO_L12P	C8 ⁵
0	IO_L13N_Y	E9
0	IO_L13P_Y	B8
0	IO_VREF_L14N_Y	K13 ²
0	IO_L14P_Y	G11
0	IO_L15N	A8 ⁴
0	IO_L15P	F10 ⁵
0	IO_L16N_YY	C9
0	IO_L16P_YY	H12
0	IO_VREF_L17N_YY	D10
0	IO_L17P_YY	A9
0	IO_L18N_Y	F11
0	IO_L18P_Y	A10
0	IO_L19N_Y	K14
0	IO_L19P_Y	C10
0	IO_VREF_L20N_YY	H13
0	IO_L20P_YY	G12
0	IO_L21N_YY	A11
0	IO_L21P_YY	B11
0	IO_L22N_Y	E12
0	IO_L22P_Y	D11
0	IO_L23N_Y	G13

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
0	IO_L23P_Y	C12
0	IO_L24N_Y	K15
0	IO_L24P_Y	A12
0	IO_L25N_Y	B12
0	IO_L25P_Y	H14
0	IO_L26N_YY	D12
0	IO_L26P_YY	F13
0	IO_VREF_L27N_YY	A13
0	IO_L27P_YY	B13
0	IO_L28N_YY	J15 ⁴
0	IO_L28P_YY	G14 ⁵
0	IO_L29N_Y	C13
0	IO_L29P_Y	F14
0	IO_L30N_Y	H15
0	IO_L30P_Y	D13
0	IO_L31N	A14 ⁴
0	IO_L31P	K16 ⁵
0	IO_L32N_YY	E14
0	IO_L32P_YY	B14
0	IO_VREF_L33N_YY	G15
0	IO_L33P_YY	D14
0	IO_L34N	J16 ⁴
0	IO_L34P	D15 ⁵
0	IO_L35N_Y	F15
0	IO_L35P_Y	B15
0	IO_L36N_Y	A15
0	IO_L36P_Y	E15
0	IO_L37N	G16 ⁴
0	IO_L37P	A16 ⁵
0	IO_L38N_YY	F16
0	IO_L38P_YY	J17
0	IO_VREF_L39N_YY	C16
0	IO_L39P_YY	B16
0	IO_L40N_Y	H17

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
6	IO_VREF_L265N_Y	AJ3
6	IO_L265P_Y	AG5
6	IO_L266N_YY	AD9 ⁴
6	IO_L266P_YY	AJ2 ⁵
6	IO_L267N_YY	AC10
6	IO_L267P_YY	AH2
6	IO_L268N_Y	AH3
6	IO_L268P_Y	AF5
6	IO_L269N_Y	AE8 ⁴
6	IO_L269P_Y	AG3 ⁵
6	IO_L270N_Y	AE7
6	IO_L270P_Y	AG2
6	IO_VREF_L271N_YY	AF6
6	IO_L271P_YY	AG1
6	IO_L272N_YY	AC9 ⁴
6	IO_L272P_YY	AG4 ⁵
6	IO_L273N_YY	AE6
6	IO_L273P_YY	AF3
6	IO_VREF_L274N_Y	AF1 ²
6	IO_L274P_Y	AF4
6	IO_L275N	AB10 ⁴
6	IO_L275P	AF2 ⁵
6	IO_L276N_Y	AC8
6	IO_L276P_Y	AE1
6	IO_VREF_L277N_YY	AD5
6	IO_L277P_YY	AE3
6	IO_L278N_YY	AC7
6	IO_L278P_YY	AD1
6	IO_L279N_Y	AD6
6	IO_L279P_Y	AD2
6	IO_VREF_L280N_YY	AB8
6	IO_L280P_YY	AC1
6	IO_L281N_YY	AC5
6	IO_L281P_YY	AC2

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
6	IO_L282N_Y	AA9
6	IO_L282P_Y	AC3
6	IO_L283N_Y	AC4
6	IO_L283P_Y	AD4
6	IO_L284N_Y	AA8
6	IO_L284P_Y	AB6
6	IO_L285N	AB1
6	IO_L285P	Y10
6	IO_L286N_Y	AB2
6	IO_L286P_Y	AA7
6	IO_VREF_L287N_Y	AA4
6	IO_L287P_Y	AA1
6	IO_L288N_YY	Y9 ⁴
6	IO_L288P_YY	AB4 ⁵
6	IO_L289N_YY	AA2
6	IO_L289P_YY	Y8
6	IO_L290N_Y	AA6
6	IO_L290P_Y	AA5
6	IO_L291N_Y	AB3 ⁴
6	IO_L291P_Y	Y7 ⁵
6	IO_L292N_Y	Y1
6	IO_L292P_Y	W10
6	IO_VREF_L293N_YY	Y5
6	IO_L293P_YY	Y2
6	IO_L294N_YY	W9 ⁴
6	IO_L294P_YY	W2 ⁵
6	IO_L295N_YY	W7
6	IO_L295P_YY	Y4
6	IO_L296N_Y	W1
6	IO_L296P_Y	Y6
6	IO_L297N_Y	W6 ⁴
6	IO_L297P_Y	W3 ⁵
6	IO_L298N_Y	V9
6	IO_L298P_Y	W4

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
7	IO_L324P_Y	L4
7	IO_L325N_YY	J1
7	IO_L325P_YY	L5
7	IO_L326N_YY	J2
7	IO_VREF_L326P_YY	K3
7	IO_L327N_Y	L7
7	IO_L327P_Y	J3
7	IO_L328N_Y	M9 ⁵
7	IO_L328P_Y	H2 ⁴
7	IO_L329N_Y	J4
7	IO_VREF_L329P_Y	K6 ²
7	IO_L330N_YY	L8
7	IO_L330P_YY	G2
7	IO_L331N_YY	H3 ⁵
7	IO_L331P_YY	K7 ⁴
7	IO_L332N_YY	G3
7	IO_VREF_L332P_YY	J5
7	IO_L333N_Y	L9
7	IO_L333P_Y	H5
7	IO_L334N_Y	J6 ⁵
7	IO_L334P_Y	H4 ⁴
7	IO_L335N_Y	G4
7	IO_L335P_Y	K8
7	IO_L336N_YY	J7
7	IO_L336P_YY	F2
7	IO_L337N_YY	F3 ⁵
7	IO_L337P_YY	L10 ⁴
7	IO_L338N_Y	E1
7	IO_VREF_L338P_Y_Y	H6
7	IO_L339N_Y	G5
7	IO_L339P_Y	E2
7	IO_L340N	K9
7	IO_L340P	D1
7	IO_L341N_Y	E3

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
7	IO_VREF_L341P_Y	J8
7	IO_L342N_Y	E4
7	IO_L342P_Y	D2
7	IO_L343N_Y	F4
7	IO_L343P_Y	D3
2	CCLK	C31
3	DONE	AM31
NA	DXN	AJ5
NA	DXP	AL5
NA	M0	AK4
NA	M1	AG7
NA	M2	AL3
NA	PROGRAM	AG28
NA	TCK	D5
NA	TDI	C30
2	TDO	K26
NA	TMS	C4
NA	VCCINT	K10
NA	VCCINT	K17
NA	VCCINT	K18
NA	VCCINT	K25
NA	VCCINT	L11
NA	VCCINT	L24
NA	VCCINT	M12
NA	VCCINT	M23
NA	VCCINT	N13
NA	VCCINT	N14
NA	VCCINT	N15
NA	VCCINT	N16
NA	VCCINT	N19
NA	VCCINT	N20
NA	VCCINT	N21

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
NA	GND	AP2
NA	GND	AN3
NA	GND	AM20
NA	GND	AK30
NA	GND	AG8
NA	GND	AC29
NA	GND	Y3
NA	GND	Y32
NA	GND	W21
NA	GND	V21
NA	GND	T8
NA	GND	T27
NA	GND	R21
NA	GND	P21
NA	GND	H19
NA	GND	F29
NA	GND	C11
NA	GND	B3
NA	GND	A32
NA	GND	AP3
NA	GND	AN32
NA	GND	AM24
NA	GND	AJ6
NA	GND	AG16
NA	GND	AA14
NA	GND	Y14
NA	GND	W8
NA	GND	W27
NA	GND	U14
NA	GND	T14
NA	GND	R3
NA	GND	R32
NA	GND	M6
NA	GND	H27

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
NA	GND	E5
NA	GND	C15
NA	GND	B32
NA	GND	A33
NA	GND	AP7
NA	GND	AN33
NA	GND	AM32
NA	GND	AJ12
NA	GND	AG19
NA	GND	AA15
NA	GND	Y15
NA	GND	W14
NA	GND	V14
NA	GND	U15
NA	GND	T15
NA	GND	R14
NA	GND	P14
NA	GND	M29
NA	GND	G1
NA	GND	E18
NA	GND	C20
NA	GND	B33
NA	GND	A34
NA	GND	AP28
NA	GND	AN34
NA	GND	AM33
NA	GND	AJ23
NA	GND	AG27
NA	GND	AA16
NA	GND	Y16
NA	GND	W15
NA	GND	V15
NA	GND	U16
NA	GND	T16

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
71	1	A27	G24	3200 2000 1000	-
72	1	G25	B27	3200 1600	-
73	1	C27	E26	3200 2600 2000 1600 1000	VREF
74	1	B28	J24	3200 2600 2000 1600 1000	-
75	1	H25	K24	3200 2600	-
76	1	F26	D27	3200 1000	-
77	1	C28	G26	3200 1000	-
78	1	J25	E27	2000 1600	-
79	1	H26	A30	3200 2600 2000 1600 1000	VREF
80	1	B29	G27	3200 2600 2000 1600 1000	-
81	1	C29	F27	3200 2600 1000	-
82	1	F28	E28	3200 2000 1000	VREF
83	1	B30	L25	3200 2000 1000	-
84	1	E29	B31	3200 1600 1000	-
85	1	D30	A31	3200 2600 2000 1600 1000	CS
86	2	D32	J27	3200 2600 2000 1600 1000	DIN, D0
87	2	E31	F30	3200 2600 2000	-
88	2	G29	F32	2600 2000 1000	-
89	2	E32	G30	3200 2600 1600 1000	VREF
90	2	M25	G31	2600 1600	-

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
91	2	L26	D33	3200 2600 1600 1000	-
92	2	D34	H29	2600 2000 1000	VREF
93	2	J28	E33	3200 2600 2000 1600	-
94	2	H28	H30	3200 2600 2000 1600 1000	-
95	2	H32	K28	3200 2600 1600 1000	-
96	2	L27	F33	3200 2600 2000	-
97	2	M26	E34	2600 2000 1000	-
98	2	H31	G32	3200 2600 2000 1600 1000	VREF
99	2	N25	J31	2000 1600	-
100	2	J30	G33	3200 2600 2000 1600 1000	-
101	2	H34	J29	2600 1000	VREF
102	2	M27	H33	3200 2600 1600	-
103	2	K29	J34	3200 2600 1600 1000	-
104	2	L29	J33	3200 2600 2000 1600 1000	VREF
105	2	M28	K34	3200 2600 2000 1600 1000	-
106	2	N27	L34	3200 1600 1000	-
107	2	K33	P26	2000 1600 1000	D1
108	2	R25	M34	3200 2600 2000	-
109	2	L31	L33	2000 1000	-
110	2	P27	M33	3200 2600 1600 1000	-