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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

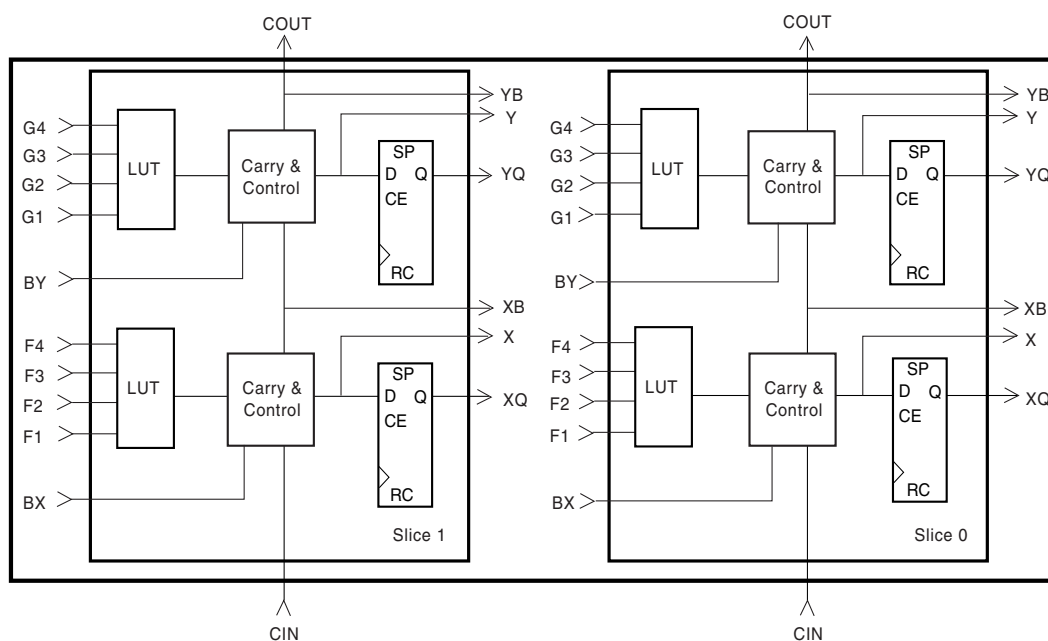
Product Status	Obsolete
Number of LABs/CLBs	1176
Number of Logic Elements/Cells	5292
Total RAM Bits	114688
Number of I/O	176
Number of Gates	306393
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv200e-7fg256c

Date	Version	Revision
11/20/00	1.8	- Upgraded speed grade -8 numbers in Virtex-E Electrical Characteristics tables to Preliminary. - Updated minimums in Table 13 and added notes to Table 14. - Added to note 2 to Absolute Maximum Ratings. - Changed speed grade -8 numbers for $T_{SHCKO32}$, T_{REG}, T_{BCCS}, and T_{ICKOF} - Changed all minimum hold times to -0.4 under Global Clock Setup and Hold for LVTTTL Standard, with DLL. - Revised maximum T_{DLLPW} in -6 speed grade for DLL Timing Parameters. - Changed GCLK0 to BA22 for FG860 package in Table 46.
2/12/01	1.9	- Revised footnote for Table 14. - Added numbers to Virtex-E Electrical Characteristics tables for XCV1000E and XCV2000E devices. - Updated Table 27 and Table 78 to include values for XCV400E and XCV600E devices. - Revised Table 62 to include pinout information for the XCV400E and XCV600E devices in the BG560 package. - Updated footnotes 1 and 2 for Table 76 to include XCV2600E and XCV3200E devices.
4/2/01	2.0	- Updated numerous values in Virtex-E Switching Characteristics tables. - Converted data sheet to modularized format. See the Virtex-E Data Sheet section.
10/25/01	2.1	Updated the Virtex-E Device/Package Combinations and Maximum I/O table to show XCV3200E in the FG1156 package.
11/09/01	2.2	Minor edits.
07/17/02	2.3	Data sheet designation upgraded from Preliminary to Production.

Virtex-E Data Sheet

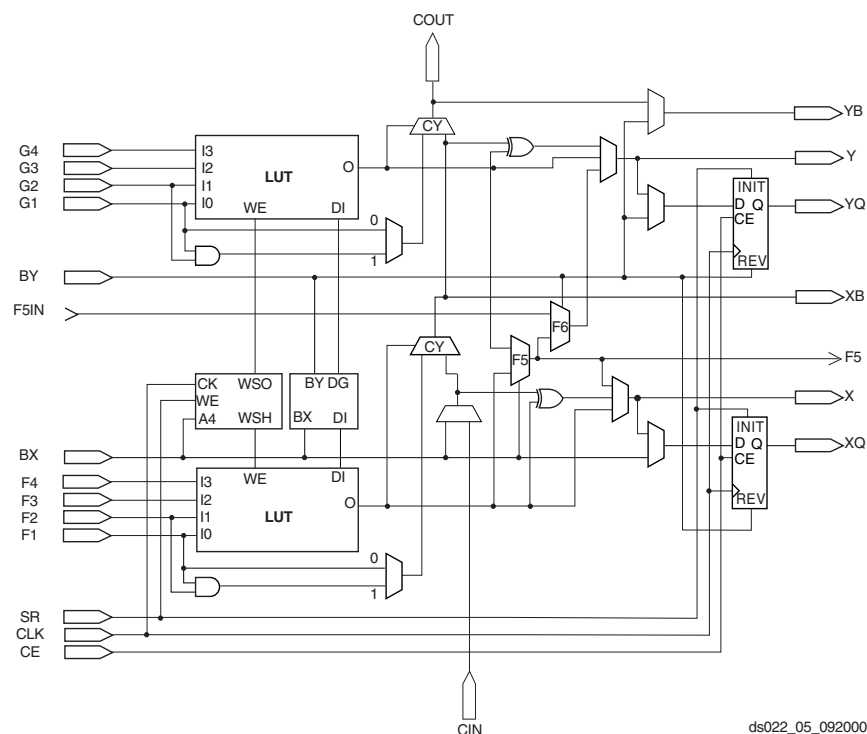
The Virtex-E Data Sheet contains the following modules:

- DS022-1, Virtex-E 1.8V FPGAs:
Introduction and Ordering Information (Module 1)
- DS022-2, Virtex-E 1.8V FPGAs:
[Functional Description \(Module 2\)](#)
- DS022-3, Virtex-E 1.8V FPGAs:
[DC and Switching Characteristics \(Module 3\)](#)
- DS022-4, Virtex-E 1.8V FPGAs:
[Pinout Tables \(Module 4\)](#)



ds022_04_121799

Figure 4: 2-Slice Virtex-E CLB



ds022_05_092000

Figure 5: Detailed View of Virtex-E Slice

Storage Elements

The storage elements in the Virtex-E slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by

the function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each Slice has synchronous set and reset signals (SR and BY). SR

Because any single DLL can access only two BUFs at most, any additional output clock signals must be routed from the DLL in this example on the high speed backbone routing.

The dll_2x files in the [xapp132.zip](#) file show the VHDL and Verilog implementation of this circuit.

Virtex-E 4x Clock

Two DLLs located in the same half-edge (top-left, top-right, bottom-right, bottom-left) can be connected together, without using a BUFG between the CLKDLLs, to generate a 4x clock as shown in [Figure 30](#). Virtex-E devices, like the Virtex devices, have four clock networks that are available for internal deskewing of the clock. Each of the eight DLLs have access to two of the four clock networks. Although all the DLLs can be used for internal deskewing, the presence of two GCLKBUFs on the top and two on the bottom indicate that only two of the four DLLs on the top (and two of the four DLLs on the bottom) can be used for this purpose.

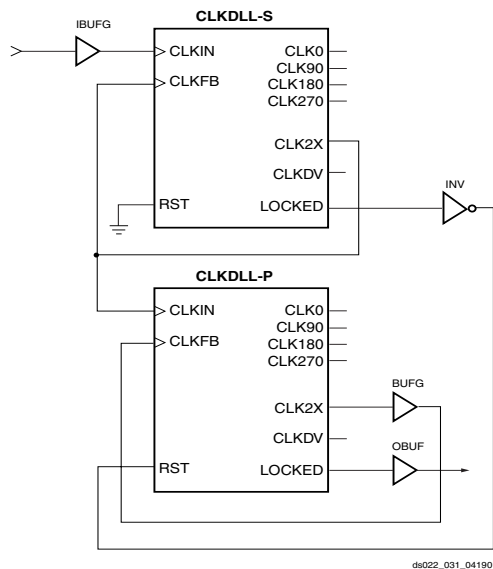


Figure 30: DLL Generation of 4x Clock in Virtex-E Devices

The dll_4xe files in the xapp132.zip file show the DLL implementation in Verilog for Virtex-E devices. These files can be found at:

<ftp://ftp.xilinx.com/pub/applications/xapp/xapp132.zip>

Using Block SelectRAM+ Features

The Virtex FPGA Series provides dedicated blocks of on-chip, true dual-read/write port synchronous RAM, with 4096 memory cells. Each port of the block SelectRAM+ memory can be independently configured as a read/write port, a read port, a write port, and can be configured to a specific data width. The block SelectRAM+ memory offers

new capabilities allowing the FPGA designer to simplify designs.

Operating Modes

Virtex-E block SelectRAM+ memory supports two operating modes:

- Read Through
- Write Back

Read Through (one clock edge)

The read address is registered on the read port clock edge and data appears on the output after the RAM access time. Some memories might place the latch/register at the outputs, depending on whether a faster clock-to-out versus set-up time is desired. This is generally considered to be an inferior solution, since it changes the read operation to an asynchronous function with the possibility of missing an address/control line transition during the generation of the read pulse clock.

Write Back (one clock edge)

The write address is registered on the write port clock edge and the data input is written to the memory and mirrored on the output.

Block SelectRAM+ Characteristics

- All inputs are registered with the port clock and have a set-up to clock timing specification.
- All outputs have a read through or write back function depending on the state of the port WE pin. The outputs relative to the port clock are available after the clock-to-out timing specification.
- The block SelectRAMs are true SRAM memories and do not have a combinatorial path from the address to the output. The LUT SelectRAM+ cells in the CLBs are still available with this function.
- The ports are completely independent from each other (*i.e.*, clocking, control, address, read/write function, and data width) without arbitration.
- A write operation requires only one clock edge.
- A read operation requires only one clock edge.

The output ports are latched with a self timed circuit to guarantee a glitch free read. The state of the output port does not change until the port executes another read or write operation.

Library Primitives

[Figure 31](#) and [Figure 32](#) show the two generic library block SelectRAM+ primitives. [Table 14](#) describes all of the available primitives for synthesis and simulation.

Data Output Bus—DO[AIB]<#:0>

The data out bus reflects the contents of the memory cells referenced by the address bus at the last active clock edge. During a write operation, the data out bus reflects the data in bus. The width of this bus equals the width of the port. The allowed widths appear in [Table 15](#).

Inverting Control Pins

The four control pins (CLK, EN, WE and RST) for each port have independent inversion control as a configuration option.

Address Mapping

Each port accesses the same set of 4096 memory cells using an addressing scheme dependent on the width of the port.

The physical RAM location addressed for a particular width are described in the following formula (of interest only when the two ports use different aspect ratios).

$$\text{Start} = ((\text{ADDR}_{\text{port}} + 1) * \text{Width}_{\text{port}}) - 1$$

$$\text{End} = \text{ADDR}_{\text{port}} * \text{Width}_{\text{port}}$$

Conflict Resolution

The block SelectRAM+ memory is a true dual-read/write port RAM that allows simultaneous access of the same memory cell from both ports. When one port writes to a given memory cell, the other port must not address that memory cell (for a write or a read) within the clock-to-clock setup window. The following lists specifics of port and memory cell write conflict resolution.

- If both ports write to the same memory cell simultaneously, violating the clock-to-clock setup requirement, consider the data stored as invalid.
- If one port attempts a read of the same memory cell the other simultaneously writes, violating the clock-to-clock setup requirement, the following occurs.
 - The write succeeds
 - The data out on the writing port accurately reflects the data written.
 - The data out on the reading port is invalid.

Conflicts do not cause any physical damage.

[Table 16](#) shows low order address mapping for each port width.

Table 16: Port Address Mapping

Port Width	Port Addresses																
1	4095...	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2	2047...	07		06		05		04		03		02		01		00	
4	1023...	03				02				01				00			
8	511...	01								00							
16	255...	00															

Creating Larger RAM Structures

The block SelectRAM+ columns have specialized routing to allow cascading blocks together with minimal routing delays. This achieves wider or deeper RAM structures with a smaller timing penalty than when using normal routing channels.

Location Constraints

Block SelectRAM+ instances can have LOC properties attached to them to constrain the placement. The block SelectRAM+ placement locations are separate from the CLB location naming convention, allowing the LOC properties to transfer easily from array to array.

The LOC properties use the following form.

$$\text{LOC} = \text{RAMB4_R\#C\#}$$

RAMB4_R0C0 is the upper left RAMB4 location on the device.

Single Port Timing

[Figure 33](#) shows a timing diagram for a single port of a block SelectRAM+ memory. The block SelectRAM+ AC switching characteristics are specified in the data sheet. The block SelectRAM+ memory is initially disabled.

At the first rising edge of the CLK pin, the ADDR, DI, EN, WE, and RST pins are sampled. The EN pin is High and the WE pin is Low indicating a read operation. The DO bus contains the contents of the memory location, 0x00, as indicated by the ADDR bus.

At the second rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN and WE pins are High indicating a write operation. The DO bus mirrors the DI bus. The DI bus is written to the memory location 0x0F.

At the third rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN pin is High and the WE pin is Low indicating a read operation. The DO bus contains the contents of the memory location 0x7E as indicated by the ADDR bus.

At the fourth rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN pin is Low

HSTL

A sample circuit illustrating a valid termination technique for HSTL_I appears in [Figure 46](#). A sample circuit illustrating a valid termination technique for HSTL_III appears in [Figure 47](#).

Table 25: HSTL Class I Voltage Specification

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF}	0.68	0.75	0.90
V_{TT}	-	$V_{CCO} \times 0.5$	-
V_{IH}	$V_{REF} + 0.1$	-	-
V_{IL}	-	-	$V_{REF} - 0.1$
V_{OH}	$V_{CCO} - 0.4$	-	-
V_{OL}			0.4
I_{OH} at V_{OH} (mA)	-8	-	-
I_{OL} at V_{OL} (mA)	8	-	-

HSTL Class I

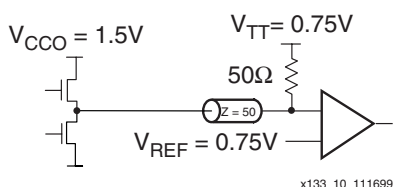


Figure 46: Terminated HSTL Class I

Table 26: HSTL Class III Voltage Specification

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
$V_{REF}^{(1)}$	-	0.90	-
V_{TT}	-	V_{CCO}	-
V_{IH}	$V_{REF} + 0.1$	-	-
V_{IL}	-	-	$V_{REF} - 0.1$
V_{OH}	$V_{CCO} - 0.4$	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	-8	-	-
I_{OL} at V_{OL} (mA)	24	-	-

Note: Per EIA/JESD8-6, "The value of V_{REF} is to be selected by the user to provide optimum noise margin in the use conditions specified by the user."

HSTL Class III

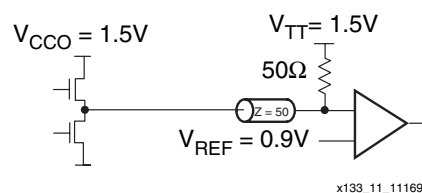


Figure 47: Terminated HSTL Class III

A sample circuit illustrating a valid termination technique for HSTL_IV appears in [Figure 48](#).

Table 27: HSTL Class IV Voltage Specification

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF}	-	0.90	-
V_{TT}	-	V_{CCO}	-
V_{IH}	$V_{REF} + 0.1$	-	-
V_{IL}	-	-	$V_{REF} - 0.1$
V_{OH}	$V_{CCO} - 0.4$	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	-8	-	-
I_{OL} at V_{OL} (mA)	48	-	-

Note: Per EIA/JESD8-6, "The value of V_{REF} is to be selected by the user to provide optimum noise margin in the use conditions specified by the user."

HSTL Class IV

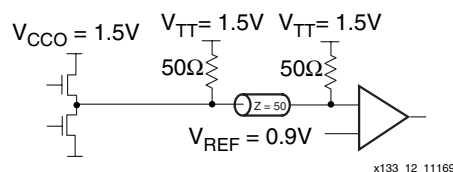


Figure 48: Terminated HSTL Class IV

DC Characteristics

Absolute Maximum Ratings

Symbol	Description ⁽¹⁾			Units
V _{CCINT}	Internal Supply voltage relative to GND		–0.5 to 2.0	V
V _{CCO}	Supply voltage relative to GND		–0.5 to 4.0	V
V _{REF}	Input Reference Voltage		–0.5 to 4.0	V
V _{IN} ⁽³⁾	Input voltage relative to GND		–0.5 to V _{CCO} +0.5	V
V _{TS}	Voltage applied to 3-state output		–0.5 to 4.0	V
V _{CC}	Longest Supply Voltage Rise Time from 0 V - 1.71 V		50	ms
T _{STG}	Storage temperature (ambient)		–65 to +150	°C
T _J	Junction temperature ⁽²⁾	Plastic packages	+125	°C

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time can affect device reliability.
- For soldering guidelines and thermal considerations, see the device packaging information on www.xilinx.com.
- Inputs configured as PCI are fully PCI compliant. This statement takes precedence over any specification that would imply that the device is not PCI compliant.

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V _{CCINT}	Internal Supply voltage relative to GND, T _J = 0 °C to +85 °C	Commercial	1.8 – 5%	1.8 + 5%	V
	Internal Supply voltage relative to GND, T _J = –40 °C to +100 °C	Industrial	1.8 – 5%	1.8 + 5%	V
V _{CCO}	Supply voltage relative to GND, T _J = 0 °C to +85 °C	Commercial	1.2	3.6	V
	Supply voltage relative to GND, T _J = –40 °C to +100 °C	Industrial	1.2	3.6	V
T _{IN}	Input signal transition time			250	ns

Virtex-E Pin Definitions

Pin Name	Dedicated Pin	Direction	Description
GCK0, GCK1, GCK2, GCK3	Yes	Input	Clock input pins that connect to Global Clock Buffers.
M0, M1, M2	Yes	Input	Mode pins are used to specify the configuration mode.
CCLK	Yes	Input or Output	The configuration Clock I/O pin: it is an input for SelectMAP and slave-serial modes, and output in master-serial mode. After configuration, it is input only, logic level = Don't Care.
PROGRAM	Yes	Input	Initiates a configuration sequence when asserted Low.
DONE	Yes	Bidirectional	Indicates that configuration loading is complete, and that the start-up sequence is in progress. The output can be open drain.
INIT	No	Bidirectional (Open-drain)	When Low, indicates that the configuration memory is being cleared. The pin becomes a user I/O after configuration.
BUSY/DOUT	No	Output	In SelectMAP mode, BUSY controls the rate at which configuration data is loaded. The pin becomes a user I/O after configuration unless the SelectMAP port is retained. In bit-serial modes, DOUT provides preamble and configuration data to downstream devices in a daisy-chain. The pin becomes a user I/O after configuration.
D0/DIN, D1, D2, D3, D4, D5, D6, D7	No	Input or Output	In SelectMAP mode, D0-7 are configuration data pins. These pins become user I/Os after configuration unless the SelectMAP port is retained. In bit-serial modes, DIN is the single data input. This pin becomes a user I/O after configuration.
WRITE	No	Input	In SelectMAP mode, the active-low Write Enable signal. The pin becomes a user I/O after configuration unless the SelectMAP port is retained.
CS	No	Input	In SelectMAP mode, the active-low Chip Select signal. The pin becomes a user I/O after configuration unless the SelectMAP port is retained.
TDI, TDO, TMS, TCK	Yes	Mixed	Boundary-scan Test-Access-Port pins, as defined in IEEE1149.1.
DXN, DXP	Yes	N/A	Temperature-sensing diode pins. (Anode: DXP, cathode: DXN)
V _{CCINT}	Yes	Input	Power-supply pins for the internal core logic.
V _{CCO}	Yes	Input	Power-supply pins for the output drivers (subject to banking rules)
V _{REF}	No	Input	Input threshold voltage pins. Become user I/Os when an external threshold voltage is not needed (subject to banking rules).
GND	Yes	Input	Ground

Table 6: PQ240 — XCV50E, XCV100E, XCV200E, XCV300E, XCV400E

Pin #	Pin Description	Bank
P74	IO_L43P_YY	5
P73 ¹	IO_VREF_L43N_YY	5
P72	IO	5
P71	IO_L44P_YY	5
P70	IO_VREF_L44N_YY	5
P68	IO_L45P_YY	5
P67	IO_L45N_YY	5
P66 ²	IO_VREF_L46P_Y	5
P65	IO_L46N_Y	5
P64	IO_L47P_YY	5
P63	IO_L47N_YY	5
P57	IO_L48N_YY	6
P56	IO_L48P_YY	6
P54 ²	IO_VREF	6
P53	IO_L49N_Y	6
P52	IO_L49P_Y	6
P50	IO_VREF_L50N_Y	6
P49	IO_L50P_Y	6
P48	IO	6
P47 ¹	IO_VREF_L51N_Y	6
P46	IO_L51P_Y	6
P42	IO_L52N_YY	6
P41	IO_L52P_YY	6
P40	IO	6
P39	IO_L53N_Y	6
P38	IO_L53P_Y	6
P36	IO_VREF_L54N_Y	6
P35	IO_L54P_Y	6
P34	IO_L55N_Y	6
P33 ³	IO_VREF_L55P_Y	6
P31	IO	6
P28	IO_L56N_YY	7
P27	IO_L56P_YY	7

Table 6: PQ240 — XCV50E, XCV100E, XCV200E, XCV300E, XCV400E

Pin #	Pin Description	Bank
P26 ³	IO_VREF	7
P24	IO_L57N_Y	7
P23	IO_VREF_L57P_Y	7
P21	IO_L58N_Y	7
P20	IO_L58P_Y	7
P19	IO	7
P18	IO_L59N_YY	7
P17	IO_L59P_YY	7
P13	IO_L60N_Y	7
P12 ¹	IO_VREF_L60P_Y	7
P11	IO	7
P10	IO_L61N_Y	7
P9	IO_VREF_L61P_Y	7
P7	IO_L62N_Y	7
P6	IO_L62P_Y	7
P5 ²	IO_VREF_L63N_Y	7
P4	IO_L63P_Y	7
P3	IO	7
P179	CCLK	2
P120	DONE	3
P60	M0	NA
P58	M1	NA
P62	M2	NA
P122	PROGRAM	NA
P183	TDI	NA
P239	TCK	NA
P181	TDO	2
P2	TMS	NA
P225	VCCINT	NA
P214	VCCINT	NA
P198	VCCINT	NA
P164	VCCINT	NA
P148	VCCINT	NA

Table 14: BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin#	See Note
4	IO_L104N_YY	AJ12	
4	IO_L105P_Y	AN11	
4	IO_L105N_Y	AK12	
4	IO_L106P_YY	AL12	
4	IO_L106N_YY	AM12	
4	IO_VREF_L107P_YY	AK13	3
4	IO_L107N_YY	AL13	
4	IO_L108P_Y	AM13	
4	IO_L108N_Y	AN13	
4	IO_L109P_YY	AJ14	
4	IO_L109N_YY	AK14	
4	IO_VREF_L110P_YY	AM14	
4	IO_L110N_YY	AN15	
4	IO_L111P_Y	AJ15	
4	IO_L111N_Y	AK15	
4	IO_L112P_Y	AL15	
4	IO_L112N_Y	AM16	
4	IO_VREF_L113P_Y	AL16	
4	IO_L113N_Y	AJ16	
4	IO_L114P_Y	AK16	
4	IO_VREF_L114N_Y	AN17	2
4	IO_LVDS_DLL_L115P	AM17	
5	GCK1	AJ17	
5	IO	AL25	
5	IO	AL28	
5	IO	AL30	
5	IO	AN28	
5	IO_LVDS_DLL_L115N	AM18	
5	IO_VREF	AL18	2
5	IO_L116P_Y	AK18	
5	IO_VREF_L116N_Y	AJ18	
5	IO_L117P_Y	AN19	
5	IO_L117N_Y	AL19	
5	IO_L118P_Y	AK19	

Table 14: BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin#	See Note
5	IO_L118N_Y	AM20	
5	IO_L119P_YY	AJ19	
5	IO_VREF_L119N_YY	AL20	
5	IO_L120P_YY	AN21	
5	IO_L120N_YY	AL21	
5	IO_L121P_Y	AJ20	
5	IO_L121N_Y	AM22	
5	IO_L122P_YY	AK21	
5	IO_VREF_L122N_YY	AN23	3
5	IO_L123P_YY	AJ21	
5	IO_L123N_YY	AM23	
5	IO_L124P_Y	AK22	
5	IO_L124N_Y	AM24	
5	IO_L125P_YY	AL23	
5	IO_L125N_YY	AJ22	
5	IO_L126P_YY	AK23	
5	IO_VREF_L126N_YY	AL24	
5	IO_L127P_Y	AN26	
5	IO_L127N_Y	AJ23	
5	IO_L128P_Y	AK24	
5	IO_VREF_L128N_Y	AM26	4
5	IO_L129P_Y	AM27	
5	IO_L129N_Y	AJ24	
5	IO_L130P_Y	AL26	
5	IO_VREF_L130N_Y	AK25	1
5	IO_L131P_YY	AN29	
5	IO_VREF_L131N_YY	AJ25	
5	IO_L132P_YY	AK26	
5	IO_L132N_YY	AM29	
5	IO_L133P_Y	AM30	
5	IO_L133N_Y	AJ26	
5	IO_L134P_YY	AK27	
5	IO_VREF_L134N_YY	AL29	
5	IO_L135P_YY	AN31	
5	IO_L135N_YY	AJ27	

Table 16: FG256 Package — XCV50E, XCV100E, XCV200E, XCV300E

Bank	Pin Description	Pin #
NA	GND	K11
NA	GND	K10
NA	GND	K9
NA	GND	K8
NA	GND	K7
NA	GND	K6
NA	GND	J10
NA	GND	J9
NA	GND	J8
NA	GND	J7
NA	GND	H10
NA	GND	H9
NA	GND	H8
NA	GND	H7
NA	GND	G11
NA	GND	G10
NA	GND	G9
NA	GND	G8
NA	GND	G7
NA	GND	G6
NA	GND	F11
NA	GND	F10
NA	GND	F7
NA	GND	F6
NA	GND	B15
NA	GND	B2
NA	GND	A16
NA	GND	A1

Notes:

1. V_{REF} or I/O option only in the XCV100E, 200E, 300E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV200E, 300E; otherwise, I/O option only.

FG256 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A $\checkmark$ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 17: FG256 Differential Pin Pair Summary XCV50E, XCV100E, XCV200E, XCV300E

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	N8	N9	NA	IO_DLL_L52P
1	5	R8	T8	NA	IO_DLL_L52N
2	1	C9	A8	NA	IO_DLL_L8P
3	0	B8	A7	NA	IO_DLL_L8N
IO LVDS					
Total Pairs: 83, Asynchronous Outputs: 35					
0	0	A3	C5	7	VREF
1	0	E6	D5	$\checkmark$	-
2	0	A4	B4	$\checkmark$	VREF
3	0	B5	D6	2	-
4	0	A5	C6	$\checkmark$	VREF
5	0	C7	B6	$\checkmark$	-
6	0	C8	D7	1	-
7	0	A6	B7	1	VREF
8	1	A8	A7	NA	IO_LVDS_DLL
9	1	A9	D9	2	-
10	1	B9	E10	1	VREF
11	1	D10	A10	1	-
12	1	A11	C10	$\checkmark$	-
13	1	E11	B11	$\checkmark$	VREF
14	1	D11	A12	2	-
15	1	C11	A13	$\checkmark$	VREF
16	1	D12	B12	$\checkmark$	-
17	1	C12	A14	7	VREF
18	1	B13	C13	$\checkmark$	CS

Table 18: FG456 — XCV200E and XCV300E

Bank	Pin Description	Pin #
NA	VCCINT	T15
NA	VCCINT	T16
NA	VCCINT	U6
NA	VCCINT	U17
NA	VCCINT	V5
NA	VCCINT	V18
NA	VCCO_7	L7
NA	VCCO_7	K7
NA	VCCO_7	K6
NA	VCCO_7	J6
NA	VCCO_7	H6
NA	VCCO_7	G6
NA	VCCO_6	N7
NA	VCCO_6	M7
NA	VCCO_6	T6
NA	VCCO_6	R6
NA	VCCO_6	P6
NA	VCCO_6	N6
NA	VCCO_5	U10
NA	VCCO_5	U9
NA	VCCO_5	U8
NA	VCCO_5	U7
NA	VCCO_5	T11
NA	VCCO_5	T10
NA	VCCO_4	U16
NA	VCCO_4	U15
NA	VCCO_4	U14
NA	VCCO_4	U13
NA	VCCO_4	T13
NA	VCCO_4	T12
NA	VCCO_3	T17
NA	VCCO_3	R17
NA	VCCO_3	P17
NA	VCCO_3	N17
NA	VCCO_3	N16
NA	VCCO_3	M16

Table 18: FG456 — XCV200E and XCV300E

Bank	Pin Description	Pin #
NA	VCCO_2	K17
NA	VCCO_2	J17
NA	VCCO_2	H17
NA	VCCO_2	G17
NA	VCCO_2	L16
NA	VCCO_2	K16
NA	VCCO_1	G13
NA	VCCO_1	G12
NA	VCCO_1	F16
NA	VCCO_1	F15
NA	VCCO_1	F14
NA	VCCO_1	F13
NA	VCCO_0	G11
NA	VCCO_0	G10
NA	VCCO_0	F10
NA	VCCO_0	F9
NA	VCCO_0	F8
NA	VCCO_0	F7
NA	GND	AB22
NA	GND	AB1
NA	GND	AA21
NA	GND	AA2
NA	GND	Y20
NA	GND	Y3
NA	GND	P14
NA	GND	P13
NA	GND	P12
NA	GND	P11
NA	GND	P10
NA	GND	P9
NA	GND	N14
NA	GND	N13
NA	GND	N12
NA	GND	N11
NA	GND	N10
NA	GND	N9

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
1	IO_L40P_YY	D20
1	IO_L41N_YY	F19
1	IO_VREF_L41P_YY	C21
1	IO_L42N_YY	B22
1	IO_L42P_YY	E20
1	IO_L43N_Y	A23
1	IO_L43P_Y	D21
1	IO_WRITE_L44N_YY	C22
1	IO_CS_L44P_YY	E21
2	IO	D25 ¹
2	IO	D26
2	IO	E26
2	IO	F26
2	IO	H26 ¹
2	IO	K26 ¹
2	IO	M25 ¹
2	IO	N26 ¹
2	IO_D1	K24
2	IO_DOUT_BUSY_L45P_YY	E23
2	IO_DIN_D0_L45N_YY	F22
2	IO_L46P_YY	E24
2	IO_L46N_YY	F20
2	IO_L47P_Y	G21
2	IO_L47N_Y	G22
2	IO_VREF_L48P_Y	F24
2	IO_L48N_Y	H20
2	IO_L49P_Y	E25
2	IO_L49N_Y	H21
2	IO_L50P_YY	F23
2	IO_L50N_YY	G23
2	IO_VREF_L51P_YY	H23
2	IO_L51N_YY	J20
2	IO_L52P_YY	G24
2	IO_L52N_YY	H22
2	IO_L53P_Y	J21
2	IO_L53N_Y	G25

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
2	IO_VREF_L54P_Y	G26 ²
2	IO_L54N_Y	J22
2	IO_L55P_YY	H24
2	IO_L55N_YY	J23
2	IO_L56P_YY	J24
2	IO_VREF_L56N_YY	K20
2	IO_D2_L57P_YY	K22
2	IO_L57N_YY	K21
2	IO_L58P_YY	H25
2	IO_L58N_YY	K23
2	IO_L59P_Y	L20
2	IO_L59N_Y	J26
2	IO_L60P_Y	K25
2	IO_L60N_Y	L22
2	IO_L61P_Y	L21
2	IO_L61N_Y	L23
2	IO_L62P_Y	M20
2	IO_L62N_Y	L24
2	IO_VREF_L63P_YY	M23
2	IO_D3_L63N_YY	M22
2	IO_L64P_YY	L26
2	IO_L64N_YY	M21
2	IO_L65P_Y	N19
2	IO_L65N_Y	M24
2	IO_VREF_L66P_Y	M26
2	IO_L66N_Y	N20
2	IO_L67P_YY	N24
2	IO_L67N_YY	N21
2	IO_L68P_YY	N23
2	IO_L68N_YY	N22
3	IO	P24
3	IO	P26 ¹
3	IO	R26 ¹
3	IO	T26 ¹
3	IO	U26 ¹
3	IO	W25

Table 23: FG680 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
52	1	B8	A8	√	VREF
53	1	A7	D9	√	-
54	1	B7	C8	3	-
55	1	A6	D8	3	-
56	1	B6	C7	√	VREF
57	1	A5	D7	√	-
58	1	B5	C6	5	VREF
59	1	A4	D6	5	-
60	1	D5	B4	√	CS
61	2	E3	C2	√	DIN, D0
62	2	D3	F3	6	-
63	2	D2	G4	4	VREF
64	2	G3	E2	4	-
65	2	H4	E1	6	VREF
66	2	H3	F2	√	-
67	2	J4	F1	4	-
68	2	J3	G2	6	-
69	2	G1	K4	√	VREF
70	2	H2	K3	√	-
71	2	H1	L4	7	VREF
72	2	J2	L3	4	-
73	2	J1	M3	√	VREF
74	2	K2	N4	√	-
75	2	K1	N3	4	-
76	2	L2	P4	√	D1
77	2	P3	L1	√	D2
78	2	R4	M2	6	-
79	2	R3	M1	4	-
80	2	T4	N2	4	-
81	2	N1	T3	6	VREF
82	2	P2	U5	√	-
83	2	P1	U4	4	-
84	2	R2	U3	6	-
85	2	V5	R1	√	D3

Table 23: FG680 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
86	2	V4	T2	√	-
87	2	V3	T1	7	-
88	2	W4	U2	4	-
89	2	W3	U1	√	VREF
90	2	AA3	V2	√	-
91	2	AA4	V1	4	VREF
92	2	AB2	W2	√	-
93	3	AB4	W1	4	VREF
94	3	AB5	Y2	√	-
95	3	AC2	Y1	√	VREF
96	3	AC3	AA1	4	-
97	3	AC4	AA2	7	-
98	3	AC5	AB1	√	-
99	3	AD3	AC1	√	VREF
100	3	AD1	AD4	6	-
101	3	AD2	AE3	4	-
102	3	AE1	AE4	√	-
103	3	AE2	AF3	6	VREF
104	3	AF4	AF1	4	-
105	3	AG3	AF2	4	-
106	3	AG4	AG1	6	-
107	3	AH3	AG2	√	D5
108	3	AH1	AJ2	√	VREF
109	3	AH2	AJ3	4	-
110	3	AJ1	AJ4	√	-
111	3	AK1	AK3	√	VREF
112	3	AK2	AK4	4	-
113	3	AL1	AL2	7	VREF
114	3	AM1	AL3	√	-
115	3	AM2	AL4	√	VREF
116	3	AM3	AN1	6	-
117	3	AM4	AP1	4	-
118	3	AN2	AP2	√	-
119	3	AN3	AR1	6	VREF

Table 23: FG680 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
188	6	AP39	AP38	4	-
189	6	AN38	AN36	6	VREF
190	6	AN39	AN37	√	-
191	6	AM38	AM36	4	-
192	6	AL36	AM37	6	-
193	6	AL37	AM39	√	VREF
194	6	AK36	AL38	√	-
195	6	AK37	AL39	7	VREF
196	6	AJ36	AK38	4	-
197	6	AJ37	AK39	√	VREF
198	6	AH37	AJ38	√	-
199	6	AH38	AJ39	4	-
200	6	AG38	AH39	√	VREF
201	6	AG39	AG36	√	-
202	6	AF39	AG37	6	-
203	6	AE38	AF36	4	-
204	6	AF38	AF37	4	-
205	6	AE36	AE39	6	VREF
206	6	AE37	AD38	√	-
207	6	AD36	AD39	4	-
208	6	AC39	AC38	6	-
209	6	AB38	AD37	√	VREF
210	6	AB39	AC35	√	-
211	6	AA38	AC36	7	-
212	6	AA39	AC37	4	-
213	6	Y38	AB35	√	VREF
214	6	Y39	AB36	√	-
215	6	AA36	AB37	4	VREF
216	7	W38	AA37	√	-
217	7	V39	W37	4	VREF
218	7	U39	W36	√	-
219	7	U38	V38	√	VREF
220	7	T39	V37	4	-
221	7	T38	V36	7	-

Table 23: FG680 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
222	7	R39	V35	√	-
223	7	U36	U37	√	VREF
224	7	U35	R38	6	-
225	7	T37	P39	4	-
226	7	T36	P38	√	-
227	7	N38	N39	6	VREF
228	7	M39	R37	4	-
229	7	M38	R36	4	-
230	7	L39	P37	6	-
231	7	N37	P36	√	-
232	7	N36	L38	√	VREF
233	7	M37	K39	4	-
234	7	L37	K38	√	-
235	7	L36	J39	√	VREF
236	7	K37	J38	4	-
237	7	K36	H39	√	VREF
238	7	J37	H38	√	-
239	7	G38	G39	√	VREF
240	7	F39	J36	6	-
241	7	F38	H37	4	-
242	7	E39	H36	√	-
243	7	E38	G37	6	VREF
244	7	D39	G36	4	-
245	7	F36	D38	4	VREF
246	7	E37	D37	6	-

Notes:

1. AO in the XCV1000E, 1600E, 2000E.
2. AO in the XCV600E, 1000E, 1600E.
3. AO in the XCV600E, 1000E.
4. AO in the XCV1000E, 1600E.
5. AO in the XCV1000E, 2000E.
6. AO in the XCV600E, 1000E, 2000E.
7. AO in the XCV1000E.
8. AO in the XCV2000E.

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
1	IO_L57N_Y	D9
1	IO_VREF_L57P_Y	A12 ²
1	IO_L58N_Y	E9
1	IO_L58P_Y	C12
1	IO_L59N_YY	B12
1	IO_VREF_L59P_YY	D8
1	IO_L60N_YY	A11
1	IO_L60P_YY	E8
1	IO_L61N_Y	C7
1	IO_L61P_Y	A10
1	IO_L62N_Y	C6
1	IO_L62P_Y	B10
1	IO_L63N_YY	A9
1	IO_VREF_L63P_YY	B9
1	IO_L64N_YY	A8
1	IO_L64P_YY	E7
1	IO_L65N_Y	B8
1	IO_L65P_Y	C5
1	IO_L66N_Y	A7
1	IO_VREF_L66P_Y	A6
1	IO_L67N_Y	B7
1	IO_L67P_Y	D6
1	IO_L68N_Y	A5
1	IO_L68P_Y	C4
1	IO_WRITE_L69N_YY	B6
1	IO_CS_L69P_YY	E6
2	IO	H2
2	IO	H3
2	IO	J1
2	IO	K5
2	IO	M2
2	IO	N1
2	IO	R5
2	IO	U1
2	IO	U4
2	IO	W3

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
2	IO	Y3
2	IO	AA3
2	IO_DOUT_BUSY_L70P_YY	F5
2	IO_DIN_D0_L70N_YY	D2
2	IO_L71P_Y	E4
2	IO_L71N_Y	E2
2	IO_L72P_Y	D3
2	IO_L72N_Y	F2
2	IO_VREF_L73P_Y	E1
2	IO_L73N_Y	F4
2	IO_L74P	G2
2	IO_L74N	E3
2	IO_L75P_Y	F1
2	IO_L75N_Y	G5
2	IO_VREF_L76P_Y	G1
2	IO_L76N_Y	F3
2	IO_L77P_YY	G4
2	IO_L77N_YY	H1
2	IO_L78P_Y	J2
2	IO_L78N_Y	G3
2	IO_L79P_Y	H5
2	IO_L79N_Y	K2
2	IO_VREF_L80P_YY	H4
2	IO_L80N_YY	K1
2	IO_L81P_YY	L2
2	IO_L81N_YY	L3
2	IO_VREF_L82P_Y	L1 ²
2	IO_L82N_Y	J5
2	IO_L83P_Y	J4
2	IO_L83N_Y	M3
2	IO_VREF_L84P_YY	J3
2	IO_L84N_YY	M1
2	IO_L85P_YY	N2
2	IO_L85N_YY	K4
2	IO_L86P_Y	N3
2	IO_L86N_Y	K3
2	IO_VREF_L87P_YY	L5

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
2	IO_D1_L87N_YY	P2
2	IO_D2_L88P_YY	P3
2	IO_L88N_YY	L4
2	IO_L89P_Y	P1
2	IO_L89N_Y	R2
2	IO_L90P_Y	M5
2	IO_L90N_Y	R3
2	IO_L91P_Y	M4
2	IO_L91N_Y	R1
2	IO_L92P	N4
2	IO_L92N	T2
2	IO_L93P_Y	P5
2	IO_L93N_Y	T3
2	IO_VREF_L94P_Y	P4
2	IO_L94N_Y	T1
2	IO_L95P_YY	U2
2	IO_L95N_YY	R4
2	IO_L96P_Y	U3
2	IO_L96N_Y	T5
2	IO_L97P_Y	T4
2	IO_L97N_Y	V2
2	IO_VREF_L98P_YY	U5
2	IO_D3_L98N_YY	V3
2	IO_L99P_YY	V1
2	IO_L99N_YY	V5
2	IO_L100P_Y	W2
2	IO_L100N_Y	V4
2	IO_L101P_Y	W5
2	IO_L101N_Y	W1
2	IO_VREF_L102P_YY	Y2
2	IO_L102N_YY	W4
2	IO_L103P_YY	Y1
2	IO_L103N_YY	Y5
2	IO_VREF_L104P_Y	AA1 ¹
2	IO_L104N_Y	Y4
2	IO_L105P_YY	AA4
2	IO_L105N_YY	AA2

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
3	IO	AB4
3	IO	AC2
3	IO	AD1
3	IO	AE3
3	IO	AF4
3	IO	AH5
3	IO	AJ2
3	IO	AL1
3	IO	AM3
3	IO	AP3
3	IO	AR5
3	IO	AU4
3	IO	AB2
3	IO_L106P_Y	AB3
3	IO_VREF_L106N_Y	AC4 ¹
3	IO_L107P_YY	AB1
3	IO_L107N_YY	AC5
3	IO_L108P_YY	AD4
3	IO_VREF_L108N_YY	AC3
3	IO_L109P_Y	AC1
3	IO_L109N_Y	AD5
3	IO_L110P_Y	AE4
3	IO_L110N_Y	AD3
3	IO_L111P_YY	AE5
3	IO_L111N_YY	AD2
3	IO_D4_L112P_YY	AE1
3	IO_VREF_L112N_YY	AF5
3	IO_L113P_Y	AE2
3	IO_L113N_Y	AG4
3	IO_L114P_Y	AG5
3	IO_L114N_Y	AF1
3	IO_L115P_YY	AH4
3	IO_L115N_YY	AF2
3	IO_L116P_Y	AF3
3	IO_VREF_L116N_Y	AJ4
3	IO_L117P_Y	AG1

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
6	IO	AJ40
6	IO	AL41
6	IO	AN38
6	IO	AN42
6	IO	AP41
6	IO	AR39
6	IO_L211N_YY	AV41
6	IO_L211P_YY	AV42
6	IO_L212N_Y	AW40
6	IO_L212P_Y	AU41
6	IO_L213N_Y	AV39
6	IO_L213P_Y	AU42
6	IO_VREF_L214N_Y	AT41
6	IO_L214P_Y	AU38
6	IO_L215N	AT42
6	IO_L215P	AV40
6	IO_L216N_Y	AR41
6	IO_L216P_Y	AU39
6	IO_VREF_L217N_Y	AR42
6	IO_L217P_Y	AU40
6	IO_L218N_YY	AT38
6	IO_L218P_YY	AP42
6	IO_L219N_Y	AN41
6	IO_L219P_Y	AT39
6	IO_L220N_Y	AT40
6	IO_L220P_Y	AM40
6	IO_VREF_L221N_YY	AR38
6	IO_L221P_YY	AM41
6	IO_L222N_YY	AM42
6	IO_L222P_YY	AR40
6	IO_VREF_L223N_Y	AL40 ²
6	IO_L223P_Y	AP38
6	IO_L224N_Y	AP39
6	IO_L224P_Y	AL42
6	IO_VREF_L225N_YY	AP40
6	IO_L225P_YY	AK40
6	IO_L226N_YY	AK41

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
6	IO_L226P_YY	AN39
6	IO_L227N_Y	AK42
6	IO_L227P_Y	AN40
6	IO_VREF_L228N_YY	AM38
6	IO_L228P_YY	AJ41
6	IO_L229N_YY	AJ42
6	IO_L229P_YY	AM39
6	IO_L230N_Y	AH40
6	IO_L230P_Y	AH41
6	IO_L231N_Y	AL38
6	IO_L231P_Y	AH42
6	IO_L232N_Y	AL39
6	IO_L232P_Y	AG41
6	IO_L233N	AK39
6	IO_L233P	AG40
6	IO_L234N_Y	AJ38
6	IO_L234P_Y	AG42
6	IO_VREF_L235N_Y	AF42
6	IO_L235P_Y	AJ39
6	IO_L236N_YY	AF41
6	IO_L236P_YY	AH38
6	IO_L237N_Y	AE42
6	IO_L237P_Y	AH39
6	IO_L238N_Y	AG38
6	IO_L238P_Y	AE41
6	IO_VREF_L239N_YY	AG39
6	IO_L239P_YY	AD42
6	IO_L240N_YY	AD40
6	IO_L240P_YY	AF39
6	IO_L241N_Y	AD41
6	IO_L241P_Y	AE38
6	IO_L242N_Y	AE39
6	IO_L242P_Y	AC40
6	IO_VREF_L243N_YY	AD38
6	IO_L243P_YY	AC41
6	IO_L244N_YY	AB42
6	IO_L244P_YY	AC38

Table 26: FG900 — XCV600E, XCV1000E, XCV1600E

Bank	Pin Description	Pin #
0	IO_L6N_Y	A5
0	IO_L6P_Y	F8
0	IO_L7N_Y	D7
0	IO_L7P_Y	N11
0	IO_L8N_YY	G9
0	IO_L8P_YY	E8
0	IO_VREF_L9N_YY	A6
0	IO_L9P_YY	J11
0	IO_L10N_Y	C7
0	IO_L10P_Y	B7
0	IO_L11N_Y	C8
0	IO_L11P_Y	H10
0	IO_L12N_YY	G10
0	IO_L12P_YY	F10
0	IO_VREF_L13N_YY	A8
0	IO_L13P_YY	H11
0	IO_L14N	D9 ⁴
0	IO_L14P	C9 ³
0	IO_L15N_YY	B9
0	IO_L15P_YY	J12
0	IO_L16N	E10 ⁴
0	IO_VREF_L16P	A9
0	IO_L17N	G11
0	IO_L17P	B10
0	IO_L18N_YY	H12 ⁴
0	IO_L18P_YY	C10 ⁴
0	IO_L19N_Y	H13
0	IO_L19P_Y	F11
0	IO_L20N_Y	E11
0	IO_L20P_Y	D11
0	IO_L21N_Y	B11 ⁴
0	IO_L21P_Y	G12 ⁴
0	IO_L22N_YY	F12
0	IO_L22P_YY	C11
0	IO_VREF_L23N_YY	A10 ¹
0	IO_L23P_YY	D12
0	IO_L24N_Y	E12

Table 26: FG900 — XCV600E, XCV1000E, XCV1600E

Bank	Pin Description	Pin #
0	IO_L24P_Y	A11
0	IO_L25N_Y	G13
0	IO_L25P_Y	B12
0	IO_L26N_YY	A12
0	IO_L26P_YY	K13
0	IO_VREF_L27N_YY	F13
0	IO_L27P_YY	B13
0	IO_L28N_Y	G14
0	IO_L28P_Y	E13
0	IO_L29N_Y	D14
0	IO_L29P_Y	B14
0	IO_L30N_YY	A14
0	IO_L30P_YY	J14
0	IO_VREF_L31N_YY	K14
0	IO_L31P_YY	J15
0	IO_L32N	B15 ⁴
0	IO_L32P	H15 ³
0	IO_VREF_L33N_YY	F15 ^{2,3}
0	IO_L33P_YY	D15 ⁴
0	IO_LVDS_DLL_L34N	A15
1	GCK2	E15
1	IO	A25 ⁴
1	IO	B17 ⁴
1	IO	B18 ⁴
1	IO	C23 ⁴
1	IO	D16 ⁴
1	IO	D17 ⁵
1	IO	D23 ⁴
1	IO	E19 ⁴
1	IO	E24 ⁵
1	IO	F22 ⁴
1	IO	G17 ⁵
1	IO	G20 ⁴
1	IO	J16 ⁴
1	IO	J17 ⁴
1	IO	J19 ⁵

Table 27: FG900 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
188	5	AA12	AJ12	√	VREF
189	5	AB12	AE11	√	-
190	5	AK12	Y13	2	-
191	5	AG11	AF11	2	-
192	5	AH11	AJ11	2	-
193	5	AE12	AG10	4	-
194	5	AD12	AK11	√	-
195	5	AJ10	AC12	√	VREF
196	5	AK10	AD11	4	-
197	5	AJ9	AE9	4	-
198	5	AH10	AF9	√	VREF
199	5	AH9	AK9	√	-
200	5	AF8	AB11	2	-
201	5	AC11	AG8	2	-
202	5	AK8	AF7	√	VREF
203	5	AG7	AK7	√	-
204	5	AJ7	AD10	1	-
205	5	AH6	AC10	1	-
206	5	AD9	AG6	√	VREF
207	5	AB10	AJ5	√	-
208	5	AD8	AK5	2	-
209	5	AC9	AJ4	2	VREF
210	5	AG5	AK4	2	-
211	5	AH5	AG3	4	-
212	6	AC6	AF3	√	-
213	6	AG2	AH2	NA	-
214	6	AE4	AB9	1	-
215	6	AH1	AE3	4	VREF
216	6	AD6	AB8	3	-
217	6	AA10	AG1	4	-
218	6	AD4	AA9	1	VREF
219	6	AD2	AD5	√	-
220	6	AF2	AD3	4	-
221	6	AA7	AA8	1	-

Table 27: FG900 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
222	6	Y9	AF1	√	VREF
223	6	AC4	AB6	√	-
224	6	W8	AE1	2	-
225	6	AB4	Y8	4	-
226	6	W9	AB3	4	VREF
227	6	W10	AA5	4	-
228	6	V10	AB1	4	-
229	6	AC1	Y7	4	VREF
230	6	AA3	V11	NA	-
231	6	U10	AA2	4	-
232	6	AA6	W7	1	-
233	6	Y4	Y6	4	-
234	6	V7	AA1	3	-
235	6	Y2	Y3	4	-
236	6	W5	Y5	1	VREF
237	6	W6	W4	√	-
238	6	W2	V6	4	-
239	6	V4	U9	1	-
240	6	T8	AB2	√	VREF
241	6	W1	U5	√	-
242	6	T9	Y1	2	-
243	6	U3	T7	4	-
244	6	V2	T5	4	VREF
245	6	T6	R9	4	-
246	6	U2	T4	4	VREF
247	7	R10	T1	NA	-
248	7	R6	R5	4	-
249	7	R4	R8	4	VREF
250	7	R3	R7	4	-
251	7	P6	P10	4	VREF
252	7	P2	P5	4	-
253	7	P4	P7	2	-
254	7	R2	N4	√	-
255	7	P1	N7	√	VREF

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
0	IO_L6P_YY	H10 ⁵
0	IO_L7N_Y	D7
0	IO_L7P_Y	B5
0	IO_L8N_Y	K12
0	IO_L8P_Y	E8
0	IO_L9N	B6 ⁴
0	IO_L9P	F9 ⁵
0	IO_L10N_YY	G10
0	IO_L10P_YY	C7
0	IO_VREF_L11N_YY	D8
0	IO_L11P_YY	B7
0	IO_L12N	H11 ⁴
0	IO_L12P	C8 ⁵
0	IO_L13N_Y	E9
0	IO_L13P_Y	B8
0	IO_VREF_L14N_Y	K13 ²
0	IO_L14P_Y	G11
0	IO_L15N	A8 ⁴
0	IO_L15P	F10 ⁵
0	IO_L16N_YY	C9
0	IO_L16P_YY	H12
0	IO_VREF_L17N_YY	D10
0	IO_L17P_YY	A9
0	IO_L18N_Y	F11
0	IO_L18P_Y	A10
0	IO_L19N_Y	K14
0	IO_L19P_Y	C10
0	IO_VREF_L20N_YY	H13
0	IO_L20P_YY	G12
0	IO_L21N_YY	A11
0	IO_L21P_YY	B11
0	IO_L22N_Y	E12
0	IO_L22P_Y	D11
0	IO_L23N_Y	G13

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
0	IO_L23P_Y	C12
0	IO_L24N_Y	K15
0	IO_L24P_Y	A12
0	IO_L25N_Y	B12
0	IO_L25P_Y	H14
0	IO_L26N_YY	D12
0	IO_L26P_YY	F13
0	IO_VREF_L27N_YY	A13
0	IO_L27P_YY	B13
0	IO_L28N_YY	J15 ⁴
0	IO_L28P_YY	G14 ⁵
0	IO_L29N_Y	C13
0	IO_L29P_Y	F14
0	IO_L30N_Y	H15
0	IO_L30P_Y	D13
0	IO_L31N	A14 ⁴
0	IO_L31P	K16 ⁵
0	IO_L32N_YY	E14
0	IO_L32P_YY	B14
0	IO_VREF_L33N_YY	G15
0	IO_L33P_YY	D14
0	IO_L34N	J16 ⁴
0	IO_L34P	D15 ⁵
0	IO_L35N_Y	F15
0	IO_L35P_Y	B15
0	IO_L36N_Y	A15
0	IO_L36P_Y	E15
0	IO_L37N	G16 ⁴
0	IO_L37P	A16 ⁵
0	IO_L38N_YY	F16
0	IO_L38P_YY	J17
0	IO_VREF_L39N_YY	C16
0	IO_L39P_YY	B16
0	IO_L40N_Y	H17