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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	1176
Number of Logic Elements/Cells	5292
Total RAM Bits	114688
Number of I/O	284
Number of Gates	306393
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv200e-7fg456i

Eight I/O banks result from separating each edge of the FPGA into two banks, as shown in Figure 3. Each bank has multiple V_{CCO} pins, all of which must be connected to the same voltage. This voltage is determined by the output standards in use.

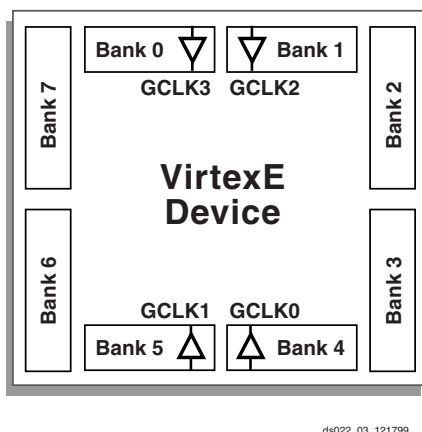


Figure 3: Virtex-E I/O Banks

Within a bank, output standards can be mixed only if they use the same V_{CCO} . Compatible standards are shown in Table 2. GTL and GTL+ appear under all voltages because their open-drain outputs do not depend on V_{CCO} .

Table 2: Compatible Output Standards

V_{CCO}	Compatible Standards
3.3 V	PCI, LVTTTL, SSTL3 I, SSTL3 II, CTT, AGP, GTL, GTL+, LVPECL
2.5 V	SSTL2 I, SSTL2 II, LVCMOS2, GTL, GTL+, BLVDS, LVDS
1.8 V	LVCMOS18, GTL, GTL+
1.5 V	HSTL I, HSTL III, HSTL IV, GTL, GTL+

Some input standards require a user-supplied threshold voltage, V_{REF} . In this case, certain user-I/O pins are automatically configured as inputs for the V_{REF} voltage. Approximately one in six of the I/O pins in the bank assume this role.

The V_{REF} pins within a bank are interconnected internally and consequently only one V_{REF} voltage can be used within each bank. All V_{REF} pins in the bank, however, must be connected to the external voltage source for correct operation.

Within a bank, inputs that require V_{REF} can be mixed with those that do not. However, only one V_{REF} voltage can be used within a bank.

In Virtex-E, input buffers with LVTTTL, LVCMOS2, LVCMOS18, PCI33_3, PCI66_3 standards are supplied by V_{CCO} rather than V_{CCINT} . For these standards, only input and output buffers that have the same V_{CCO} can be mixed together.

The V_{CCO} and V_{REF} pins for each bank appear in the device pin-out tables and diagrams. The diagrams also show the bank affiliation of each I/O.

Within a given package, the number of V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices, more I/O pins convert to V_{REF} pins. Since these are always a super set of the V_{REF} pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device if necessary. All the V_{REF} pins for the largest device anticipated must be connected to the V_{REF} voltage, and not used for I/O.

In smaller devices, some V_{CCO} pins used in larger devices do not connect within the package. These unconnected pins can be left unconnected externally, or can be connected to the V_{CCO} voltage to permit migration to a larger device if necessary.

Configurable Logic Blocks

The basic building block of the Virtex-E CLB is the logic cell (LC). An LC includes a 4-input function generator, carry logic, and a storage element. The output from the function generator in each LC drives both the CLB output and the D input of the flip-flop. Each Virtex-E CLB contains four LCs, organized in two similar slices, as shown in Figure 4. Figure 5 shows a more detailed view of a single slice.

In addition to the four basic LCs, the Virtex-E CLB contains logic that combines function generators to provide functions of five or six inputs. Consequently, when estimating the number of system gates provided by a given device, each CLB counts as 4.5 LCs.

Look-Up Tables

Virtex-E function generators are implemented as 4-input look-up tables (LUTs). In addition to operating as a function generator, each LUT can provide a 16 x 1-bit synchronous RAM. Furthermore, the two LUTs within a slice can be combined to create a 16 x 2-bit or 32 x 1-bit synchronous RAM, or a 16 x 1-bit dual-port synchronous RAM.

The Virtex-E LUT can also provide a 16-bit shift register that is ideal for capturing high-speed or burst-mode data. This mode can also be used to store data in applications such as Digital Signal Processing.

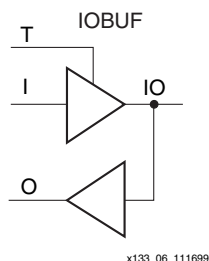


Figure 42: Input/Output Buffer Symbol (IOBUF)

The following list details variations of the IOBUF symbol.

- IOBUF
- IOBUF_S_2
- IOBUF_S_4
- IOBUF_S_6
- IOBUF_S_8
- IOBUF_S_12
- IOBUF_S_16
- IOBUF_S_24
- IOBUF_F_2
- IOBUF_F_4
- IOBUF_F_6
- IOBUF_F_8
- IOBUF_F_12
- IOBUF_F_16
- IOBUF_F_24
- IOBUF_LVCMOS2
- IOBUF_PCI33_3
- IOBUF_PCI66_3
- IOBUF_GTL
- IOBUF_GTLP
- IOBUF_HSTL_I
- IOBUF_HSTL_III
- IOBUF_HSTL_IV
- IOBUF_SSTL3_I
- IOBUF_SSTL3_II
- IOBUF_SSTL2_I
- IOBUF_SSTL2_II
- IOBUF_CTT
- IOBUF_AGP
- IOBUF_LVCMOS18
- IOBUF_LVDS
- IOBUF_LVPECL

When the IOBUF symbol used supports an I/O standard that requires a differential amplifier input, the IOBUF automatically configures with a differential amplifier input buffer.

The low-voltage I/O standards with a differential amplifier input require an external reference voltage input V_{REF} .

The voltage reference signal is “banked” within the Virtex-E device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 38, page 34 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

IOBUF placement restrictions require any differential amplifier input signals within a bank be of the same standard.

The Virtex-E series supports eight banks for the HQ and PQ packages. The CS package supports four V_{CCO} banks.

Additional restrictions on the Virtex-E SelectI/O IOBUF placement require that within a given V_{CCO} bank each IOBUF must share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within the same V_{CCO} bank. The LOC property can specify a location for the IOBUF.

An optional delay element is associated with the input path in each IOBUF. When the IOBUF drives an input flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Override this default with the NODELAY=TRUE property.

In the case when the IOBUF does not drive an input flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak “keeper” circuit. Control this feature by adding the appropriate symbol to the output net of the IOBUF (PULLUP, PULLDOWN, or KEEPER).

SelectI/O Properties

Access to some of the SelectI/O features (for example, location constraints, input delay, output drive strength, and slew rate) is available through properties associated with these features.

Input Delay Properties

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Use the NODELAY=TRUE property to override this default.

In the case when the IBUF does not drive a flip-flop within the IOB, the delay element by default de-activates to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

Virtex-E Data Sheet

The Virtex-E Data Sheet contains the following modules:

- DS022-1, Virtex-E 1.8V FPGAs:
[Introduction and Ordering Information \(Module 1\)](#)
- DS022-2, Virtex-E 1.8V FPGAs:
Functional Description (Module 2)
- DS022-3, Virtex-E 1.8V FPGAs:
[DC and Switching Characteristics \(Module 3\)](#)
- DS022-4, Virtex-E 1.8V FPGAs:
[Pinout Tables \(Module 4\)](#)

Virtex-E Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation net list. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Virtex-E devices unless otherwise noted.

IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVTTTL levels in [Table 2](#). For other standards, adjust the delays with the values shown in [IOB Input Switching Characteristics Standard Adjustments](#), page 8.

Table 2: IOB Input Switching Characteristics

			Speed Grade ⁽¹⁾				Units
Description ⁽²⁾	Symbol	Device	Min	-8	-7	-6	
Propagation Delays							
Pad to I output, no delay	T _{IOPI}	All	0.43	0.8	0.8	0.8	ns, max
Pad to I output, with delay	T _{IOPID}	XCV50E	0.51	1.0	1.0	1.0	ns, max
		XCV100E	0.51	1.0	1.0	1.0	ns, max
		XCV200E	0.51	1.0	1.0	1.0	ns, max
		XCV300E	0.51	1.0	1.0	1.0	ns, max
		XCV400E	0.51	1.0	1.0	1.0	ns, max
		XCV600E	0.51	1.0	1.0	1.0	ns, max
		XCV1000E	0.55	1.1	1.1	1.1	ns, max
		XCV1600E	0.55	1.1	1.1	1.1	ns, max
		XCV2000E	0.55	1.1	1.1	1.1	ns, max
		XCV2600E	0.55	1.1	1.1	1.1	ns, max
XCV3200E	0.55	1.1	1.1	1.1	ns, max		
Pad to output IQ via transparent latch, no delay	T _{IOPLI}	All	0.8	1.4	1.5	1.6	ns, max
Pad to output IQ via transparent latch, with delay	T _{IOPLID}	XCV50E	1.31	2.9	3.0	3.1	ns, max
		XCV100E	1.31	2.9	3.0	3.1	ns, max
		XCV200E	1.39	3.1	3.2	3.3	ns, max
		XCV300E	1.39	3.1	3.2	3.3	ns, max
		XCV400E	1.43	3.2	3.3	3.4	ns, max
		XCV600E	1.55	3.5	3.6	3.7	ns, max
		XCV1000E	1.55	3.5	3.6	3.7	ns, max
		XCV1600E	1.59	3.6	3.7	3.8	ns, max
		XCV2000E	1.59	3.6	3.7	3.8	ns, max
		XCV2600E	1.59	3.6	3.7	3.8	ns, max
XCV3200E	1.59	3.6	3.7	3.8	ns, max		

Low Voltage Differential Signals

The Virtex-E family incorporates low-voltage signalling (LVDS and LVPECL). Two pins are utilized for these signals to be connected to a Virtex-E device. These are known as differential pin pairs. Each differential pin pair has a Positive (P) and a Negative (N) pin. These pairs are labeled in the following manner.

IO_L#[P/N]

where

L = LVDS or LVPECL pin

= Pin Pair Number

P = Positive

N = Negative

I/O pins for differential signals can either be synchronous or asynchronous, input or output. The pin pairs can be used for synchronous input and output signals as well as asynchronous input signals. However, only some of the low-voltage pairs can be used for asynchronous output signals.

Differential signals require the pins of a pair to switch almost simultaneously. If the signals driving the pins are from IOB flip-flops, they are synchronous. If the signals driving the pins are from internal logic, they are asynchronous. [Table 2](#) defines the names and function of the different types of low-voltage pin pairs in the Virtex-E family.

Table 2: LVDS Pin Pairs

Pin Name	Description
IO_L#[P/N] Example: IO_L22N	Represents a general IO or a synchronous input/output differential signal. When used as a differential signal, N means Negative I/O and P means Positive I/O.
IO_L#[P/N]_Y Example: IO_L22N_Y	Represents a general IO or a synchronous input/output differential signal, or a part-dependent asynchronous output differential signal.
IO_L#[P/N]_YY Example: O_L22N_YY	Represents a general IO or a synchronous input/output differential signal, or an asynchronous output differential signal.
IO_LVDS_DLL_L#[P/N] Example: IO_LVDS_DLL_L16N	Represents a general IO or a synchronous input/output differential signal, a differential clock input signal, or a DLL input. When used as a differential clock input, this pin is paired with the adjacent GCK pin. The GCK pin is always the positive input in the differential clock input configuration.

Virtex-E Package Pinouts

The Virtex-E family of FPGAs is available in 12 popular packages, including chip-scale, plastic and high heat-dissipation quad flat packs, and ball grid and fine-pitch ball grid arrays. Family members have footprint compatibility across devices provided in the same package. The pinout tables in

this section indicate function, pin, and bank information for each package/device combination. Following each pinout table is an additional table summarizing information specific to differential pin pairs for all devices provided in that package.

Table 7: PQ240 Differential Pin Pair Summary
XCV50E, XCV100E, XCV200E, XCV300E, XCV400E

Pair	Bank	P Pin	N Pin	AO	Other Functions
48	6	P56	P57	√	-
49	6	P52	P53	2	-
50	6	P49	P50	3	VREF
51	6	P46	P47	4	VREF
52	6	P41	P42	√	-
53	6	P38	P39	2	-
54	6	P35	P36	4	VREF
55	6	P33	P34	5	VREF
56	7	P27	P28	√	-
57	7	P23	P24	4	VREF
58	7	P20	P21	2	-
59	7	P17	P18	√	-
60	7	P12	P13	4	VREF
61	7	P9	P10	3	VREF
62	7	P6	P7	2	-
63	7	P4	P5	6	VREF

Notes:

1. AO in the XCV50E.
2. AO in the XCV50E, 100E, 200E, 300E.
3. AO in the XCV50E, 200E, 300E, 400E.
4. AO in the XCV50E, 300E, 400E.
5. AO in the XCV100E, 200E, 400E.
6. AO in the XCV100E, 400E.
7. AO in the XCV50E, 200E, 400E.
8. AO in the XCV100E.

HQ240 High-Heat Quad Flat-Pack Packages

XCV600E and XCV1000E devices in High-heat dissipation Quad Flat-pack packages have footprint compatibility. Pins labeled IO_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF} it can be used as general I/O. Immediately following Table 8, see Table 9 for Differential Pair information.

Table 8: HQ240 — XCV600E, XCV1000E

Pin #	Pin Description	Bank
P240	VCCO	7
P239	TCK	NA
P238	IO	0
P237	IO_L0N	0
P236	IO_VREF_L0P	0
P235	IO_L1N_YY	0
P234	IO_L1P_YY	0
P233	GND	NA
P232	VCCO	0
P231	IO_VREF	0
P230	IO_VREF	0
P229	IO_VREF_L2N_YY	0
P228	IO_L2P_YY	0
P227	GND	NA
P226	VCCO	0
P225	VCCINT	NA
P224	IO_L3N_YY	0
P223	IO_L3P_YY	0
P222	IO_VREF	0 ¹
P221	IO_L4N_Y	0
P220	IO_L4P_Y	0
P219	GND	NA
P218	IO_VREF_L5N_Y	0
P217	IO_L5P_Y	0
P216	IO_VREF	0
P215	IO_LVDS_DLL_L6N	0
P214	VCCINT	NA
P213	GCK3	0
P212	VCCO	0
P211	GND	NA

Table 8: HQ240 — XCV600E, XCV1000E

Pin #	Pin Description	Bank
P138	IO_D5_L26N_YY	3
P137	VCCINT	NA
P136	VCCO	3
P135	GND	NA
P134	IO_D6_L27P_Y	3
P133	IO_VREF_L27N_Y	3
P132	IO_VREF	3
P131	IO_L28P_Y	3
P130	IO_VREF_L28N_Y	3
P129	GND	NA
P128	IO_L29P_Y	3
P127	IO_L29N_Y	3
P126	IO_VREF_L30P_Y	3
P125	IO_L30N_Y	3
P124	IO_D7_L31P_YY	3
P123	IO_INIT_L31N_YY	3
P122	PROGRAM	NA
P121	VCCO	3
P120	DONE	3
P119	GND	NA
P118	IO_L32P_YY	4
P117	IO_L32N_YY	4
P116	VCCO	4
P115	IO_VREF	4
P114	IO_L33P_YY	4
P113	IO_L33N_YY	4
P112	GND	NA
P111	IO_VREF_L34P_YY	4
P110	IO_L34N_YY	4
P109	IO_VREF	4
P108	IO_VREF_L35P_YY	4
P107	IO_L35N_YY	4
P106	GND	NA
P105	VCCO	4
P104	VCCINT	NA
P103	IO_L36P_YY	4

Table 8: HQ240 — XCV600E, XCV1000E

Pin #	Pin Description	Bank
P102	IO_L36N_YY	4
P101 ¹	IO_VREF	4
P100	IO_L37P_Y	4
P99	IO_L37N_Y	4
P98	GND	NA
P97	IO_VREF_L38P_Y	4
P96	IO_L38N_Y	4
P95	IO_L39P	4
P94	IO_VREF_L39N	4
P93	IO_LVDS_DLL_L40P	4
P92	GCK0	4
P91	GND	NA
P90	VCCO	4
P89	GCK1	5
P88	VCCINT	NA
P87	IO_LVDS_DLL_L40N	5
P86	IO_VREF	5
P85	VCCO	5
P84	IO_VREF_L41P	5
P83	GND	NA
P82	IO_L41N	5
P81	IO	5
P80 ¹	IO_VREF	5
P79	IO_L42P_YY	5
P78	IO_L42N_YY	5
P77	VCCINT	NA
P76	VCCO	5
P75	GND	NA
P74	IO_L43P_YY	5
P73	IO_VREF_L43N_YY	5
P72	IO_VREF	5
P71	IO_L44P_YY	5
P70	IO_VREF_L44N_YY	5
P69	GND	NA
P68	IO_L45P_YY	5
P67	IO_L45N_YY	5

Table 12: BG432 — XCV300E, XCV400E, XCV600E

Bank	Pin Description	Pin #
2	IO_L41N_Y	H2
2	IO_VREF_L42P_Y	H1 ¹
2	IO_L42N_Y	J4
2	IO_VREF_L43P_YY	J2
2	IO_D1_L43N_YY	K4
2	IO_D2_L44P_YY	K2
2	IO_L44N_YY	K1
2	IO_L45P_Y	L2
2	IO_L45N_Y	M4
2	IO_L46P_Y	M3
2	IO_L46N_Y	M2
2	IO_L47P_Y	N4
2	IO_L47N_Y	N3
2	IO_VREF_L48P_YY	N1
2	IO_D3_L48N_YY	P4
2	IO_L49P_Y	P3
2	IO_L49N_Y	P2
2	IO_VREF_L50P_Y	R3 ²
2	IO_L50N_Y	R4
2	IO_L51P_YY	R1
2	IO_L51N_YY	T3
3	IO	AA2
3	IO	AC2
3	IO	AE2
3	IO	U3
3	IO	W1
3	IO_L52P_Y	U4
3	IO_VREF_L52N_Y	U2 ²
3	IO_L53P_Y	U1
3	IO_L53N_Y	V3
3	IO_D4_L54P_YY	V4
3	IO_VREF_L54N_YY	V2
3	IO_L55P_Y	W3
3	IO_L55N_Y	W4
3	IO_L56P_Y	Y1

Table 12: BG432 — XCV300E, XCV400E, XCV600E

Bank	Pin Description	Pin #
3	IO_L56N_Y	Y3
3	IO_L57P_Y	Y4
3	IO_L57N_Y	Y2
3	IO_L58P_YY	AA3
3	IO_D5_L58N_YY	AB1
3	IO_D6_L59P_YY	AB3
3	IO_VREF_L59N_YY	AB4
3	IO_L60P_Y	AD1
3	IO_VREF_L60N_Y	AC3 ¹
3	IO_L61P_Y	AC4
3	IO_L61N_Y	AD2
3	IO_L62P_YY	AD3
3	IO_VREF_L62N_YY	AD4
3	IO_L63P_Y	AF2
3	IO_L63N_Y	AE3
3	IO_L64P	AE4
3	IO_L64N	AG1
3	IO_L65P_Y	AG2
3	IO_VREF_L65N_Y	AF3
3	IO_L66P_Y	AF4
3	IO_L66N_Y	AH1
3	IO_L67P	AH2
3	IO_L67N	AG3
3	IO_D7_L68P_YY	AG4
3	IO_INIT_L68N_YY	AJ2
3	IO	T2
4	GCK0	AL16
4	IO	AH10
4	IO	AJ11
4	IO	AK7
4	IO	AL12
4	IO	AL15
4	IO_L69P_YY	AJ4
4	IO_L69N_YY	AK3
4	IO_L70P_Y	AH5

Table 14: BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin#	See Note
0	IO_L11P_YY	B24	
0	IO_L12N_Y	E22	
0	IO_L12P_Y	C23	
0	IO_L13N_YY	A23	
0	IO_L13P_YY	D22	
0	IO_VREF_L14N_YY	E21	3
0	IO_L14P_YY	B22	
0	IO_L15N_Y	D21	
0	IO_L15P_Y	C21	
0	IO_L16N_YY	B21	
0	IO_L16P_YY	E20	
0	IO_VREF_L17N_YY	D20	
0	IO_L17P_YY	C20	
0	IO_L18N_Y	B20	
0	IO_L18P_Y	E19	
0	IO_L19N_Y	D19	
0	IO_L19P_Y	C19	
0	IO_VREF_L20N_Y	A19	
0	IO_L20P_Y	D18	
0	IO_LVDS_DLL_L21N	C18	
0	IO_VREF	E18	2
1	GCK2	D17	
1	IO	A3	
1	IO	D9	
1	IO	E8	
1	IO	E11	
1	IO_LVDS_DLL_L21P	E17	
1	IO_VREF_L22N_Y	C17	2
1	IO_L22P_Y	B17	
1	IO_L23N_Y	B16	
1	IO_VREF_L23P_Y	D16	
1	IO_L24N_Y	E16	
1	IO_L24P_Y	C16	
1	IO_L25N_Y	A15	

Table 14: BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin#	See Note
1	IO_L25P_Y	C15	
1	IO_L26N_YY	D15	
1	IO_VREF_L26P_YY	E15	
1	IO_L27N_YY	C14	
1	IO_L27P_YY	D14	
1	IO_L28N_Y	A13	
1	IO_L28P_Y	E14	
1	IO_L29N_YY	C13	
1	IO_VREF_L29P_YY	D13	3
1	IO_L30N_YY	C12	
1	IO_L30P_YY	E13	
1	IO_L31N_Y	A11	
1	IO_L31P_Y	D12	
1	IO_L32N_YY	B11	
1	IO_L32P_YY	C11	
1	IO_L33N_YY	B10	
1	IO_VREF_L33P_YY	D11	
1	IO_L34N_Y	C10	
1	IO_L34P_Y	A9	
1	IO_L35N_Y	C9	
1	IO_VREF_L35P_Y	D10	4
1	IO_L36N_Y	A8	
1	IO_L36P_Y	B8	
1	IO_L37N_Y	E10	
1	IO_VREF_L37P_Y	C8	1
1	IO_L38N_YY	B7	
1	IO_VREF_L38P_YY	A6	
1	IO_L39N_YY	C7	
1	IO_L39P_YY	D8	
1	IO_L40N_Y	A5	
1	IO_L40P_Y	B5	
1	IO_L41N_YY	C6	
1	IO_VREF_L41P_YY	D7	
1	IO_L42N_YY	A4	
1	IO_L42P_YY	B4	

Table 19: FG456 Differential Pin Pair Summary
XCV200E, XCV300E

Pair	Bank	P Pin	N Pin	AO	Other Functions
18	1	C14	B14	2	-
19	1	A15	F12	2	-
20	1	C15	B15	√	-
21	1	E14	A16	√	VREF
22	1	C16	D14	2	-
23	1	A17	D15	2	-
24	1	A18	B17	√	VREF
25	1	C17	D16	√	-
26	1	A19	B18	√	VREF
27	1	C18	D17	√	-
28	1	C19	A20	√	CS
29	2	C21	D20	√	DIN, D0
30	2	C22	D21	√	-
31	2	D22	E21	√	VREF
32	2	E22	F18	√	-
33	2	F21	F19	√	VREF
34	2	F22	G19	2	-
35	2	G20	G18	1	-
36	2	H18	H22	2	D1, VREF
37	2	H20	H19	√	D2
38	2	H21	J19	√	-
39	2	J18	J20	√	-
40	2	K18	J21	2	-
41	2	K22	K21	1	VREF
42	2	K19	L22	2	-
43	2	L21	L18	√	-
44	2	L17	L20	√	-
45	3	M18	M20	√	-
46	3	M19	M17	2	-
47	3	N22	N21	2	VREF
48	3	N20	N18	√	-
49	3	N19	P21	√	-
50	3	P20	P19	√	-
51	3	P18	R21	√	D5
52	3	T22	R19	2	VREF

Table 19: FG456 Differential Pin Pair Summary
XCV200E, XCV300E

Pair	Bank	P Pin	N Pin	AO	Other Functions
53	3	U22	R18	2	-
54	3	T21	V22	√	-
55	3	T20	U21	√	VREF
56	3	W22	T18	√	-
57	3	U19	U20	√	VREF
58	3	W21	AA22	√	-
59	3	Y21	V19	√	INIT
60	4	W18	AA20	√	-
61	4	Y18	V17	NA	-
62	4	AB20	W17	√	VREF
63	4	AA18	V16	NA	-
64	4	AB19	AB18	√	VREF
65	4	W16	AA17	1	-
66	4	Y16	V15	1	-
67	4	AB16	Y15	√	VREF
68	4	AA15	AB15	√	-
69	4	W15	Y14	1	-
70	4	V14	AA14	1	-
71	4	AB14	V13	NA	-
72	4	AA13	AB13	√	VREF
73	4	W13	AA12	2	-
74	4	Y12	V12	2	-
75	5	U12	AA11	NA	IO_LVDS_DLL
76	5	AB11	W11	1	-
77	5	V11	Y10	√	VREF
78	5	AB10	W10	√	-
79	5	V10	Y9	2	-
80	5	AB9	W9	2	-
81	5	V9	AA8	√	-
82	5	Y8	W8	√	VREF
83	5	W7	AA7	2	-
84	5	AB6	AA6	2	-
85	5	AB5	AA5	√	VREF
86	5	Y7	W6	√	-
87	5	AA4	Y6	√	VREF

Table 19: FG456 Differential Pin Pair Summary
XCV200E, XCV300E

Pair	Bank	P Pin	N Pin	AO	Other Functions
88	5	V7	AB3	√	-
89	6	Y2	W3	√	-
90	6	V3	V4	√	-
91	6	U4	Y1	√	VREF
92	6	W1	V2	√	-
93	6	U2	T3	√	VREF
94	6	V1	T5	2	-
95	6	U1	R5	1	-
96	6	T1	R4	2	VREF
97	6	P3	R2	√	-
98	6	R1	P5	√	-
99	6	N5	P2	√	-
100	6	N4	P1	2	-
101	6	N2	N3	1	VREF
102	6	M4	N1	2	-
103	6	M6	M3	√	-
104	7	L4	L3	√	-
105	7	L1	L5	√	-
106	7	K2	L6	2	-
107	7	K3	K4	2	VREF
108	7	K5	K1	√	-
109	7	J2	J3	√	-
110	7	H1	J5	√	-
111	7	H3	H2	√	-
112	7	H4	G1	2	VREF
113	7	F2	F1	2	-
114	7	G3	H5	√	-
115	7	E2	E1	√	VREF
116	7	G5	F3	√	-
117	7	D2	E3	√	VREF
118	7	C1	F5	√	-

Notes:

1. AO in the XCV200E.
2. AO in the XCV300E.

FG676 Fine-Pitch Ball Grid Array Package

XCV400E and XCV600E devices in the FG676 fine-pitch Ball Grid Array package have footprint compatibility. Pins labeled IO_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF} it can be used as general I/O. Immediately following Table 20, see Table 21 for Differential Pair information.

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
0	GCK3	E13
0	IO	A6
0	IO	A9 ¹
0	IO	A10 ¹
0	IO	B3
0	IO	B4 ¹
0	IO	B12 ¹
0	IO	C6
0	IO	C8
0	IO	D5
0	IO	D13 ¹
0	IO	G13
0	IO_L0N_Y	C4
0	IO_L0P_Y	F7
0	IO_L1N_YY	G8
0	IO_L1P_YY	C5
0	IO_VREF_L2N_YY	D6
0	IO_L2P_YY	E7
0	IO_L3N	A4
0	IO_L3P	F8
0	IO_L4N	B5
0	IO_L4P	D7
0	IO_VREF_L5N_YY	E8
0	IO_L5P_YY	G9
0	IO_L6N_YY	A5
0	IO_L6P_YY	F9
0	IO_L7N_Y	D8
0	IO_L7P_Y	C7
0	IO_VREF_L8N_Y	B7 ²
0	IO_L8P_Y	E9

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
NA	GND	P14
NA	GND	P13
NA	GND	P12
NA	GND	P11
NA	GND	P10
NA	GND	N2
NA	GND	N17
NA	GND	N16
NA	GND	N15
NA	GND	N14
NA	GND	N13
NA	GND	N12
NA	GND	N11
NA	GND	N10
NA	GND	M17
NA	GND	M16
NA	GND	M15
NA	GND	M14
NA	GND	M13
NA	GND	M12
NA	GND	M11
NA	GND	M10
NA	GND	L17
NA	GND	L16
NA	GND	L15
NA	GND	L14
NA	GND	L13
NA	GND	L12
NA	GND	L11
NA	GND	L10
NA	GND	K17
NA	GND	K16
NA	GND	K15
NA	GND	K14
NA	GND	K13
NA	GND	K12
NA	GND	K11

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
NA	GND	K10
NA	GND	J25
NA	GND	J2
NA	GND	E5
NA	GND	E22
NA	GND	D4
NA	GND	D23
NA	GND	C3
NA	GND	C24
NA	GND	B9
NA	GND	B25
NA	GND	B2
NA	GND	B18
NA	GND	B14
NA	GND	AF26
NA	GND	AF1
NA	GND	AE9
NA	GND	AE25
NA	GND	AE2
NA	GND	AE18
NA	GND	AE13
NA	GND	AD3
NA	GND	AD24
NA	GND	AC4
NA	GND	AC23
NA	GND	AB5
NA	GND	AB22
NA	GND	A26
NA	GND	A1

Notes:

1. NC in the XCV400E.
2. V_{REF} or I/O option only in the XCV600E; otherwise, I/O option only.

Table 25: FG860 Differential Pin Pair Summary
XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
52	1	D11	B15	√	VREF
53	1	C14	E11	2	-
54	1	B14	C10	2	-
55	1	E10	A13	√	VREF
56	1	C9	C13	√	-
57	1	A12	D9	1	VREF
58	1	C12	E9	1	-
59	1	D8	B12	√	VREF
60	1	E8	A11	√	-
61	1	A10	C7	5	-
62	1	B10	C6	5	-
63	1	B9	A9	√	VREF
64	1	E7	A8	√	-
65	1	C5	B8	5	-
66	1	A6	A7	1	VREF
67	1	D6	B7	1	-
68	1	C4	A5	2	-
69	1	E6	B6	√	CS
70	2	F5	D2	√	DIN, D0
71	2	E4	E2	3	-
72	2	D3	F2	1	-
73	2	E1	F4	2	VREF
74	2	G2	E3	4	-
75	2	F1	G5	2	-
76	2	G1	F3	1	VREF
77	2	G4	H1	√	-
78	2	J2	G3	2	-
79	2	H5	K2	1	-
80	2	H4	K1	√	VREF
81	2	L2	L3	√	-
82	2	L1	J5	5	VREF
83	2	J4	M3	2	-
84	2	J3	M1	√	VREF
85	2	N2	K4	√	-

Table 25: FG860 Differential Pin Pair Summary
XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
86	2	N3	K3	2	-
87	2	L5	P2	√	D1
88	2	P3	L4	√	D2
89	2	P1	R2	3	-
90	2	M5	R3	1	-
91	2	M4	R1	2	-
92	2	N4	T2	4	-
93	2	P5	T3	2	-
94	2	P4	T1	1	VREF
95	2	U2	R4	√	-
96	2	U3	T5	2	-
97	2	T4	V2	1	-
98	2	U5	V3	√	D3
99	2	V1	V5	√	-
100	2	W2	V4	5	-
101	2	W5	W1	2	-
102	2	Y2	W4	√	VREF
103	2	Y1	Y5	√	-
104	2	AA1	Y4	2	VREF
105	2	AA4	AA2	√	-
106	3	AB3	AC4	2	VREF
107	3	AB1	AC5	√	-
108	3	AD4	AC3	√	VREF
109	3	AC1	AD5	2	-
110	3	AE4	AD3	5	-
111	3	AE5	AD2	√	-
112	3	AE1	AF5	√	VREF
113	3	AE2	AG4	1	-
114	3	AG5	AF1	2	-
115	3	AH4	AF2	√	-
116	3	AF3	AJ4	1	VREF
117	3	AG1	AJ5	2	-
118	3	AG2	AK4	4	-
119	3	AG3	AL4	2	-

Table 26: FG900 — XCV600E, XCV1000E, XCV1600E

Bank	Pin Description	Pin #
NA	VCCO_0	C12
NA	VCCO_1	B25
NA	VCCO_1	C19
NA	VCCO_1	M18
NA	VCCO_1	M17
NA	VCCO_1	L17
NA	VCCO_1	H17
NA	VCCO_1	L16
NA	VCCO_1	M16
NA	VCCO_2	F29
NA	VCCO_2	M28
NA	VCCO_2	P23
NA	VCCO_2	R20
NA	VCCO_2	P20
NA	VCCO_2	R19
NA	VCCO_2	N19
NA	VCCO_2	P19
NA	VCCO_3	AE29
NA	VCCO_3	W28
NA	VCCO_3	U23
NA	VCCO_3	U20
NA	VCCO_3	T20
NA	VCCO_3	V19
NA	VCCO_3	T19
NA	VCCO_3	U19
NA	VCCO_4	AJ25
NA	VCCO_4	AH19
NA	VCCO_4	W18
NA	VCCO_4	AC17
NA	VCCO_4	Y17
NA	VCCO_4	W17
NA	VCCO_4	W16
NA	VCCO_4	Y16
NA	VCCO_5	AJ6
NA	VCCO_5	Y15
NA	VCCO_5	W15
NA	VCCO_5	AC14

Table 26: FG900 — XCV600E, XCV1000E, XCV1600E

Bank	Pin Description	Pin #
NA	VCCO_5	Y14
NA	VCCO_5	W14
NA	VCCO_5	W13
NA	VCCO_5	AH12
NA	VCCO_6	AE2
NA	VCCO_6	V12
NA	VCCO_6	U12
NA	VCCO_6	T12
NA	VCCO_6	U11
NA	VCCO_6	T11
NA	VCCO_6	U8
NA	VCCO_6	W3
NA	VCCO_7	F2
NA	VCCO_7	R12
NA	VCCO_7	P12
NA	VCCO_7	N12
NA	VCCO_7	R11
NA	VCCO_7	P11
NA	VCCO_7	P8
NA	VCCO_7	M3
NA	GND	Y18
NA	GND	AH7
NA	GND	AK30
NA	GND	AJ30
NA	GND	B30
NA	GND	A30
NA	GND	AK29
NA	GND	AJ29
NA	GND	AC29
NA	GND	H29
NA	GND	B29
NA	GND	A29
NA	GND	AH28
NA	GND	V28
NA	GND	N28
NA	GND	C28

Table 27: FG900 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
120	3	AA30	W24	4	-
121	3	AA29	V20	1	-
122	3	Y27	W23	NA	-
123	3	Y26	AB30	√	D5
124	3	V21	AA28	√	VREF
125	3	Y25	AA27	4	-
126	3	W22	Y23	4	-
127	3	Y24	AB28	4	VREF
128	3	AC30	AA25	√	-
129	3	W21	AA24	2	-
130	3	AB26	AD30	√	-
131	3	Y22	AC27	√	VREF
132	3	AD28	AB25	2	-
133	3	AC26	AE30	4	-
134	3	AD27	AF30	√	-
135	3	AF29	AB24	1	VREF
136	3	AB23	AE28	4	-
137	3	AG30	AC25	3	-
138	3	AE26	AG29	4	VREF
139	3	AH30	AC24	1	-
140	3	AF28	AD25	NA	-
141	3	AH29	AA22	√	INIT
142	4	AF27	AK28	√	-
143	4	AG26	AH27	4	-
144	4	AD23	AJ27	2	-
145	4	AB21	AF25	2	VREF
146	4	AC22	AH26	2	-
147	4	AA21	AG25	√	-
148	4	AJ26	AD22	√	VREF
149	4	AA20	AH25	1	-
150	4	AC21	AF24	1	-
151	4	AG24	AK26	√	-
152	4	AJ24	AF23	√	VREF
153	4	AE23	AB20	2	-

Table 27: FG900 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
154	4	AC20	AG23	2	-
155	4	AF22	AE22	√	-
156	4	AJ22	AG22	√	VREF
157	4	AK24	AD20	NA	-
158	4	AA19	AF21	4	-
159	4	AH22	AA18	NA	VREF
160	4	AG21	AK23	NA	-
161	4	AH21	AD19	4	-
162	4	AE20	AJ21	2	-
163	4	AG20	AF20	2	-
164	4	AC18	AF19	2	-
165	4	AJ20	AE19	√	-
166	4	AK22	AH20	√	VREF
167	4	AG19	AB17	1	-
168	4	AJ19	AD17	1	-
169	4	AA16	AA17	√	-
170	4	AK21	AB16	√	VREF
171	4	AG18	AK20	2	-
172	4	AK19	AD16	2	-
173	4	AE16	AE17	√	-
174	4	AG17	AJ17	√	VREF
175	4	AD15	AH17	NA	-
176	4	AG16	AK17	4	VREF
177	5	AF16	AH16	NA	IO_LVDS_DLL
178	5	AC15	AG15	4	VREF
179	5	AB15	AF15	√	-
180	5	AA15	AF14	√	VREF
181	5	AH15	AK15	√	-
182	5	AB14	AF13	2	-
183	5	AH14	AJ14	2	-
184	5	AE14	AG13	√	VREF
185	5	AK13	AD13	√	-
186	5	AE13	AF12	1	-
187	5	AC13	AA13	1	-

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
0	IO_L40P_Y	A17
0	IO_VREF_L41N_Y	G17 ¹
0	IO_L41P_Y	B17
0	IO_LVDS_DLL_L42N	C17
1	GCK2	D17
1	IO	A18
1	IO	B18 ³
1	IO	B24
1	IO	B25
1	IO	E22 ³
1	IO	E23 ³
1	IO	D18 ³
1	IO	D19
1	IO	D25 ³
1	IO	D26 ³
1	IO	D28 ³
1	IO	D29 ³
1	IO	G23 ³
1	IO	J23 ³
1	IO_LVDS_DLL_L42P	J18
1	IO_L43N_Y	G18
1	IO_VREF_L43P_Y	C18 ¹
1	IO_L44N_Y	H18
1	IO_L44P_Y	F18
1	IO_L45N_YY	B19
1	IO_VREF_L45P_YY	A19
1	IO_L46N_YY	K19
1	IO_L46P_YY	C19
1	IO_L47N	F19 ⁵
1	IO_L47P	E19 ⁴
1	IO_L48N_Y	G19
1	IO_L48P_Y	J19
1	IO_L49N_Y	A20

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
1	IO_L49P_Y	G20
1	IO_L50N	B20 ⁵
1	IO_L50P	F20 ⁴
1	IO_L51N_YY	D20
1	IO_VREF_L51P_YY	E20
1	IO_L52N_YY	H20
1	IO_L52P_YY	A21
1	IO_L53N	E21 ⁵
1	IO_L53P	J20 ⁴
1	IO_L54N_Y	D21
1	IO_L54P_Y	K20
1	IO_L55N_Y	B21
1	IO_L55P_Y	H21
1	IO_L56N_YY	G21 ⁵
1	IO_L56P_YY	F21 ⁴
1	IO_L57N_YY	A22
1	IO_VREF_L57P_YY	B22
1	IO_L58N_YY	J21
1	IO_L58P_YY	C22
1	IO_L59N_Y	D22
1	IO_L59P_Y	G22
1	IO_L60N_Y	K21
1	IO_L60P_Y	A23
1	IO_L61N_Y	F22
1	IO_L61P_Y	B23
1	IO_L62N_Y	C23
1	IO_L62P_Y	H22
1	IO_L63N_YY	D23
1	IO_L63P_YY	K22
1	IO_L64N_YY	A24
1	IO_VREF_L64P_YY	J22
1	IO_L65N_Y	H23
1	IO_L65P_Y	D24
1	IO_L66N_Y	A25

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
2	IO_L126N_YY	T32
2	IO_VREF_L127P_Y	U29 ¹
2	IO_L127N_Y	U33
2	IO_L128P_YY	V33
2	IO_L128N_YY	U31
3	IO	V27 ³
3	IO	V31
3	IO	V32 ³
3	IO	W33
3	IO	AB25 ³
3	IO	AB26 ³
3	IO	AB31 ³
3	IO	AC31 ³
3	IO	AF34
3	IO	AG31 ³
3	IO	AG33 ³
3	IO	AG34
3	IO	AH29 ³
3	IO	AJ30 ³
3	IO_L129P_Y	V26
3	IO_VREF_L129N_Y	V30 ¹
3	IO_L130P_YY	W34
3	IO_L130N_YY	V28
3	IO_L131P_YY	W32
3	IO_VREF_L131N_YY	W30
3	IO_L132P_Y	V29
3	IO_L132N_Y	Y34
3	IO_L133P	W29 ⁵
3	IO_L133N	Y33 ⁴
3	IO_L134P_Y	W26
3	IO_L134N_Y	W28
3	IO_L135P_YY	Y31
3	IO_L135N_YY	Y30

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
3	IO_L136P_YY	AA34 ⁵
3	IO_L136N_YY	W31 ⁴
3	IO_D4_L137P_YY	AA33
3	IO_VREF_L137N_YY	Y29
3	IO_L138P_Y	W25
3	IO_L138N_Y	AB34
3	IO_L139P_Y	Y28 ⁵
3	IO_L139N_Y	AB33 ⁴
3	IO_L140P_Y	AA30
3	IO_L140N_Y	Y26
3	IO_L141P_YY	Y27
3	IO_L141N_YY	AA31
3	IO_L142P_YY	AA27 ⁵
3	IO_L142N_YY	AA29 ⁴
3	IO_L143P_Y	AB32
3	IO_VREF_L143N_Y	AB29
3	IO_L144P_Y	AA28
3	IO_L144N_Y	AC34
3	IO_L145P	Y25
3	IO_L145N	AD34
3	IO_L146P_Y	AB30
3	IO_L146N_Y	AC33
3	IO_L147P_Y	AA26
3	IO_L147N_Y	AC32
3	IO_L148P_Y	AD33
3	IO_L148N_Y	AB28
3	IO_L149P_YY	AE34
3	IO_D5_L149N_YY	AB27
3	IO_D6_L150P_YY	AE33
3	IO_VREF_L150N_YY	AC30
3	IO_L151P_Y	AA25
3	IO_L151N_Y	AE32
3	IO_L152P_YY	AE31
3	IO_L152N_YY	AD29

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
NA	GND	R15
NA	GND	P15
NA	GND	L3
NA	GND	G7
NA	GND	E30
NA	GND	C24
NA	GND	B34
NA	GND	AP32
NA	GND	AM1
NA	GND	AM34
NA	GND	AJ29
NA	GND	AF9
NA	GND	AA17
NA	GND	Y17
NA	GND	W16
NA	GND	V16
NA	GND	U17
NA	GND	T17
NA	GND	R16
NA	GND	P16
NA	GND	L32
NA	GND	G28
NA	GND	D4
NA	GND	C32
NA	GND	A1
NA	GND	AP33
NA	GND	AM2
NA	GND	AL4
NA	GND	AH1
NA	GND	AF26
NA	GND	AA18
NA	GND	Y18
NA	GND	W17
NA	GND	V17

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
NA	GND	U18
NA	GND	T18
NA	GND	R17
NA	GND	P17
NA	GND	J9
NA	GND	G34
NA	GND	D31
NA	GND	C33
NA	GND	A2
NA	GND	AB17
NA	GND	AB18
NA	GND	N17
NA	GND	N18
NA	GND	U13
NA	GND	V13
NA	GND	U22
NA	GND	V22

Notes:

1. V_{REF} or I/O option only in the XCV1600E, XCV2000E, XCV2600E, and XCV3200E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV2000E, XCV2600E, and XCV3200E; otherwise, I/O option only.
3. No Connect in the XCV1000E, XCV1600E.
4. No Connect in the XCV1000E.
5. I/O in the XCV1000E.

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
71	1	A27	G24	3200 2000 1000	-
72	1	G25	B27	3200 1600	-
73	1	C27	E26	3200 2600 2000 1600 1000	VREF
74	1	B28	J24	3200 2600 2000 1600 1000	-
75	1	H25	K24	3200 2600	-
76	1	F26	D27	3200 1000	-
77	1	C28	G26	3200 1000	-
78	1	J25	E27	2000 1600	-
79	1	H26	A30	3200 2600 2000 1600 1000	VREF
80	1	B29	G27	3200 2600 2000 1600 1000	-
81	1	C29	F27	3200 2600 1000	-
82	1	F28	E28	3200 2000 1000	VREF
83	1	B30	L25	3200 2000 1000	-
84	1	E29	B31	3200 1600 1000	-
85	1	D30	A31	3200 2600 2000 1600 1000	CS
86	2	D32	J27	3200 2600 2000 1600 1000	DIN, D0
87	2	E31	F30	3200 2600 2000	-
88	2	G29	F32	2600 2000 1000	-
89	2	E32	G30	3200 2600 1600 1000	VREF
90	2	M25	G31	2600 1600	-

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
91	2	L26	D33	3200 2600 1600 1000	-
92	2	D34	H29	2600 2000 1000	VREF
93	2	J28	E33	3200 2600 2000 1600	-
94	2	H28	H30	3200 2600 2000 1600 1000	-
95	2	H32	K28	3200 2600 1600 1000	-
96	2	L27	F33	3200 2600 2000	-
97	2	M26	E34	2600 2000 1000	-
98	2	H31	G32	3200 2600 2000 1600 1000	VREF
99	2	N25	J31	2000 1600	-
100	2	J30	G33	3200 2600 2000 1600 1000	-
101	2	H34	J29	2600 1000	VREF
102	2	M27	H33	3200 2600 1600	-
103	2	K29	J34	3200 2600 1600 1000	-
104	2	L29	J33	3200 2600 2000 1600 1000	VREF
105	2	M28	K34	3200 2600 2000 1600 1000	-
106	2	N27	L34	3200 1600 1000	-
107	2	K33	P26	2000 1600 1000	D1
108	2	R25	M34	3200 2600 2000	-
109	2	L31	L33	2000 1000	-
110	2	P27	M33	3200 2600 1600 1000	-

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
192	4	AK24	AH23	2600 1600 1000	-
193	4	AF22	AP24	3200 2600 2000 1600 1000	VREF
194	4	AL24	AK23	3200 2600 2000 1600 1000	-
195	4	AG22	AN23	3200 1600 1000	-
196	4	AP23	AM23	3200 2000 1000	-
197	4	AH22	AP22	3200 2000 1000	-
198	4	AL23	AF21	3200 2600 1000	-
199	4	AL22	AJ22	3200 2600 2000 1600 1000	-
200	4	AK22	AM22	3200 2600 2000 1600 1000	VREF
201	4	AG21	AJ21	2000 1600	-
202	4	AP21	AE20	3200 2600 1000	-
203	4	AH21	AL21	3200 2600 1000	-
204	4	AN21	AF20	3200	-
205	4	AK21	AP20	3200 2600 2000 1600 1000	-
206	4	AE19	AN20	3200 2600 2000 1600 1000	VREF
207	4	AG20	AL20	3200 1600	-
208	4	AH20	AK20	3200 2000 1000	-
209	4	AN19	AJ20	3200 2000 1000	-
210	4	AF19	AP19	3200 2600	-

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
211	4	AM19	AH19	3200 2600 2000 1600 1000	-
212	4	AJ19	AP18	3200 2600 2000 1600 1000	VREF
213	4	AF18	AP17	2600 1600 1000	-
214	4	AJ18	AL18	2600 1600 1000	VREF
215	5	AM18	AL17	None	IO_LVDS_DLL
216	5	AH17	AM17	2600 1600 1000	VREF
217	5	AJ17	AG17	2600 1600 1000	-
218	5	AP16	AL16	3200 2600 2000 1600 1000	VREF
219	5	AJ16	AM16	3200 2600 2000 1600 1000	-
220	5	AK16	AP15	3200 2600	-
221	5	AL15	AH16	3200 2000 1000	-
222	5	AN15	AF16	3200 2000 1000	-
223	5	AP14	AE16	3200 1600	-
224	5	AK15	AJ15	3200 2600 2000 1600 1000	VREF
225	5	AH15	AN14	3200 2600 2000 1600 1000	-
226	5	AK14	AG15	3200	-
227	5	AM13	AF15	3200 2600 1000	-
228	5	AG14	AP13	3200 2600 1000	-
229	5	AE14	AE15	2000 1600	-
230	5	AN13	AG13	3200 2600 2000 1600 1000	VREF