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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	1176
Number of Logic Elements/Cells	5292
Total RAM Bits	114688
Number of I/O	260
Number of Gates	306393
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	352-LBGA Exposed Pad, Metal
Supplier Device Package	352-MBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv200e-8bg352c

Development System

Virtex-E FPGAs are supported by the Xilinx Foundation and Alliance Series CAE tools. The basic methodology for Virtex-E design consists of three interrelated steps: design entry, implementation, and verification. Industry-standard tools are used for design entry and simulation (for example, Synopsys FPGA Express), while Xilinx provides proprietary architecture-specific tools for implementation.

The Xilinx development system is integrated under the Xilinx Design Manager (XDM™) software, providing designers with a common user interface regardless of their choice of entry and verification tools. The XDM software simplifies the selection of implementation options with pull-down menus and on-line help.

Application programs ranging from schematic capture to Placement and Routing (PAR) can be accessed through the XDM software. The program command sequence is generated prior to execution, and stored for documentation.

Several advanced software features facilitate Virtex-E design. RPMs, for example, are schematic-based macros with relative location constraints to guide their placement. They help ensure optimal implementation of common functions.

For HDL design entry, the Xilinx FPGA Foundation development system provides interfaces to the following synthesis design environments.

- Synopsys (FPGA Compiler, FPGA Express)
- Exemplar (Spectrum)
- Synplicity (Synplify)

For schematic design entry, the Xilinx FPGA Foundation and Alliance development system provides interfaces to the following schematic-capture design environments.

- Mentor Graphics V8 (Design Architect, QuickSim II)
- Viewlogic Systems (Viewdraw)

Third-party vendors support many other environments.

A standard interface-file specification, Electronic Design Interchange Format (EDIF), simplifies file transfers into and out of the development system.

Virtex-E FPGAs are supported by a unified library of standard functions. This library contains over 400 primitives and macros, ranging from 2-input AND gates to 16-bit accumulators, and includes arithmetic functions, comparators, counters, data registers, decoders, encoders, I/O functions, latches, Boolean functions, multiplexers, shift registers, and barrel shifters.

The “soft macro” portion of the library contains detailed descriptions of common logic functions, but does not contain any partitioning or placement information. The performance of these macros depends, therefore, on the partitioning and placement obtained during implementation.

RPMs, on the other hand, do contain predetermined partitioning and placement information that permits optimal

implementation of these functions. Users can create their own library of soft macros or RPMs based on the macros and primitives in the standard library.

The design environment supports hierarchical design entry, with high-level schematics that comprise major functional blocks, while lower-level schematics define the logic in these blocks. These hierarchical design elements are automatically combined by the implementation tools. Different design entry tools can be combined within a hierarchical design, thus allowing the most convenient entry method to be used for each portion of the design.

Design Implementation

The place-and-route tools (PAR) automatically provide the implementation flow described in this section. The partitioner takes the EDIF net list for the design and maps the logic into the architectural resources of the FPGA (CLBs and IOBs, for example). The placer then determines the best locations for these blocks based on their interconnections and the desired performance. Finally, the router interconnects the blocks.

The PAR algorithms support fully automatic implementation of most designs. For demanding applications, however, the user can exercise various degrees of control over the process. User partitioning, placement, and routing information is optionally specified during the design-entry process. The implementation of highly structured designs can benefit greatly from basic floor planning.

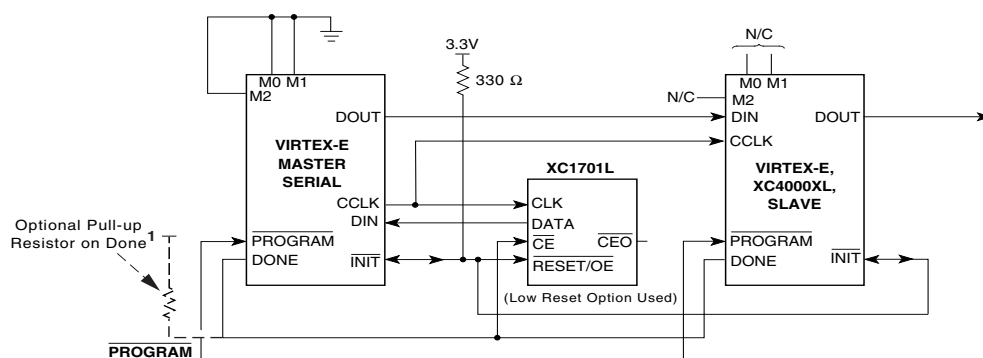
The implementation software incorporates Timing Wizard® timing-driven placement and routing. Designers specify timing requirements along entire paths during design entry. The timing path analysis routines in PAR then recognize these user-specified requirements and accommodate them.

Timing requirements are entered on a schematic in a form directly relating to the system requirements, such as the targeted clock frequency, or the maximum allowable delay between two registers. In this way, the overall performance of the system along entire signal paths is automatically tailored to user-generated specifications. Specific timing information for individual nets is unnecessary.

Design Verification

In addition to conventional software simulation, FPGA users can use in-circuit debugging techniques. Because Xilinx devices are infinitely reprogrammable, designs can be verified in real time without the need for extensive sets of software simulation vectors.

The development system supports both software simulation and in-circuit debugging techniques. For simulation, the system extracts the post-layout timing information from the design database, and back-annotates this information into the net list for use by the simulator. Alternatively, the user can verify timing-critical portions of the design using the TRCE® static timing analyzer.



Note 1: If none of the Virtex FPGAs have been selected to drive DONE, an external pull-up resistor of 330 Ω should be added to the common DONE line. (For Spartan-XL devices, add a 4.7K Ω pull-up resistor.) This pull-up is not needed if the DriveDONE attribute is set. If used, DriveDONE should be selected only for the last device in the configuration chain.

XCVE ds_013_050103

Figure 13: Master/Slave Serial Mode Circuit Diagram

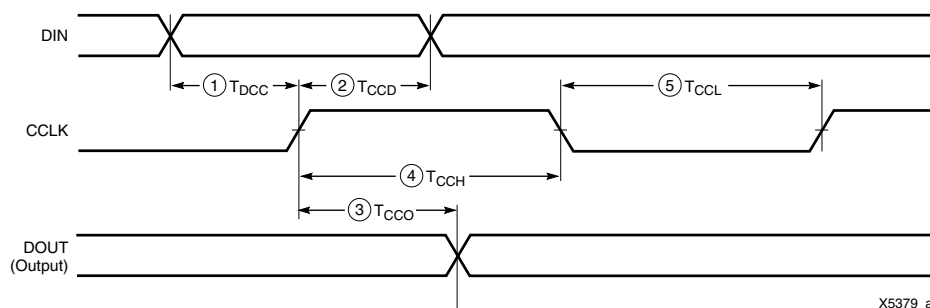


Figure 14: Slave-Serial Mode Programming Switching Characteristics

Master-Serial Mode

In master-serial mode, the CCLK output of the FPGA drives a Xilinx Serial PROM that feeds bit-serial data to the DIN input. The FPGA accepts this data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge. The maximum capacity for a single LOUT/DOUT write is $2^{20}-1$ (1,048,575) 32-bit words, or 33,554,400 bits.

The interface is identical to slave-serial except that an internal oscillator is used to generate the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK, which always starts at a slow default frequency. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration. Switching to a lower frequency is prohibited.

The CCLK frequency is set using the ConfigRate option in the bitstream generation software. The maximum CCLK fre-

quency that can be selected is 60 MHz. When selecting a CCLK frequency, ensure that the serial PROM and any daisy-chained FPGAs are fast enough to support the clock rate.

On power-up, the CCLK frequency is approximately 2.5 MHz. This frequency is used until the ConfigRate bits have been loaded when the frequency changes to the selected ConfigRate. Unless a different frequency is specified in the design, the default ConfigRate is 4 MHz.

In a full master/slave system ([Figure 13](#)), the left-most device operates in master-serial mode. The remaining devices operate in slave-serial mode. The SPROM $\overline{\text{RESET}}$ pin is driven by $\overline{\text{INIT}}$, and the $\overline{\text{CE}}$ input is driven by DONE . There is the potential for contention on the DONE pin, depending on the start-up sequence options chosen.

The sequence of operations necessary to configure a Virtex-E FPGA serially appears in **Figure 15**.

Useful Application Examples

The Virtex-E DLL can be used in a variety of creative and useful applications. The following examples show some of the more common applications. The Verilog and VHDL example files are available at:

<ftp://ftp.xilinx.com/pub/applications/xapp/xapp132.zip>

Standard Usage

The circuit shown in **Figure 27** resembles the BUFGDLL macro implemented to provide access to the RST and LOCKED pins of the CLKDLL.

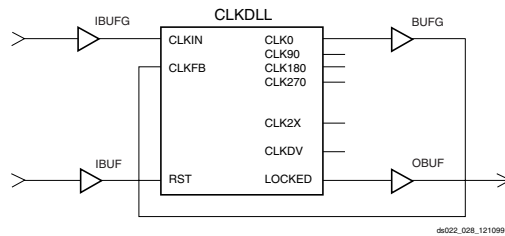


Figure 27: Standard DLL Implementation

Board Level Deskew of Multiple Non-Virtex-E Devices

The circuit shown in **Figure 28** can be used to deskew a system clock between a Virtex-E chip and other non-Virtex-E chips on the same board. This application is commonly used when the Virtex-E device is used in conjunction with other standard products such as SRAM or DRAM devices. While designing the board level route, ensure that the return net delay to the source equals the delay to the other chips involved.

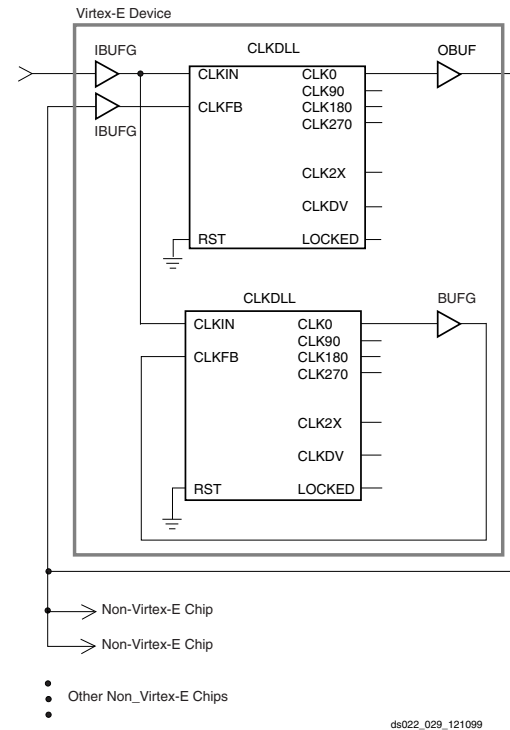


Figure 28: DLL Deskew of Board Level Clock

Board-level deskew is not required for low-fanout clock networks. It is recommended for systems that have fanout limitations on the clock network, or if the clock distribution chip cannot handle the load.

Do not use the DLL output clock signals until after activation of the LOCKED signal. Prior to the activation of the LOCKED signal, the DLL output clocks are not valid and can exhibit glitches, spikes, or other spurious movement.

The dll_mirror_1 files in the [xapp132.zip](#) file show the VHDL and Verilog implementation of this circuit.

Deskew of Clock and Its 2x Multiple

The circuit shown in **Figure 29** implements a 2x clock multiplier and also uses the CLK0 clock output with a zero ns skew between registers on the same chip. Alternatively, a clock divider circuit can be implemented using similar connections.

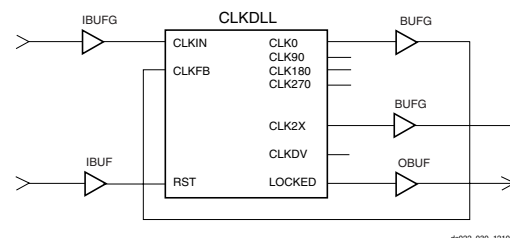


Figure 29: DLL Deskew of Clock and 2x Multiple

SSTL3_I

A sample circuit illustrating a valid termination technique for SSTL3_I appears in Figure 49. DC voltage specifications appear in Table 28.

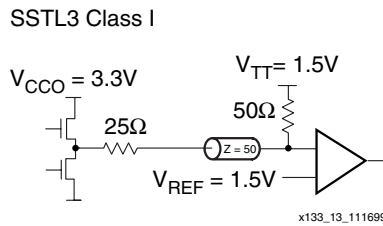


Figure 49: Terminated SSTL3 Class I

Table 28: SSTL3_I Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} = V_{REF} + 0.2$	1.5	1.7	3.9 ⁽¹⁾
$V_{IL} = V_{REF} - 0.2$	-0.3 ⁽²⁾	1.3	1.5
$V_{OH} = V_{REF} + 0.6$	1.9	-	-
$V_{OL} = V_{REF} - 0.6$	-	-	1.1
I_{OH} at V_{OH} (mA)	-8	-	-
I_{OL} at V_{OL} (mA)	8	-	-

Notes:

- V_{IH} maximum is $V_{CCO} + 0.3$
- V_{IL} minimum does not conform to the formula

SSTL3_II

A sample circuit illustrating a valid termination technique for SSTL3_II appears in Figure 50. DC voltage specifications appear in Table 29.

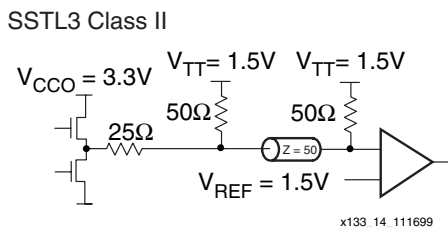


Figure 50: Terminated SSTL3 Class II

Table 29: SSTL3_II Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} = V_{REF} + 0.2$	1.5	1.7	3.9 ⁽¹⁾
$V_{IL} = V_{REF} - 0.2$	-0.3 ⁽²⁾	1.3	1.5
$V_{OH} = V_{REF} + 0.8$	2.1	-	-
$V_{OL} = V_{REF} - 0.8$	-	-	0.9
I_{OH} at V_{OH} (mA)	-16	-	-
I_{OL} at V_{OL} (mA)	16	-	-

Notes:

- V_{IH} maximum is $V_{CCO} + 0.3$
- V_{IL} minimum does not conform to the formula

SSTL2_I

A sample circuit illustrating a valid termination technique for SSTL2_I appears in Figure 51. DC voltage specifications appear in Table 30.

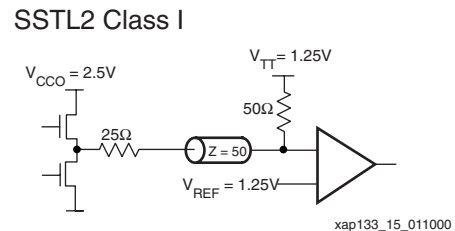


Figure 51: Terminated SSTL2 Class I

Table 30: SSTL2_I Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
$V_{REF} = 0.5 \times V_{CCO}$	1.15	1.25	1.35
$V_{TT} = V_{REF} + N^{(1)}$	1.11	1.25	1.39
$V_{IH} = V_{REF} + 0.18$	1.33	1.43	3.0 ⁽²⁾
$V_{IL} = V_{REF} - 0.18$	-0.3 ⁽³⁾	1.07	1.17
$V_{OH} = V_{REF} + 0.61$	1.76	-	-
$V_{OL} = V_{REF} - 0.61$	-	-	0.74
I_{OH} at V_{OH} (mA)	-7.6	-	-
I_{OL} at V_{OL} (mA)	7.6	-	-

Notes:

- N must be greater than or equal to -0.04 and less than or equal to 0.04.
- V_{IH} maximum is $V_{CCO} + 0.3$.
- V_{IL} minimum does not conform to the formula.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
CTT	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.4$	$V_{REF} + 0.4$	8	-8
AGP	-0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2

Notes:

1. V_{OL} and V_{OH} for lower drive currents are sample tested.
2. Tested according to the relevant specifications.
3. DC input and output levels for HSTL18 (HSTL I/O standard with V_{CCO} of 1.8 V) are provided in an HSTL white paper on www.xilinx.com.

LVDS DC Specifications

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}		2.375	2.5	2.625	V
Output High Voltage for Q and $\bar{Q}$	V_{OH}	$R_T = 100 \Omega$ across Q and $\bar{Q}$ signals	1.25	1.425	1.6	V
Output Low Voltage for Q and $\bar{Q}$	V_{OL}	$R_T = 100 \Omega$ across Q and $\bar{Q}$ signals	0.9	1.075	1.25	V
Differential Output Voltage (Q - $\bar{Q}$), Q = High ($\bar{Q}$ - Q), $\bar{Q}$ = High	V_{ODIFF}	$R_T = 100 \Omega$ across Q and $\bar{Q}$ signals	250	350	450	mV
Output Common-Mode Voltage	V_{OCM}	$R_T = 100 \Omega$ across Q and $\bar{Q}$ signals	1.125	1.25	1.375	V
Differential Input Voltage (Q - $\bar{Q}$), Q = High ($\bar{Q}$ - Q), $\bar{Q}$ = High	V_{IDIFF}	Common-mode input voltage = 1.25 V	100	350	NA	mV
Input Common-Mode Voltage	V_{ICM}	Differential input voltage = ± 350 mV	0.2	1.25	2.2	V

Note: Refer to the Design Consideration section for termination schematics.

LVPECL DC Specifications

These values are valid at the output of the source termination pack shown under **LVPECL**, with a 100 Ω differential load only. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. The following table summarizes the DC output specifications of LVPECL.

DC Parameter	Min	Max	Min	Max	Min	Max	Units
V_{CCO}	3.0		3.3		3.6		V
V_{OH}	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{IH}	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential Input Voltage	0.3	-	0.3	-	0.3	-	V

CS144 Chip-Scale Package

XCV50E, XCV100E, XCV200E, XCV300E and XCV400E devices in CS144 Chip-scale packages have footprint compatibility. In the CS144 package, bank pairs that share a side are internally interconnected, permitting four choices for V_{CCO} . See [Table 3](#).

Table 3: I/O Bank Pairs and Shared V_{CCO} Pins

Paired Banks	Shared V_{CCO} Pins
Banks 0 & 1	A2, A13, D7
Banks 2 & 3	B12, G11, M13
Banks 4 & 5	N1, N7, N13
Banks 6 & 7	B2, G2, M2

Pins labeled IO_VREF can be used as either in all parts unless device-dependent, as indicated in the footnotes. If the pin is not used as V_{REF} , it can be used as general I/O. Immediately following [Table 4](#), see [Table 5](#) is Differential Pair information.

Table 4: CS144 — XCV50E, XCV100E, XCV200E

Bank	Pin Description	Pin #
0	GCK3	A6
0	IO	B3
0	IO_VREF_L0N_YY	B4 ²
0	IO_L0P_YY	A4
0	IO_L1N_YY	B5
0	IO_L1P_YY	A5
0	IO_LVDS_DLL_L2N	C6
0	IO_VREF	A3 ¹
0	IO_VREF	C4
0	IO_VREF	D6
1	GCK2	A7
1	IO	A8
1	IO_LVDS_DLL_L2P	B7
1	IO_L3N_YY	C8
1	IO_L3P_YY	D8
1	IO_L4N_YY	C9
1	IO_VREF_L4P_YY	D9 ²
1	IO_WRITE_L5N_YY	C10
1	IO_CS_L5P_YY	D10

Table 4: CS144 — XCV50E, XCV100E, XCV200E

Bank	Pin Description	Pin #
1	IO_VREF	A10
1	IO_VREF	B8
1	IO_VREF	B10 ¹
2	IO	D12
2	IO	F12
2	IO_DOUT_BUSY_L6P_YY	C11
2	IO_DIN_D0_L6N_YY	C12
2	IO_D1_L7N	E10
2	IO_VREF_L7P	D13 ²
2	IO_L8N_YY	E13
2	IO_D2_L8P_YY	E12
2	IO_D3_L9N	F11
2	IO_VREF_L9P	F10
2	IO_L10P	F13
2	IO_VREF	C13 ¹
2	IO_VREF	D11
3	IO	H13
3	IO	K13
3	IO_L10N	G13
3	IO_VREF_L11N	H11
3	IO_D4_L11P	H12
3	IO_D5_L12N_YY	J13
3	IO_L12P_YY	H10
3	IO_VREF_L13N	J10 ²
3	IO_D6_L13P	J11
3	IO_INIT_L14N_YY	L13
3	IO_D7_L14P_YY	K10
3	IO_VREF	K11 ¹
3	IO_VREF	K12
4	GCK0	K7
4	IO	M8
4	IO	M10

Table 6: PQ240 — XCV50E, XCV100E, XCV200E, XCV300E, XCV400E

Pin #	Pin Description	Bank
P74	IO_L43P_YY	5
P73 ¹	IO_VREF_L43N_YY	5
P72	IO	5
P71	IO_L44P_YY	5
P70	IO_VREF_L44N_YY	5
P68	IO_L45P_YY	5
P67	IO_L45N_YY	5
P66 ²	IO_VREF_L46P_Y	5
P65	IO_L46N_Y	5
P64	IO_L47P_YY	5
P63	IO_L47N_YY	5
P57	IO_L48N_YY	6
P56	IO_L48P_YY	6
P54 ²	IO_VREF	6
P53	IO_L49N_Y	6
P52	IO_L49P_Y	6
P50	IO_VREF_L50N_Y	6
P49	IO_L50P_Y	6
P48	IO	6
P47 ¹	IO_VREF_L51N_Y	6
P46	IO_L51P_Y	6
P42	IO_L52N_YY	6
P41	IO_L52P_YY	6
P40	IO	6
P39	IO_L53N_Y	6
P38	IO_L53P_Y	6
P36	IO_VREF_L54N_Y	6
P35	IO_L54P_Y	6
P34	IO_L55N_Y	6
P33 ³	IO_VREF_L55P_Y	6
P31	IO	6
P28	IO_L56N_YY	7
P27	IO_L56P_YY	7

Table 6: PQ240 — XCV50E, XCV100E, XCV200E, XCV300E, XCV400E

Pin #	Pin Description	Bank
P26 ³	IO_VREF	7
P24	IO_L57N_Y	7
P23	IO_VREF_L57P_Y	7
P21	IO_L58N_Y	7
P20	IO_L58P_Y	7
P19	IO	7
P18	IO_L59N_YY	7
P17	IO_L59P_YY	7
P13	IO_L60N_Y	7
P12 ¹	IO_VREF_L60P_Y	7
P11	IO	7
P10	IO_L61N_Y	7
P9	IO_VREF_L61P_Y	7
P7	IO_L62N_Y	7
P6	IO_L62P_Y	7
P5 ²	IO_VREF_L63N_Y	7
P4	IO_L63P_Y	7
P3	IO	7
P179	CCLK	2
P120	DONE	3
P60	M0	NA
P58	M1	NA
P62	M2	NA
P122	PROGRAM	NA
P183	TDI	NA
P239	TCK	NA
P181	TDO	2
P2	TMS	NA
P225	VCCINT	NA
P214	VCCINT	NA
P198	VCCINT	NA
P164	VCCINT	NA
P148	VCCINT	NA

Table 8: HQ240 — XCV600E, XCV1000E

Pin #	Pin Description	Bank
P66	IO_VREF_L46P	5
P65	IO_L46N	5
P64	IO_L47P_YY	5
P63	IO_L47N_YY	5
P62	M2	NA
P61	VCCO	5
P60	M0	NA
P59	GND	NA
P58	M1	NA
P57	IO_L48N_YY	6
P56	IO_L48P_YY	6
P55	VCCO	6
P54	IO_VREF	6
P53	IO_L49N_Y	6
P52	IO_L49P_Y	6
P51	GND	NA
P50	IO_VREF_L50N_Y	6
P49	IO_L50P_Y	6
P48	IO_VREF	6
P47	IO_VREF_L51N_Y	6
P46	IO_L51P_Y	6
P45	GND	NA
P44	VCCO	6
P43	VCCINT	NA
P42	IO_L52N_YY	6
P41	IO_L52P_YY	6
P40 ¹	IO_VREF	6
P39	IO_L53N_Y	6
P38	IO_L53P_Y	6
P37	GND	NA
P36	IO_VREF_L54N_Y	6
P35	IO_L54P_Y	6
P34	IO_L55N_Y	6
P33	IO_VREF_L55P_Y	6
P32	VCCINT	NA
P31	IO	6

Table 8: HQ240 — XCV600E, XCV1000E

Pin #	Pin Description	Bank
P30	VCCO	6
P29	GND	NA
P28	IO_L56N_YY	7
P27	IO_L56P_YY	7
P26	IO_VREF	7
P25	VCCO	7
P24	IO_L57N_Y	7
P23	IO_VREF_L57P_Y	7
P22	GND	NA
P21	IO_L58N_Y	7
P20	IO_L58P_Y	7
P19 ¹	IO_VREF	7
P18	IO_L59N_YY	7
P17	IO_L59P_YY	7
P16	VCCINT	NA
P15	VCCO	7
P14	GND	NA
P13	IO_L60N_Y	7
P12	IO_VREF_L60P_Y	7
P11	IO_VREF	7
P10	IO_L61N_Y	7
P9	IO_VREF_L61P_Y	7
P8	GND	NA
P7	IO_L62N_Y	7
P6	IO_L62P_Y	7
P5	IO_VREF_L63N_Y	7
P4	IO_L63P_Y	7
P3	IO	7
P2	TMS	NA
P1	GND	NA

Notes:

1. V_{REF} or I/O option only in the XCV1000E; otherwise, I/O option only.

HQ240 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A ✓ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 9: HQ240 Differential Pin Pair Summary
XCV600E, XCV1000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	P92	P93	NA	IO_DLL_L40P
1	5	P89	P87	NA	IO_DLL_L40N
2	1	P210	P209	NA	IO_DLL_L6P
3	0	P213	P215	NA	IO_DLL_L6N
IO LVDS					
Total Pairs: 64, Asynchronous Output Pairs: 53					
0	0	P236	P237	NA	VREF
1	0	P234	P235	✓	-
2	0	P228	P229	✓	VREF
3	0	P223	P224	✓	-
4	0	P220	P221	✓	-
5	0	P217	P218	✓	VREF
6	1	P209	P215	NA	IO_LVDS_DLL
7	1	P205	P206	✓	VREF
8	1	P202	P203	✓	-
9	1	P199	P200	✓	-
10	1	P194	P195	✓	VREF
11	1	P191	P192	✓	VREF
12	1	P188	P189	✓	-
13	1	P186	P187	NA	VREF
14	1	P184	P185	✓	CS
15	2	P178	P177	✓	DIN, D0

Table 9: HQ240 Differential Pin Pair Summary
XCV600E, XCV1000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
16	2	P174	P173	✓	-
17	2	P171	P170	✓	VREF
18	2	P168	P167	✓	D1
19	2	P163	P162	✓	D2
20	2	P160	P159	✓	-
21	2	P157	P156	✓	D3
22	2	P155	P154	1	VREF
23	2	P153	P152	✓	-
24	3	P145	P144	✓	D4, VREF
25	3	P142	P141	✓	-
26	3	P139	P138	✓	D5
27	3	P134	P133	✓	VREF
28	3	P131	P130	✓	VREF
29	3	P128	P127	✓	-
30	3	P126	P125	1	VREF
31	3	P124	P123	✓	INIT
32	4	P118	P117	✓	-
33	4	P114	P113	✓	-
34	4	P111	P110	✓	VREF
35	4	P108	P107	✓	VREF
36	4	P103	P102	✓	-
37	4	P100	P99	✓	-
38	4	P97	P96	✓	VREF
39	4	P95	P94	NA	VREF
40	5	P93	P87	NA	IO_LVDS_DLL
41	5	P84	P82	NA	VREF
42	5	P79	P78	✓	-
43	5	P74	P73	✓	VREF
44	5	P71	P70	✓	VREF
45	5	P68	P67	✓	-
46	5	P66	P65	NA	VREF
47	5	P64	P63	✓	-

Table 15: BG560 Differential Pin Pair Summary
XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
171	7	J33	M29	√	-
172	7	K31	L30	√	VREF
173	7	H33	L29	4	-
174	7	H32	J31	18	VREF
175	7	H31	K29	14	-
176	7	G32	J30	20	VREF
177	7	G31	J29	√	VREF
178	7	E32	E33	15	-
179	7	F31	H29	14	-
180	7	E31	D32	15	VREF
181	7	C33	G29	14	-
182	7	D31	F30	14	VREF

Notes:

1. AO in the XCV1600E.
2. AO in the XCV2000E.
3. AO in the XCV1600E, 2000E.
4. AO in the XCV1000E, 1600E.
5. AO in the XCV1000E, 2000E.
6. AO in the XCV1000E.
7. AO in the XCV1000E, 1600E, 2000E.
8. AO in the XCV600E, 1600E.
9. AO in the XCV400E, 600E, 1600E.
10. AO in the XCV400E, 600E, 1000E, 2000E.
11. AO in the XCV400E, 600E, 1000E.
12. AO in the XCV400E, 1000E, 2000E.
13. AO in the XCV400E, 600E, 1000E, 1600E.
14. AO in the XCV400E, 1000E, 1600E.
15. AO in the XCV600E, 1000E, 2000E.
16. AO in the XCV600E, 2000E.
17. AO in the XCV400E, 600E, 1600E, 2000E.
18. AO in the XCV600E, 1000E, 1600E, 2000E.
19. AO in the XCV400E, 600E, 2000E.
20. AO in the XCV400E, 1000E.

FG256 Fine-Pitch Ball Grid Array Packages

XCV50E, XCV100E, XCV200E, and XCV300E devices in FG256 fine-pitch Ball Grid Array packages have footprint compatibility. Pins labeled IO_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF} , it can be used as general I/O. Immediately following Table 16, see Table 17 for Differential Pair information.

Table 16: FG256 Package — XCV50E, XCV100E, XCV200E, XCV300E

Bank	Pin Description	Pin #
0	GCK3	B8
0	IO	B3
0	IO	E7
0	IO	D8
0	IO_L0N_Y	C5
0	IO_VREF_L0P_Y	A3 ²
0	IO_L1N_YY	D5
0	IO_L1P_YY	E6
0	IO_VREF_L2N_YY	B4
0	IO_L2P_YY	A4
0	IO_L3N_Y	D6
0	IO_L3P_Y	B5
0	IO_VREF_L4N_YY	C6 ¹
0	IO_L4P_YY	A5
0	IO_L5N_YY	B6
0	IO_L5P_YY	C7
0	IO_L6N_Y	D7
0	IO_L6P_Y	C8
0	IO_VREF_L7N_Y	B7
0	IO_L7P_Y	A6
0	IO_LVDS_DLL_L8N	A7
1	GCK2	C9
1	IO	B10
1	IO_LVDS_DLL_L8P	A8
1	IO_L9N_Y	D9
1	IO_L9P_Y	A9
1	IO_L10N_Y	E10
1	IO_VREF_L10P_Y	B9

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
4	IO_VREF_L132P_YY	AV8
4	IO_L132N_YY	AU9
4	IO_L133P_Y	AW8
4	IO_L133N_Y	AT10
4	IO_VREF_L134P_Y	AV9 ³
4	IO_L134N_Y	AU10
4	IO_L135P_YY	AW9
4	IO_L135N_YY	AT11
4	IO_VREF_L136P_YY	AV10
4	IO_L136N_YY	AU11
4	IO_L137P_Y	AW10
4	IO_L137N_Y	AU12
4	IO_L138P_Y	AV11
4	IO_L138N_Y	AT13
4	IO_VREF_L139P_YY	AW11
4	IO_L139N_YY	AU13
4	IO_L140P_YY	AT14
4	IO_L140N_YY	AV12
4	IO_L141P_Y	AU14
4	IO_L141N_Y	AW12
4	IO_L142P_Y	AT15
4	IO_L142N_Y	AV13
4	IO_L143P_YY	AU15
4	IO_L143N_YY	AW13
4	IO_VREF_L144P_YY	AV14 ¹
4	IO_L144N_YY	AT16
4	IO_L145P_Y	AW14
4	IO_L145N_Y	AU16
4	IO_L146P_Y	AV15
4	IO_L146N_Y	AR17
4	IO_L147P_YY	AW15
4	IO_L147N_YY	AT17
4	IO_VREF_L148P_YY	AU17
4	IO_L148N_YY	AV16
4	IO_L149P_Y	AR18
4	IO_L149N_Y	AW16

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
4	IO_L150P_Y	AT18
4	IO_L150N_Y	AV17
4	IO_L151P_YY	AU18
4	IO_L151N_YY	AW17
4	IO_VREF_L152P_YY	AT19
4	IO_L152N_YY	AV18
4	IO_L153P_Y	AU19
4	IO_L153N_Y	AW18
4	IO_VREF_L154P	AU21 ²
4	IO_L154N	AV19
4	IO_LVDS_DLL_L155P	AT21
5	GCK1	AU22
5	IO	AT34
5	IO	AW20
5	IO_LVDS_DLL_L155N	AT22
5	IO_VREF_L156P_Y	AV20 ²
5	IO_L156N_Y	AR22
5	IO_L157P_YY	AV23
5	IO_VREF_L157N_YY	AW21
5	IO_L158P_YY	AU23
5	IO_L158N_YY	AV21
5	IO_L159P_Y	AT23
5	IO_L159N_Y	AW22
5	IO_L160P_Y	AR23
5	IO_L160N_Y	AV22
5	IO_L161P_YY	AV24
5	IO_VREF_L161N_YY	AW23
5	IO_L162P_YY	AW24
5	IO_L162N_YY	AU24
5	IO_L163P_Y	AW25
5	IO_L163N_Y	AT24
5	IO_L164P_Y	AV25
5	IO_L164N_Y	AU25
5	IO_L165P_YY	AW26
5	IO_VREF_L165N_YY	AT25 ¹

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
6	IO_VREF_L200N_YY	AH39
6	IO_L200P_YY	AG38
6	IO_L201N_YY	AG36
6	IO_L201P_YY	AG39
6	IO_L202N_Y	AG37
6	IO_L202P_Y	AF39
6	IO_L203N	AF36
6	IO_L203P	AE38
6	IO_L204N	AF37
6	IO_L204P	AF38
6	IO_VREF_L205N_Y	AE39 ¹
6	IO_L205P_Y	AE36
6	IO_L206N_YY	AD38
6	IO_L206P_YY	AE37
6	IO_L207N	AD39
6	IO_L207P	AD36
6	IO_L208N_Y	AC38
6	IO_L208P_Y	AC39
6	IO_VREF_L209N_YY	AD37
6	IO_L209P_YY	AB38
6	IO_L210N_YY	AC35
6	IO_L210P_YY	AB39
6	IO_L211N	AC36
6	IO_L211P	AA38
6	IO_L212N	AC37
6	IO_L212P	AA39
6	IO_VREF_L213N_YY	AB35
6	IO_L213P_YY	Y38
6	IO_L214N_YY	AB36
6	IO_L214P_YY	Y39
6	IO_VREF_L215N	AB37 ²
6	IO_L215P	AA36
7	IO	C38
7	IO	B37
7	IO	F37

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
7	IO_L216N_YY	AA37
7	IO_L216P_YY	W38
7	IO_L217N	W37
7	IO_VREF_L217P	V39 ²
7	IO_L218N_YY	W36
7	IO_L218P_YY	U39
7	IO_L219N_YY	V38
7	IO_VREF_L219P_YY	U38
7	IO_L220N	V37
7	IO_L220P	T39
7	IO_L221N	V36
7	IO_L221P	T38
7	IO_L222N_YY	V35
7	IO_L222P_YY	R39
7	IO_L223N_YY	U37
7	IO_VREF_L223P_YY	U36
7	IO_L224N_Y	R38
7	IO_L224P_Y	U35
7	IO_L225N	P39
7	IO_L225P	T37
7	IO_L226N_YY	P38
7	IO_L226P_YY	T36
7	IO_L227N_Y	N39
7	IO_VREF_L227P_Y	N38 ¹
7	IO_L228N	R37
7	IO_L228P	M39
7	IO_L229N	R36
7	IO_L229P	M38
7	IO_L230N_Y	P37
7	IO_L230P_Y	L39
7	IO_L231N_YY	P36
7	IO_L231P_YY	N37
7	IO_L232N_YY	L38
7	IO_VREF_L232P_YY	N36
7	IO_L233N	K39
7	IO_L233P	M37

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
3	IO_L117N_Y	AJ5
3	IO_L118P	AG2
3	IO_L118N	AK4
3	IO_L119P_Y	AG3
3	IO_L119N_Y	AL4
3	IO_L120P_Y	AH1
3	IO_L120N_Y	AL5
3	IO_L121P_Y	AH2
3	IO_L121N_Y	AM4
3	IO_L122P_YY	AH3
3	IO_D5_L122N_YY	AM5
3	IO_D6_L123P_YY	AJ1
3	IO_VREF_L123N_YY	AN3
3	IO_L124P_Y	AN4
3	IO_L124N_Y	AJ3
3	IO_L125P_YY	AN5
3	IO_L125N_YY	AK1
3	IO_L126P_YY	AK2
3	IO_VREF_L126N_YY	AP4
3	IO_L127P_Y	AK3
3	IO_L127N_Y	AP5
3	IO_L128P_Y	AR3
3	IO_VREF_L128N_Y	AL2 ²
3	IO_L129P_YY	AR4
3	IO_L129N_YY	AL3
3	IO_L130P_YY	AM1
3	IO_VREF_L130N_YY	AT3
3	IO_L131P_Y	AM2
3	IO_L131N_Y	AT4
3	IO_L132P_Y	AT5
3	IO_L132N_Y	AN1
3	IO_L133P_YY	AU3
3	IO_L133N_YY	AN2
3	IO_L134P_Y	AP1
3	IO_VREF_L134N_Y	AP2
3	IO_L135P_Y	AR1
3	IO_L135N_Y	AV3

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
3	IO_L136P	AR2
3	IO_L136N	AT1
3	IO_L137P_Y	AV4
3	IO_VREF_L137N_Y	AT2
3	IO_L138P_Y	AU1
3	IO_L138N_Y	AU5
3	IO_L139P_Y	AU2
3	IO_L139N_Y	AW3
3	IO_D7_L140P_YY	AV1
3	IO_INIT_L140N_YY	AW5
4	GCK0	BA22
4	IO	AV17
4	IO	AY11
4	IO	AY12
4	IO	AY13
4	IO	AY14
4	IO	BA8
4	IO	BA17
4	IO	BA19
4	IO	BA20
4	IO	BA21
4	IO	BB9
4	IO	BB18
4	IO_L141P_YY	AV6
4	IO_L141N_YY	BA4
4	IO_L142P_Y	AY4
4	IO_L142N_Y	BA5
4	IO_L143P_Y	AW6
4	IO_L143N_Y	BB5
4	IO_VREF_L144P_Y	BA6
4	IO_L144N_Y	AY5
4	IO_L145P_Y	BB6
4	IO_L145N_Y	AY6
4	IO_L146P_YY	BA7
4	IO_L146N_YY	AV7
4	IO_VREF_L147P_YY	BB7

FG860 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A $\checkmark$ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 25: FG860 Differential Pin Pair Summary
XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
3	0	C22	A22	NA	IO_DLL_L34N
2	1	B22	D22	NA	IO_DLL_L34P
1	5	AY22	AW21	NA	IO_DLL_L176N
0	4	BA22	AW20	NA	IO_DLL_L176P
IO LVDS					
Total Pairs: 281, Asynchronous Output Pairs: 111					
0	0	D38	A38	2	-
1	0	E37	B37	1	-
2	0	C39	A37	1	VREF
3	0	C38	B36	1	-
4	0	B35	A36	$\checkmark$	-
5	0	D37	A35	$\checkmark$	VREF
6	0	A34	C37	5	-
7	0	B33	E36	5	-
8	0	C32	A33	$\checkmark$	-
9	0	B32	C36	$\checkmark$	VREF
10	0	D35	A32	1	-
11	0	C35	C31	1	VREF
12	0	A31	E34	$\checkmark$	-
13	0	C30	D34	$\checkmark$	VREF
14	0	E33	B30	2	-
15	0	D33	A30	2	-
16	0	B29	C33	$\checkmark$	VREF
17	0	A29	E32	$\checkmark$	-

Table 25: FG860 Differential Pin Pair Summary
XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
18	0	C28	D32	2	-
19	0	B28	E31	1	-
20	0	A28	D31	1	-
21	0	C27	D30	5	-
22	0	B27	E29	$\checkmark$	-
23	0	A27	D29	$\checkmark$	VREF
24	0	D28	C26	5	-
25	0	F27	B26	5	-
26	0	C25	E27	$\checkmark$	-
27	0	B25	D27	$\checkmark$	VREF
28	0	D26	A25	1	-
29	0	E25	A24	1	-
30	0	B24	D25	$\checkmark$	-
31	0	A23	E24	$\checkmark$	VREF
32	0	E23	C23	2	-
33	0	D23	B23	2	VREF
34	1	D22	A22	NA	IO_LVDS_DLL
35	1	B21	D21	2	VREF
36	1	A21	D20	2	-
37	1	D19	C20	$\checkmark$	VREF
38	1	E19	B20	$\checkmark$	-
39	1	A19	D18	1	-
40	1	C19	E18	1	-
41	1	E17	B19	$\checkmark$	VREF
42	1	D16	A18	$\checkmark$	-
43	1	B18	E16	5	-
44	1	A17	F16	5	-
45	1	E15	C17	$\checkmark$	VREF
46	1	D14	B17	$\checkmark$	-
47	1	E14	A16	5	-
48	1	D13	C16	1	-
49	1	D12	B16	1	-
50	1	E12	A15	2	-
51	1	C11	C15	$\checkmark$	-

Table 25: FG860 Differential Pin Pair Summary
XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
52	1	D11	B15	√	VREF
53	1	C14	E11	2	-
54	1	B14	C10	2	-
55	1	E10	A13	√	VREF
56	1	C9	C13	√	-
57	1	A12	D9	1	VREF
58	1	C12	E9	1	-
59	1	D8	B12	√	VREF
60	1	E8	A11	√	-
61	1	A10	C7	5	-
62	1	B10	C6	5	-
63	1	B9	A9	√	VREF
64	1	E7	A8	√	-
65	1	C5	B8	5	-
66	1	A6	A7	1	VREF
67	1	D6	B7	1	-
68	1	C4	A5	2	-
69	1	E6	B6	√	CS
70	2	F5	D2	√	DIN, D0
71	2	E4	E2	3	-
72	2	D3	F2	1	-
73	2	E1	F4	2	VREF
74	2	G2	E3	4	-
75	2	F1	G5	2	-
76	2	G1	F3	1	VREF
77	2	G4	H1	√	-
78	2	J2	G3	2	-
79	2	H5	K2	1	-
80	2	H4	K1	√	VREF
81	2	L2	L3	√	-
82	2	L1	J5	5	VREF
83	2	J4	M3	2	-
84	2	J3	M1	√	VREF
85	2	N2	K4	√	-

Table 25: FG860 Differential Pin Pair Summary
XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
86	2	N3	K3	2	-
87	2	L5	P2	√	D1
88	2	P3	L4	√	D2
89	2	P1	R2	3	-
90	2	M5	R3	1	-
91	2	M4	R1	2	-
92	2	N4	T2	4	-
93	2	P5	T3	2	-
94	2	P4	T1	1	VREF
95	2	U2	R4	√	-
96	2	U3	T5	2	-
97	2	T4	V2	1	-
98	2	U5	V3	√	D3
99	2	V1	V5	√	-
100	2	W2	V4	5	-
101	2	W5	W1	2	-
102	2	Y2	W4	√	VREF
103	2	Y1	Y5	√	-
104	2	AA1	Y4	2	VREF
105	2	AA4	AA2	√	-
106	3	AB3	AC4	2	VREF
107	3	AB1	AC5	√	-
108	3	AD4	AC3	√	VREF
109	3	AC1	AD5	2	-
110	3	AE4	AD3	5	-
111	3	AE5	AD2	√	-
112	3	AE1	AF5	√	VREF
113	3	AE2	AG4	1	-
114	3	AG5	AF1	2	-
115	3	AH4	AF2	√	-
116	3	AF3	AJ4	1	VREF
117	3	AG1	AJ5	2	-
118	3	AG2	AK4	4	-
119	3	AG3	AL4	2	-

Table 25: FG860 Differential Pin Pair Summary
XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
188	5	AY27	AV28	√	-
189	5	BA27	AW29	5	-
190	5	BB28	AV29	1	-
191	5	AY28	AW30	1	-
192	5	BA28	AW31	2	-
193	5	BB29	AV31	√	-
194	5	AY29	AY32	√	VREF
195	5	AW32	BB30	2	-
196	5	AV32	AY30	2	-
197	5	BA30	AW33	√	VREF
198	5	BB31	AV33	√	-
199	5	AY34	BA31	1	VREF
200	5	AW34	BB32	1	-
201	5	BA32	AY35	√	VREF
202	5	BB33	AW35	√	-
203	5	AV35	BB34	5	-
204	5	AY36	BA34	5	-
205	5	BB35	AV36	√	VREF
206	5	BA35	AY37	√	-
207	5	BB36	BA36	5	-
208	5	AW37	BB37	1	VREF
209	5	BA37	AY38	1	-
210	5	BB38	AY39	2	-
211	6	AV42	AV41	√	-
212	6	AU41	AW40	3	-
213	6	AU42	AV39	1	-
214	6	AU38	AT41	2	VREF
215	6	AV40	AT42	4	-
216	6	AU39	AR41	2	-
217	6	AU40	AR42	1	VREF
218	6	AP42	AT38	√	-
219	6	AT39	AN41	2	-
220	6	AM40	AT40	1	-
221	6	AM41	AR38	√	VREF

Table 25: FG860 Differential Pin Pair Summary
XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
222	6	AR40	AM42	√	-
223	6	AP38	AL40	5	VREF
224	6	AL42	AP39	2	-
225	6	AK40	AP40	√	VREF
226	6	AN39	AK41	√	-
227	6	AN40	AK42	2	-
228	6	AJ41	AM38	√	VREF
229	6	AM39	AJ42	√	-
230	6	AH41	AH40	3	-
231	6	AH42	AL38	1	-
232	6	AG41	AL39	2	-
233	6	AG40	AK39	4	-
234	6	AG42	AJ38	2	-
235	6	AJ39	AF42	1	VREF
236	6	AH38	AF41	√	-
237	6	AH39	AE42	2	-
238	6	AE41	AG38	1	-
239	6	AD42	AG39	√	VREF
240	6	AF39	AD40	√	-
241	6	AE38	AD41	5	-
242	6	AC40	AE39	2	-
243	6	AC41	AD38	√	VREF
244	6	AC38	AB42	√	-
245	6	AC39	AB40	2	VREF
246	7	AB39	AA41	√	-
247	7	AA39	Y41	2	VREF
248	7	Y39	Y40	√	-
249	7	W41	Y38	√	VREF
250	7	W39	W40	2	-
251	7	V41	W38	5	-
252	7	V40	V39	√	-
253	7	U39	V42	√	VREF
254	7	U38	U41	1	-
255	7	T39	U42	2	-

Table 27: FG900 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
52	1	A22	C21	√	VREF
53	1	B22	H19	4	-
54	1	D22	E21	4	-
55	1	C22	F21	√	VREF
56	1	E22	H20	√	-
57	1	A23	G21	2	-
58	1	K19	A24	2	-
59	1	B24	C24	√	VREF
60	1	G22	H21	√	-
61	1	C25	E23	1	-
62	1	A26	D24	1	-
63	1	K20	B26	√	VREF
64	1	J21	D25	√	-
65	1	F23	C26	2	-
66	1	G23	B27	2	VREF
67	1	F24	A27	2	-
68	1	A28	B28	4	-
69	1	C27	K21	√	CS
70	2	J22	E27	√	DIN, D0
71	2	C29	D28	NA	-
72	2	G25	E25	1	-
73	2	E28	C30	4	VREF
74	2	K22	F27	3	-
75	2	D30	J23	4	-
76	2	L21	F28	1	VREF
77	2	G28	E30	√	-
78	2	G27	E29	4	-
79	2	K23	H26	1	-
80	2	F30	L22	√	VREF
81	2	H27	G29	√	-
82	2	G30	M21	2	-
83	2	J24	J26	4	-
84	2	H30	L23	4	VREF
85	2	K26	J28	4	-

Table 27: FG900 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
86	2	J29	K24	4	-
87	2	K27	J30	4	VREF
88	2	M22	K29	NA	D2
89	2	K28	L25	4	-
90	2	N21	K25	1	-
91	2	L24	L27	4	-
92	2	L29	M23	3	-
93	2	L26	L28	4	-
94	2	L30	M27	1	VREF
95	2	M26	M29	√	-
96	2	N29	M30	4	-
97	2	N25	N27	1	-
98	2	N30	P21	√	D3
99	2	N26	P28	√	-
100	2	P29	N24	2	-
101	2	P22	R26	√	-
102	2	P25	R29	4	VREF
103	2	R21	R28	4	-
104	2	R25	T30	4	VREF
105	2	P24	R27	4	-
106	3	R24	U29	NA	-
107	3	R22	T27	4	VREF
108	3	R23	T28	4	-
109	3	T21	T25	4	VREF
110	3	U28	U30	4	-
111	3	T23	U27	2	-
112	3	U25	V27	√	-
113	3	U24	V29	√	VREF
114	3	W30	U22	1	-
115	3	U21	W29	4	-
116	3	V26	W27	√	-
117	3	W26	Y29	1	VREF
118	3	W25	Y30	4	-
119	3	V24	Y28	3	-

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
6	IO_VREF_L265N_Y	AJ3
6	IO_L265P_Y	AG5
6	IO_L266N_YY	AD9 ⁴
6	IO_L266P_YY	AJ2 ⁵
6	IO_L267N_YY	AC10
6	IO_L267P_YY	AH2
6	IO_L268N_Y	AH3
6	IO_L268P_Y	AF5
6	IO_L269N_Y	AE8 ⁴
6	IO_L269P_Y	AG3 ⁵
6	IO_L270N_Y	AE7
6	IO_L270P_Y	AG2
6	IO_VREF_L271N_YY	AF6
6	IO_L271P_YY	AG1
6	IO_L272N_YY	AC9 ⁴
6	IO_L272P_YY	AG4 ⁵
6	IO_L273N_YY	AE6
6	IO_L273P_YY	AF3
6	IO_VREF_L274N_Y	AF1 ²
6	IO_L274P_Y	AF4
6	IO_L275N	AB10 ⁴
6	IO_L275P	AF2 ⁵
6	IO_L276N_Y	AC8
6	IO_L276P_Y	AE1
6	IO_VREF_L277N_YY	AD5
6	IO_L277P_YY	AE3
6	IO_L278N_YY	AC7
6	IO_L278P_YY	AD1
6	IO_L279N_Y	AD6
6	IO_L279P_Y	AD2
6	IO_VREF_L280N_YY	AB8
6	IO_L280P_YY	AC1
6	IO_L281N_YY	AC5
6	IO_L281P_YY	AC2

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
6	IO_L282N_Y	AA9
6	IO_L282P_Y	AC3
6	IO_L283N_Y	AC4
6	IO_L283P_Y	AD4
6	IO_L284N_Y	AA8
6	IO_L284P_Y	AB6
6	IO_L285N	AB1
6	IO_L285P	Y10
6	IO_L286N_Y	AB2
6	IO_L286P_Y	AA7
6	IO_VREF_L287N_Y	AA4
6	IO_L287P_Y	AA1
6	IO_L288N_YY	Y9 ⁴
6	IO_L288P_YY	AB4 ⁵
6	IO_L289N_YY	AA2
6	IO_L289P_YY	Y8
6	IO_L290N_Y	AA6
6	IO_L290P_Y	AA5
6	IO_L291N_Y	AB3 ⁴
6	IO_L291P_Y	Y7 ⁵
6	IO_L292N_Y	Y1
6	IO_L292P_Y	W10
6	IO_VREF_L293N_YY	Y5
6	IO_L293P_YY	Y2
6	IO_L294N_YY	W9 ⁴
6	IO_L294P_YY	W2 ⁵
6	IO_L295N_YY	W7
6	IO_L295P_YY	Y4
6	IO_L296N_Y	W1
6	IO_L296P_Y	Y6
6	IO_L297N_Y	W6 ⁴
6	IO_L297P_Y	W3 ⁵
6	IO_L298N_Y	V9
6	IO_L298P_Y	W4

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
153	3	AD31	AF33	3200 2600 2000 1600 1000	VREF
154	3	AC28	AF31	3200 2600 1600 1000	-
155	3	AC27	AF32	3200 2600 1600	-
156	3	AE29	AD28	2600 1000	VREF
157	3	AD30	AG32	3200 2600 2000 1600 1000	-
158	3	AC26	AH33	2000 1600	-
159	3	AD26	AF30	3200 2600 2000 1600 1000	VREF
160	3	AC25	AH32	2600 2000 1000	-
161	3	AE28	AL34	3200 2600 2000	-
162	3	AG30	AD27	3200 2600 1600 1000	-
163	3	AF29	AK34	3200 2600 2000 1600 1000	-
164	3	AD25	AE27	3200 2600 2000 1600	-
165	3	AJ33	AH31	2600 2000 1000	VREF
166	3	AE26	AL33	3200 2600 1600 1000	-
167	3	AF28	AL32	2600 1600	-
168	3	AJ31	AF27	3200 2600 1600 1000	VREF
169	3	AG29	AJ32	2600 2000 1000	-
170	3	AK33	AH30	3200 2600 2000	-
171	3	AK32	AK31	3200 2600 2000 1600 1000	INIT

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
172	4	AP31	AK29	3200 2600 2000 1600 1000	-
173	4	AP30	AN31	3200 1600 1000	-
174	4	AH27	AN30	3200 2000 1000	-
175	4	AM30	AK28	3200 2000 1000	VREF
176	4	AG26	AN29	3200 2600 1000	-
177	4	AF25	AM29	3200 2600 2000 1600 1000	-
178	4	AL29	AL28	3200 2600 2000 1600 1000	VREF
179	4	AE24	AN28	2000 1600	-
180	4	AJ27	AH26	3200 1000	-
181	4	AG25	AK27	3200 1000	-
182	4	AM28	AF24	3200 2600	-
183	4	AJ26	AP27	3200 2600 2000 1600 1000	-
184	4	AK26	AN27	3200 2600 2000 1600 1000	VREF
185	4	AE23	AM27	3200 1600	-
186	4	AL26	AP26	3200 2000 1000	-
187	4	AN26	AJ25	3200 2000 1000	VREF
188	4	AG24	AP25	3200 2600	-
189	4	AF23	AM26	3200 2600 2000 1600 1000	-
190	4	AJ24	AN25	3200 2600 2000 1600 1000	VREF
191	4	AE22	AM25	2600 1600 1000	-

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
270	6	AG2	AE7	2600 2000 1000	-
271	6	AG1	AF6	3200 2600 2000 1600 1000	VREF
272	6	AG4	AC9	2000 1600	-
273	6	AF3	AE6	3200 2600 2000 1600 1000	-
274	6	AF4	AF1	2600 1000	VREF
275	6	AF2	AB10	3200 2600 1600	-
276	6	AE1	AC8	3200 2600 1600 1000	-
277	6	AE3	AD5	3200 2600 2000 1600 1000	VREF
278	6	AD1	AC7	3200 2600 2000 1600 1000	-
279	6	AD2	AD6	3200 1600 1000	-
280	6	AC1	AB8	2000 1600 1000	VREF
281	6	AC2	AC5	3200 2600 2000 1600 1000	-
282	6	AC3	AA9	3200 2600 2000	-
283	6	AD4	AC4	2000 1000	-
284	6	AB6	AA8	3200 2600 1600 1000	-
285	6	Y10	AB1	2600 1600	-
286	6	AA7	AB2	3200 1600 1000	-
287	6	AA1	AA4	2600 2000 1000	VREF
288	6	AB4	Y9	3200 2600 2000 1600	-
289	6	Y8	AA2	3200 2600 2000 1600 1000	-

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
290	6	AA5	AA6	3200 2600 1600 1000	-
291	6	Y7	AB3	3200 2600 2000	-
292	6	W10	Y1	2600 2000 1000	-
293	6	Y2	Y5	2000 1600 1000	VREF
294	6	W2	W9	2000 1600	-
295	6	Y4	W7	3200 2600 2000 1600 1000	-
296	6	Y6	W1	1000	-
297	6	W3	W6	3200 1600	-
298	6	W4	V9	3200 2600 1600 1000	-
299	6	V1	W5	2000 1600 1000	VREF
300	6	U2	V7	2000 1600 1000	-
301	6	U1	V6	3200 2600 1600 1000	VREF
302	7	U4	U9	3200 2600 2000 1600 1000	-
303	7	U5	U7	3200 2600 1600 1000	VREF
304	7	U6	U3	2000 1600 1000	-
305	7	T6	T3	2000 1600 1000	VREF
306	7	T4	T9	3200 2600 1600 1000	-
307	7	R1	T5	3200 1600	-
308	7	T10	R6	1000	-
309	7	R5	R2	3200 2600 2000 1600 1000	-
310	7	P5	P1	2000 1600 1000	VREF