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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1536
Number of Logic Elements/Cells	6912
Total RAM Bits	131072
Number of I/O	316
Number of Gates	411955
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	432-LBGA Exposed Pad, Metal
Supplier Device Package	432-MBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv300e-6bg432i

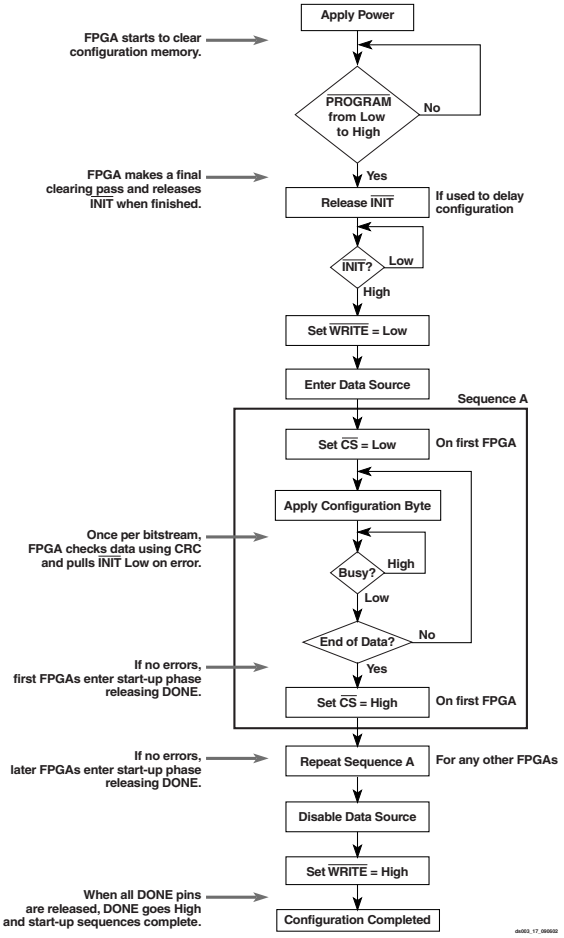

Figure 18: **SelectMAP Flowchart for Write Operations**

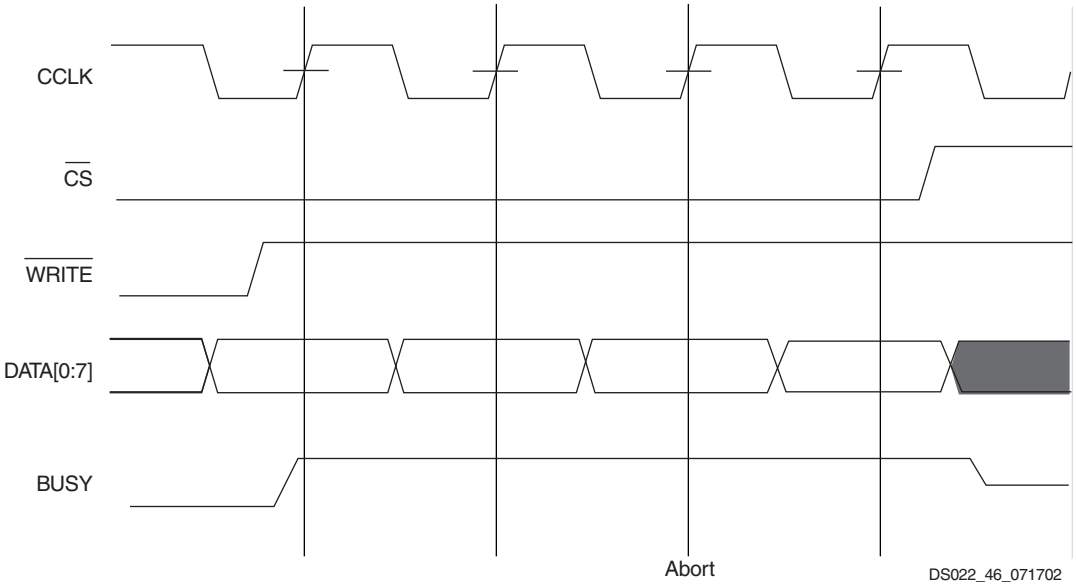

Figure 19: **SelectMAP Write Abort Waveforms**

Boundary Scan Mode

In the Boundary Scan mode, configuration is done through the IEEE 1149.1 Test Access Port. Note that the PROGRAM pin must be pulled High prior to reconfiguration. A Low on the PROGRAM pin resets the TAP controller and no JTAG operations can be performed.

ground. As the DLL delay taps reset to zero, glitches can occur on the DLL clock output pins. Activation of the RST pin can also severely affect the duty cycle of the clock output pins. Furthermore, the DLL output clocks no longer deskew with respect to one another. For these reasons, rarely use the reset pin unless re-configuring the device or changing the input frequency.

2x Clock Output — CLK2X

The output pin CLK2X provides a frequency-doubled clock with an automatic 50/50 duty-cycle correction. Until the CLKDLL has achieved lock, the CLK2X output appears as a 1x version of the input clock with a 25/75 duty cycle. This behavior allows the DLL to lock on the correct edge with respect to source clock. This pin is not available on the CLKDLLHF primitive.

Clock Divide Output — CLKDV

The clock divide output pin CLKDV provides a lower frequency version of the source clock. The CLKDV_DIVIDE property controls CLKDV such that the source clock is divided by N where N is either 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

This feature provides automatic duty cycle correction such that the CLKDV output pin always has a 50/50 duty cycle, with the exception of noninteger divides in HF mode, where the duty cycle is 1/3 for N=1.5 and 2/5 for N=2.5.

1x Clock Outputs — CLK[0|90|180|270]

The 1x clock output pin CLK0 represents a delay-compensated version of the source clock (CLKIN) signal. The CLKDLL primitive provides three phase-shifted versions of the CLK0 signal while CLKDLLHF provides only the 180 phase-shifted version. The relationship between phase shift and the corresponding period shift appears in Table 13.

Table 13: **Relationship of Phase-Shifted Output Clock to Period Shift**

Phase (degrees)	Period Shift (percent)
0	0%
90	25%
180	50%
270	75%

The timing diagrams in Figure 25 illustrate the DLL clock output characteristics.

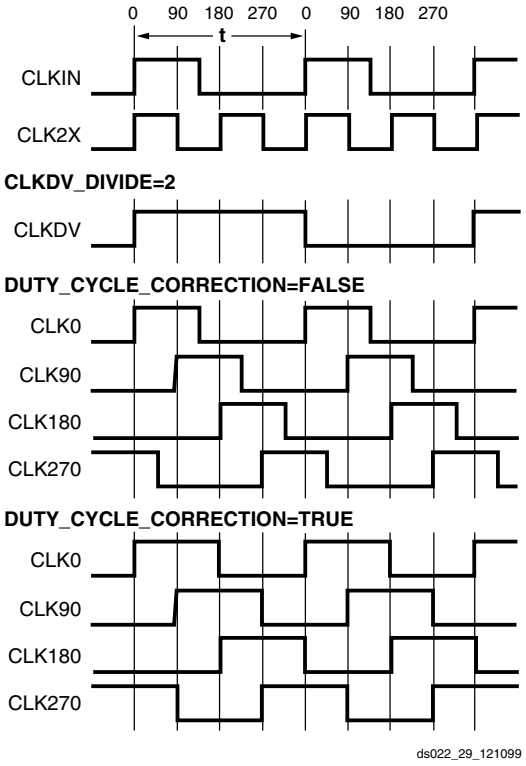

Figure 25: **DLL Output Characteristics**

The DLL provides duty cycle correction on all 1x clock outputs such that all 1x clock outputs by default have a 50/50 duty cycle. The DUTY_CYCLE_CORRECTION property (TRUE by default), controls this feature. In order to deactivate the DLL duty cycle correction, attach the DUTY_CYCLE_CORRECTION=FALSE property to the DLL symbol. When duty cycle correction deactivates, the output clock has the same duty cycle as the source clock.

The DLL clock outputs can drive an OBUF, a BUFG, or they can route directly to destination clock pins. The DLL clock outputs can only drive the BUFGs that reside on the same edge (top or bottom).

Locked Output — LOCKED

To achieve lock, the DLL might need to sample several thousand clock cycles. After the DLL achieves lock, the LOCKED signal activates. The DLL timing parameter section of the data sheet provides estimates for locking times.

To guarantee that the system clock is established prior to the device “waking up,” the DLL can delay the completion of the device configuration process until after the DLL locks. The STARTUP_WAIT property activates this feature.

Until the LOCKED signal activates, the DLL output clocks are not valid and can exhibit glitches, spikes, or other spurious movement. In particular the CLK2X output appears as a 1x clock with a 25/75 duty cycle.

The voltage reference signal is “banked” within the Virtex-E device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 38 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

IBUF placement restrictions require that any differential amplifier input signals within a bank be of the same standard. How to specify a specific location for the IBUF via the LOC property is described below. Table 19 summarizes the Virtex-E input standards compatibility requirements.

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element by default activates to ensure a zero hold-time requirement. The NODELAY=TRUE property overrides this default.

When the IBUF does not drive a flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

Table 19: **Xilinx Input Standards Compatibility Requirements**

Rule 1	Standards with the same input V_{CCO}, output V_{CCO}, and V_{REF} can be placed within the same bank.

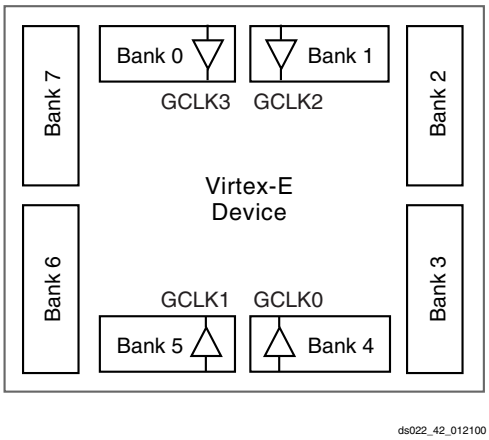

Figure 38: **Virtex-E I/O Banks**

IBUFG

Signals used as high fanout clock inputs to the Virtex-E device should drive a global clock input buffer (IBUFG) via an external input port in order to take advantage of one of the four dedicated global clock distribution networks. The output of the IBUFG should only drive a CLKDLL, CLKDLLHF, or BUFG symbol. The generic Virtex-E IBUFG symbol appears in Figure 39.

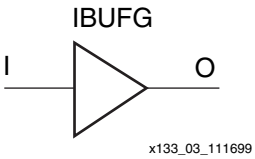

Figure 39: **Virtex-E Global Clock Input Buffer (IBUFG) Symbol**

The extension to the base name determines which I/O standard is used by the IBUFG. With no extension specified for the generic IBUFG symbol, the assumed standard is LVTTL.

The following list details variations of the IBUFG symbol.

- IBUFG
- IBUFG_LVCMOS2
- IBUFG_PCI33_3
- IBUFG_PCI66_3
- IBUFG_GTL
- IBUFG_GTLP
- IBUFG_HSTL_I
- IBUFG_HSTL_III
- IBUFG_HSTL_IV
- IBUFG_SSTL3_I
- IBUFG_SSTL3_II
- IBUFG_SSTL2_I
- IBUFG_SSTL2_II
- IBUFG_CTT
- IBUFG_AGP
- IBUFG_LVCMOS18
- IBUFG_LVDS
- IBUFG_LVPECL

When the IBUFG symbol supports an I/O standard that requires a differential amplifier input, the IBUFG automatically configures as a differential amplifier input buffer. The low-voltage I/O standards with a differential amplifier input require an external reference voltage input V_{REF}.

The voltage reference signal is “banked” within the Virtex-E device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 38 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

IBUFG placement restrictions require any differential amplifier input signals within a bank be of the same standard. The LOC property can specify a location for the IBUFG.

As an added convenience, the BUFGP can be used to instantiate a high fanout clock input. The BUFGP symbol

represents a combination of the LVTTL IBUFG and BUFG symbols, such that the output of the BUFGP can connect directly to the clock pins throughout the design.

Unlike previous architectures, the Virtex-E BUFGP symbol can only be placed in a global clock pad location. The LOC property can specify a location for the BUFGP.

OBUF

An OBUF must drive outputs through an external output port. The generic output buffer (OBUF) symbol appears in Figure 40.

The extension to the base name defines which I/O standard the OBUF uses. With no extension specified for the generic OBUF symbol, the assumed standard is slew rate limited LVTTL with 12 mA drive strength.

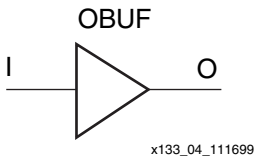

Figure 40: **Virtex-E Output Buffer (OBUF) Symbol**

The LVTTL OBUF additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL output buffers have selectable drive strengths.

The format for LVTTL OBUF symbol names is as follows:

OBUF_<slew_rate>_<drive_strength>

where <slew_rate> is either F (Fast) or S (Slow), and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

The following list details variations of the OBUF symbol.

- OBUF
- OBUF_S_2
- OBUF_S_4
- OBUF_S_6
- OBUF_S_8
- OBUF_S_12
- OBUF_S_16
- OBUF_S_24
- OBUF_F_2
- OBUF_F_4
- OBUF_F_6
- OBUF_F_8
- OBUF_F_12
- OBUF_F_16
- OBUF_F_24
- OBUF_LVCMOS2
- OBUF_PCI33_3
- OBUF_PCI66_3
- OBUF_GTL
- OBUF_GTLP
- OBUF_HSTL_I
- OBUF_HSTL_III
- OBUF_HSTL_IV
- OBUF_SSTL3_I
- OBUF_SSTL3_II
- OBUF_SSTL2_I
- OBUF_SSTL2_II
- OBUF_CTT
- OBUF_AGP
- OBUF_LVCMOS18
- OBUF_LVDS
- OBUF_LVPECL

The Virtex-E series supports eight banks for the HQ and PQ packages. The CS packages support four V_{CCO} banks.

OBUF placement restrictions require that within a given V_{CCO} bank each OBUF share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within any V_{CCO} bank. Table 20 summarizes the Virtex-E output compatibility requirements. The LOC property can specify a location for the OBUF.

Table 20: **Output Standards Compatibility Requirements**

Rule 1	Only outputs with standards that share compatible V_{CCO} can be used within the same bank.
Rule 2	There are no placement restrictions for outputs with standards that do not require a V_{CCO}.
V_{CCO}	Compatible Standards
3.3	LVTTL, SSTL3_I, SSTL3_II, CTT, AGP, GTL, GTL+, PCI33_3, PCI66_3
2.5	SSTL2_I, SSTL2_II, LVCMOS2, GTL, GTL+
1.5	HSTL_I, HSTL_III, HSTL_IV, GTL, GTL+

OBUFT

The generic 3-state output buffer OBUFT (see Figure 41) typically implements 3-state outputs or bidirectional I/O.

The extension to the base name defines which I/O standard OBUFT uses. With no extension specified for the generic OBUFT symbol, the assumed standard is slew rate limited LVTTL with 12 mA drive strength.

The LVTTL OBUFT additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

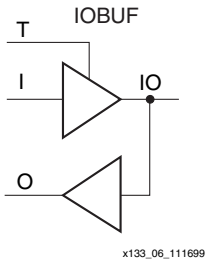

Figure 42: **Input/Output Buffer Symbol (IOBUF)**

The following list details variations of the IOBUF symbol.

- IOBUF
- IOBUF_S_2
- IOBUF_S_4
- IOBUF_S_6
- IOBUF_S_8
- IOBUF_S_12
- IOBUF_S_16
- IOBUF_S_24
- IOBUF_F_2
- IOBUF_F_4
- IOBUF_F_6
- IOBUF_F_8
- IOBUF_F_12
- IOBUF_F_16
- IOBUF_F_24
- IOBUF_LVCMOS2
- IOBUF_PCI33_3
- IOBUF_PCI66_3
- IOBUF_GTL
- IOBUF_GTLP
- IOBUF_HSTL_I
- IOBUF_HSTL_III
- IOBUF_HSTL_IV
- IOBUF_SSTL3_I
- IOBUF_SSTL3_II
- IOBUF_SSTL2_I
- IOBUF_SSTL2_II
- IOBUF_CTT
- IOBUF_AGP
- IOBUF_LVCMOS18
- IOBUF_LVDS
- IOBUF_LVPECL

When the IOBUF symbol used supports an I/O standard that requires a differential amplifier input, the IOBUF automatically configures with a differential amplifier input buffer.

The low-voltage I/O standards with a differential amplifier input require an external reference voltage input V_{REF}.

The voltage reference signal is “banked” within the Virtex-E device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 38, page 34 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

IOBUF placement restrictions require any differential amplifier input signals within a bank be of the same standard.

The Virtex-E series supports eight banks for the HQ and PQ packages. The CS package supports four V_{CCO} banks.

Additional restrictions on the Virtex-E SelectI/O IOBUF placement require that within a given V_{CCO} bank each IOBUF must share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within the same V_{CCO} bank. The LOC property can specify a location for the IOBUF.

An optional delay element is associated with the input path in each IOBUF. When the IOBUF drives an input flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Override this default with the NODELAY=TRUE property.

In the case when the IOBUF does not drive an input flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak “keeper” circuit. Control this feature by adding the appropriate symbol to the output net of the IOBUF (PULLUP, PULLDOWN, or KEEPER).

SelectI/O Properties

Access to some of the SelectI/O features (for example, location constraints, input delay, output drive strength, and slew rate) is available through properties associated with these features.

Input Delay Properties

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Use the NODELAY=TRUE property to override this default.

In the case when the IBUF does not drive a flip-flop within the IOB, the delay element by default de-activates to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

Optional N-side

Some designers might prefer to also instantiate the N-side buffer for the global clock buffer. This allows the top-level net list to include net connections for both PCB layout and system-level integration. In this case, only the output P-side IBUFG connection has a net connected to it. Since the N-side IBUFG does not have a connection in the EDIF net list, it is trimmed from the design in MAP.

VHDL Instantiation

```
gclk0_p : IBUFG_LVDS port map
(I=>clk_p_external, O=>clk_internal);

gclk0_n : IBUFG_LVDS port map
(I=>clk_n_external, O=>clk_internal);
```

Verilog Instantiation

```
IBUFG_LVDS gclk0_p (.I(clk_p_external),
.O(clk_internal));

IBUFG_LVDS gclk0_n (.I(clk_n_external),
.O(clk_internal));
```

Location Constraints

All LVDS buffers must be explicitly placed on a device. For the global clock input buffers this can be done with the following constraint in the .ucf or .ncf file.

```
NET clk_p_external LOC = GCLKPAD3;

NET clk_n_external LOC = C17;
```

GCLKPAD3 can also be replaced with the package pin name, such as D17 for the BG432 package.

Creating LVDS Input Buffers

An LVDS input buffer can be placed in a wide number of IOB locations. The exact location is dependent on the package that is used. The Virtex-E package information lists the possible locations as IO_L#P for the P-side and IO_L#N for the N-side where # is the pair number.

HDL Instantiation

Only one input buffer is required to be instantiated in the design and placed on the correct IO_L#P location. The N-side of the buffer is reserved and no other IOB is allowed to be placed on this location. In the physical device, a configuration option is enabled that routes the pad wire from the IO_L#N IOB to the differential input buffer located in the IO_L#P IOB. The output of this buffer then drives the output of the IO_L#P cell or the input register in the IO_L#P IOB. In EPIC it appears that the second buffer is unused. Any attempt to use this location for another purpose leads to a DRC error in the software.

VHDL Instantiation

```
data0_p : IBUF_LVDS port map (I=>data(0),
O=>data_int(0));
```

Verilog Instantiation

```
IBUF_LVDS data0_p (.I(data[0]),
.O(data_int[0]));
```

Location Constraints

All LVDS buffers must be explicitly placed on a device. For the input buffers this can be done with the following constraint in the .ucf or .ncf file.

```
NET data<0> LOC = D28; # IO_L0P
```

Optional N-side

Some designers might prefer to also instantiate the N-side buffer for the input buffer. This allows the top-level net list to include net connections for both PCB layout and system-level integration. In this case, only the output P-side IBUF connection has a net connected to it. Since the N-side IBUF does not have a connection in the EDIF net list, it is trimmed from the design in MAP.

VHDL Instantiation

```
data0_p : IBUF_LVDS port map
(I=>data_p(0), O=>data_int(0));

data0_n : IBUF_LVDS port map
(I=>data_n(0), O=>open);
```

Verilog Instantiation

```
IBUF_LVDS data0_p (.I(data_p[0]),
.O(data_int[0]));

IBUF_LVDS data0_n (.I(data_n[0]), .O());
```

Location Constraints

All LVDS buffers must be explicitly placed on a device. For the global clock input buffers this can be done with the following constraint in the .ucf or .ncf file.

```
NET data_p<0> LOC = D28; # IO_L0P

NET data_n<0> LOC = B29; # IO_L0N
```

Adding an Input Register

All LVDS buffers can have an input register in the IOB. The input register is in the P-side IOB only. All the normal IOB register options are available (FD, FDE, FDC, FDCE, FDP, FDPE, FDR, FDRE, FDS, FDSE, LD, LDE, LDC, LDCE, LDP, LDPE). The register elements can be inferred or explicitly instantiated in the HDL code.

The register elements can be packed in the IOB using the IOB property to TRUE on the register or by using the “map -pr [i|o|b]” where “i” is inputs only, “o” is outputs only and “b” is both inputs and outputs.

To improve design coding times VHDL and Verilog synthesis macro libraries available to explicitly create these structures. The input library macros are listed in Table 42. The I and IB inputs to the macros are the external net connections.

The register elements can be packed in the IOB using the IOB property to TRUE on the register or by using the “map -pr [i|o|b]” where “i” is inputs only, “o” is outputs only and “b” is both inputs and outputs.

To improve design coding times VHDL and Verilog synthesis macro libraries have been developed to explicitly create these structures. The input library macros are listed below. The 3-state is configured to be 3-stated at GSR and when the PRE,CLR,S or R is asserted and shares it's clock enable with the output register. If this is not desirable then the library can be updated by the user for the desired functionality. The O and OB inputs to the macros are the external net connections.

Creating a LVDS Bidirectional Buffer

LVDS bidirectional buffers can be placed in a wide number of IOB locations. The exact locations are dependent on the package used. The Virtex-E package information lists the possible locations as IO_L#P for the P-side and IO_L#N for the N-side, where # is the pair number.

HDL Instantiation

Both bidirectional buffers are required to be instantiated in the design and placed on the correct IO_L#P and IO_L#N locations. The IOB must have the same net source the following pins, clock (C), set/reset (SR), 3-state (T), 3-state clock enable (TCE), output (O), output clock enable (OCE). In addition, the output (O) pins must be inverted with respect to each other, and if output registers are used, the INIT states must be opposite values (one HIGH and one LOW). If 3-state registers are used, they must be initialized to the same state. Failure to follow these rules leads to DRC errors in the software.

VHDL Instantiation

```
data0_p:   IOBUF_LVDS port map
(I=>data_out(0), T=>data_tri,
IO=>data_p(0), O=>data_int(0));

data0_inv: INV        port map
(I=>data_out(0),   O=>data_n_out(0));

data0_n  : IOBUF_LVDS port map
(I=>data_n_out(0), T=>data_tri,
IO=>data_n(0), O=>open);
```

Verilog Instantiation

```
IOBUF_LVDS data0_p(.I(data_out[0]),
.T(data_tri), .IO(data_p[0]),
.O(data_int[0]);

INV        data0_inv (.I(data_out[0],
.O(data_n_out[0]);

IOBUF_LVDS
data0_n(.I(data_n_out[0]),.T(data_tri),.
IO(data_n[0]).O());
```

Location Constraints

All LVDS buffers must be explicitly placed on a device. For the output buffers this can be done with the following constraint in the .ucf or .ncf file.

```
NET data_p<0> LOC = D28; # IO_L0P

NET data_n<0> LOC = B29; # IO_L0N
```

Synchronous vs. Asynchronous Bidirectional Buffers

If the output side of the bidirectional buffers are synchronous (registered in the IOB), then any IO_L#PIN pair can be used. If the output side of the bidirectional buffers are asynchronous (no output register), then they must use one of the pairs that is a part of the asynchronous LVDS IOB group. This applies for either the 3-state pin or the data out pin.

The LVDS pairs that can be used as asynchronous bidirectional buffers are listed in the Virtex-E pinout tables. Some pairs are marked as asynchronous capable for all devices in that package, and others are marked as available only for that device in the package. If the device size might change at some point in the product’s lifetime, then only the common pairs for all packages should be used.

Adding Output and 3-State Registers

All LVDS buffers can have an output and input registers in the IOB. The output registers must be in both the P-side and N-side IOBs, the input register is only in the P-side. All the normal IOB register options are available (FD, FDE, FDC, FDCE, FDP, FDPE, FDR, FDRE, FDS, FDSE, LD, LDE, LDC, LDCE, LDP, LDPE). The register elements can be inferred or explicitly instantiated in the HDL code. Special care must be taken to insure that the D pins of the registers are inverted and that the INIT states of the registers are opposite. The 3-state (T), 3-state clock enable (CE), clock pin (C), output clock enable (CE), and set/reset (CLR/PRE or S/R) pins must connect to the same source. Failure to do this leads to a DRC error in the software.

The register elements can be packed in the IOB using the IOB property to TRUE on the register or by using the “map -pr [i|o|b]” where “i” is inputs only, “o” is outputs only and “b” is both inputs and outputs. To improve design coding times VHDL and Verilog synthesis macro libraries have been developed to explicitly create these structures. The bidirectional I/O library macros are listed in Table 44. The 3-state is configured to be 3-stated at GSR and when the PRE,CLR,S or R is asserted and shares its clock enable with the output and input register. If this is not desirable then the library can be updated be the user for the desired functionality. The I/O and IOB inputs to the macros are the external net connections.

Virtex-E Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation net list. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Virtex-E devices unless otherwise noted.

IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVTTL levels in Table 2. For other standards, adjust the delays with the values shown in **IOB Input Switching Characteristics Standard Adjustments**, page 8.

Table 2: **IOB Input Switching Characteristics**

			Speed Grade(1)				
Description(2)	**Symbol**	**Device**	**Min**	**-8**	**-7**	**-6**	**Units**
Propagation Delays							
Pad to I output, no delay	T_{IOPI}	All	0.43	0.8	0.8	0.8	ns, max
Pad to I output, with delay	T_{IOPID}	XCV50E	0.51	1.0	1.0	1.0	ns, max
		XCV100E	0.51	1.0	1.0	1.0	ns, max
		XCV200E	0.51	1.0	1.0	1.0	ns, max
		XCV300E	0.51	1.0	1.0	1.0	ns, max
		XCV400E	0.51	1.0	1.0	1.0	ns, max
		XCV600E	0.51	1.0	1.0	1.0	ns, max
		XCV1000E	0.55	1.1	1.1	1.1	ns, max
		XCV1600E	0.55	1.1	1.1	1.1	ns, max
		XCV2000E	0.55	1.1	1.1	1.1	ns, max
		XCV2600E	0.55	1.1	1.1	1.1	ns, max
		XCV3200E	0.55	1.1	1.1	1.1	ns, max
Pad to output IQ via transparent latch, no delay	T_{IOPLI}	All	0.8	1.4	1.5	1.6	ns, max
Pad to output IQ via transparent latch, with delay	T_{IOPLID}	XCV50E	1.31	2.9	3.0	3.1	ns, max
		XCV100E	1.31	2.9	3.0	3.1	ns, max
		XCV200E	1.39	3.1	3.2	3.3	ns, max
		XCV300E	1.39	3.1	3.2	3.3	ns, max
		XCV400E	1.43	3.2	3.3	3.4	ns, max
		XCV600E	1.55	3.5	3.6	3.7	ns, max
		XCV1000E	1.55	3.5	3.6	3.7	ns, max
		XCV1600E	1.59	3.6	3.7	3.8	ns, max
		XCV2000E	1.59	3.6	3.7	3.8	ns, max
		XCV2600E	1.59	3.6	3.7	3.8	ns, max
		XCV3200E	1.59	3.6	3.7	3.8	ns, max

IOB Output Switching Characteristics, Figure 1

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 10.

Description[2]	Symbol	Speed Grade[1]				Units
		Min	-8	-7	-6	
Propagation Delays						
O input to Pad	T_{IOOP}	1.04	2.5	2.7	2.9	ns, max
O input to Pad via transparent latch	T_{IOOLP}	1.24	2.9	3.1	3.4	ns, max
3-State Delays						
T input to Pad high-impedance (Note 2)	T_{IOTHZ}	0.73	1.5	1.7	1.9	ns, max
T input to valid data on Pad	T_{IOTON}	1.13	2.7	2.9	3.1	ns, max
T input to Pad high-impedance via transparent latch (Note 2)	$T_{IOTLPHZ}$	0.86	1.8	2.0	2.2	ns, max
T input to valid data on Pad via transparent latch	$T_{IOTLPON}$	1.26	3.0	3.2	3.4	ns, max
GTS to Pad high impedance (Note 2)	T_{GTS}	1.94	4.1	4.6	4.9	ns, max
Sequential Delays						
Clock CLK						
Minimum Pulse Width, High	T_{CH}	0.56	1.2	1.3	1.4	ns, min
Minimum Pulse Width, Low	T_{CL}	0.56	1.2	1.3	1.4	ns, min
Clock CLK to Pad	T_{IOCKP}	0.97	2.4	2.8	2.9	ns, max
Clock CLK to Pad high-impedance (synchronous) (Note 2)	T_{IOCKHZ}	0.77	1.6	2.0	2.2	ns, max
Clock CLK to valid data on Pad (synchronous)	T_{IOCKON}	1.17	2.8	3.2	3.4	ns, max
Setup and Hold Times before/after Clock CLK						
O input	T_{IOOCK} / T_{IOCKO}	0.43 / 0	0.9 / 0	1.0 / 0	1.1 / 0	ns, min
OCE input	$T_{IOOCECK}$ / $T_{IOCKOCE}$	0.28 / 0	0.55 / 0.01	0.7 / 0	0.7 / 0	ns, min
SR input (OFF)	$T_{IOSRCKO}$ / $T_{IOCKOSR}$	0.40 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
3-State Setup Times, T input	T_{IOTCK} / T_{IOCKT}	0.26 / 0	0.51 / 0	0.6 / 0	0.7 / 0	ns, min
3-State Setup Times, TCE input	$T_{IOTCECK}$ / $T_{IOCKTCE}$	0.30 / 0	0.6 / 0	0.7 / 0	0.8 / 0	ns, min
3-State Setup Times, SR input (TFF)	$T_{IOSRCKT}$ / $T_{IOCKTSR}$	0.38 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
Set/Reset Delays						
SR input to Pad (asynchronous)	T_{IOSRP}	1.30	3.1	3.3	3.5	ns, max
SR input to Pad high-impedance (asynchronous) (Note 2)	T_{IOSRHZ}	1.08	2.2	2.4	2.7	ns, max
SR input to valid data on Pad (asynchronous)	T_{IOSRON}	1.48	3.4	3.7	3.9	ns, max
GSR to Pad	T_{IOGSRQ}	3.88	7.6	8.5	9.7	ns, max

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. 3-state turn-off delays should not be adjusted.

Pinout Differences Between Virtex and Virtex-E Families

The same device in the same package for the Virtex-E and Virtex families are pin-compatible with some minor exceptions, listed in Table 1.

XCV200E Device, FG456 Package

The Virtex-E XCV200E has two I/O pins swapped with the Virtex XCV200 to accommodate differential clock pairing.

XCV400E Device, FG676 Package

The Virtex-E XCV400E has two I/O pins swapped with the Virtex XCV400 to accommodate differential clock pairing.

All Devices, PQ240 and HQ240 Packages

The Virtex devices in PQ240 and HQ240 packages do not have V_{CCO} banking, but Virtex-E devices do. To achieve this, eight Virtex I/O pins (P232, P207, P176, P146, P116, P85, P55, and P25) are now VCCO pins in the Virtex-E family. This change also requires one Virtex I/O or VREF pin to be swapped with a standard I/O pin.

Additionally, accommodating differential clock input pairs in Virtex-E caused some IO_V_{REF} differences in the XCV400E and XCV600E devices only. Virtex IO_V_{REF} pins P215 and P87 are Virtex-E IO_V_{REF} pins P216 and P86, respectively. Virtex-E pins P215 and P87 are IO_DLL.

Table 1: **Pinout Differences Summary**

Part	Package	Pins	Virtex	Virtex-E
XCV200	FG456	E11, U11	I/O	No Connect
		B11, AA11	No Connect	IO_LVDS_DLL
XCV400	FG676	D13, Y13	I/O	No Connect
		B13, AF13	No Connect	IO_LVDS_DLL
XCV400/600	PQ240/HQ240	P215, P87	IO_V_{REF}	IO_LVDS_DLL
		P216, P86	I/O	IO_V_{REF}
All	PQ240/HQ240	P232, P207, P176, P146, P116, P85, P55, and P25	I/O	V_{CCO}
		P231	I/O	IO_V_{REF}

PQ240 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 7: **PQ240 Differential Pin Pair Summary XCV50E, XCV100E, XCV200E, XCV300E, XCV400E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	P92	P93	NA	IO_DLL_L40P
1	5	P89	P87	NA	IO_DLL_L40N
2	1	P210	P209	NA	IO_DLL_L6P
3	0	P213	P215	NA	IO_DLL_L6N
IO LVDS Total Pairs: 64, Asynchronous Outputs Pairs: 27					
0	0	P236	P237	1	VREF
1	0	P234	P235	√	-
2	0	P228	P229	√	VREF
3	0	P223	P224	√	-
4	0	P220	P221	3	-
5	0	P217	P218	3	VREF
6	1	P209	P215	NA	IO_LVDS_DLL
7	1	P205	P206	3	VREF
8	1	P202	P203	3	-
9	1	P199	P200	√	-
10	1	P194	P195	√	VREF
11	1	P191	P192	√	VREF
12	1	P188	P189	√	-
13	1	P186	P187	1	VREF
14	1	P184	P185	√	CS
15	2	P178	P177	√	DIN, D0
16	2	P174	P173	2	-
17	2	P171	P170	3	VREF
18	2	P168	P167	4	D1, VREF
19	2	P163	P162	√	D2
20	2	P160	P159	2	-
21	2	P157	P156	4	D3, VREF
22	2	P155	P154	5	VREF
23	2	P153	P152	√	-
24	3	P145	P144	4	D4, VREF
25	3	P142	P141	2	-
26	3	P139	P138	√	D5
27	3	P134	P133	4	VREF
28	3	P131	P130	3	VREF
29	3	P128	P127	2	-
30	3	P126	P125	6	VREF
31	3	P124	P123	√	INIT
32	4	P118	P117	√	-
33	4	P114	P113	√	-
34	4	P111	P110	√	VREF
35	4	P108	P107	√	VREF
36	4	P103	P102	√	-
37	4	P100	P99	3	-
38	4	P97	P96	3	VREF
39	4	P95	P94	7	VREF
40	5	P93	P87	NA	IO_LVDS_DLL
41	5	P84	P82	8	VREF
42	5	P79	P78	√	-
43	5	P74	P73	√	VREF
44	5	P71	P70	√	VREF
45	5	P68	P67	√	-
46	5	P66	P65	1	VREF
47	5	P64	P63	√	-

BG352 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A check (√) in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock

Table 11: **BG352 Differential Pin Pair Summary XCV100E, XCV200E, XCV300E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	AE13	AC13	NA	IO LVDS 55
1	5	AF14	AD14	NA	IO LVDS 55
2	1	B14	A13	NA	IO LVDS 9
3	0	D14	A15	NA	IO LVDS 9
IO LVDS Total Outputs: 87, Asynchronous Output Pairs: 43					
0	0	B23	D21	√	VREF_0
1	0	D20	A23	√	-
2	0	B22	C21	√	VREF_0
3	0	A21	B20	2	-
4	0	B19	C19	√	VREF_0
5	0	C18	D17	√	-
6	0	A18	C17	2	-
7	0	C16	B17	√	-
8	0	D15	A16	√	VREF_0
9	1	A13	A15	√	GCLK LVDS 3/2
10	1	A12	C13	2	-
11	1	C12	B12	√	VREF_1
12	1	B11	A11	√	-
13	1	D11	C11	2	-
14	1	C10	B9	√	-
15	1	C9	B8	√	VREF_1
16	1	A7	D9	1	-
17	1	B6	A6	√	VREF_1
18	1	A4	C7	√	-

Table 11: **BG352 Differential Pin Pair Summary XCV100E, XCV200E, XCV300E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
19	1	D6	C6	√	VREF_1
20	1	C4	D5	√	CS
21	2	E4	D3	√	DIN_D0
22	2	D2	C1	√	VREF_2
23	2	G4	F3	√	-
24	2	E2	F2	√	VREF_2
25	2	F1	J4	2	-
26	2	H2	G1	√	D1
27	2	J3	J2	√	D2
28	2	J1	L4	1	-
29	2	L3	L2	√	-
30	2	M4	M3	√	D3
31	2	M2	M1	2	-
32	2	N4	N2	√	-
33	3	R1	R2	2	-
34	3	R3	R4	√	VREF_3
35	3	T2	U2	√	-
36	3	T4	V1	1	-
37	3	U3	U4	√	D5
38	3	V3	V4	√	VREF_3
39	3	Y1	Y2	1	-
40	3	AA2	Y3	√	VREF_3
41	3	AC1	AB2	√	-
42	3	AA4	AC2	√	VREF_3
43	3	AC3	AD2	√	INIT
44	4	AC5	AD4	√	-
45	4	AE4	AF3	√	VREF_4
46	4	AC7	AD6	√	-
47	4	AE5	AE6	√	VREF_4
48	4	AF6	AC9	2	-
49	4	AE8	AF7	√	VREF_4
50	4	AD9	AE9	√	-
51	4	AF9	AC11	2	-
52	4	AD11	AE11	√	-
53	4	AC12	AD12	√	VREF_4
54	4	AE12	AF12	2	-

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
NA	NC	L2
NA	NC	F6
NA	NC	F25
NA	NC	F21
NA	NC	F2
NA	NC	C26
NA	NC	C25
NA	NC	C2
NA	NC	C1
NA	NC	B6
NA	NC	B26
NA	NC	B24
NA	NC	B21
NA	NC	B16
NA	NC	B11
NA	NC	B1
NA	NC	AF25
NA	NC	AF24
NA	NC	AF2
NA	NC	AE6
NA	NC	AE3
NA	NC	AE26
NA	NC	AE24
NA	NC	AE21
NA	NC	AE16
NA	NC	AE14
NA	NC	AE11
NA	NC	AE1
NA	NC	AD25
NA	NC	AD2
NA	NC	AD1
NA	NC	AA6
NA	NC	AA25
NA	NC	AA21
NA	NC	AA2
NA	NC	A3
NA	NC	A25

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
NA	NC	A2
NA	NC	A15
NA	VCCINT	G7
NA	VCCINT	G20
NA	VCCINT	H8
NA	VCCINT	H19
NA	VCCINT	J9
NA	VCCINT	J10
NA	VCCINT	J11
NA	VCCINT	J16
NA	VCCINT	J17
NA	VCCINT	J18
NA	VCCINT	K9
NA	VCCINT	K18
NA	VCCINT	L9
NA	VCCINT	L18
NA	VCCINT	T9
NA	VCCINT	T18
NA	VCCINT	U9
NA	VCCINT	U18
NA	VCCINT	V9
NA	VCCINT	V10
NA	VCCINT	V11
NA	VCCINT	V16
NA	VCCINT	V17
NA	VCCINT	V18
NA	VCCINT	Y7
NA	VCCINT	Y20
NA	VCCINT	W8
NA	VCCINT	W19
0	VCCO	J13
0	VCCO	J12
0	VCCO	H9
0	VCCO	H12
0	VCCO	H11

Table 21: **FG676 Differential Pin Pair Summary XCV400E, XCV600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
52	2	G24	H22	√	-
53	2	J21	G25	2	-
54	2	G26	J22	1	VREF
55	2	H24	J23	√	-
56	2	J24	K20	√	VREF
57	2	K22	K21	√	D2
58	2	H25	K23	√	-
59	2	L20	J26	2	-
60	2	K25	L22	1	-
61	2	L21	L23	1	-
62	2	M20	L24	1	-
63	2	M23	M22	√	D3
64	2	L26	M21	√	-
65	2	N19	M24	2	-
66	2	M26	N20	1	VREF
67	2	N24	N21	√	-
68	2	N23	N22	√	-
69	3	P21	P23	√	-
70	3	P22	R25	1	VREF
71	3	P19	P20	2	-
72	3	R21	R22	√	-
73	3	R24	R23	√	VREF
74	3	T24	R20	1	-
75	3	T22	U24	1	-
76	3	T23	U25	1	-
77	3	T21	U20	2	-
78	3	U22	V26	√	-
79	3	T20	U23	√	D5
80	3	V24	U21	√	VREF
81	3	V23	W24	√	-
82	3	V22	W26	1	VREF
83	3	Y25	V21	2	-
84	3	V20	AA26	√	-
85	3	Y24	W23	√	VREF

Table 21: **FG676 Differential Pin Pair Summary XCV400E, XCV600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
86	3	AA24	Y23	1	-
87	3	AB26	W21	2	-
88	3	Y22	W22	1	VREF
89	3	AA23	AB24	2	-
90	3	W20	AC24	√	-
91	3	AB23	Y21	√	INIT
92	4	AC22	AD26	√	-
93	4	AD23	AA20	1	-
94	4	Y19	AC21	√	-
95	4	AD22	AB20	√	VREF
96	4	AE22	Y18	NA	-
97	4	AF22	AA19	NA	-
98	4	AD21	AB19	√	VREF
99	4	AC20	AA18	√	-
100	4	AC19	AD20	1	-
101	4	AF20	AB18	1	VREF
102	4	AD19	Y17	NA	-
103	4	AE19	AD18	NA	VREF
104	4	AF19	AA17	√	-
105	4	AC17	AB17	1	-
106	4	Y16	AE17	√	-
107	4	AF17	AA16	√	-
108	4	AD17	AB16	NA	-
109	4	AC16	AD16	√	-
110	4	AC15	Y15	√	VREF
111	4	AD15	AA15	√	-
112	4	W14	AB15	1	-
113	4	AF15	Y14	1	VREF
114	4	AD14	AB14	NA	-
115	5	AC14	AF13	NA	IO_LVDS_DLL
116	5	AA13	AF12	1	VREF
117	5	AC13	W13	1	-
118	5	AA12	AD12	√	-
119	5	AC12	AB12	√	VREF

Table 23: **FG680 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
120	3	AN4	AT1	4	-
121	3	AR2	AP4	4	VREF
122	3	AT2	AR3	6	-
123	3	AR4	AU2	√	INIT
124	4	AU4	AV5	√	-
125	4	AT6	AV4	5	-
126	4	AU6	AW4	5	VREF
127	4	AT7	AW5	√	-
128	4	AU7	AV6	√	VREF
129	4	AT8	AW6	3	-
130	4	AU8	AV7	3	-
131	4	AT9	AW7	√	-
132	4	AV8	AU9	√	VREF
133	4	AW8	AT10	5	-
134	4	AV9	AU10	5	VREF
135	4	AW9	AT11	√	-
136	4	AV10	AU11	√	VREF
137	4	AW10	AU12	2	-
138	4	AV11	AT13	2	-
139	4	AW11	AU13	√	VREF
140	4	AT14	AV12	√	-
141	4	AU14	AW12	5	-
142	4	AT15	AV13	5	-
143	4	AU15	AW13	√	-
144	4	AV14	AT16	√	VREF
145	4	AW14	AU16	3	-
146	4	AV15	AR17	3	-
147	4	AW15	AT17	√	-
148	4	AU17	AV16	√	VREF
149	4	AR18	AW16	5	-
150	4	AT18	AV17	5	-
151	4	AU18	AW17	√	-
152	4	AT19	AV18	√	VREF
153	4	AU19	AW18	2	-

Table 23: **FG680 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
154	4	AU21	AV19	2	VREF
155	5	AT21	AT22	NA	IO_LVDS_DLL
156	5	AV20	AR22	8	VREF
157	5	AV23	AW21	√	VREF
158	5	AU23	AV21	√	-
159	5	AT23	AW22	5	-
160	5	AR23	AV22	5	-
161	5	AV24	AW23	√	VREF
162	5	AW24	AU24	√	-
163	5	AW25	AT24	3	-
164	5	AV25	AU25	3	-
165	5	AW26	AT25	√	VREF
166	5	AV26	AW27	√	-
167	5	AU26	AV27	5	-
168	5	AT26	AW28	5	-
169	5	AU27	AV28	√	-
170	5	AW29	AT27	√	VREF
171	5	AW30	AU28	2	-
172	5	AV30	AV29	2	-
173	5	AW31	AU29	√	VREF
174	5	AV31	AT29	√	-
175	5	AW32	AU30	5	VREF
176	5	AW33	AT30	5	-
177	5	AV33	AU31	√	VREF
178	5	AT31	AW34	√	-
179	5	AV32	AV34	3	-
180	5	AU32	AW35	3	-
181	5	AT32	AV35	√	VREF
182	5	AU33	AW36	√	-
183	5	AT33	AV36	5	VREF
184	5	AU34	AU36	5	-
185	6	AT38	AR36	√	-
186	6	AP36	AR38	6	-
187	6	AP37	AT39	4	VREF

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
1	IO_L57N_Y	D9
1	IO_VREF_L57P_Y	A12[2]
1	IO_L58N_Y	E9
1	IO_L58P_Y	C12
1	IO_L59N_YY	B12
1	IO_VREF_L59P_YY	D8
1	IO_L60N_YY	A11
1	IO_L60P_YY	E8
1	IO_L61N_Y	C7
1	IO_L61P_Y	A10
1	IO_L62N_Y	C6
1	IO_L62P_Y	B10
1	IO_L63N_YY	A9
1	IO_VREF_L63P_YY	B9
1	IO_L64N_YY	A8
1	IO_L64P_YY	E7
1	IO_L65N_Y	B8
1	IO_L65P_Y	C5
1	IO_L66N_Y	A7
1	IO_VREF_L66P_Y	A6
1	IO_L67N_Y	B7
1	IO_L67P_Y	D6
1	IO_L68N_Y	A5
1	IO_L68P_Y	C4
1	IO_WRITE_L69N_YY	B6
1	IO_CS_L69P_YY	E6
2	IO	H2
2	IO	H3
2	IO	J1
2	IO	K5
2	IO	M2
2	IO	N1
2	IO	R5
2	IO	U1
2	IO	U4
2	IO	W3
2	IO	Y3
2	IO	AA3
2	IO_DOUT_BUSY_L70P_YY	F5
2	IO_DIN_D0_L70N_YY	D2
2	IO_L71P_Y	E4
2	IO_L71N_Y	E2
2	IO_L72P_Y	D3
2	IO_L72N_Y	F2
2	IO_VREF_L73P_Y	E1
2	IO_L73N_Y	F4
2	IO_L74P	G2
2	IO_L74N	E3
2	IO_L75P_Y	F1
2	IO_L75N_Y	G5
2	IO_VREF_L76P_Y	G1
2	IO_L76N_Y	F3
2	IO_L77P_YY	G4
2	IO_L77N_YY	H1
2	IO_L78P_Y	J2
2	IO_L78N_Y	G3
2	IO_L79P_Y	H5
2	IO_L79N_Y	K2
2	IO_VREF_L80P_YY	H4
2	IO_L80N_YY	K1
2	IO_L81P_YY	L2
2	IO_L81N_YY	L3
2	IO_VREF_L82P_Y	L1[2]
2	IO_L82N_Y	J5
2	IO_L83P_Y	J4
2	IO_L83N_Y	M3
2	IO_VREF_L84P_YY	J3
2	IO_L84N_YY	M1
2	IO_L85P_YY	N2
2	IO_L85N_YY	K4
2	IO_L86P_Y	N3
2	IO_L86N_Y	K3
2	IO_VREF_L87P_YY	L5

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
NA	VCCO_1	F15
NA	VCCO_1	F19
NA	VCCO_1	F20
NA	VCCO_1	F7
NA	VCCO_1	F8
NA	VCCO_2	G6
NA	VCCO_2	H6
NA	VCCO_2	L6
NA	VCCO_2	M6
NA	VCCO_2	P6
NA	VCCO_2	R6
NA	VCCO_2	W6
NA	VCCO_2	Y6
NA	VCCO_3	AC6
NA	VCCO_3	AD6
NA	VCCO_3	AH6
NA	VCCO_3	AJ6
NA	VCCO_3	AL6
NA	VCCO_3	AM6
NA	VCCO_3	AR6
NA	VCCO_3	AT6
NA	VCCO_4	AU11
NA	VCCO_4	AU12
NA	VCCO_4	AU14
NA	VCCO_4	AU15
NA	VCCO_4	AU19
NA	VCCO_4	AU20
NA	VCCO_4	AU7
NA	VCCO_4	AU8
NA	VCCO_5	AU23
NA	VCCO_5	AU24
NA	VCCO_5	AU28
NA	VCCO_5	AU29
NA	VCCO_5	AU31
NA	VCCO_5	AU32
NA	VCCO_5	AU35
NA	VCCO_5	AU36

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
NA	VCCO_6	AC37
NA	VCCO_6	AD37
NA	VCCO_6	AH37
NA	VCCO_6	AJ37
NA	VCCO_6	AL37
NA	VCCO_6	AM37
NA	VCCO_6	AR37
NA	VCCO_6	AT37
NA	VCCO_7	G37
NA	VCCO_7	H37
NA	VCCO_7	L37
NA	VCCO_7	M37
NA	VCCO_7	P37
NA	VCCO_7	R37
NA	VCCO_7	W37
NA	VCCO_7	Y37
NA	GND	N6
NA	GND	N5
NA	GND	N38
NA	GND	N37
NA	GND	F6
NA	GND	F37
NA	GND	F30
NA	GND	F22
NA	GND	F21
NA	GND	F13
NA	GND	E5
NA	GND	E38
NA	GND	E30
NA	GND	E22
NA	GND	E21
NA	GND	E13
NA	GND	D42
NA	GND	D4
NA	GND	D39
NA	GND	D1

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
0	IO_L6N_Y	A5
0	IO_L6P_Y	F8
0	IO_L7N_Y	D7
0	IO_L7P_Y	N11
0	IO_L8N_YY	G9
0	IO_L8P_YY	E8
0	IO_VREF_L9N_YY	A6
0	IO_L9P_YY	J11
0	IO_L10N_Y	C7
0	IO_L10P_Y	B7
0	IO_L11N_Y	C8
0	IO_L11P_Y	H10
0	IO_L12N_YY	G10
0	IO_L12P_YY	F10
0	IO_VREF_L13N_YY	A8
0	IO_L13P_YY	H11
0	IO_L14N	D9[4]
0	IO_L14P	C9[3]
0	IO_L15N_YY	B9
0	IO_L15P_YY	J12
0	IO_L16N	E10[4]
0	IO_VREF_L16P	A9
0	IO_L17N	G11
0	IO_L17P	B10
0	IO_L18N_YY	H12[4]
0	IO_L18P_YY	C10[4]
0	IO_L19N_Y	H13
0	IO_L19P_Y	F11
0	IO_L20N_Y	E11
0	IO_L20P_Y	D11
0	IO_L21N_Y	B11[4]
0	IO_L21P_Y	G12[4]
0	IO_L22N_YY	F12
0	IO_L22P_YY	C11
0	IO_VREF_L23N_YY	A10[1]
0	IO_L23P_YY	D12
0	IO_L24N_Y	E12

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
0	IO_L24P_Y	A11
0	IO_L25N_Y	G13
0	IO_L25P_Y	B12
0	IO_L26N_YY	A12
0	IO_L26P_YY	K13
0	IO_VREF_L27N_YY	F13
0	IO_L27P_YY	B13
0	IO_L28N_Y	G14
0	IO_L28P_Y	E13
0	IO_L29N_Y	D14
0	IO_L29P_Y	B14
0	IO_L30N_YY	A14
0	IO_L30P_YY	J14
0	IO_VREF_L31N_YY	K14
0	IO_L31P_YY	J15
0	IO_L32N	B15[4]
0	IO_L32P	H15[3]
0	IO_VREF_L33N_YY	F15[2,3]
0	IO_L33P_YY	D15[4]
0	IO_LVDS_DLL_L34N	A15
1	GCK2	E15
1	IO	A25[4]
1	IO	B17[4]
1	IO	B18[4]
1	IO	C23[4]
1	IO	D16[4]
1	IO	D17[5]
1	IO	D23[4]
1	IO	E19[4]
1	IO	E24[5]
1	IO	F22[4]
1	IO	G17[5]
1	IO	G20[4]
1	IO	J16[4]
1	IO	J17[4]
1	IO	J19[5]

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
2	IO_L99P_YY	N26
2	IO_L99N_YY	P28
2	IO_L100P	P29
2	IO_L100N	N24
2	IO_L101P_YY	P22
2	IO_L101N_YY	R26
2	IO_VREF_L102P_YY	P25
2	IO_L102N_YY	R29
2	IO_L103P_YY	R21[4]
2	IO_L103N_YY	R28[3]
2	IO_VREF_L104P_YY	R25[2]
2	IO_L104N_YY	T30
2	IO_L105P_YY	P24[4]
2	IO_L105N_YY	R27[3]
2	IO_L106P	R24
3	IO	T22[4]
3	IO	T24[4]
3	IO	T26[4]
3	IO	T29[4]
3	IO	U26[5]
3	IO	V23[4]
3	IO	V25[4]
3	IO	V30[5]
3	IO	Y21[4]
3	IO	AA26[4]
3	IO	AA23[4]
3	IO	AB27[4]
3	IO	AB29[4]
3	IO	AC28[5]
3	IO	AD26[4]
3	IO	AD29[5]
3	IO	AE27[5]
3	IO_L106N	U29
3	IO_L107P_YY	R22
3	IO_VREF_L107N_YY	T27[2]
3	IO_L108P_YY	R23

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
3	IO_L108N_YY	T28
3	IO_L109P_YY	T21
3	IO_VREF_L109N_YY	T25
3	IO_L110P_YY	U28
3	IO_L110N_YY	U30
3	IO_L111P	T23
3	IO_L111N	U27
3	IO_L112P_YY	U25
3	IO_L112N_YY	V27
3	IO_D4_L113P_YY	U24
3	IO_VREF_L113N_YY	V29
3	IO_L114P	W30
3	IO_L114N	U22
3	IO_L115P_YY	U21
3	IO_L115N_YY	W29
3	IO_L116P_YY	V26
3	IO_L116N_YY	W27
3	IO_L117P	W26
3	IO_VREF_L117N	Y29[1]
3	IO_L118P_YY	W25
3	IO_L118N_YY	Y30
3	IO_L119P_Y	V24[4]
3	IO_L119N_Y	Y28[4]
3	IO_L120P_YY	AA30
3	IO_L120N_YY	W24
3	IO_L121P	AA29
3	IO_L121N	V20
3	IO_L122P	Y27[4]
3	IO_L122N	W23[4]
3	IO_L123P_YY	Y26
3	IO_D5_L123N_YY	AB30
3	IO_D6_L124P_YY	V21
3	IO_VREF_L124N_YY	AA28
3	IO_L125P_YY	Y25
3	IO_L125N_YY	AA27
3	IO_L126P_YY	W22
3	IO_L126N_YY	Y23

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
270	6	AG2	AE7	2600 2000 1000	-
271	6	AG1	AF6	3200 2600 2000 1600 1000	VREF
272	6	AG4	AC9	2000 1600	-
273	6	AF3	AE6	3200 2600 2000 1600 1000	-
274	6	AF4	AF1	2600 1000	VREF
275	6	AF2	AB10	3200 2600 1600	-
276	6	AE1	AC8	3200 2600 1600 1000	-
277	6	AE3	AD5	3200 2600 2000 1600 1000	VREF
278	6	AD1	AC7	3200 2600 2000 1600 1000	-
279	6	AD2	AD6	3200 1600 1000	-
280	6	AC1	AB8	2000 1600 1000	VREF
281	6	AC2	AC5	3200 2600 2000 1600 1000	-
282	6	AC3	AA9	3200 2600 2000	-
283	6	AD4	AC4	2000 1000	-
284	6	AB6	AA8	3200 2600 1600 1000	-
285	6	Y10	AB1	2600 1600	-
286	6	AA7	AB2	3200 1600 1000	-
287	6	AA1	AA4	2600 2000 1000	VREF
288	6	AB4	Y9	3200 2600 2000 1600	-
289	6	Y8	AA2	3200 2600 2000 1600 1000	-

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
290	6	AA5	AA6	3200 2600 1600 1000	-
291	6	Y7	AB3	3200 2600 2000	-
292	6	W10	Y1	2600 2000 1000	-
293	6	Y2	Y5	2000 1600 1000	VREF
294	6	W2	W9	2000 1600	-
295	6	Y4	W7	3200 2600 2000 1600 1000	-
296	6	Y6	W1	1000	-
297	6	W3	W6	3200 1600	-
298	6	W4	V9	3200 2600 1600 1000	-
299	6	V1	W5	2000 1600 1000	VREF
300	6	U2	V7	2000 1600 1000	-
301	6	U1	V6	3200 2600 1600 1000	VREF
302	7	U4	U9	3200 2600 2000 1600 1000	-
303	7	U5	U7	3200 2600 1600 1000	VREF
304	7	U6	U3	2000 1600 1000	-
305	7	T6	T3	2000 1600 1000	VREF
306	7	T4	T9	3200 2600 1600 1000	-
307	7	R1	T5	3200 1600	-
308	7	T10	R6	1000	-
309	7	R5	R2	3200 2600 2000 1600 1000	-
310	7	P5	P1	2000 1600 1000	VREF