Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1536
Number of Logic Elements/Cells	6912
Total RAM Bits	131072
Number of I/O	176
Number of Gates	411955
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv300e-6fg256i

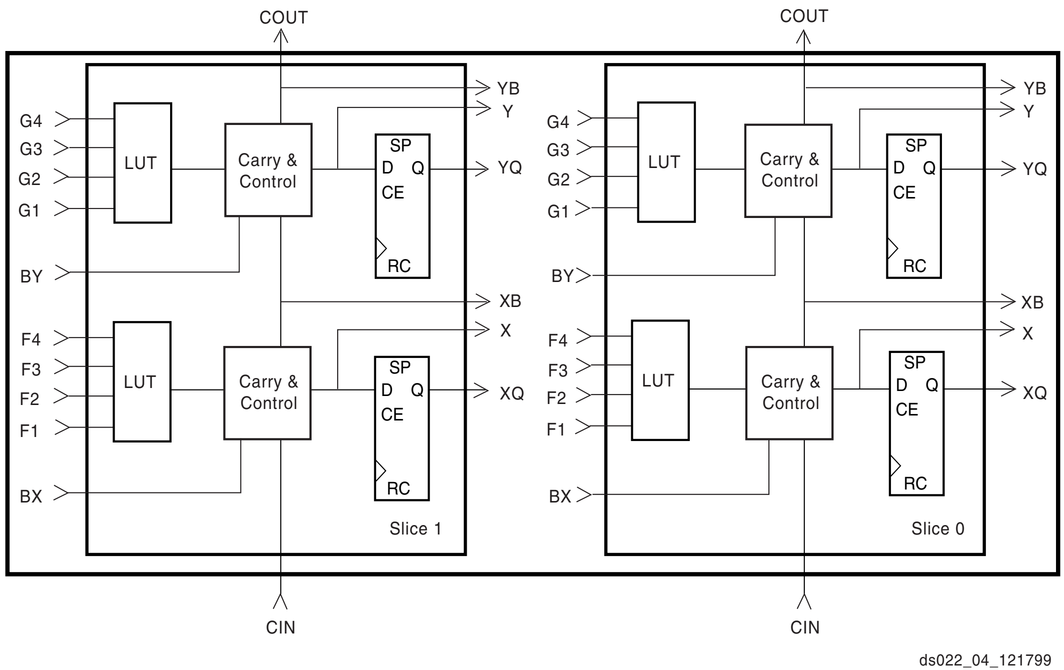

Figure 4: **2-Slice Virtex-E CLB**

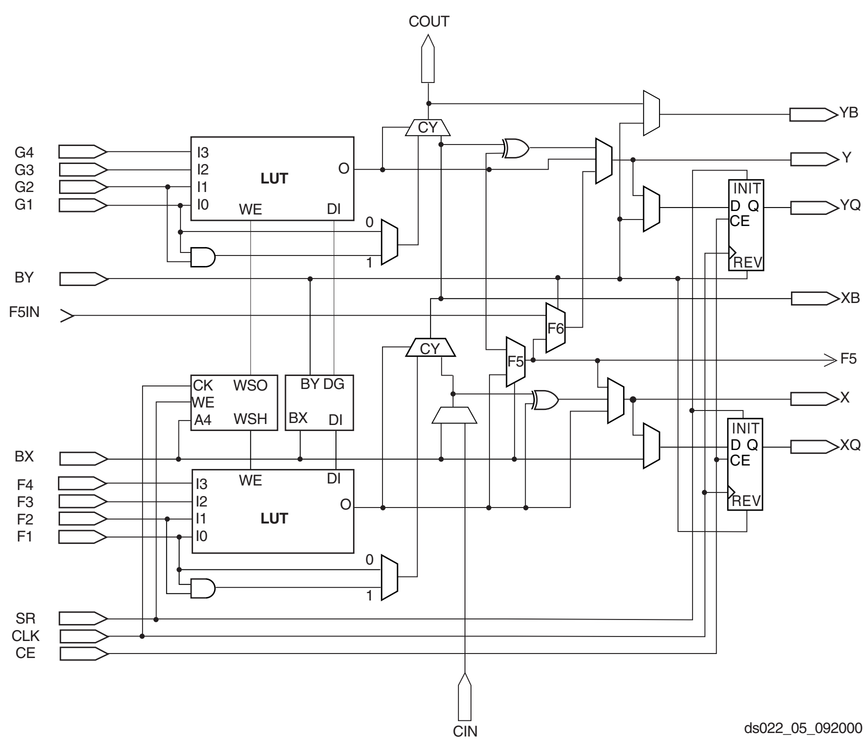

Figure 5: **Detailed View of Virtex-E Slice**

Storage Elements

The storage elements in the Virtex-E slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by the function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each Slice has synchronous set and reset signals (SR and BY). SR

DLL Properties

Properties provide access to some of the Virtex-E series DLL features, (for example, clock division and duty cycle correction).

Duty Cycle Correction Property

The 1x clock outputs, CLK0, CLK90, CLK180, and CLK270, use the duty-cycle corrected default, exhibiting a 50/50 duty cycle. The DUTY_CYCLE_CORRECTION property (by default TRUE) controls this feature. To deactivate the DLL duty-cycle correction for the 1x clock outputs, attach the DUTY_CYCLE_CORRECTION=FALSE property to the DLL symbol.

Clock Divide Property

The CLKDV_DIVIDE property specifies how the signal on the CLKDV pin is frequency divided with respect to the CLK0 pin. The values allowed for this property are 1.5, 2, 2.5, 3, 4, 5, 8, or 16; the default value is 2.

Startup Delay Property

This property, STARTUP_WAIT, takes on a value of TRUE or FALSE (the default value). When TRUE the device configuration DONE signal waits until the DLL locks before going to High.

Virtex-E DLL Location Constraints

As shown in Figure 26, there are four additional DLLs in the Virtex-E devices, for a total of eight per Virtex-E device. These DLLs are located in silicon, at the top and bottom of the two innermost block SelectRAM columns. The location constraint LOC, attached to the DLL symbol with the identifier DLL0S, DLL0P, DLL1S, DLL1P, DLL2S, DLL2P, DLL3S, or DLL3P, controls the DLL location.

The LOC property uses the following form:

LOC = DLL0P

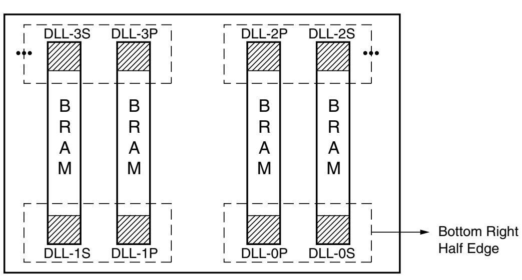

Figure 26: **Virtex Series DLLs**

Design Factors

Use the following design considerations to avoid pitfalls and improve success designing with Xilinx devices.

Input Clock

The output clock signal of a DLL, essentially a delayed version of the input clock signal, reflects any instability on the input clock in the output waveform. For this reason the quality of the DLL input clock relates directly to the quality of the output clock waveforms generated by the DLL. The DLL input clock requirements are specified in the data sheet.

In most systems a crystal oscillator generates the system clock. The DLL can be used with any commercially available quartz crystal oscillator. For example, most crystal oscillators produce an output waveform with a frequency tolerance of 100 PPM, meaning 0.01 percent change in the clock period. The DLL operates reliably on an input waveform with a frequency drift of up to 1 ns — orders of magnitude in excess of that needed to support any crystal oscillator in the industry. However, the cycle-to-cycle jitter must be kept to less than 300 ps in the low frequencies and 150 ps for the high frequencies.

Input Clock Changes

Changing the period of the input clock beyond the maximum drift amount requires a manual reset of the CLKDLL. Failure to reset the DLL produces an unreliable lock signal and output clock.

It is possible to stop the input clock with little impact to the DLL. Stopping the clock should be limited to less than 100 μs to keep device cooling to a minimum. The clock should be stopped during a Low phase, and when restored the full High period should be seen. During this time, LOCKED stays High and remains High when the clock is restored.

When the clock is stopped, one to four more clocks are still observed as the delay line is flushed. When the clock is restarted, the output clocks are not observed for one to four clocks as the delay line is filled. The most common case is two or three clocks.

In a similar manner, a phase shift of the input clock is also possible. The phase shift propagates to the output one to four clocks after the original shift, with no disruption to the CLKDLL control.

Output Clocks

As mentioned earlier in the DLL pin descriptions, some restrictions apply regarding the connectivity of the output pins. The DLL clock outputs can drive an OBUF, a global clock buffer BUFG, or they can route directly to destination clock pins. The only BUFGs that the DLL clock outputs can drive are the two on the same edge of the device (top or bottom). In addition, the CLK2X output of the secondary DLL can connect directly to the CLKIN of the primary DLL in the same quadrant.

Do not use the DLL output clock signals until after activation of the LOCKED signal. Prior to the activation of the LOCKED signal, the DLL output clocks are not valid and can exhibit glitches, spikes, or other spurious movement.

Because any single DLL can access only two BUFGs at most, any additional output clock signals must be routed from the DLL in this example on the high speed backbone routing.

The dll_2x files in the xapp132.zip file show the VHDL and Verilog implementation of this circuit.

Virtex-E 4x Clock

Two DLLs located in the same half-edge (top-left, top-right, bottom-right, bottom-left) can be connected together, without using a BUFG between the CLKDLLs, to generate a 4x clock as shown in Figure 30. Virtex-E devices, like the Virtex devices, have four clock networks that are available for internal deskewing of the clock. Each of the eight DLLs have access to two of the four clock networks. Although all the DLLs can be used for internal deskewing, the presence of two GCLKBUFs on the top and two on the bottom indicate that only two of the four DLLs on the top (and two of the four DLLs on the bottom) can be used for this purpose.

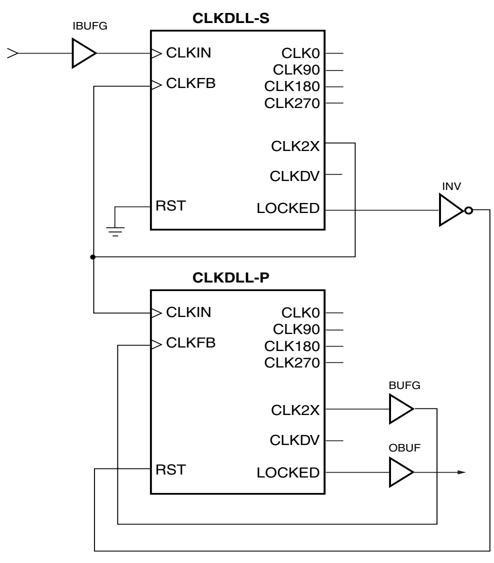

Figure 30: **DLL Generation of 4x Clock in Virtex-E Devices**

The dll_4xe files in the xapp132.zip file show the DLL implementation in Verilog for Virtex-E devices. These files can be found at:

ftp://ftp.xilinx.com/pub/applications/xapp/xapp132.zip

Using Block SelectRAM+ Features

The Virtex FPGA Series provides dedicated blocks of on-chip, true dual-read/write port synchronous RAM, with 4096 memory cells. Each port of the block SelectRAM+ memory can be independently configured as a read/write port, a read port, a write port, and can be configured to a specific data width. The block SelectRAM+ memory offers new capabilities allowing the FPGA designer to simplify designs.

Operating Modes

VIrtex-E block SelectRAM+ memory supports two operating modes:

- Read Through
- Write Back

Read Through (one clock edge)

The read address is registered on the read port clock edge and data appears on the output after the RAM access time. Some memories might place the latch/register at the outputs, depending on whether a faster clock-to-out versus set-up time is desired. This is generally considered to be an inferior solution, since it changes the read operation to an asynchronous function with the possibility of missing an address/control line transition during the generation of the read pulse clock.

Write Back (one clock edge)

The write address is registered on the write port clock edge and the data input is written to the memory and mirrored on the output.

Block SelectRAM+ Characteristics

- All inputs are registered with the port clock and have a set-up to clock timing specification.
- All outputs have a read through or write back function depending on the state of the port WE pin. The outputs relative to the port clock are available after the clock-to-out timing specification.
- The block SelectRAMs are true SRAM memories and do not have a combinatorial path from the address to the output. The LUT SelectRAM+ cells in the CLBs are still available with this function.
- The ports are completely independent from each other (*i.e.,* clocking, control, address, read/write function, and data width) without arbitration.
- A write operation requires only one clock edge.
- A read operation requires only one clock edge.

The output ports are latched with a self timed circuit to guarantee a glitch free read. The state of the output port does not change until the port executes another read or write operation.

Library Primitives

Figure 31 and Figure 32 show the two generic library block SelectRAM+ primitives. Table 14 describes all of the available primitives for synthesis and simulation.

Input termination techniques include the following.

- None
- Parallel (Shunt)

These termination techniques can be applied in any combination. A generic example of each combination of termination methods appears in Figure 43.

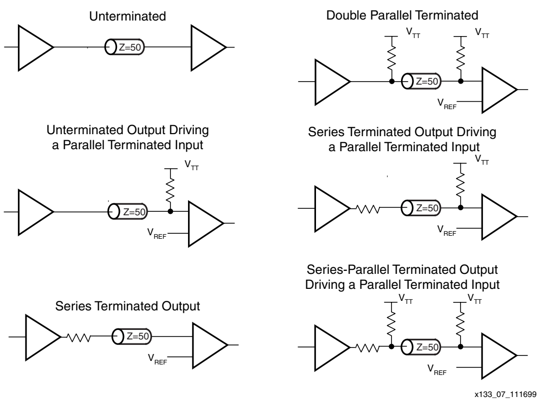

Figure 43: **Overview of Standard Input and Output Termination Methods**

Simultaneous Switching Guidelines

Ground bounce can occur with high-speed digital ICs when multiple outputs change states simultaneously, causing undesired transient behavior on an output, or in the internal logic. This problem is also referred to as the Simultaneous Switching Output (SSO) problem.

Ground bounce is primarily due to current changes in the combined inductance of ground pins, bond wires, and ground metallization. The IC internal ground level deviates from the external system ground level for a short duration (a few nanoseconds) after multiple outputs change state simultaneously.

Ground bounce affects stable Low outputs and all inputs because they interpret the incoming signal by comparing it to the internal ground. If the ground bounce amplitude exceeds the actual instantaneous noise margin, then a non-changing input can be interpreted as a short pulse with a polarity opposite to the ground bounce.

Table 21 provides guidelines for the maximum number of simultaneously switching outputs allowed per output power/ground pair to avoid the effects of ground bounce. See Table 22 for the number of effective output power/ground pairs for each Virtex-E device and package combination.

Table 21: **Guidelines for Max Number of Simultaneously Switching Outputs per Power/Ground Pair**

Standard	Package		
	BGA, CS, FGA	HQ	PQ, TQ
LVTTL Slow Slew Rate, 2 mA drive	68	49	36
LVTTL Slow Slew Rate, 4 mA drive	41	31	20
LVTTL Slow Slew Rate, 6 mA drive	29	22	15
LVTTL Slow Slew Rate, 8 mA drive	22	17	12
LVTTL Slow Slew Rate, 12 mA drive	17	12	9
LVTTL Slow Slew Rate, 16 mA drive	14	10	7
LVTTL Slow Slew Rate, 24 mA drive	9	7	5
LVTTL Fast Slew Rate, 2 mA drive	40	29	21
LVTTL Fast Slew Rate, 4 mA drive	24	18	12
LVTTL Fast Slew Rate, 6 mA drive	17	13	9
LVTTL Fast Slew Rate, 8 mA drive	13	10	7
LVTTL Fast Slew Rate, 12 mA drive	10	7	5
LVTTL Fast Slew Rate, 16 mA drive	8	6	4
LVTTL Fast Slew Rate, 24 mA drive	5	4	3
LVCMOS	10	7	5
PCI	8	6	4
GTL	4	4	4
GTL+	4	4	4

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply. This is the time required to reach the nominal power supply voltage of the device[1] from 0V. The fastest ramp rate is 0V to nominal voltage in 2 ms, and the slowest allowed ramp rate is 0V to nominal voltage in 50 ms. For more details on power supply requirements, see XAPP158 on www.xilinx.com.

Product (Commercial Grade)	Description[(2)]	Current Requirement[(3)]
XCV50E - XCV600E	Minimum required current supply	500 mA
XCV812E - XCV2000E	Minimum required current supply	1 A
XCV2600E - XCV3200E	Minimum required current supply	1.2 A
Virtex-E Family, Industrial Grade	Minimum required current supply	2 A

Notes:
1. Ramp rate used for this specification is from 0 - 1.8 V DC. Peak current occurs on or near the internal power-on reset threshold and lasts for less than 3 ms.
2. Devices are guaranteed to initialize properly with the minimum current available from the power supply as noted above.
3. Larger currents might result if ramp rates are forced to be faster.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTL[(1)]	– 0.5	0.8	2.0	3.6	0.4	2.4	24	– 24
LVCMOS2	– 0.5	0.7	1.7	2.7	0.4	1.9	12	– 12
LVCMOS18	– 0.5	35% V_{CCO}	65% V_{CCO}	1.95	0.4	V_{CCO} – 0.4	8	– 8
PCI, 3.3 V	– 0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
GTL	– 0.5	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	n/a	40	n/a
GTL+	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	n/a	36	n/a
HSTL I[(3)]	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	8	–8
HSTL III	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	24	–8
HSTL IV	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	48	–8
SSTL3 I	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.6	V_{REF} + 0.6	8	–8
SSTL3 II	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.8	V_{REF} + 0.8	16	–16
SSTL2 I	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.61	V_{REF} + 0.61	7.6	–7.6
SSTL2 II	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.80	V_{REF} + 0.80	15.2	–15.2

Table 2: **IOB Input Switching Characteristics** ***(Continued)***

			Speed Grade(1)				
Description(2)	**Symbol**	**Device**	**Min**	**-8**	**-7**	**-6**	**Units**
Sequential Delays							
Clock CLK							
Minimum Pulse Width, High	T_{CH}	All	0.56	1.2	1.3	1.4	ns, min
Minimum Pulse Width, Low	T_{CL}		0.56	1.2	1.3	1.4	ns, min
Clock CLK to output IQ	T_{IOCKIQ}		0.18	0.4	0.7	0.7	ns, max
Setup and Hold Times with respect to Clock at IOB Input Register							
Pad, no delay	T_{IOPICK}/ T_{IOICKP}	All	0.69 / 0	1.3 / 0	1.4 / 0	1.5 / 0	ns, min
Pad, with delay	$T_{IOPICKD}$/ $T_{IOICKPD}$	XCV50E	1.25 / 0	2.8 / 0	2.9 / 0	2.9 / 0	ns, min
		XCV100E	1.25 / 0	2.8 / 0	2.9 / 0	2.9 / 0	ns, min
		XCV200E	1.33 / 0	3.0 / 0	3.1 / 0	3.1 / 0	ns, min
		XCV300E	1.33 / 0	3.0 / 0	3.1 / 0	3.1 / 0	ns, min
		XCV400E	1.37 / 0	3.1 / 0	3.2 / 0	3.2 / 0	ns, min
		XCV600E	1.49 / 0	3.4 / 0	3.5 / 0	3.5 / 0	ns, min
		XCV1000E	1.49 / 0	3.4 / 0	3.5 / 0	3.5 / 0	ns, min
		XCV1600E	1.53 / 0	3.5 / 0	3.6 / 0	3.6 / 0	ns, min
		XCV2000E	1.53 / 0	3.5 / 0	3.6 / 0	3.6 / 0	ns, min
		XCV2600E	1.53 / 0	3.5 / 0	3.6 / 0	3.6 / 0	ns, min
		XCV3200E	1.53 / 0	3.5 / 0	3.6 / 0	3.6 / 0	ns, min
ICE input	$T_{IOICECK}$/ $T_{IOCKICE}$	All	0.28 / 0.0	0.55 / 0.01	0.7 / 0.01	0.7 / 0.01	ns, min
SR input (IFF, synchronous)	$T_{IOSRCKI}$	All	0.38	0.8	0.9	1.0	ns, min
Set/Reset Delays							
SR input to IQ (asynchronous)	T_{IOSRIQ}	All	0.54	1.1	1.2	1.4	ns, max
GSR to output IQ	T_{GSRQ}	All	3.88	7.6	8.5	9.7	ns, max

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. Input timing i for LVTTL is measured at 1.4 V. For other I/O standards, see Table 4.

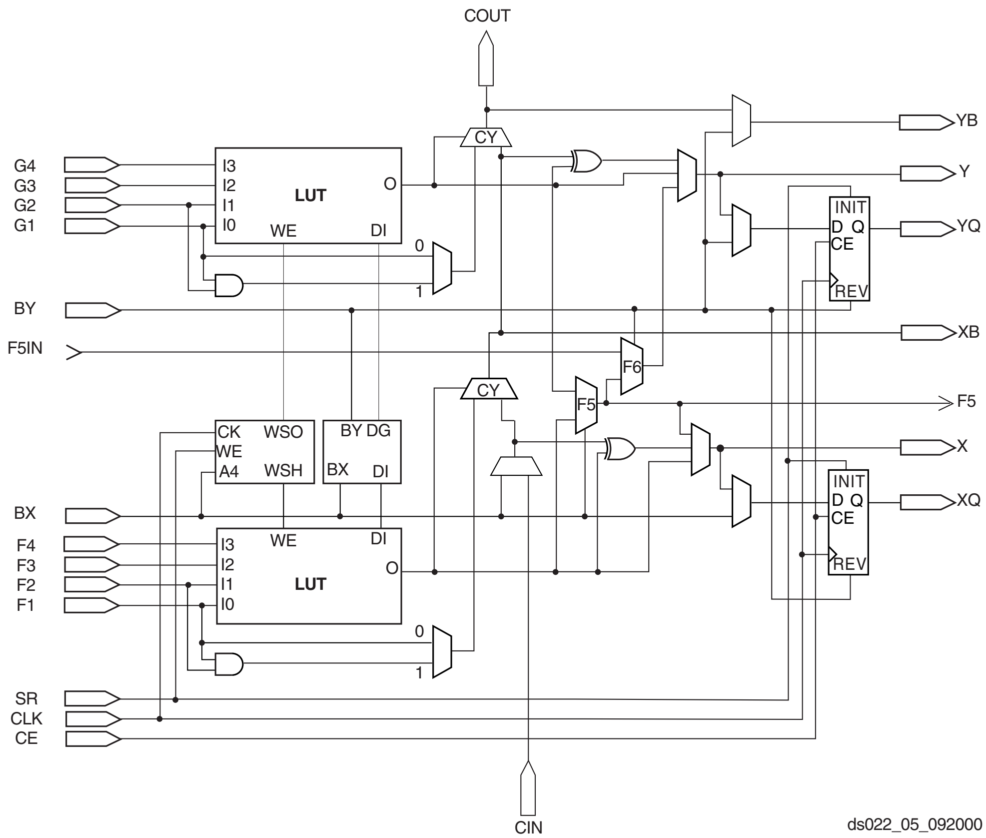

Figure 2: **Detailed View of Virtex-E Slice**

PQ240 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 7: **PQ240 Differential Pin Pair Summary XCV50E, XCV100E, XCV200E, XCV300E, XCV400E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	P92	P93	NA	IO_DLL_L40P
1	5	P89	P87	NA	IO_DLL_L40N
2	1	P210	P209	NA	IO_DLL_L6P
3	0	P213	P215	NA	IO_DLL_L6N
IO LVDS Total Pairs: 64, Asynchronous Outputs Pairs: 27					
0	0	P236	P237	1	VREF
1	0	P234	P235	√	-
2	0	P228	P229	√	VREF
3	0	P223	P224	√	-
4	0	P220	P221	3	-
5	0	P217	P218	3	VREF
6	1	P209	P215	NA	IO_LVDS_DLL
7	1	P205	P206	3	VREF
8	1	P202	P203	3	-
9	1	P199	P200	√	-
10	1	P194	P195	√	VREF
11	1	P191	P192	√	VREF
12	1	P188	P189	√	-
13	1	P186	P187	1	VREF
14	1	P184	P185	√	CS
15	2	P178	P177	√	DIN, D0

Table 7: **PQ240 Differential Pin Pair Summary XCV50E, XCV100E, XCV200E, XCV300E, XCV400E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
16	2	P174	P173	2	-
17	2	P171	P170	3	VREF
18	2	P168	P167	4	D1, VREF
19	2	P163	P162	√	D2
20	2	P160	P159	2	-
21	2	P157	P156	4	D3, VREF
22	2	P155	P154	5	VREF
23	2	P153	P152	√	-
24	3	P145	P144	4	D4, VREF
25	3	P142	P141	2	-
26	3	P139	P138	√	D5
27	3	P134	P133	4	VREF
28	3	P131	P130	3	VREF
29	3	P128	P127	2	-
30	3	P126	P125	6	VREF
31	3	P124	P123	√	INIT
32	4	P118	P117	√	-
33	4	P114	P113	√	-
34	4	P111	P110	√	VREF
35	4	P108	P107	√	VREF
36	4	P103	P102	√	-
37	4	P100	P99	3	-
38	4	P97	P96	3	VREF
39	4	P95	P94	7	VREF
40	5	P93	P87	NA	IO_LVDS_DLL
41	5	P84	P82	8	VREF
42	5	P79	P78	√	-
43	5	P74	P73	√	VREF
44	5	P71	P70	√	VREF
45	5	P68	P67	√	-
46	5	P66	P65	1	VREF
47	5	P64	P63	√	-

Table 12: **BG432 — XCV300E, XCV400E, XCV600E**

Bank	Pin Description	Pin #
6	IO	AA30
6	IO	AC30
6	IO	AD29
6	IO	U31
6	IO	W28
6	IO_L103N_YY	AJ30
6	IO_L103P_YY	AH30
6	IO_L104N	AG28
6	IO_L104P	AH31
6	IO_L105N_Y	AG29
6	IO_L105P_Y	AG30
6	IO_VREF_L106N_Y	AF28
6	IO_L106P_Y	AG31
6	IO_L107N	AF29
6	IO_L107P	AF30
6	IO_L108N_Y	AE28
6	IO_L108P_Y	AF31
6	IO_VREF_L109N_YY	AE30
6	IO_L109P_YY	AD28
6	IO_L110N_Y	AD30
6	IO_L110P_Y	AD31
6	IO_VREF_L111N_Y	AC28[1]
6	IO_L111P_Y	AC29
6	IO_VREF_L112N_YY	AB28
6	IO_L112P_YY	AB29
6	IO_L113N_YY	AB31
6	IO_L113P_YY	AA29
6	IO_L114N_Y	Y28
6	IO_L114P_Y	Y29
6	IO_L115N_Y	Y30
6	IO_L115P_Y	Y31
6	IO_L116N_Y	W29
6	IO_L116P_Y	W30
6	IO_VREF_L117N_YY	V28
6	IO_L117P_YY	V29
6	IO_L118N_Y	V30

Table 12: **BG432 — XCV300E, XCV400E, XCV600E**

Bank	Pin Description	Pin #
6	IO_L118P_Y	U29
6	IO_VREF_L119N_Y	U28[2]
6	IO_L119P_Y	U30
6	IO	T30
7	IO	C30
7	IO	H29
7	IO	H31
7	IO	L29
7	IO	M31
7	IO	R28
7	IO_L120N_YY	T31
7	IO_L120P_YY	R29
7	IO_L121N_Y	R30
7	IO_VREF_L121P_Y	R31[2]
7	IO_L122N_Y	P29
7	IO_L122P_Y	P28
7	IO_L123N_YY	P30
7	IO_VREF_L123P_YY	N30
7	IO_L124N_Y	N28
7	IO_L124P_Y	N31
7	IO_L125N_Y	M29
7	IO_L125P_Y	M28
7	IO_L126N_Y	M30
7	IO_L126P_Y	L30
7	IO_L127N_YY	K31
7	IO_L127P_YY	K30
7	IO_L128N_YY	K28
7	IO_VREF_L128P_YY	J30
7	IO_L129N_Y	J29
7	IO_VREF_L129P_Y	J28[1]
7	IO_L130N_Y	H30
7	IO_L130P_Y	G30
7	IO_L131N_YY	H28
7	IO_VREF_L131P_YY	F31
7	IO_L132N_Y	G29

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
3	IO_D4_L73P_YY	W4	
3	IO_VREF_L73N_YY	W5	
3	IO_L74P_Y	Y3	
3	IO_L74N_Y	Y4	
3	IO_L75P_Y	AA1	
3	IO_L75N_Y	Y5	
3	IO_L76P_Y	AA3	
3	IO_VREF_L76N_Y	AA4	3
3	IO_L77P_Y	AB3	
3	IO_L77N_Y	AA5	
3	IO_L78P_Y	AC1	
3	IO_L78N_Y	AB4	
3	IO_L79P_YY	AC3	
3	IO_D5_L79N_YY	AB5	
3	IO_D6_L80P_YY	AC4	
3	IO_VREF_L80N_YY	AD3	
3	IO_L81P_Y	AE1	
3	IO_L81N_Y	AC5	
3	IO_L82P_Y	AD4	
3	IO_VREF_L82N_Y	AF1	4
3	IO_L83P_Y	AF2	
3	IO_L83N_Y	AD5	
3	IO_L84P_Y	AG2	
3	IO_VREF_L84N_Y	AE4	1
3	IO_L85P_YY	AH1	
3	IO_VREF_L85N_YY	AE5	
3	IO_L86P_Y	AF4	
3	IO_L86N_Y	AJ1	
3	IO_L87P_Y	AJ2	
3	IO_L87N_Y	AF5	
3	IO_L88P_Y	AG4	
3	IO_VREF_L88N_Y	AK2	
3	IO_L89P_Y	AJ3	
3	IO_L89N_Y	AG5	
3	IO_L90P_Y	AL1	
3	IO_VREF_L90N_Y	AH4	3
3	IO_D7_L91P_YY	AJ4	
3	IO_INIT_L91N_YY	AH5	
3	IO	U4	
4	GCK0	AL17	
4	IO	AJ8	
4	IO	AJ11	
4	IO	AK6	
4	IO	AK9	
4	IO_L92P_YY	AL4	
4	IO_L92N_YY	AJ6	
4	IO_L93P_Y	AK5	
4	IO_VREF_L93N_Y	AN3	3
4	IO_L94P_YY	AL5	
4	IO_L94N_YY	AJ7	
4	IO_VREF_L95P_YY	AM4	
4	IO_L95N_YY	AM5	
4	IO_L96P_Y	AK7	
4	IO_L96N_Y	AL6	
4	IO_L97P_YY	AM6	
4	IO_L97N_YY	AN6	
4	IO_VREF_L98P_YY	AL7	
4	IO_L98N_YY	AJ9	
4	IO_L99P_Y	AN7	
4	IO_VREF_L99N_Y	AL8	1
4	IO_L100P_Y	AM8	
4	IO_L100N_Y	AJ10	
4	IO_VREF_L101P_Y	AL9	4
4	IO_L101N_Y	AM9	
4	IO_L102P_Y	AK10	
4	IO_L102N_Y	AN9	
4	IO_VREF_L103P_YY	AL10	
4	IO_L103N_YY	AM10	
4	IO_L104P_YY	AL11	

Table 21: **FG676 Differential Pin Pair Summary XCV400E, XCV600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
120	5	AD11	Y12	√	-
121	5	AB11	AD10	NA	-
122	5	AC11	AE10	√	-
123	5	AC10	AA11	√	-
124	5	Y11	AD9	1	-
125	5	AB10	AF9	√	-
126	5	AD8	AA10	√	VREF
127	5	AE8	Y10	√	-
128	5	AC9	AF8	1	VREF
129	5	AF7	AB9	1	-
130	5	AA9	AF6	√	-
131	5	AC8	AC7	√	VREF
132	5	AD6	Y9	√	-
133	5	AE5	AA8	√	-
134	5	AC6	AB8	√	VREF
135	5	AD5	AA7	√	-
136	5	AF4	AC5	2	-
137	6	AC3	AA5	√	-
138	6	AB4	AC2	√	-
139	6	AA4	W6	2	-
140	6	Y5	AB3	1	VREF
141	6	V7	AB2	1	-
142	6	Y4	AB1	√	-
143	6	W5	V5	√	VREF
144	6	V6	AA1	√	-
145	6	Y3	W4	2	-
146	6	U7	Y1	1	VREF
147	6	V4	W1	√	-
148	6	U6	W2	√	VREF
149	6	T5	V3	√	-
150	6	U4	U5	√	-
151	6	U3	T7	2	-
152	6	T6	U2	1	-
153	6	T4	U1	1	-

Table 21: **FG676 Differential Pin Pair Summary XCV400E, XCV600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
154	6	T3	R7	1	-
155	6	R6	R4	√	VREF
156	6	R5	R3	√	-
157	6	P7	P8	2	-
158	6	P6	R1	1	VREF
159	6	P4	P5	√	-
160	7	N8	N5	√	-
161	7	N3	N6	√	-
162	7	M2	N4	1	VREF
163	7	M7	N7	2	-
164	7	M3	M6	√	-
165	7	M5	M4	√	VREF
166	7	L7	L3	1	-
167	7	K2	L6	1	-
168	7	K1	L4	1	-
169	7	L5	K3	2	-
170	7	J3	K5	√	-
171	7	J4	K4	√	-
172	7	K6	H3	√	VREF
173	7	G3	K7	√	-
174	7	H1	J5	1	VREF
175	7	J6	G2	2	-
176	7	F1	J7	√	-
177	7	G4	H4	√	VREF
178	7	H5	F3	1	-
179	7	H6	E2	2	-
180	7	F4	G5	1	VREF
181	7	G6	H7	2	-
182	7	E4	E3	√	-

Notes:
1. AO in the XCV600E.
2. AO in the XCV400E.

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
4	IO_VREF_L132P_YY	AV8
4	IO_L132N_YY	AU9
4	IO_L133P_Y	AW8
4	IO_L133N_Y	AT10
4	IO_VREF_L134P_Y	AV9[3]
4	IO_L134N_Y	AU10
4	IO_L135P_YY	AW9
4	IO_L135N_YY	AT11
4	IO_VREF_L136P_YY	AV10
4	IO_L136N_YY	AU11
4	IO_L137P_Y	AW10
4	IO_L137N_Y	AU12
4	IO_L138P_Y	AV11
4	IO_L138N_Y	AT13
4	IO_VREF_L139P_YY	AW11
4	IO_L139N_YY	AU13
4	IO_L140P_YY	AT14
4	IO_L140N_YY	AV12
4	IO_L141P_Y	AU14
4	IO_L141N_Y	AW12
4	IO_L142P_Y	AT15
4	IO_L142N_Y	AV13
4	IO_L143P_YY	AU15
4	IO_L143N_YY	AW13
4	IO_VREF_L144P_YY	AV14[1]
4	IO_L144N_YY	AT16
4	IO_L145P_Y	AW14
4	IO_L145N_Y	AU16
4	IO_L146P_Y	AV15
4	IO_L146N_Y	AR17
4	IO_L147P_YY	AW15
4	IO_L147N_YY	AT17
4	IO_VREF_L148P_YY	AU17
4	IO_L148N_YY	AV16
4	IO_L149P_Y	AR18
4	IO_L149N_Y	AW16

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
4	IO_L150P_Y	AT18
4	IO_L150N_Y	AV17
4	IO_L151P_YY	AU18
4	IO_L151N_YY	AW17
4	IO_VREF_L152P_YY	AT19
4	IO_L152N_YY	AV18
4	IO_L153P_Y	AU19
4	IO_L153N_Y	AW18
4	IO_VREF_L154P	AU21[2]
4	IO_L154N	AV19
4	IO_LVDS_DLL_L155P	AT21
5	GCK1	AU22
5	IO	AT34
5	IO	AW20
5	IO_LVDS_DLL_L155N	AT22
5	IO_VREF_L156P_Y	AV20[2]
5	IO_L156N_Y	AR22
5	IO_L157P_YY	AV23
5	IO_VREF_L157N_YY	AW21
5	IO_L158P_YY	AU23
5	IO_L158N_YY	AV21
5	IO_L159P_Y	AT23
5	IO_L159N_Y	AW22
5	IO_L160P_Y	AR23
5	IO_L160N_Y	AV22
5	IO_L161P_YY	AV24
5	IO_VREF_L161N_YY	AW23
5	IO_L162P_YY	AW24
5	IO_L162N_YY	AU24
5	IO_L163P_Y	AW25
5	IO_L163N_Y	AT24
5	IO_L164P_Y	AV25
5	IO_L164N_Y	AU25
5	IO_L165P_YY	AW26
5	IO_VREF_L165N_YY	AT25[1]

FG680 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 23: **FG680 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
GCLK LVDS					
3	0	A20	C22	NA	IO_DLL_L29N
2	1	D21	A19	NA	IO_DLL_L29P
1	5	AU22	AT22	NA	IO_DLL_L155N
0	4	AW19	AT21	NA	IO_DLL_L155P
IO LVDS Total Pairs: 247, Asynchronous Output Pairs: 111					
0	0	A36	C35	5	-
1	0	B35	D34	5	VREF
2	0	A35	C34	√	-
3	0	B34	D33	√	VREF
4	0	A34	C33	3	-
5	0	B33	D32	3	-
6	0	D31	C32	√	-
7	0	C31	A33	√	VREF
8	0	B31	B32	5	-
9	0	D30	A32	5	VREF
10	0	C30	A31	√	-
11	0	D29	B30	√	VREF
12	0	C29	A30	2	-
13	0	B29	A29	2	-
14	0	A28	B28	√	VREF
15	0	B27	C28	√	-
16	0	A27	D27	5	-
17	0	B26	C27	5	-

Table 23: **FG680 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
18	0	C26	D26	√	-
19	0	D25	A26	√	VREF
20	0	C25	B25	3	-
21	0	D24	A25	3	-
22	0	B23	A24	√	-
23	0	A23	C24	√	VREF
24	0	B22	B24	5	-
25	0	A22	E23	5	-
26	0	B21	D23	√	-
27	0	A21	C23	√	VREF
28	0	B20	E22	2	-
29	1	A19	C22	NA	IO_LVDS_DLL
30	1	B19	C21	2	VREF
31	1	A18	C19	2	-
32	1	B18	D19	√	VREF
33	1	A17	C18	√	-
34	1	B17	D18	5	-
35	1	A16	E18	5	-
36	1	D17	C17	√	VREF
37	1	E17	B16	√	-
38	1	C16	A15	3	-
39	1	D16	B15	3	-
40	1	B14	A14	√	VREF
41	1	A13	C15	√	-
42	1	B13	D15	5	-
43	1	A12	C14	5	-
44	1	C13	D14	√	-
45	1	D13	B12	√	VREF
46	1	C12	A11	2	-
47	1	C11	B11	2	-
48	1	D11	A10	√	VREF
49	1	C10	B10	√	-
50	1	D10	A9	5	VREF
51	1	C9	B9	5	-

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
1	IO_L57N_Y	D9
1	IO_VREF_L57P_Y	A12[2]
1	IO_L58N_Y	E9
1	IO_L58P_Y	C12
1	IO_L59N_YY	B12
1	IO_VREF_L59P_YY	D8
1	IO_L60N_YY	A11
1	IO_L60P_YY	E8
1	IO_L61N_Y	C7
1	IO_L61P_Y	A10
1	IO_L62N_Y	C6
1	IO_L62P_Y	B10
1	IO_L63N_YY	A9
1	IO_VREF_L63P_YY	B9
1	IO_L64N_YY	A8
1	IO_L64P_YY	E7
1	IO_L65N_Y	B8
1	IO_L65P_Y	C5
1	IO_L66N_Y	A7
1	IO_VREF_L66P_Y	A6
1	IO_L67N_Y	B7
1	IO_L67P_Y	D6
1	IO_L68N_Y	A5
1	IO_L68P_Y	C4
1	IO_WRITE_L69N_YY	B6
1	IO_CS_L69P_YY	E6
2	IO	H2
2	IO	H3
2	IO	J1
2	IO	K5
2	IO	M2
2	IO	N1
2	IO	R5
2	IO	U1
2	IO	U4
2	IO	W3

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
2	IO	Y3
2	IO	AA3
2	IO_DOUT_BUSY_L70P_YY	F5
2	IO_DIN_D0_L70N_YY	D2
2	IO_L71P_Y	E4
2	IO_L71N_Y	E2
2	IO_L72P_Y	D3
2	IO_L72N_Y	F2
2	IO_VREF_L73P_Y	E1
2	IO_L73N_Y	F4
2	IO_L74P	G2
2	IO_L74N	E3
2	IO_L75P_Y	F1
2	IO_L75N_Y	G5
2	IO_VREF_L76P_Y	G1
2	IO_L76N_Y	F3
2	IO_L77P_YY	G4
2	IO_L77N_YY	H1
2	IO_L78P_Y	J2
2	IO_L78N_Y	G3
2	IO_L79P_Y	H5
2	IO_L79N_Y	K2
2	IO_VREF_L80P_YY	H4
2	IO_L80N_YY	K1
2	IO_L81P_YY	L2
2	IO_L81N_YY	L3
2	IO_VREF_L82P_Y	L1[2]
2	IO_L82N_Y	J5
2	IO_L83P_Y	J4
2	IO_L83N_Y	M3
2	IO_VREF_L84P_YY	J3
2	IO_L84N_YY	M1
2	IO_L85P_YY	N2
2	IO_L85N_YY	K4
2	IO_L86P_Y	N3
2	IO_L86N_Y	K3
2	IO_VREF_L87P_YY	L5

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
0	IO_L6N_Y	A5
0	IO_L6P_Y	F8
0	IO_L7N_Y	D7
0	IO_L7P_Y	N11
0	IO_L8N_YY	G9
0	IO_L8P_YY	E8
0	IO_VREF_L9N_YY	A6
0	IO_L9P_YY	J11
0	IO_L10N_Y	C7
0	IO_L10P_Y	B7
0	IO_L11N_Y	C8
0	IO_L11P_Y	H10
0	IO_L12N_YY	G10
0	IO_L12P_YY	F10
0	IO_VREF_L13N_YY	A8
0	IO_L13P_YY	H11
0	IO_L14N	D9[4]
0	IO_L14P	C9[3]
0	IO_L15N_YY	B9
0	IO_L15P_YY	J12
0	IO_L16N	E10[4]
0	IO_VREF_L16P	A9
0	IO_L17N	G11
0	IO_L17P	B10
0	IO_L18N_YY	H12[4]
0	IO_L18P_YY	C10[4]
0	IO_L19N_Y	H13
0	IO_L19P_Y	F11
0	IO_L20N_Y	E11
0	IO_L20P_Y	D11
0	IO_L21N_Y	B11[4]
0	IO_L21P_Y	G12[4]
0	IO_L22N_YY	F12
0	IO_L22P_YY	C11
0	IO_VREF_L23N_YY	A10[1]
0	IO_L23P_YY	D12
0	IO_L24N_Y	E12

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
0	IO_L24P_Y	A11
0	IO_L25N_Y	G13
0	IO_L25P_Y	B12
0	IO_L26N_YY	A12
0	IO_L26P_YY	K13
0	IO_VREF_L27N_YY	F13
0	IO_L27P_YY	B13
0	IO_L28N_Y	G14
0	IO_L28P_Y	E13
0	IO_L29N_Y	D14
0	IO_L29P_Y	B14
0	IO_L30N_YY	A14
0	IO_L30P_YY	J14
0	IO_VREF_L31N_YY	K14
0	IO_L31P_YY	J15
0	IO_L32N	B15[4]
0	IO_L32P	H15[3]
0	IO_VREF_L33N_YY	F15[2,3]
0	IO_L33P_YY	D15[4]
0	IO_LVDS_DLL_L34N	A15
1	GCK2	E15
1	IO	A25[4]
1	IO	B17[4]
1	IO	B18[4]
1	IO	C23[4]
1	IO	D16[4]
1	IO	D17[5]
1	IO	D23[4]
1	IO	E19[4]
1	IO	E24[5]
1	IO	F22[4]
1	IO	G17[5]
1	IO	G20[4]
1	IO	J16[4]
1	IO	J17[4]
1	IO	J19[5]

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
2	IO	D29[5]
2	IO	G26[4]
2	IO	H24[4]
2	IO	H25[4]
2	IO	H28[5]
2	IO	J25[4]
2	IO	J27[5]
2	IO	K30[4]
2	IO	M24[4]
2	IO	M25[4]
2	IO	N20
2	IO	N23[4]
2	IO	P26[5]
2	IO	P27[5]
2	IO	P30[4]
2	IO	R30
2	IO_DOUT_BUSY_L70P_YY	J22
2	IO_DIN_D0_L70N_YY	E27
2	IO_L71P	C29[4]
2	IO_L71N	D28[3]
2	IO_L72P_Y	G25
2	IO_L72N_Y	E25
2	IO_VREF_L73P_YY	E28[1]
2	IO_L73N_YY	C30
2	IO_L74P_Y	K22[4]
2	IO_L74N_Y	F27[3]
2	IO_L75P_YY	D30
2	IO_L75N_YY	J23
2	IO_VREF_L76P_Y	L21
2	IO_L76N_Y	F28
2	IO_L77P_YY	G28
2	IO_L77N_YY	E30
2	IO_L78P_YY	G27
2	IO_L78N_YY	E29
2	IO_L79P	K23
2	IO_L79N	H26
2	IO_VREF_L80P_YY	F30

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
2	IO_L80N_YY	L22
2	IO_L81P_YY	H27
2	IO_L81N_YY	G29
2	IO_L82P	G30
2	IO_L82N	M21
2	IO_L83P_YY	J24
2	IO_L83N_YY	J26
2	IO_VREF_L84P_YY	H30
2	IO_L84N_YY	L23
2	IO_L85P_YY	K26[4]
2	IO_L85N_YY	J28[3]
2	IO_L86P_YY	J29
2	IO_L86N_YY	K24
2	IO_L87P_YY	K27[4]
2	IO_VREF_L87N_YY	J30
2	IO_D1_L88P	M22
2	IO_D2_L88N	K29
2	IO_L89P_YY	K28[3]
2	IO_L89N_YY	L25[4]
2	IO_L90P	N21
2	IO_L90N	K25
2	IO_L91P_YY	L24
2	IO_L91N_YY	L27
2	IO_L92P_Y	L29[4]
2	IO_L92N_Y	M23[4]
2	IO_L93P_YY	L26
2	IO_L93N_YY	L28
2	IO_VREF_L94P	L30[1]
2	IO_L94N	M27
2	IO_L95P_YY	M26
2	IO_L95N_YY	M29
2	IO_L96P_YY	N29
2	IO_L96N_YY	M30
2	IO_L97P	N25
2	IO_L97N	N27
2	IO_VREF_L98P_YY	N30
2	IO_D3_L98N_YY	P21

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
5	IO_L182N	AF13
5	IO_L183P	AH14
5	IO_L183N	AJ14
5	IO_L184P_YY	AE14
5	IO_VREF_L184N_YY	AG13
5	IO_L185P_YY	AK13
5	IO_L185N_YY	AD13
5	IO_L186P	AE13
5	IO_L186N	AF12
5	IO_L187P	AC13
5	IO_L187N	AA13
5	IO_L188P_YY	AA12
5	IO_VREF_L188N_YY	AJ12[1]
5	IO_L189P_YY	AB12
5	IO_L189N_YY	AE11
5	IO_L190P	AK12[4]
5	IO_L190N	Y13[4]
5	IO_L191P	AG11
5	IO_L191N	AF11
5	IO_L192P	AH11
5	IO_L192N	AJ11
5	IO_L193P_YY	AE12[4]
5	IO_L193N_YY	AG10[4]
5	IO_L194P_YY	AD12
5	IO_L194N_YY	AK11
5	IO_L195P_YY	AJ10
5	IO_VREF_L195N_YY	AC12
5	IO_L196P_YY	AK10
5	IO_L196N_YY	AD11
5	IO_L197P_YY	AJ9
5	IO_L197N_YY	AE9
5	IO_L198P_YY	AH10
5	IO_VREF_L198N_YY	AF9
5	IO_L199P_YY	AH9
5	IO_L199N_YY	AK9
5	IO_L200P	AF8
5	IO_L200N	AB11
5	IO_L201P	AC11
5	IO_L201N	AG8
5	IO_L202P_YY	AK8
5	IO_VREF_L202N_YY	AF7
5	IO_L203P_YY	AG7
5	IO_L203N_YY	AK7
5	IO_L204P	AJ7
5	IO_L204N	AD10
5	IO_L205P	AH6
5	IO_L205N	AC10
5	IO_L206P_YY	AD9
5	IO_VREF_L206N_YY	AG6
5	IO_L207P_YY	AB10
5	IO_L207N_YY	AJ5
5	IO_L208P	AD8[4]
5	IO_L208N	AK5[4]
5	IO_L209P	AC9
5	IO_VREF_L209N	AJ4[1]
5	IO_L210P	AG5
5	IO_L210N	AK4
5	IO_L211P_YY	AH5[3]
5	IO_L211N_YY	AG3[4]
6	IO	T2[4]
6	IO	T10[4]
6	IO	U1
6	IO	U4[5]
6	IO	U6[4]
6	IO	U7[4]
6	IO	V1[4]
6	IO	V5[5]
6	IO	V8
6	IO	Y10[4]
6	IO	AA4[4]
6	IO	AB5[5]
6	IO	AB7[4]
6	IO	AC3[5]

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
1	IO_L66P_Y	E24
1	IO_L67N_YY	A26
1	IO_VREF_L67P_YY	C25
1	IO_L68N_YY	F24
1	IO_L68P_YY	B26
1	IO_L69N	K23[5]
1	IO_L69P	F25[4]
1	IO_L70N_Y	C26
1	IO_VREF_L70P_Y	H24[2]
1	IO_L71N_Y	G24
1	IO_L71P_Y	A27
1	IO_L72N	B27[5]
1	IO_L72P	G25[4]
1	IO_L73N_YY	E26
1	IO_VREF_L73P_YY	C27
1	IO_L74N_YY	J24
1	IO_L74P_YY	B28
1	IO_L75N	K24[5]
1	IO_L75P	H25[4]
1	IO_L76N_Y	D27
1	IO_L76P_Y	F26
1	IO_L77N_Y	G26
1	IO_L77P_Y	C28
1	IO_L78N_YY	E27[5]
1	IO_L78P_YY	J25[4]
1	IO_L79N_YY	A30
1	IO_VREF_L79P_YY	H26
1	IO_L80N_YY	G27
1	IO_L80P_YY	B29
1	IO_L81N_Y	F27
1	IO_L81P_Y	C29
1	IO_L82N_Y	E28
1	IO_VREF_L82P_Y	F28
1	IO_L83N_Y	L25

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
1	IO_L83P_Y	B30
1	IO_L84N	B31
1	IO_L84P	E29
1	IO_WRITE_L85N_YY	A31
1	IO_CS_L85P_YY	D30
2	IO	F31[3]
2	IO	J32
2	IO	K27[3]
2	IO	K31[3]
2	IO	L28[3]
2	IO	L30[3]
2	IO	M32[3]
2	IO	N26
2	IO	N28[3]
2	IO	P25[3]
2	IO	U26[3]
2	IO	U30
2	IO	U32[3]
2	IO	U34
2	IO_D2	M30
2	IO_DOUT_BUSY_L86P_YY	D32
2	IO_DIN_D0_L86N_YY	J27
2	IO_L87P_Y	E31
2	IO_L87N_Y	F30
2	IO_L88P_Y	G29
2	IO_L88N_Y	F32
2	IO_VREF_L89P_Y	E32
2	IO_L89N_Y	G30
2	IO_L90P	M25
2	IO_L90N	G31
2	IO_L91P_Y	L26
2	IO_L91N_Y	D33
2	IO_VREF_L92P_Y	D34

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
2	IO_L126N_YY	T32
2	IO_VREF_L127P_Y	U29[1]
2	IO_L127N_Y	U33
2	IO_L128P_YY	V33
2	IO_L128N_YY	U31
3	IO	V27[3]
3	IO	V31
3	IO	V32[3]
3	IO	W33
3	IO	AB25[3]
3	IO	AB26[3]
3	IO	AB31[3]
3	IO	AC31[3]
3	IO	AF34
3	IO	AG31[3]
3	IO	AG33[3]
3	IO	AG34
3	IO	AH29[3]
3	IO	AJ30[3]
3	IO_L129P_Y	V26
3	IO_VREF_L129N_Y	V30[1]
3	IO_L130P_YY	W34
3	IO_L130N_YY	V28
3	IO_L131P_YY	W32
3	IO_VREF_L131N_YY	W30
3	IO_L132P_Y	V29
3	IO_L132N_Y	Y34
3	IO_L133P	W29[5]
3	IO_L133N	Y33[4]
3	IO_L134P_Y	W26
3	IO_L134N_Y	W28
3	IO_L135P_YY	Y31
3	IO_L135N_YY	Y30
3	IO_L136P_YY	AA34[5]
3	IO_L136N_YY	W31[4]
3	IO_D4_L137P_YY	AA33
3	IO_VREF_L137N_YY	Y29
3	IO_L138P_Y	W25
3	IO_L138N_Y	AB34
3	IO_L139P_Y	Y28[5]
3	IO_L139N_Y	AB33[4]
3	IO_L140P_Y	AA30
3	IO_L140N_Y	Y26
3	IO_L141P_YY	Y27
3	IO_L141N_YY	AA31
3	IO_L142P_YY	AA27[5]
3	IO_L142N_YY	AA29[4]
3	IO_L143P_Y	AB32
3	IO_VREF_L143N_Y	AB29
3	IO_L144P_Y	AA28
3	IO_L144N_Y	AC34
3	IO_L145P	Y25
3	IO_L145N	AD34
3	IO_L146P_Y	AB30
3	IO_L146N_Y	AC33
3	IO_L147P_Y	AA26
3	IO_L147N_Y	AC32
3	IO_L148P_Y	AD33
3	IO_L148N_Y	AB28
3	IO_L149P_YY	AE34
3	IO_D5_L149N_YY	AB27
3	IO_D6_L150P_YY	AE33
3	IO_VREF_L150N_YY	AC30
3	IO_L151P_Y	AA25
3	IO_L151N_Y	AE32
3	IO_L152P_YY	AE31
3	IO_L152N_YY	AD29

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
NA	VCCINT	N22
NA	VCCINT	P13
NA	VCCINT	P22
NA	VCCINT	R13
NA	VCCINT	R22
NA	VCCINT	T13
NA	VCCINT	T22
NA	VCCINT	U10
NA	VCCINT	U25
NA	VCCINT	V10
NA	VCCINT	V25
NA	VCCINT	W13
NA	VCCINT	W22
NA	VCCINT	Y13
NA	VCCINT	Y22
NA	VCCINT	AA13
NA	VCCINT	AA22
NA	VCCINT	AB13
NA	VCCINT	AB14
NA	VCCINT	AB15
NA	VCCINT	AB16
NA	VCCINT	AB19
NA	VCCINT	AB20
NA	VCCINT	AB21
NA	VCCINT	AB22
NA	VCCINT	AC12
NA	VCCINT	AC23
NA	VCCINT	AD24
NA	VCCINT	AD11
NA	VCCINT	AE10
NA	VCCINT	AE17
NA	VCCINT	AE18
NA	VCCINT	AE25

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
NA	VCCO_0	M17
NA	VCCO_0	L17
NA	VCCO_0	L16
NA	VCCO_0	E10
NA	VCCO_0	C14
NA	VCCO_0	A6
NA	VCCO_0	M13
NA	VCCO_0	M14
NA	VCCO_0	M15
NA	VCCO_0	M16
NA	VCCO_0	L12
NA	VCCO_0	L13
NA	VCCO_0	L14
NA	VCCO_0	L15
NA	VCCO_1	M18
NA	VCCO_1	L18
NA	VCCO_1	L23
NA	VCCO_1	E25
NA	VCCO_1	C21
NA	VCCO_1	A29
NA	VCCO_1	M19
NA	VCCO_1	M20
NA	VCCO_1	M21
NA	VCCO_1	M22
NA	VCCO_1	L19
NA	VCCO_1	L20
NA	VCCO_1	L21
NA	VCCO_1	L22
NA	VCCO_2	U24
NA	VCCO_2	U23
NA	VCCO_2	N24
NA	VCCO_2	M24
NA	VCCO_2	K30
NA	VCCO_2	F34