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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1536
Number of Logic Elements/Cells	6912
Total RAM Bits	131072
Number of I/O	260
Number of Gates	411955
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	352-LBGA Exposed Pad, Metal
Supplier Device Package	352-MBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv300e-7bg352c

Termination Resistor Packs

Resistor packs are available with the values and the configuration required for LVDS and LVPECL termination from Bourns, Inc., as listed in Table. For pricing and availability, please contact Bourns directly at **http://www.bourns.com**.

Table 40: **Bourns LVDS/LVPECL Resistor Packs**

Part Number	I/O Standard	Term. for:	Pairs/ Pack	Pins
CAT16–LV2F6	LVDS	Driver	2	8
CAT16–LV4F12	LVDS	Driver	4	16
CAT16–PC2F6	LVPECL	Driver	2	8
CAT16–PC4F12	LVPECL	Driver	4	16
CAT16–PT2F2	LVDS/LVPECL	Receiver	2	8
CAT16–PT4F4	LVDS/LVPECL	Receiver	4	16

LVDS Design Guide

The SelectI/O library elements have been expanded for Virtex-E devices to include new LVDS variants. At this time all of the cells might not be included in the Synthesis libraries. The 2.1i-Service Pack 2 update for Alliance and Foundation software includes these cells in the VHDL and Verilog libraries. It is necessary to combine these cells to create the P-side (positive) and N-side (negative) as described in the input, output, 3-state and bidirectional sections.

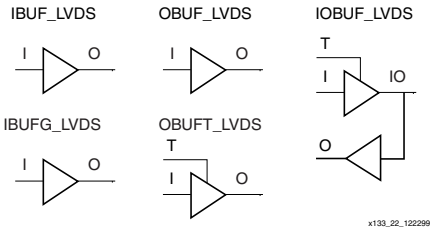

Figure 58: **LVDS elements**

Creating LVDS Global Clock Input Buffers

Global clock input buffers can be combined with adjacent IOBs to form LVDS clock input buffers. P-side is the GCLKPAD location; N-side is the adjacent IO_LVDS_DLL site.

Table 41: **Global Clock Input Buffer Pair Locations**

	GCLK 3		GCLK 2		GCLK 1		GCLK 0	
Pkg	P	N	P	N	P	N	P	N
CS144	A6	C6	A7	B7	M7	M6	K7	N8
PQ240	P213	P215	P210	P209	P89	P87	P92	P93
HQ240	P213	P215	P210	P209	P89	P87	P92	P93
BG352	D14	A15	B14	A13	AF14	AD14	AE13	AC13
BG432	D17	C17	A16	B16	AK16	AL17	AL16	AH15
BG560	A17	C18	D17	E17	AJ17	AM18	AL17	AM17
FG256	B8	A7	C9	A8	R8	T8	N8	N9
FG456	C11	B11	A11	D11	YII	AA11	W12	U12
FG676	E13	B13	C13	F14	AB13	AF13	AA14	AC14
FG680	A20	C22	D21	A19	AU22	AT22	AW19	AT21
FG860	C22	A22	B22	D22	AY22	AW21	BA22	AW20
FG900	C15	A15	E15	E16	AK16	AH16	AJ16	AF16
FG1156	E17	C17	D17	J18	AI19	AL17	AH18	AM18

HDL Instantiation

Only one global clock input buffer is required to be instantiated in the design and placed on the correct GCLKPAD location. The N-side of the buffer is reserved and no other IOB is allowed to be placed on this location.

In the physical device, a configuration option is enabled that routes the pad wire to the differential input buffer located in the GCLKIOB. The output of this buffer then drives the output of the GCLKIOB cell. In EPIC it appears that the second buffer is unused. Any attempt to use this location for another purpose leads to a DRC error in the software.

VHDL Instantiation

```
gclk0_p : IBUFG_LVDS port map
(I=>clk_external, O=>clk_internal);
```

Verilog Instantiation

```
IBUFG_LVDS gclk0_p (.I(clk_external),
.O(clk_internal));
```

Location constraints

All LVDS buffers must be explicitly placed on a device. For the global clock input buffers this can be done with the following constraint in the .ucf or .ncf file.

```
NET clk_external LOC = GCLKPAD3;
```

GCLKPAD3 can also be replaced with the package pin name such as D17 for the BG432 package.

Calculation of T_{ioop} as a Function of Capacitance

T_{ioop} is the propagation delay from the O Input of the IOB to the pad. The values for T_{ioop} are based on the standard capacitive load (C_{sl}) for each I/O standard as listed in Table 3.

Table 3: **Constants for Use in Calculation of T_{ioop}**

Standard	Csl (pF)	fl (ns/pF)
LVTTL Fast Slew Rate, 2mA drive	35	0.41
LVTTL Fast Slew Rate, 4mA drive	35	0.20
LVTTL Fast Slew Rate, 6mA drive	35	0.13
LVTTL Fast Slew Rate, 8mA drive	35	0.079
LVTTL Fast Slew Rate, 12mA drive	35	0.044
LVTTL Fast Slew Rate, 16mA drive	35	0.043
LVTTL Fast Slew Rate, 24mA drive	35	0.033
LVTTL Slow Slew Rate, 2mA drive	35	0.41
LVTTL Slow Slew Rate, 4mA drive	35	0.20
LVTTL Slow Slew Rate, 6mA drive	35	0.10
LVTTL Slow Slew Rate, 8mA drive	35	0.086
LVTTL Slow Slew Rate, 12mA drive	35	0.058
LVTTL Slow Slew Rate, 16mA drive	35	0.050
LVTTL Slow Slew Rate, 24mA drive	35	0.048
LVCMOS2	35	0.041
LVCMOS18	35	0.050
PCI 33 MHZ 3.3 V	10	0.050
PCI 66 MHz 3.3 V	10	0.033
GTL	0	0.014
GTL+	0	0.017
HSTL Class I	20	0.022
HSTL Class III	20	0.016
HSTL Class IV	20	0.014
SSTL2 Class I	30	0.028
SSTL2 Class II	30	0.016
SSTL3 Class I	30	0.029
SSTL3 Class II	30	0.016
CTT	20	0.035
AGP	10	0.037

Notes:
1. I/O parameter measurements are made with the capacitance values shown above. See the application examples (in Module 2 of this data sheet) for appropriate terminations.
2. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

For other capacitive loads, use the formulas below to calculate the corresponding T_{ioop}:

$$T_{ioop} = T_{ioop} + T_{opadjust} + (C_{load} - C_{sl}) * fl$$

where:

$T_{opadjust}$ is reported above in the Output Delay Adjustment section.

C_{load} is the capacitive load for the design.

Table 4: **Delay Measurement Methodology**

Standard	V_L[1]	V_H[1]	Meas. Point	V_{REF} (Typ)[2]
LVTTL	0	3	1.4	-
LVCMOS2	0	2.5	1.125	-
PCI33_3	Per PCI Spec			-
PCI66_3	Per PCI Spec			-
GTL	V_{REF} –0.2	V_{REF} +0.2	V_{REF}	0.80
GTL+	V_{REF} –0.2	V_{REF} +0.2	V_{REF}	1.0
HSTL Class I	V_{REF} –0.5	V_{REF} +0.5	V_{REF}	0.75
HSTL Class III	V_{REF} –0.5	V_{REF} +0.5	V_{REF}	0.90
HSTL Class IV	V_{REF} –0.5	V_{REF} +0.5	V_{REF}	0.90
SSTL3 I & II	V_{REF} –1.0	V_{REF} +1.0	V_{REF}	1.5
SSTL2 I & II	V_{REF} –0.75	V_{REF} +0.75	V_{REF}	1.25
CTT	V_{REF} –0.2	V_{REF} +0.2	V_{REF}	1.5
AGP	V_{REF} – (0.2xV_{CCO})	V_{REF} + (0.2xV_{CCO})	V_{REF}	Per AGP Spec
LVDS	1.2 –0.125	1.2 + 0.125	1.2	
LVPECL	1.6 –0.3	1.6 + 0.3	1.6	

Notes:
1. Input waveform switches between V_L and V_H.
2. Measurements are made at V_{REF} (Typ), Maximum, and Minimum. Worst-case values are reported.

   I/O parameter measurements are made with the capacitance values shown in Table 3. See the application examples (in Module 2 of this data sheet) for appropriate terminations.

   I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *without* DLL

Description[1]	Symbol	Device	Speed Grade[2]				Units
			Min	-8	-7	-6	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *without* DLL. For data *output* with different standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 10.	T_{ICKOF}	XCV50E	1.5	4.2	4.4	4.6	ns
		XCV100E	1.5	4.2	4.4	4.6	ns
		XCV200E	1.5	4.3	4.5	4.7	ns
		XCV300E	1.5	4.3	4.5	4.7	ns
		XCV400E	1.5	4.4	4.6	4.8	ns
		XCV600E	1.6	4.5	4.7	4.9	ns
		XCV1000E	1.7	4.6	4.8	5.0	ns
		XCV1600E	1.8	4.7	4.9	5.1	ns
		XCV2000E	1.8	4.8	5.0	5.2	ns
		XCV2600E	2.0	5.0	5.2	5.4	ns
		XCV3200E	2.2	5.2	5.4	5.6	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For other I/O standards and different loads, see Table 3 and Table 4.

Global Clock Set-Up and Hold for LVTTL Standard, *without* DLL

Description[1]	Symbol	Device	Speed Grade[2, 3]				Units
			Min	-8	-7	-6	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in **IOB Input Switching Characteristics Standard Adjustments**, page 8.							
Full Delay	T_{PSFD}/T_{PHFD}	XCV50E	1.8 / 0	1.8 / 0	1.8 / 0	1.8 / 0	ns
Global Clock and IFF, without DLL		XCV100E	1.8 / 0	1.8 / 0	1.8 / 0	1.8 / 0	ns
		XCV200E	1.9 / 0	1.9 / 0	1.9 / 0	1.9 / 0	ns
		XCV300E	2.0 / 0	2.0 / 0	2.0 / 0	2.0 / 0	ns
		XCV400E	2.0 / 0	2.0 / 0	2.0 / 0	2.0 / 0	ns
		XCV600E	2.1 / 0	2.1 / 0	2.1 / 0	2.1 / 0	ns
		XCV1000E	2.3 / 0	2.3 / 0	2.3 / 0	2.3 / 0	ns
		XCV1600E	2.5 / 0	2.5 / 0	2.5 / 0	2.5 / 0	ns
		XCV2000E	2.5 / 0	2.5 / 0	2.5 / 0	2.5 / 0	ns
		XCV2600E	2.7 / 0	2.7 / 0	2.7 / 0	2.7 / 0	ns
		XCV3200E	2.8 / 0	2.8 / 0	2.8 / 0	2.8 / 0	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

DLL Clock Tolerance, Jitter, and Phase Information

All DLL output jitter and phase specifications determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers.

			CLKDLLHF		CLKDLL		
Description	**Symbol**	**F_{CLKIN}**	**Min**	**Max**	**Min**	**Max**	**Units**
Input Clock Period Tolerance	T_{IPTOL}		-	1.0	-	1.0	ns
Input Clock Jitter Tolerance (Cycle to Cycle)	T_{IJITCC}		-	± 150	-	± 300	ps
Time Required for DLL to Acquire Lock(6)	T_{LOCK}	> 60 MHz	-	20	-	20	µs
		50 - 60 MHz	-	-	-	25	µs
		40 - 50 MHz	-	-	-	50	µs
		30 - 40 MHz	-	-	-	90	µs
		25 - 30 MHz	-	-	-	120	µs
Output Jitter (cycle-to-cycle) for any DLL Clock Output(1)	T_{OJITCC}			± 60		± 60	ps
Phase Offset between CLKIN and CLKO(2)	T_{PHIO}			± 100		± 100	ps
Phase Offset between Clock Outputs on the DLL(3)	T_{PHOO}			± 140		± 140	ps
Maximum Phase Difference between CLKIN and CLKO(4)	T_{PHIOM}			± 160		± 160	ps
Maximum Phase Difference between Clock Outputs on the DLL(5)	T_{PHOOM}			± 200		± 200	ps

Notes:

1. **Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock and is based on a maximum tap delay resolution, *excluding* input clock jitter.
2. **Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* Output Jitter and input clock jitter.
3. **Phase Offset between Clock Outputs on the DLL** is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* Output Jitter and input clock jitter.
4. **Maximum Phase Difference between CLKIN an CLKO** is the sum of Output Jitter and Phase Offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).
5. **Maximum Phase DIfference between Clock Outputs on the DLL** is the sum of Output JItter and Phase Offset between any DLL clock outputs, or the greatest difference between any two DLL output rising edges sue to DLL alone (*excluding* input clock jitter).
6. Add 30% to the value for industrial grade parts.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/7/99	1.0	Initial Xilinx release.
1/10/00	1.1	Re-released with spd.txt v. 1.18, FG860/900/1156 package information, and additional DLL, Select RAM and SelectI/O information.
1/28/00	1.2	Added Delay Measurement Methodology table, updated SelectI/O section, Figures 30, 54, & 55, text explaining Table 5, T_{BYP} values, buffered Hex Line info, p. 8, I/O Timing Measurement notes, notes for Tables 15, 16, and corrected F1156 pinout table footnote references.
2/29/00	1.3	Updated pinout tables, V_{CC} page 20, and corrected Figure 20.
5/23/00	1.4	Correction to table on p. 22.
7/10/00	1.5	• Numerous minor edits. • Data sheet upgraded to Preliminary. • Preview -8 numbers added to **Virtex-E Electrical Characteristics** tables.
8/1/00	1.6	• Reformatted entire document to follow new style guidelines. • Changed speed grade values in tables on pages 35-37.
9/20/00	1.7	• Min values added to **Virtex-E Electrical Characteristics** tables. • XCV2600E and XCV3200E numbers added to **Virtex-E Electrical Characteristics** tables (Module 3). • Corrected user I/O count for XCV100E device in Table 1 (Module 1). • Changed several pins to “No Connect in the XCV100E“ and removed duplicate V_{CCINT} pins in Table ~ (Module 4). • Changed pin J10 to “No connect in XCV600E” in Table 74 (Module 4). • Changed pin J30 to “VREF option only in the XCV600E” in Table 74 (Module 4). • Corrected pair 18 in Table 75 (Module 4) to be “AO in the XCV1000E, XCV1600E“.
11/20/00	1.8	• Upgraded speed grade -8 numbers in **Virtex-E Electrical Characteristics** tables to Preliminary. • Updated minimums in Table 13 and added notes to Table 14. • Added to note 2 to **Absolute Maximum Ratings**. • Changed speed grade -8 numbers for $T_{SHCKO32}$, T_{REG}, T_{BCCS}, and T_{ICKOF} • Changed all minimum hold times to –0.4 under **Global Clock Set-Up and Hold for LVTTL Standard, with DLL**. • Revised maximum T_{DLLPW} in -6 speed grade for **DLL Timing Parameters**. • Changed GCLK0 to BA22 for FG860 package in Table 46.
2/12/01	1.9	• Revised footnote for Table 14. • Added numbers to **Virtex-E Electrical Characteristics** tables for XCV1000E and XCV2000E devices. • Updated Table 27 and Table 78 to include values for XCV400E and XCV600E devices. • Revised Table 62 to include pinout information for the XCV400E and XCV600E devices in the BG560 package. • Updated footnotes 1 and 2 for Table 76 to include XCV2600E and XCV3200E devices.
4/02/01	2.0	• Updated numerous values in **Virtex-E Switching Characteristics** tables. • Converted data sheet to modularized format. See the **Virtex-E Data Sheet** section.
4/19/01	2.1	• Updated values in **Virtex-E Switching Characteristics** tables.

Table 4: **CS144 — XCV50E, XCV100E, XCV200E**

Bank	Pin Description	Pin #
4	IO_L15N_YY	M11
4	IO_L15P_YY	L11
4	IO_L16N_YY	K9
4	IO_VREF_L16P_YY	N10[2]
4	IO_L17N_YY	K8
4	IO_L17P_YY	N9
4	IO_LVDS_DLL_L18P	N8
4	IO_VREF	L8
4	IO_VREF	L10
4	IO_VREF	N11[1]
5	GCK1	M7
5	IO	M4
5	IO_LVDS_DLL_L18N	M6
5	IO_L19N_YY	N5
5	IO_L19P_YY	K6
5	IO_VREF_L20N_YY	N4[2]
5	IO_L20P_YY	K5
5	IO_L21N_YY	M3
5	IO_L21P_YY	N3
5	IO_VREF	K4[1]
5	IO_VREF	L4
5	IO_VREF	L6
6	IO	G4
6	IO	J4
6	IO_L25P	H1
6	IO_VREF_L25N	H2
6	IO_L24P_YY	H3
6	IO_L24N_YY	H4
6	IO_L23P	J2
6	IO_VREF_L23N	J3[2]
6	IO_VREF	K1
6	IO_VREF	K2[1]
6	IO_L22N_YY	L1
6	IO_L22P_YY	K3

Table 4: **CS144 — XCV50E, XCV100E, XCV200E**

Bank	Pin Description	Pin #
6	IO_L26N	G1
7	IO	C2
7	IO	D3
7	IO	F3
7	IO_L26P	F2
7	IO_L27N	F4
7	IO_VREF_L27P	E1
7	IO_L28N_YY	E2
7	IO_L28P_YY	E3
7	IO_L29N	D1
7	IO_VREF_L29P	D2[2]
7	IO_VREF	C1[1]
7	IO_VREF	D4
2	CCLK	B13
3	DONE	M12
NA	M0	M1
NA	M1	L2
NA	M2	N2
NA	PROGRAM	L12
NA	TDI	A11
NA	TCK	C3
2	TDO	A12
NA	TMS	B1
NA	VCCINT	A9
NA	VCCINT	B6
NA	VCCINT	C5
NA	VCCINT	G3
NA	VCCINT	G12
NA	VCCINT	M5
NA	VCCINT	M9
NA	VCCINT	N6
0	VCCO	A2

Table 10: **BG352 — XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
2	IO_D3_L30N _Y	M3
2	IO_L31P	M2
2	IO_L31N	M1
2	IO	N3[1]
2	IO_L32P_YY	N4
2	IO_L32N_YY	N2
3	IO	P1
3	IO	P3[1]
3	IO_L33P	R1
3	IO_L33N	R2
3	IO_D4_L34P _Y	R3
3	IO_VREF_3_L34N _Y	R4
3	IO_L35P_YY	T2
3	IO_L35N_YY	U2
3	IO	T3[1]
3	IO_L36P	T4
3	IO_L36N	V1
3	IO	V2[1]
3	IO_L37P_YY	U3
3	IO_D5_L37N_YY	U4
3	IO_D6_L38P _Y	V3
3	IO_VREF_3_L38N _Y	V4
3	IO_L39P _Y	Y1
3	IO_L39N _Y	Y2
3	IO	W3
3	IO	W4[1]
3	IO	AA1[1]
3	IO_L40P_Y	AA2
3	IO_VREF_3_L40N_Y	Y3
3	IO_L41P_YY	AC1
3	IO_L41N_YY	AB2
3	IO	AA3[1]
3	IO_L42P_YY	AA4

Table 10: **BG352 — XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
3	IO_VREF_3_L42N_YY	AC2[2]
3	IO	AB3
3	IO	AD1[1]
3	IO	AB4[1]
3	IO_D7_L43P_YY	AC3
3	IO_INIT_L43N_YY	AD2
4	IO_L44P_YY	AC5
4	IO_L44N_YY	AD4
4	IO	AE3[1]
4	IO	AD5[1]
4	IO	AC6
4	IO_VREF_4_L45P_YY	AE4[2]
4	IO_L45N_YY	AF3
4	IO	AF4[1]
4	IO_L46P_YY	AC7
4	IO_L46N_YY	AD6
4	IO_VREF_4_L47P_YY	AE5
4	IO_L47N_YY	AE6
4	IO	AD7[1]
4	IO	AE7[1]
4	IO_L48P	AF6
4	IO_L48N	AC9
4	IO	AD8
4	IO_VREF_4_L49P_YY	AE8
4	IO_L49N_YY	AF7
4	IO_L50P_YY	AD9
4	IO_L50N_YY	AE9
4	IO	AD10[1]
4	IO_L51P	AF9
4	IO_L51N	AC11
4	IO	AE10[1]
4	IO_L52P_Y	AD11
4	IO_L52N_Y	AE11

Table 13: **BG432 Differential Pin Pair Summary XCV300E, XCV400E, XC600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
48	2	N1	P4	√	D3
49	2	P3	P2	4	-
50	2	R3	R4	1	VREF
51	2	R1	T3	√	-
52	3	U4	U2	1	VREF
53	3	U1	V3	4	-
54	3	V4	V2	√	VREF
55	3	W3	W4	1	-
56	3	Y1	Y3	1	-
57	3	Y4	Y2	4	-
58	3	AA3	AB1	√	D5
59	3	AB3	AB4	√	VREF
60	3	AD1	AC3	1	VREF
61	3	AC4	AD2	4	-
62	3	AD3	AD4	√	VREF
63	3	AF2	AE3	1	-
64	3	AE4	AG1	5	-
65	3	AG2	AF3	1	VREF
66	3	AF4	AH1	4	-
67	3	AH2	AG3	3	-
68	3	AG4	AJ2	√	INIT
69	4	AJ4	AK3	√	-
70	4	AH5	AK4	1	-
71	4	AJ5	AH6	√	-
72	4	AL4	AK5	√	VREF
73	4	AJ6	AH7	2	-
74	4	AL5	AK6	√	-
75	4	AJ7	AL6	√	VREF
76	4	AH9	AJ8	1	-
77	4	AK8	AJ9	1	VREF
78	4	AL8	AK9	√	VREF
79	4	AK10	AL10	√	-

Table 13: **BG432 Differential Pin Pair Summary XCV300E, XCV400E, XC600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
80	4	AH12	AK11	√	-
81	4	AJ12	AK12	√	-
82	4	AH13	AJ13	√	-
83	4	AL13	AK14	√	VREF
84	4	AH14	AJ14	1	-
85	4	AK15	AJ15	1	VREF
86	5	AH15	AL17	NA	IO_LVDS_DLL
87	5	AK17	AJ17	1	VREF
88	5	AH17	AK18	1	-
89	5	AL19	AJ18	√	VREF
90	5	AH18	AL20	√	-
91	5	AK20	AH19	√	-
92	5	AJ20	AK21	√	-
93	5	AJ21	AL22	√	-
94	5	AJ22	AK23	√	VREF
95	5	AH22	AL24	1	VREF
96	5	AK24	AH23	1	-
97	5	AK25	AJ25	√	VREF
98	5	AL26	AK26	√	-
99	5	AH25	AL27	2	-
100	5	AJ26	AK27	√	VREF
101	5	AH26	AL28	√	-
102	5	AJ27	AK28	1	-
103	6	AH30	AJ30	√	-
104	6	AH31	AG28	3	-
105	6	AG30	AG29	4	-
106	6	AG31	AF28	1	VREF
107	6	AF30	AF29	5	-
108	6	AF31	AE28	1	-
109	6	AD28	AE30	√	VREF
110	6	AD31	AD30	4	-
111	6	AC29	AC28	1	VREF

Table 13: **BG432 Differential Pin Pair Summary XCV300E, XCV400E, XC600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
112	6	AB29	AB28	√	VREF
113	6	AA29	AB31	√	-
114	6	Y29	Y28	4	-
115	6	Y31	Y30	1	-
116	6	W30	W29	1	-
117	6	V29	V28	√	VREF
118	6	U29	V30	4	-
119	6	U30	U28	1	VREF
120	7	R29	T31	√	-
121	7	R31	R30	1	VREF
122	7	P28	P29	4	-
123	7	N30	P30	√	VREF
124	7	N31	N28	1	-
125	7	M28	M29	1	-
126	7	L30	M30	4	-
127	7	K30	K31	√	-
128	7	J30	K28	√	VREF
129	7	J28	J29	1	VREF
130	7	G30	H30	4	-
131	7	F31	H28	√	VREF
132	7	G28	G29	1	-
133	7	E30	E31	5	-
134	7	F28	F29	1	VREF
135	7	D30	D31	4	-
136	7	E28	E29	3	-

Notes:
1. AO in the XCV300E, 600E.
2. AO in the XCV300E.
3. AO in the XCV400E, 600E.
4. AO in the XCV300E, 400E.
5. AO in the XCV600E.

BG560 Ball Grid Array Packages

XCV1000E, XCV1600E, and XCV2000E devices in BG560 Ball Grid Array packages have footprint compatibility. Pins labeled I0_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 14, see Table 15 for Differential Pair information.

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
0	GCK3	A17	
0	IO	A27	
0	IO	B25	
0	IO	C28	
0	IO	C30	
0	IO	D30	
0	IO_L0N	E28	
0	IO_VREF_L0P	D29	3
0	IO_L1N_YY	D28	
0	IO_L1P_YY	A31	
0	IO_VREF_L2N_YY	E27	
0	IO_L2P_YY	C29	
0	IO_L3N_Y	B30	
0	IO_L3P_Y	D27	
0	IO_L4N_YY	E26	
0	IO_L4P_YY	B29	
0	IO_VREF_L5N_YY	D26	
0	IO_L5P_YY	C27	
0	IO_L6N_Y	E25	
0	IO_VREF_L6P_Y	A28	1
0	IO_L7N_Y	D25	
0	IO_L7P_Y	C26	
0	IO_VREF_L8N_Y	E24	4
0	IO_L8P_Y	B26	
0	IO_L9N_Y	C25	
0	IO_L9P_Y	D24	
0	IO_VREF_L10N_YY	E23	
0	IO_L10P_YY	A25	
0	IO_L11N_YY	D23	

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
1	IO_L23P_Y	A17
1	IO_L24N_YY	B17
1	IO_VREF_L24P_YY	A18
1	IO_L25N_YY	D16
1	IO_L25P_YY	C17
1	IO_L26N_YY	B18
1	IO_VREF_L26P_YY	A19
1	IO_L27N_YY	D17
1	IO_L27P_YY	C18
1	IO_WRITE_L28N_YY	A20
1	IO_CS_L28P_YY	C19
2	IO	D18[1]
2	IO	E19[1]
2	IO	E20
2	IO	F20
2	IO	G21
2	IO	G22[1]
2	IO	J22
2	IO	L19[1]
2	IO_D3	K20
2	IO_DOUT_BUSY_L29P_YY	C21
2	IO_DIN_D0_L29N_YY	D20
2	IO_L30P_YY	C22
2	IO_L30N_YY	D21
2	IO_VREF_L31P_YY	D22
2	IO_L31N_YY	E21
2	IO_L32P_YY	E22
2	IO_L32N_YY	F18
2	IO_VREF_L33P_YY	F21
2	IO_L33N_YY	F19
2	IO_L34P_Y	F22
2	IO_L34N_Y	G19
2	IO_L35P_Y	G20
2	IO_L35N_Y	G18
2	IO_VREF_L36P_Y	H18
2	IO_D1_L36N_Y	H22

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
2	IO_D2_L37P_YY	H20
2	IO_L37N_YY	H19
2	IO_L38P_YY	H21
2	IO_L38N_YY	J19
2	IO_L39P_YY	J18
2	IO_L39N_YY	J20
2	IO_L40P_Y	K18
2	IO_L40N_Y	J21
2	IO_L41P	K22
2	IO_VREF_L41N	K21
2	IO_L42P_Y	K19
2	IO_L42N_Y	L22
2	IO_L43P_YY	L21
2	IO_L43N_YY	L18
2	IO_L44P_YY	L17
2	IO_L44N_YY	L20
3	IO	M21[1]
3	IO	P22
3	IO	R20[1]
3	IO	R22
3	IO	T19
3	IO	U18[1]
3	IO	V20
3	IO	V21
3	IO	Y22[1]
3	IO_L45P_YY	M18
3	IO_L45N_YY	M20
3	IO_L46P_Y	M19
3	IO_L46N_Y	M17
3	IO_D4_L47P_Y	N22
3	IO_VREF_L47N_Y	N21
3	IO_L48P_YY	N20
3	IO_L48N_YY	N18
3	IO_L49P_YY	N19
3	IO_L49N_YY	P21
3	IO_L50P_YY	P20

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
0	IO_L9N	A7
0	IO_L9P	D9
0	IO_L10N	B8
0	IO_VREF_L10P	G10
0	IO_L11N_YY	C9
0	IO_L11P_YY	F10
0	IO_L12N_Y	A8
0	IO_L12P_Y	E10
0	IO_L13N_YY	G11
0	IO_L13P_YY	D10
0	IO_L14N_YY	B10
0	IO_L14P_YY	F11
0	IO_L15N	C10
0	IO_L15P	E11
0	IO_L16N_YY	G12
0	IO_L16P_YY	D11
0	IO_VREF_L17N_YY	C11
0	IO_L17P_YY	F12
0	IO_L18N_YY	A11
0	IO_L18P_YY	E12
0	IO_L19N_Y	D12
0	IO_L19P_Y	C12
0	IO_VREF_L20N_Y	A12
0	IO_L20P_Y	H13
0	IO_LVDS_DLL_L21N	B13
1	GCK2	C13
1	IO	A13[1]
1	IO	A16[1]
1	IO	A19
1	IO	A20
1	IO	A22
1	IO	A24[1]
1	IO	B15[1]
1	IO	B17[1]
1	IO	B23
1	IO_LVDS_DLL_L21P	F14

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
1	IO_L22N	E14
1	IO_L22P	F13
1	IO_L23N_Y	D14
1	IO_VREF_L23P_Y	A14
1	IO_L24N_Y	C14
1	IO_L24P_Y	H14
1	IO_L25N_YY	G14
1	IO_L25P_YY	C15
1	IO_L26N_YY	E15
1	IO_VREF_L26P_YY	D15
1	IO_L27N_YY	C16
1	IO_L27P_YY	F15
1	IO_L28N	G15
1	IO_L28P	D16
1	IO_L29N_YY	E16
1	IO_L29P_YY	A17
1	IO_L30N_YY	C17
1	IO_L30P_YY	E17
1	IO_L31N_Y	F16
1	IO_L31P_Y	D17
1	IO_L32N_YY	F17
1	IO_L32P_YY	C18
1	IO_L33N_YY	A18
1	IO_VREF_L33P_YY	G16
1	IO_L34N_YY	C19
1	IO_L34P_YY	G17
1	IO_L35N_Y	D18
1	IO_VREF_L35P_Y	B19[2]
1	IO_L36N_Y	D19
1	IO_L36P_Y	E18
1	IO_L37N_YY	F18
1	IO_L37P_YY	B20
1	IO_L38N_YY	G19
1	IO_VREF_L38P_YY	C20
1	IO_L39N_YY	G18
1	IO_L39P_YY	E19
1	IO_L40N_YY	A21

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
0	VCCO	H10
1	VCCO	J15
1	VCCO	J14
1	VCCO	H18
1	VCCO	H17
1	VCCO	H16
1	VCCO	H15
2	VCCO	N18
2	VCCO	M19
2	VCCO	M18
2	VCCO	L19
2	VCCO	K19
2	VCCO	J19
3	VCCO	V19
3	VCCO	U19
3	VCCO	T19
3	VCCO	R19
3	VCCO	R18
3	VCCO	P18
4	VCCO	W18
4	VCCO	W17
4	VCCO	W16
4	VCCO	W15
4	VCCO	V15
4	VCCO	V14
5	VCCO	W9
5	VCCO	W12
5	VCCO	W11
5	VCCO	W10
5	VCCO	V13
5	VCCO	V12
6	VCCO	V8
6	VCCO	U8
6	VCCO	T8
6	VCCO	R9
6	VCCO	R8
6	VCCO	P9

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
7	VCCO	N9
7	VCCO	M9
7	VCCO	M8
7	VCCO	L8
7	VCCO	K8
7	VCCO	J8
NA	GND	V25
NA	GND	V2
NA	GND	U17
NA	GND	U16
NA	GND	U15
NA	GND	U14
NA	GND	U13
NA	GND	U12
NA	GND	U11
NA	GND	U10
NA	GND	T17
NA	GND	T16
NA	GND	T15
NA	GND	T14
NA	GND	T13
NA	GND	T12
NA	GND	T11
NA	GND	T10
NA	GND	R17
NA	GND	R16
NA	GND	R15
NA	GND	R14
NA	GND	R13
NA	GND	R12
NA	GND	R11
NA	GND	R10
NA	GND	P25
NA	GND	P17
NA	GND	P16
NA	GND	P15

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
4	IO_VREF_L132P_YY	AV8
4	IO_L132N_YY	AU9
4	IO_L133P_Y	AW8
4	IO_L133N_Y	AT10
4	IO_VREF_L134P_Y	AV9[3]
4	IO_L134N_Y	AU10
4	IO_L135P_YY	AW9
4	IO_L135N_YY	AT11
4	IO_VREF_L136P_YY	AV10
4	IO_L136N_YY	AU11
4	IO_L137P_Y	AW10
4	IO_L137N_Y	AU12
4	IO_L138P_Y	AV11
4	IO_L138N_Y	AT13
4	IO_VREF_L139P_YY	AW11
4	IO_L139N_YY	AU13
4	IO_L140P_YY	AT14
4	IO_L140N_YY	AV12
4	IO_L141P_Y	AU14
4	IO_L141N_Y	AW12
4	IO_L142P_Y	AT15
4	IO_L142N_Y	AV13
4	IO_L143P_YY	AU15
4	IO_L143N_YY	AW13
4	IO_VREF_L144P_YY	AV14[1]
4	IO_L144N_YY	AT16
4	IO_L145P_Y	AW14
4	IO_L145N_Y	AU16
4	IO_L146P_Y	AV15
4	IO_L146N_Y	AR17
4	IO_L147P_YY	AW15
4	IO_L147N_YY	AT17
4	IO_VREF_L148P_YY	AU17
4	IO_L148N_YY	AV16
4	IO_L149P_Y	AR18
4	IO_L149N_Y	AW16

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
4	IO_L150P_Y	AT18
4	IO_L150N_Y	AV17
4	IO_L151P_YY	AU18
4	IO_L151N_YY	AW17
4	IO_VREF_L152P_YY	AT19
4	IO_L152N_YY	AV18
4	IO_L153P_Y	AU19
4	IO_L153N_Y	AW18
4	IO_VREF_L154P	AU21[2]
4	IO_L154N	AV19
4	IO_LVDS_DLL_L155P	AT21
5	GCK1	AU22
5	IO	AT34
5	IO	AW20
5	IO_LVDS_DLL_L155N	AT22
5	IO_VREF_L156P_Y	AV20[2]
5	IO_L156N_Y	AR22
5	IO_L157P_YY	AV23
5	IO_VREF_L157N_YY	AW21
5	IO_L158P_YY	AU23
5	IO_L158N_YY	AV21
5	IO_L159P_Y	AT23
5	IO_L159N_Y	AW22
5	IO_L160P_Y	AR23
5	IO_L160N_Y	AV22
5	IO_L161P_YY	AV24
5	IO_VREF_L161N_YY	AW23
5	IO_L162P_YY	AW24
5	IO_L162N_YY	AU24
5	IO_L163P_Y	AW25
5	IO_L163N_Y	AT24
5	IO_L164P_Y	AV25
5	IO_L164N_Y	AU25
5	IO_L165P_YY	AW26
5	IO_VREF_L165N_YY	AT25[1]

FG680 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 23: **FG680 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
GCLK LVDS					
3	0	A20	C22	NA	IO_DLL_L29N
2	1	D21	A19	NA	IO_DLL_L29P
1	5	AU22	AT22	NA	IO_DLL_L155N
0	4	AW19	AT21	NA	IO_DLL_L155P
IO LVDS Total Pairs: 247, Asynchronous Output Pairs: 111					
0	0	A36	C35	5	-
1	0	B35	D34	5	VREF
2	0	A35	C34	√	-
3	0	B34	D33	√	VREF
4	0	A34	C33	3	-
5	0	B33	D32	3	-
6	0	D31	C32	√	-
7	0	C31	A33	√	VREF
8	0	B31	B32	5	-
9	0	D30	A32	5	VREF
10	0	C30	A31	√	-
11	0	D29	B30	√	VREF
12	0	C29	A30	2	-
13	0	B29	A29	2	-
14	0	A28	B28	√	VREF
15	0	B27	C28	√	-
16	0	A27	D27	5	-
17	0	B26	C27	5	-

Table 23: **FG680 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
18	0	C26	D26	√	-
19	0	D25	A26	√	VREF
20	0	C25	B25	3	-
21	0	D24	A25	3	-
22	0	B23	A24	√	-
23	0	A23	C24	√	VREF
24	0	B22	B24	5	-
25	0	A22	E23	5	-
26	0	B21	D23	√	-
27	0	A21	C23	√	VREF
28	0	B20	E22	2	-
29	1	A19	C22	NA	IO_LVDS_DLL
30	1	B19	C21	2	VREF
31	1	A18	C19	2	-
32	1	B18	D19	√	VREF
33	1	A17	C18	√	-
34	1	B17	D18	5	-
35	1	A16	E18	5	-
36	1	D17	C17	√	VREF
37	1	E17	B16	√	-
38	1	C16	A15	3	-
39	1	D16	B15	3	-
40	1	B14	A14	√	VREF
41	1	A13	C15	√	-
42	1	B13	D15	5	-
43	1	A12	C14	5	-
44	1	C13	D14	√	-
45	1	D13	B12	√	VREF
46	1	C12	A11	2	-
47	1	C11	B11	2	-
48	1	D11	A10	√	VREF
49	1	C10	B10	√	-
50	1	D10	A9	5	VREF
51	1	C9	B9	5	-

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
5	IO_L182N	AF13
5	IO_L183P	AH14
5	IO_L183N	AJ14
5	IO_L184P_YY	AE14
5	IO_VREF_L184N_YY	AG13
5	IO_L185P_YY	AK13
5	IO_L185N_YY	AD13
5	IO_L186P	AE13
5	IO_L186N	AF12
5	IO_L187P	AC13
5	IO_L187N	AA13
5	IO_L188P_YY	AA12
5	IO_VREF_L188N_YY	AJ12[1]
5	IO_L189P_YY	AB12
5	IO_L189N_YY	AE11
5	IO_L190P	AK12[4]
5	IO_L190N	Y13[4]
5	IO_L191P	AG11
5	IO_L191N	AF11
5	IO_L192P	AH11
5	IO_L192N	AJ11
5	IO_L193P_YY	AE12[4]
5	IO_L193N_YY	AG10[4]
5	IO_L194P_YY	AD12
5	IO_L194N_YY	AK11
5	IO_L195P_YY	AJ10
5	IO_VREF_L195N_YY	AC12
5	IO_L196P_YY	AK10
5	IO_L196N_YY	AD11
5	IO_L197P_YY	AJ9
5	IO_L197N_YY	AE9
5	IO_L198P_YY	AH10
5	IO_VREF_L198N_YY	AF9
5	IO_L199P_YY	AH9
5	IO_L199N_YY	AK9
5	IO_L200P	AF8
5	IO_L200N	AB11

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
5	IO_L201P	AC11
5	IO_L201N	AG8
5	IO_L202P_YY	AK8
5	IO_VREF_L202N_YY	AF7
5	IO_L203P_YY	AG7
5	IO_L203N_YY	AK7
5	IO_L204P	AJ7
5	IO_L204N	AD10
5	IO_L205P	AH6
5	IO_L205N	AC10
5	IO_L206P_YY	AD9
5	IO_VREF_L206N_YY	AG6
5	IO_L207P_YY	AB10
5	IO_L207N_YY	AJ5
5	IO_L208P	AD8[4]
5	IO_L208N	AK5[4]
5	IO_L209P	AC9
5	IO_VREF_L209N	AJ4[1]
5	IO_L210P	AG5
5	IO_L210N	AK4
5	IO_L211P_YY	AH5[3]
5	IO_L211N_YY	AG3[4]
6	IO	T2[4]
6	IO	T10[4]
6	IO	U1
6	IO	U4[5]
6	IO	U6[4]
6	IO	U7[4]
6	IO	V1[4]
6	IO	V5[5]
6	IO	V8
6	IO	Y10[4]
6	IO	AA4[4]
6	IO	AB5[5]
6	IO	AB7[4]
6	IO	AC3[5]

Table 27: **FG900 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
256	7	N6	M6	1	-
257	7	N1	N5	4	-
258	7	M5	M4	√	-
259	7	M1	M2	1	VREF
260	7	L2	L4	4	-
261	7	L5	M7	3	-
262	7	M8	L1	4	-
263	7	M9	K2	1	-
264	7	M10	L3	NA	-
265	7	K1	K5	√	-
266	7	K3	L6	√	VREF
267	7	K4	L7	4	-
268	7	J5	L8	4	-
269	7	H4	K6	4	VREF
270	7	K7	H1	4	-
271	7	J2	J7	2	-
272	7	G2	H5	√	-
273	7	G5	L9	√	VREF
274	7	K8	F3	1	-
275	7	E1	G3	4	-
276	7	E2	H6	√	-
277	7	K9	E4	1	VREF
278	7	F4	J8	4	-
279	7	H7	D1	3	-
280	7	C2	G6	4	VREF
281	7	F5	D2	1	-
282	7	K10	D3	4	-

Notes:
1. AO in the XCV600E, 1000E.
2. AO in the XCV1000E.
3. AO in the XCV1600E.
4. AO in the XCV1000E, XCV1600E.

FG1156 Fine-Pitch Ball Grid Array Package

XCV1000E, XCV1600E, XCV2000E, XCV2600E, and XCV3200E devices in the FG1156 fine-pitch Ball Grid Array package have footprint compatibility. Pins labeled IO_VREF can be used as either V_{REF} or general I/O, unless indicated in the footnotes. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 28, see Table 29 for Differential Pair information.

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
0	GCK3	E17
0	IO	B4
0	IO	B9
0	IO	B10
0	IO	D9[3]
0	IO	D16
0	IO	E7[3]
0	IO	E11[3]
0	IO	E13[3]
0	IO	E16[3]
0	IO	F17[3]
0	IO	J12[3]
0	IO	J13[3]
0	IO	J14[3]
0	IO	K11[3]
0	IO_L0N_Y	F7
0	IO_L0P_Y	H9
0	IO_L1N_Y	C5
0	IO_L1P_Y	J10
0	IO_VREF_L2N_Y	E6
0	IO_L2P_Y	D6
0	IO_L3N_Y	A4
0	IO_L3P_Y	G8
0	IO_L4N_YY	C6
0	IO_L4P_YY	J11
0	IO_VREF_L5N_YY	G9
0	IO_L5P_YY	F8
0	IO_L6N_YY	A5[4]

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
4	IO_L178N_YY	AL28
4	IO_L179P_YY	AE24[4]
4	IO_L179N_YY	AN28[5]
4	IO_L180P_Y	AJ27
4	IO_L180N_Y	AH26
4	IO_L181P_Y	AG25
4	IO_L181N_Y	AK27
4	IO_L182P	AM28[4]
4	IO_L182N	AF24[5]
4	IO_L183P_YY	AJ26
4	IO_L183N_YY	AP27
4	IO_VREF_L184P_YY	AK26
4	IO_L184N_YY	AN27
4	IO_L185P	AE23[4]
4	IO_L185N	AM27[5]
4	IO_L186P_Y	AL26
4	IO_L186N_Y	AP26
4	IO_VREF_L187P_Y	AN26[2]
4	IO_L187N_Y	AJ25
4	IO_L188P	AG24[4]
4	IO_L188N	AP25[5]
4	IO_L189P_YY	AF23
4	IO_L189N_YY	AM26
4	IO_VREF_L190P_YY	AJ24
4	IO_L190N_YY	AN25
4	IO_L191P_Y	AE22
4	IO_L191N_Y	AM25
4	IO_L192P_Y	AK24
4	IO_L192N_Y	AH23
4	IO_VREF_L193P_YY	AF22
4	IO_L193N_YY	AP24
4	IO_L194P_YY	AL24
4	IO_L194N_YY	AK23
4	IO_L195P_Y	AG22

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
4	IO_L195N_Y	AN23
4	IO_L196P_Y	AP23
4	IO_L196N_Y	AM23
4	IO_L197P_Y	AH22
4	IO_L197N_Y	AP22
4	IO_L198P_Y	AL23
4	IO_L198N_Y	AF21
4	IO_L199P_YY	AL22
4	IO_L199N_YY	AJ22
4	IO_VREF_L200P_YY	AK22
4	IO_L200N_YY	AM22
4	IO_L201P_YY	AG21[4]
4	IO_L201N_YY	AJ21[5]
4	IO_L202P_Y	AP21
4	IO_L202N_Y	AE20
4	IO_L203P_Y	AH21
4	IO_L203N_Y	AL21
4	IO_L204P	AN21[4]
4	IO_L204N	AF20[5]
4	IO_L205P_YY	AK21
4	IO_L205N_YY	AP20
4	IO_VREF_L206P_YY	AE19
4	IO_L206N_YY	AN20
4	IO_L207P_Y	AG20[4]
4	IO_L207N_Y	AL20[5]
4	IO_L208P_Y	AH20
4	IO_L208N_Y	AK20
4	IO_L209P_Y	AN19
4	IO_L209N_Y	AJ20
4	IO_L210P	AF19[4]
4	IO_L210N	AP19[5]
4	IO_L211P_YY	AM19
4	IO_L211N_YY	AH19
4	IO_VREF_L212P_YY	AJ19

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
5	IO_L239P_Y	AP9
5	IO_L239N_Y	AK11
5	IO_L240P_YY	AL11
5	IO_VREF_L240N_YY	AL10
5	IO_L241P_YY	AE13
5	IO_L241N_YY	AM9
5	IO_L242P	AF12[5]
5	IO_L242N	AP8[4]
5	IO_L243P_Y	AL9
5	IO_VREF_L243N_Y	AH11[2]
5	IO_L244P_Y	AF11
5	IO_L244N_Y	AN8
5	IO_L245P_Y	AM8[5]
5	IO_L245N_Y	AG11[4]
5	IO_L246P_YY	AL8
5	IO_VREF_L246N_YY	AK9
5	IO_L247P_YY	AH10
5	IO_L247N_YY	AN7
5	IO_L248P	AE12[5]
5	IO_L248N	AJ9[4]
5	IO_L249P_Y	AM7
5	IO_L249N_Y	AL7
5	IO_L250P_Y	AG10
5	IO_L250N_Y	AN6
5	IO_L251P_YY	AK8[5]
5	IO_L251N_YY	AH9[4]
5	IO_L252P_YY	AP5
5	IO_VREF_L252N_YY	AJ8
5	IO_L253P_YY	AE11
5	IO_L253N_YY	AN5
5	IO_L254P_Y	AF10
5	IO_L254N_Y	AM6
5	IO_L255P_Y	AL6
5	IO_VREF_L255N_Y	AG9

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
5	IO_L256P_Y	AH8
5	IO_L256N_Y	AP4
5	IO_L257P_Y	AN4
5	IO_L257N_Y	AJ7
5	IO_L258P_YY	AM5
5	IO_L258N_YY	AK6
6	IO	T1
6	IO	V2
6	IO	V3
6	IO	V5[3]
6	IO	V8[3]
6	IO	AA10[3]
6	IO	AB5[3]
6	IO	AB7[3]
6	IO	AB9[3]
6	IO	AD7[3]
6	IO	AD8[3]
6	IO	AE2
6	IO	AE4
6	IO	AJ4[3]
6	IO	AH5[3]
6	IO_L259N_YY	AH6
6	IO_L259P_YY	AF8
6	IO_L260N_Y	AE9
6	IO_L260P_Y	AK3
6	IO_L261N_Y	AD10
6	IO_L261P_Y	AL2
6	IO_VREF_L262N_Y	AL1
6	IO_L262P_Y	AH4
6	IO_L263N	AG6
6	IO_L263P	AK1
6	IO_L264N_Y	AF7
6	IO_L264P_Y	AK2