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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1536
Number of Logic Elements/Cells	6912
Total RAM Bits	131072
Number of I/O	316
Number of Gates	411955
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	432-LBGA Exposed Pad, Metal
Supplier Device Package	432-MBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv300e-7bg432c

Data Registers

The primary data register is the Boundary Scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out, and 3-State Control. Non-IOB pins have appropriate partial bit population if input-only or output-only. Each EXTEST CAPTURED-OR state captures all In, Out, and 3-state pins.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream Boundary Scan device.

The FPGA supports up to two additional internal scan chains that can be specified using the BSCAN macro. The macro provides two user pins (SEL1 and SEL2) which are decodes of the USER1 and USER2 instructions respectively. For these instructions, two corresponding pins (T DO1 and TDO2) allow user scan data to be shifted out of TDO.

Likewise, there are individual clock pins (DRCK1 and DRCK2) for each user register. There is a common input pin (TDI) and shared output pins that represent the state of the TAP controller (RESET, SHIFT, and UPDATE).

Bit Sequence

The order within each IOB is: In, Out, 3-State. The input-only pins contribute only the In bit to the Boundary Scan I/O data register, while the output-only pins contributes all three bits.

From a cavity-up view of the chip (as shown in EPIC), starting in the upper right chip corner, the Boundary Scan data-register bits are ordered as shown in Figure 12.

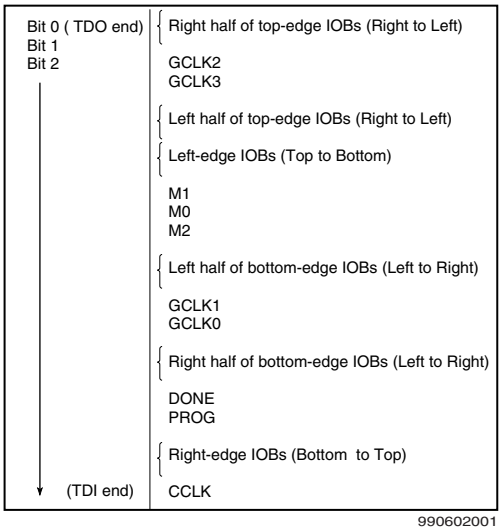


Figure 12: **Boundary Scan Bit Sequence**

BSDL (Boundary Scan Description Language) files for Virtex-E Series devices are available on the Xilinx web site in the File Download area.

Identification Registers

The IDCODE register is supported. By using the IDCODE, the device connected to the JTAG port can be determined.

The IDCODE register has the following binary format:

vvvv:ffff:fffa:aaaa:aaaa:cccc:cccc:ccc1

where

v = the die version number

f = the family code (05 for Virtex-E family)

a = the number of CLB rows (ranges from 16 for

XCV50E to 104 for XCV3200E)

c = the company code (49h for Xilinx)

The USERCODE register is supported. By using the USERCODE, a user-programmable identification code can be loaded and shifted out for examination. The identification code (see Table 7) is embedded in the bitstream during bitstream generation and is valid only after configuration.

Table 7: **IDCODEs Assigned to Virtex-E FPGAs**

FPGA	IDCODE
XCV50E	v0A10093h
XCV100E	v0A14093h
XCV200E	v0A1C093h
XCV300E	v0A20093h
XCV400E	v0A28093h
XCV600E	v0A30093h
XCV1000E	v0A40093h
XCV1600E	v0A48093h
XCV2000E	v0A50093h
XCV2600E	v0A5C093h
XCV3200E	v0A68093h

Note:

Attempting to load an incorrect bitstream causes configuration to fail and can damage the device.

Including Boundary Scan in a Design

Since the Boundary Scan pins are dedicated, no special element needs to be added to the design unless an internal data register (USER1 or USER2) is desired.

If an internal data register is used, insert the Boundary Scan symbol and connect the necessary pins as appropriate.

Table 9 lists the total number of bits required to configure each device.

Table 9: **Virtex-E Bitstream Lengths**

Device	# of Configuration Bits
XCV50E	630,048
XCV100E	863,840
XCV200E	1,442,016
XCV300E	1, 875,648
XCV400E	2,693,440
XCV600E	3,961,632
XCV1000E	6,587,520
XCV1600E	8,308,992
XCV2000E	10,159,648
XCV2600E	12,922,336
XCV3200E	16,283,712

Slave-Serial Mode

In slave-serial mode, the FPGA receives configuration data in bit-serial form from a serial PROM or other source of serial configuration data. The serial bitstream must be set up at the DIN input pin a short time before each rising edge of an externally generated CCLK.

For more detailed information on serial PROMs, see the PROM data sheet at **http://www.xilinx.com/bvdocs/publications/ds026.pdf**.

Multiple FPGAs can be daisy-chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed to the DOUT pin. The maximum capacity for a single LOUT/DOUT write is 2^{20}-1 (1,048,575) 32-bit words, or 33,554,4000 bits. The data on the DOUT pin changes on the rising edge of CCLK.

The change of DOUT on the rising edge of CCLK differs from previous families, but does not cause a problem for mixed configuration chains. This change was made to improve serial configuration rates for Virtex and Virtex-E only chains.

Figure 13 shows a full master/slave system. A Virtex-E device in slave-serial mode should be connected as shown in the right-most device.

Slave-serial mode is selected by applying <111> or <011> to the mode pins (M2, M1, M0). A weak pull-up on the mode pins makes slave serial the default mode if the pins are left unconnected. However, it is recommended to drive the configuration mode pins externally. Figure 14 shows slave-serial mode programming switching characteristics.

Table 10 provides more detail about the characteristics shown in Figure 14. Configuration must be delayed until the $\overline{\text{INIT}}$ pins of all daisy-chained FPGAs are High.

Table 10: **Master/Slave Serial Mode Programming Switching**

	Description	Figure References	Symbol	Values	Units
CCLK	DIN setup/hold, slave mode	1/2	T_{DCC}/T_{CCD}	5.0 / 0.0	ns, min
	DIN setup/hold, master mode	1/2	T_{DSCK}/T_{CKDS}	5.0 / 0.0	ns, min
	DOUT	3	T_{CCO}	12.0	ns, max
	High time	4	T_{CCH}	5.0	ns, min
	Low time	5	T_{CCL}	5.0	ns, min
	Maximum Frequency		F_{CC}	66	MHz, max
	Frequency Tolerance, master mode with respect to nominal			+45% –30%	

IOB Output Switching Characteristics, Figure 1

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 10.

Description[2]	Symbol	Speed Grade[1]				Units
		Min	-8	-7	-6	
Propagation Delays						
O input to Pad	T_{IOOP}	1.04	2.5	2.7	2.9	ns, max
O input to Pad via transparent latch	T_{IOOLP}	1.24	2.9	3.1	3.4	ns, max
3-State Delays						
T input to Pad high-impedance (Note 2)	T_{IOTHZ}	0.73	1.5	1.7	1.9	ns, max
T input to valid data on Pad	T_{IOTON}	1.13	2.7	2.9	3.1	ns, max
T input to Pad high-impedance via transparent latch (Note 2)	$T_{IOTLPHZ}$	0.86	1.8	2.0	2.2	ns, max
T input to valid data on Pad via transparent latch	$T_{IOTLPON}$	1.26	3.0	3.2	3.4	ns, max
GTS to Pad high impedance (Note 2)	T_{GTS}	1.94	4.1	4.6	4.9	ns, max
Sequential Delays						
Clock CLK						
Minimum Pulse Width, High	T_{CH}	0.56	1.2	1.3	1.4	ns, min
Minimum Pulse Width, Low	T_{CL}	0.56	1.2	1.3	1.4	ns, min
Clock CLK to Pad	T_{IOCKP}	0.97	2.4	2.8	2.9	ns, max
Clock CLK to Pad high-impedance (synchronous) (Note 2)	T_{IOCKHZ}	0.77	1.6	2.0	2.2	ns, max
Clock CLK to valid data on Pad (synchronous)	T_{IOCKON}	1.17	2.8	3.2	3.4	ns, max
Setup and Hold Times before/after Clock CLK						
O input	T_{IOOCK} / T_{IOCKO}	0.43 / 0	0.9 / 0	1.0 / 0	1.1 / 0	ns, min
OCE input	$T_{IOOCECK}$ / $T_{IOCKOCE}$	0.28 / 0	0.55 / 0.01	0.7 / 0	0.7 / 0	ns, min
SR input (OFF)	$T_{IOSRCKO}$ / $T_{IOCKOSR}$	0.40 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
3-State Setup Times, T input	T_{IOTCK} / T_{IOCKT}	0.26 / 0	0.51 / 0	0.6 / 0	0.7 / 0	ns, min
3-State Setup Times, TCE input	$T_{IOTCECK}$ / $T_{IOCKTCE}$	0.30 / 0	0.6 / 0	0.7 / 0	0.8 / 0	ns, min
3-State Setup Times, SR input (TFF)	$T_{IOSRCKT}$ / $T_{IOCKTSR}$	0.38 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
Set/Reset Delays						
SR input to Pad (asynchronous)	T_{IOSRP}	1.30	3.1	3.3	3.5	ns, max
SR input to Pad high-impedance (asynchronous) (Note 2)	T_{IOSRHZ}	1.08	2.2	2.4	2.7	ns, max
SR input to valid data on Pad (asynchronous)	T_{IOSRON}	1.48	3.4	3.7	3.9	ns, max
GSR to Pad	T_{IOGSRQ}	3.88	7.6	8.5	9.7	ns, max

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. 3-state turn-off delays should not be adjusted.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *without* DLL

Description[1]	Symbol	Device	Speed Grade[2]				Units
			Min	-8	-7	-6	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *without* DLL. For data *output* with different standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 10.	T_{ICKOF}	XCV50E	1.5	4.2	4.4	4.6	ns
		XCV100E	1.5	4.2	4.4	4.6	ns
		XCV200E	1.5	4.3	4.5	4.7	ns
		XCV300E	1.5	4.3	4.5	4.7	ns
		XCV400E	1.5	4.4	4.6	4.8	ns
		XCV600E	1.6	4.5	4.7	4.9	ns
		XCV1000E	1.7	4.6	4.8	5.0	ns
		XCV1600E	1.8	4.7	4.9	5.1	ns
		XCV2000E	1.8	4.8	5.0	5.2	ns
		XCV2600E	2.0	5.0	5.2	5.4	ns
		XCV3200E	2.2	5.2	5.4	5.6	ns

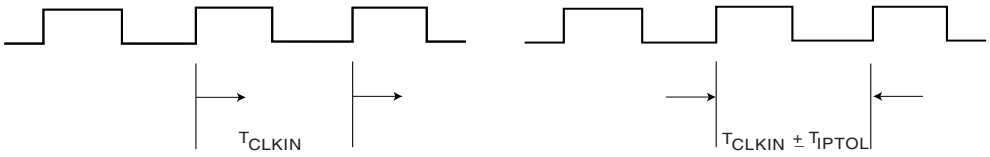
Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For other I/O standards and different loads, see Table 3 and Table 4.

DLL Timing Parameters

All devices are 100 percent functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

Description	Symbol	F_{CLKIN}	Speed Grade						Units
			-8		-7		-6		
			Min	Max	Min	Max	Min	Max	
Input Clock Frequency (CLKDLLHF)	FCLKINHF		60	350	60	320	60	275	MHz
Input Clock Frequency (CLKDLL)	FCLKINLF		25	160	25	160	25	135	MHz
Input Clock Low/High Pulse Width	T_{DLLPW}	≥2□5 MHz	5.0		5.0		5.0		ns
		≥□50 MHz	3.0		3.0		3.0		ns
		≥100 MHz	2.4		2.4		2.4		ns
		≥□150 MHz	2.0		2.0		2.0		ns
		≥□200 MHz	1.8		1.8		1.8		ns
		≥□250 MHz	1.5		1.5		1.5		ns
		≥□300 MHz	1.3		1.3		NA		ns

Period Tolerance: the allowed input clock period change in nanoseconds.



Output Jitter: the difference between an ideal reference clock edge and the actual design.

Phase Offset and Maximum Phase Difference

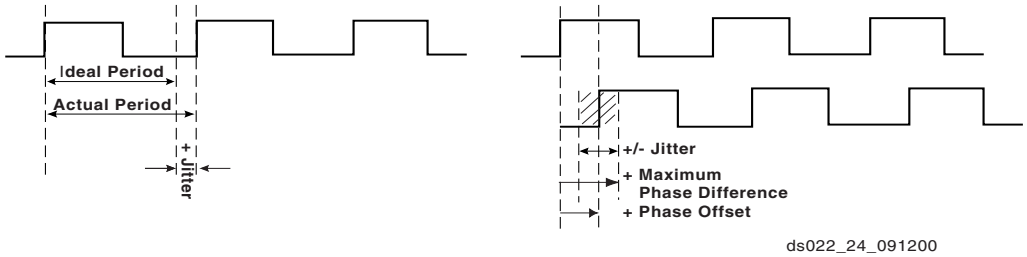


Figure 4: **DLL Timing Waveforms**

Pinout Differences Between Virtex and Virtex-E Families

The same device in the same package for the Virtex-E and Virtex families are pin-compatible with some minor exceptions, listed in Table 1.

XCV200E Device, FG456 Package

The Virtex-E XCV200E has two I/O pins swapped with the Virtex XCV200 to accommodate differential clock pairing.

XCV400E Device, FG676 Package

The Virtex-E XCV400E has two I/O pins swapped with the Virtex XCV400 to accommodate differential clock pairing.

All Devices, PQ240 and HQ240 Packages

The Virtex devices in PQ240 and HQ240 packages do not have V_{CCO} banking, but Virtex-E devices do. To achieve this, eight Virtex I/O pins (P232, P207, P176, P146, P116, P85, P55, and P25) are now VCCO pins in the Virtex-E family. This change also requires one Virtex I/O or VREF pin to be swapped with a standard I/O pin.

Additionally, accommodating differential clock input pairs in Virtex-E caused some IO_V_{REF} differences in the XCV400E and XCV600E devices only. Virtex IO_V_{REF} pins P215 and P87 are Virtex-E IO_V_{REF} pins P216 and P86, respectively. Virtex-E pins P215 and P87 are IO_DLL.

Table 1: **Pinout Differences Summary**

Part	Package	Pins	Virtex	Virtex-E
XCV200	FG456	E11, U11	I/O	No Connect
		B11, AA11	No Connect	IO_LVDS_DLL
XCV400	FG676	D13, Y13	I/O	No Connect
		B13, AF13	No Connect	IO_LVDS_DLL
XCV400/600	PQ240/HQ240	P215, P87	IO_V_{REF}	IO_LVDS_DLL
		P216, P86	I/O	IO_V_{REF}
All	PQ240/HQ240	P232, P207, P176, P146, P116, P85, P55, and P25	I/O	V_{CCO}
		P231	I/O	IO_V_{REF}

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P138	IO_D5_L26N_YY	3
P137	VCCINT	NA
P136	VCCO	3
P135	GND	NA
P134	IO_D6_L27P_Y	3
P133	IO_VREF_L27N_Y	3
P132	IO_VREF	3
P131	IO_L28P_Y	3
P130	IO_VREF_L28N_Y	3
P129	GND	NA
P128	IO_L29P_Y	3
P127	IO_L29N_Y	3
P126	IO_VREF_L30P_Y	3
P125	IO_L30N_Y	3
P124	IO_D7_L31P_YY	3
P123	IO_INIT_L31N_YY	3
P122	PROGRAM	NA
P121	VCCO	3
P120	DONE	3
P119	GND	NA
P118	IO_L32P_YY	4
P117	IO_L32N_YY	4
P116	VCCO	4
P115	IO_VREF	4
P114	IO_L33P_YY	4
P113	IO_L33N_YY	4
P112	GND	NA
P111	IO_VREF_L34P_YY	4
P110	IO_L34N_YY	4
P109	IO_VREF	4
P108	IO_VREF_L35P_YY	4
P107	IO_L35N_YY	4
P106	GND	NA
P105	VCCO	4
P104	VCCINT	NA
P103	IO_L36P_YY	4

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P102	IO_L36N_YY	4
P101[1]	IO_VREF	4
P100	IO_L37P_Y	4
P99	IO_L37N_Y	4
P98	GND	NA
P97	IO_VREF_L38P_Y	4
P96	IO_L38N_Y	4
P95	IO_L39P	4
P94	IO_VREF_L39N	4
P93	IO_LVDS_DLL_L40P	4
P92	GCK0	4
P91	GND	NA
P90	VCCO	4
P89	GCK1	5
P88	VCCINT	NA
P87	IO_LVDS_DLL_L40N	5
P86	IO_VREF	5
P85	VCCO	5
P84	IO_VREF_L41P	5
P83	GND	NA
P82	IO_L41N	5
P81	IO	5
P80[1]	IO_VREF	5
P79	IO_L42P_YY	5
P78	IO_L42N_YY	5
P77	VCCINT	NA
P76	VCCO	5
P75	GND	NA
P74	IO_L43P_YY	5
P73	IO_VREF_L43N_YY	5
P72	IO_VREF	5
P71	IO_L44P_YY	5
P70	IO_VREF_L44N_YY	5
P69	GND	NA
P68	IO_L45P_YY	5
P67	IO_L45N_YY	5

Table 10: **BG352 — XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
NA	VCCINT	V24
NA	VCCINT	R23
NA	VCCINT	P25
NA	VCCINT	L25
NA	VCCINT	J24
0	VCCO	D19
0	VCCO	B25
0	VCCO	A17
1	VCCO	D13
1	VCCO	D7
1	VCCO	A10
2	VCCO	K1
2	VCCO	H4
2	VCCO	B2
3	VCCO	Y4
3	VCCO	U1
3	VCCO	P4
4	VCCO	AF10
4	VCCO	AE2
4	VCCO	AC8
5	VCCO	AF17
5	VCCO	AC20
5	VCCO	AC14
6	VCCO	AE25
6	VCCO	W23
6	VCCO	U26
7	VCCO	N23
7	VCCO	K26
7	VCCO	G23
NA	GND	A26
NA	GND	A25
NA	GND	A22

Table 10: **BG352 — XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
NA	GND	A19
NA	GND	A14
NA	GND	A8
NA	GND	A5
NA	GND	A2
NA	GND	A1
NA	GND	B26
NA	GND	B1
NA	GND	E26
NA	GND	E1
NA	GND	H26
NA	GND	H1
NA	GND	N1
NA	GND	P26
NA	GND	W26
NA	GND	W1
NA	GND	AB26
NA	GND	AB1
NA	GND	AE26
NA	GND	AE1
NA	GND	AF26
NA	GND	AF25
NA	GND	AF22
NA	GND	AF19
NA	GND	AF13
NA	GND	AF8
NA	GND	AF5
NA	GND	AF2
NA	GND	AF1

Notes:
1. No Connect in the XCV100E.
2. V_{REF} or I/O option only in the XCV200E and XCV300E; otherwise, I/O option only.

Table 12: **BG432 — XCV300E, XCV400E, XCV600E**

Bank	Pin Description	Pin #
0	IO_L12N_YY	A20
0	IO_L12P_YY	D19
0	IO_VREF_L13N_YY	B19
0	IO_L13P_YY	A19
0	IO_L14N_Y	B18
0	IO_L14P_Y	D18
0	IO_VREF_L15N_Y	C18[2]
0	IO_L15P_Y	B17
0	IO_LVDS_DLL_L16N	C17
1	GCK2	A16
1	IO	A12
1	IO	B9
1	IO	B11
1	IO	C16
1	IO	D9
1	IO_LVDS_DLL_L16P	B16
1	IO_L17N_Y	A15
1	IO_VREF_L17P_Y	B15[2]
1	IO_L18N_Y	C15
1	IO_L18P_Y	D15
1	IO_L19N_YY	B14
1	IO_VREF_L19P_YY	A13
1	IO_L20N_YY	B13
1	IO_L20P_YY	D14
1	IO_L21N_YY	C13
1	IO_L21P_YY	B12
1	IO_L22N_YY	D13
1	IO_L22P_YY	C12
1	IO_L23N_YY	D12
1	IO_L23P_YY	C11
1	IO_L24N_YY	B10
1	IO_VREF_L24P_YY	C10
1	IO_L25N_Y	C9
1	IO_VREF_L25P_Y	D10[1]
1	IO_L26N_Y	A8

Table 12: **BG432 — XCV300E, XCV400E, XCV600E**

Bank	Pin Description	Pin #
1	IO_L26P_Y	B8
1	IO_L27N_YY	C8
1	IO_VREF_L27P_YY	B7
1	IO_L28N_YY	D8
1	IO_L28P_YY	A6
1	IO_L29N_Y	B6
1	IO_L29P_Y	D7
1	IO_L30N_YY	A5
1	IO_VREF_L30P_YY	C6
1	IO_L31N_YY	B5
1	IO_L31P_YY	D6
1	IO_L32N_Y	A4
1	IO_L32P_Y	C5
1	IO_WRITE_L33N_YY	B4
1	IO_CS_L33P_YY	D5
2	IO	H4
2	IO	J3
2	IO	L3
2	IO	M1
2	IO	R2
2	IO_DOUT_BUSY_L34P_YY	D3
2	IO_DIN_D0_L34N_YY	C2
2	IO_L35P	D2
2	IO_L35N	E4
2	IO_L36P_Y	D1
2	IO_L36N_Y	E3
2	IO_VREF_L37P_Y	E2
2	IO_L37N_Y	F4
2	IO_L38P	E1
2	IO_L38N	F3
2	IO_L39P_Y	F2
2	IO_L39N_Y	G4
2	IO_VREF_L40P_YY	G3
2	IO_L40N_YY	G2
2	IO_L41P_Y	H3

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
7	IO_L165N_YY	P32	
7	IO_VREF_L165P_YY	P31	
7	IO_L166N_Y	P30	
7	IO_L166P_Y	P29	
7	IO_L167N_Y	M32	
7	IO_L167P_Y	N31	
7	IO_L168N_Y	N30	
7	IO_VREF_L168P_Y	L33	3
7	IO_L169N_Y	M31	
7	IO_L169P_Y	L32	
7	IO_L170N_Y	M30	
7	IO_L170P_Y	L31	
7	IO_L171N_YY	M29	
7	IO_L171P_YY	J33	
7	IO_L172N_YY	L30	
7	IO_VREF_L172P_YY	K31	
7	IO_L173N_Y	L29	
7	IO_L173P_Y	H33	
7	IO_L174N_Y	J31	
7	IO_VREF_L174P_Y	H32	4
7	IO_L175N_Y	K29	
7	IO_L175P_Y	H31	
7	IO_L176N_Y	J30	
7	IO_VREF_L176P_Y	G32	1
7	IO_L177N_YY	J29	
7	IO_VREF_L177P_YY	G31	
7	IO_L178N_Y	E33	
7	IO_L178P_Y	E32	
7	IO_L179N_Y	H29	
7	IO_L179P_Y	F31	
7	IO_L180N_Y	D32	
7	IO_VREF_L180P_Y	E31	
7	IO_L181N_Y	G29	
7	IO_L181P_Y	C33	
7	IO_L182N_Y	F30	

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
7	IO_VREF_L182P_Y	D31	3
2	CCLK	C4	
3	DONE	AJ5	
NA	DXN	AK29	
NA	DXP	AJ28	
NA	M0	AJ29	
NA	M1	AK30	
NA	M2	AN32	
NA	PROGRAM	AM1	
NA	TCK	E29	
NA	TDI	D5	
2	TDO	E6	
NA	TMS	B33	
NA	NC	C31	
NA	NC	AC2	
NA	NC	AK4	
NA	NC	AL3	
NA	VCCINT	A21	
NA	VCCINT	B12	
NA	VCCINT	B14	
NA	VCCINT	B18	
NA	VCCINT	B28	
NA	VCCINT	C22	
NA	VCCINT	C24	
NA	VCCINT	E9	
NA	VCCINT	E12	
NA	VCCINT	F2	
NA	VCCINT	H30	
NA	VCCINT	J1	
NA	VCCINT	K32	
NA	VCCINT	M3	
NA	VCCINT	N1	

Table 16: **FG256 Package — XCV50E, XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
NA	GND	K11
NA	GND	K10
NA	GND	K9
NA	GND	K8
NA	GND	K7
NA	GND	K6
NA	GND	J10
NA	GND	J9
NA	GND	J8
NA	GND	J7
NA	GND	H10
NA	GND	H9
NA	GND	H8
NA	GND	H7
NA	GND	G11
NA	GND	G10
NA	GND	G9
NA	GND	G8
NA	GND	G7
NA	GND	G6
NA	GND	F11
NA	GND	F10
NA	GND	F7
NA	GND	F6
NA	GND	B15
NA	GND	B2
NA	GND	A16
NA	GND	A1

Notes:
1. V_{REF} or I/O option only in the XCV100E, 200E, 300E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV200E, 300E; otherwise, I/O option only.

FG256 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 17: **FG256 Differential Pin Pair Summary XCV50E, XCV100E, XCV200E, XCV300E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	N8	N9	NA	IO_DLL_L52P
1	5	R8	T8	NA	IO_DLL_L52N
2	1	C9	A8	NA	IO_DLL_L8P
3	0	B8	A7	NA	IO_DLL_L8N
IO LVDS Total Pairs: 83, Asynchronous Outputs: 35					
0	0	A3	C5	7	VREF
1	0	E6	D5	√	-
2	0	A4	B4	√	VREF
3	0	B5	D6	2	-
4	0	A5	C6	√	VREF
5	0	C7	B6	√	-
6	0	C8	D7	1	-
7	0	A6	B7	1	VREF
8	1	A8	A7	NA	IO_LVDS_DLL
9	1	A9	D9	2	-
10	1	B9	E10	1	VREF
11	1	D10	A10	1	-
12	1	A11	C10	√	-
13	1	E11	B11	√	VREF
14	1	D11	A12	2	-
15	1	C11	A13	√	VREF
16	1	D12	B12	√	-
17	1	C12	A14	7	VREF
18	1	B13	C13	√	CS

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
6	IO_VREF_L200N_YY	AH39
6	IO_L200P_YY	AG38
6	IO_L201N_YY	AG36
6	IO_L201P_YY	AG39
6	IO_L202N_Y	AG37
6	IO_L202P_Y	AF39
6	IO_L203N	AF36
6	IO_L203P	AE38
6	IO_L204N	AF37
6	IO_L204P	AF38
6	IO_VREF_L205N_Y	AE39[1]
6	IO_L205P_Y	AE36
6	IO_L206N_YY	AD38
6	IO_L206P_YY	AE37
6	IO_L207N	AD39
6	IO_L207P	AD36
6	IO_L208N_Y	AC38
6	IO_L208P_Y	AC39
6	IO_VREF_L209N_YY	AD37
6	IO_L209P_YY	AB38
6	IO_L210N_YY	AC35
6	IO_L210P_YY	AB39
6	IO_L211N	AC36
6	IO_L211P	AA38
6	IO_L212N	AC37
6	IO_L212P	AA39
6	IO_VREF_L213N_YY	AB35
6	IO_L213P_YY	Y38
6	IO_L214N_YY	AB36
6	IO_L214P_YY	Y39
6	IO_VREF_L215N	AB37[2]
6	IO_L215P	AA36
7	IO	C38
7	IO	B37
7	IO	F37

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
7	IO_L216N_YY	AA37
7	IO_L216P_YY	W38
7	IO_L217N	W37
7	IO_VREF_L217P	V39[2]
7	IO_L218N_YY	W36
7	IO_L218P_YY	U39
7	IO_L219N_YY	V38
7	IO_VREF_L219P_YY	U38
7	IO_L220N	V37
7	IO_L220P	T39
7	IO_L221N	V36
7	IO_L221P	T38
7	IO_L222N_YY	V35
7	IO_L222P_YY	R39
7	IO_L223N_YY	U37
7	IO_VREF_L223P_YY	U36
7	IO_L224N_Y	R38
7	IO_L224P_Y	U35
7	IO_L225N	P39
7	IO_L225P	T37
7	IO_L226N_YY	P38
7	IO_L226P_YY	T36
7	IO_L227N_Y	N39
7	IO_VREF_L227P_Y	N38[1]
7	IO_L228N	R37
7	IO_L228P	M39
7	IO_L229N	R36
7	IO_L229P	M38
7	IO_L230N_Y	P37
7	IO_L230P_Y	L39
7	IO_L231N_YY	P36
7	IO_L231P_YY	N37
7	IO_L232N_YY	L38
7	IO_VREF_L232P_YY	N36
7	IO_L233N	K39
7	IO_L233P	M37

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
0	IO_VREF_L27N_YY	D27
0	IO_L27P_YY	B25
0	IO_L28N_Y	A25
0	IO_L28P_Y	D26
0	IO_L29N_Y	A24
0	IO_L29P_Y	E25
0	IO_L30N_YY	D25
0	IO_L30P_YY	B24
0	IO_VREF_L31N_YY	E24
0	IO_L31P_YY	A23
0	IO_L32N_Y	C23
0	IO_L32P_Y	E23
0	IO_VREF_L33N_Y	B23[1]
0	IO_L33P_Y	D23
0	IO_LVDS_DLL_L34N	A22
1	GCK2	B22
1	IO	A14
1	IO	A20
1	IO	B11
1	IO	B13
1	IO	C8
1	IO	C18
1	IO	C21
1	IO	D7
1	IO	D10
1	IO	D15
1	IO	D17
1	IO	E20
1	IO_LVDS_DLL_L34P	D22
1	IO_L35N_Y	D21
1	IO_VREF_L35P_Y	B21[1]
1	IO_L36N_Y	D20
1	IO_L36P_Y	A21
1	IO_L37N_YY	C20
1	IO_VREF_L37P_YY	D19
1	IO_L38N_YY	B20

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
1	IO_L38P_YY	E19
1	IO_L39N_Y	D18
1	IO_L39P_Y	A19
1	IO_L40N_Y	E18
1	IO_L40P_Y	C19
1	IO_L41N_YY	B19
1	IO_VREF_L41P_YY	E17
1	IO_L42N_YY	A18
1	IO_L42P_YY	D16
1	IO_L43N_Y	E16
1	IO_L43P_Y	B18
1	IO_L44N_Y	F16
1	IO_L44P_Y	A17
1	IO_L45N_YY	C17
1	IO_VREF_L45P_YY	E15
1	IO_L46N_YY	B17
1	IO_L46P_YY	D14
1	IO_L47N_Y	A16
1	IO_L47P_Y	E14
1	IO_L48N_Y	C16
1	IO_L48P_Y	D13
1	IO_L49N_Y	B16
1	IO_L49P_Y	D12
1	IO_L50N_Y	A15
1	IO_L50P_Y	E12
1	IO_L51N_YY	C15
1	IO_L51P_YY	C11
1	IO_L52N_YY	B15
1	IO_VREF_L52P_YY	D11
1	IO_L53N_Y	E11
1	IO_L53P_Y	C14
1	IO_L54N_Y	C10
1	IO_L54P_Y	B14
1	IO_L55N_YY	A13
1	IO_VREF_L55P_YY	E10
1	IO_L56N_YY	C13
1	IO_L56P_YY	C9

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
6	IO_VREF_L245N_Y	AB40[1]
6	IO_L245P_Y	AC39
7	IO	F38
7	IO	H40
7	IO	H41
7	IO	J42
7	IO	K39
7	IO	L42
7	IO	N40
7	IO	T40
7	IO	U40
7	IO	V38
7	IO	W42
7	IO	Y42
7	IO	AA42
7	IO_L246N_YY	AA41
7	IO_L246P_YY	AB39
7	IO_L247N_Y	Y41
7	IO_VREF_L247P_Y	AA39[1]
7	IO_L248N_YY	Y40
7	IO_L248P_YY	Y39
7	IO_L249N_YY	Y38
7	IO_VREF_L249P_YY	W41
7	IO_L250N_Y	W40
7	IO_L250P_Y	W39
7	IO_L251N_Y	W38
7	IO_L251P_Y	V41
7	IO_L252N_YY	V39
7	IO_L252P_YY	V40
7	IO_L253N_YY	V42
7	IO_VREF_L253P_YY	U39
7	IO_L254N_Y	U41
7	IO_L254P_Y	U38
7	IO_L255N_Y	U42
7	IO_L255P_Y	T39
7	IO_L256N_YY	T41

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
7	IO_L256P_YY	T38
7	IO_L257N_Y	R39
7	IO_VREF_L257P_Y	T42
7	IO_L258N_Y	R42
7	IO_L258P_Y	R38
7	IO_L259N	R40
7	IO_L259P	P39
7	IO_L260N_Y	R41
7	IO_L260P_Y	P38
7	IO_L261N_Y	P42
7	IO_L261P_Y	N39
7	IO_L262N_Y	P40
7	IO_L262P_Y	M39
7	IO_L263N_YY	P41
7	IO_L263P_YY	M38
7	IO_L264N_YY	N42
7	IO_VREF_L264P_YY	L39
7	IO_L265N_Y	L38
7	IO_L265P_Y	N41
7	IO_L266N_YY	K40
7	IO_L266P_YY	M42
7	IO_L267N_YY	M40
7	IO_VREF_L267P_YY	K38
7	IO_L268N_Y	M41
7	IO_L268P_Y	J40
7	IO_L269N_Y	J39
7	IO_VREF_L269P_Y	L40
7	IO_L270N_YY	J38
7	IO_L270P_YY	L41
7	IO_L271N_YY	K42
7	IO_VREF_L271P_YY	H39
7	IO_L272N_Y	K41
7	IO_L272P_Y	H38
7	IO_L273N_Y	J41
7	IO_L273P_Y	G40
7	IO_L274N_YY	H42
7	IO_L274P_YY	G39

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
NA	VCCO_2	T23
NA	VCCO_2	T24
NA	VCCO_2	R23
NA	VCCO_2	R24
NA	VCCO_2	P23
NA	VCCO_2	P24
NA	VCCO_2	P32
NA	VCCO_2	N23
NA	VCCO_3	V23
NA	VCCO_3	V24
NA	VCCO_3	Y23
NA	VCCO_3	Y24
NA	VCCO_3	W23
NA	VCCO_3	W24
NA	VCCO_3	AJ34
NA	VCCO_3	AE30
NA	VCCO_3	AC24
NA	VCCO_3	AB23
NA	VCCO_3	AB24
NA	VCCO_3	AA23
NA	VCCO_3	AA24
NA	VCCO_3	AA32
NA	VCCO_4	AD18
NA	VCCO_4	AC18
NA	VCCO_4	AC19
NA	VCCO_4	AC20
NA	VCCO_4	AC21
NA	VCCO_4	AC22
NA	VCCO_4	AP29
NA	VCCO_4	AM21
NA	VCCO_4	AK25
NA	VCCO_4	AD19
NA	VCCO_4	AD20
NA	VCCO_4	AD21

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
NA	VCCO_4	AD22
NA	VCCO_4	AD23
NA	VCCO_5	AC17
NA	VCCO_5	AD17
NA	VCCO_5	AC13
NA	VCCO_5	AC14
NA	VCCO_5	AC15
NA	VCCO_5	AC16
NA	VCCO_5	AP6
NA	VCCO_5	AM14
NA	VCCO_5	AK10
NA	VCCO_5	AD12
NA	VCCO_5	AD13
NA	VCCO_5	AD14
NA	VCCO_5	AD15
NA	VCCO_5	AD16
NA	VCCO_6	V11
NA	VCCO_6	V12
NA	VCCO_6	Y11
NA	VCCO_6	Y12
NA	VCCO_6	W11
NA	VCCO_6	W12
NA	VCCO_6	AJ1
NA	VCCO_6	AE5
NA	VCCO_6	AC11
NA	VCCO_6	AB11
NA	VCCO_6	AB12
NA	VCCO_6	AA3
NA	VCCO_6	AA11
NA	VCCO_6	AA12
NA	VCCO_7	U11
NA	VCCO_7	U12
NA	VCCO_7	N12
NA	VCCO_7	M11

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
NA	VCCO_7	K5
NA	VCCO_7	F1
NA	VCCO_7	T11
NA	VCCO_7	T12
NA	VCCO_7	R11
NA	VCCO_7	R12
NA	VCCO_7	P3
NA	VCCO_7	P11
NA	VCCO_7	P12
NA	VCCO_7	N11
NA	GND	K32
NA	GND	R4
NA	GND	AN1
NA	GND	AM11
NA	GND	AK5
NA	GND	AH28
NA	GND	AD32
NA	GND	AA20
NA	GND	Y20
NA	GND	W19
NA	GND	V19
NA	GND	U20
NA	GND	T20
NA	GND	R19
NA	GND	P19
NA	GND	H8
NA	GND	F12
NA	GND	C2
NA	GND	B1
NA	GND	A7
NA	GND	AP1
NA	GND	AN2
NA	GND	AM15

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
NA	GND	AK17
NA	GND	AH34
NA	GND	AC6
NA	GND	AA21
NA	GND	Y21
NA	GND	W20
NA	GND	V20
NA	GND	U21
NA	GND	T21
NA	GND	R20
NA	GND	P20
NA	GND	H16
NA	GND	F23
NA	GND	C3
NA	GND	B2
NA	GND	A28
NA	GND	AP34
NA	GND	AM3
NA	GND	AL31
NA	GND	AH7
NA	GND	AD3
NA	GND	AA19
NA	GND	Y19
NA	GND	W18
NA	GND	V18
NA	GND	U19
NA	GND	T19
NA	GND	R18
NA	GND	P18
NA	GND	J26
NA	GND	F6
NA	GND	C1
NA	GND	C34
NA	GND	A3

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
111	2	M31	R26	2600 1600	-
112	2	N30	P28	3200 1600 1000	-
113	2	N29	N33	2600 2000 1000	VREF
114	2	T25	N34	3200 2600 2000 1600	-
115	2	P34	R27	3200 2600 2000 1600 1000	-
116	2	P29	P31	3200 2600 1600 1000	-
117	2	P33	T26	3200 2600 2000	-
118	2	R34	R28	2600 2000 1000	-
119	2	N31	N32	2000 1600 1000	D3
120	2	P30	R33	2000 1600	-
121	2	R29	T34	3200 2600 2000 1600 1000	-
122	2	R30	T30	1000	-
123	2	T28	R31	3200 1600	-
124	2	T29	U27	3200 2600 1600 1000	-
125	2	T31	T33	2000 1600 1000	VREF
126	2	U28	T32	2000 1600 1000	-
127	2	U29	U33	3200 2600 1600 1000	VREF
128	2	V33	U31	3200 2600 2000 1600 1000	-
129	3	V26	V30	3200 2600 1600 1000	VREF
130	3	W34	V28	2000 1600 1000	-
131	3	W32	W30	2000 1600 1000	VREF

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
132	3	V29	Y34	3200 2600 1600 1000	-
133	3	W29	Y33	3200 1600	-
134	3	W26	W28	1000	-
135	3	Y31	Y30	3200 2600 2000 1600 1000	-
136	3	AA34	W31	2000 1600	-
137	3	AA33	Y29	2000 1600 1000	VREF
138	3	W25	AB34	2600 2000 1000	-
139	3	Y28	AB33	3200 2600 2000	-
140	3	AA30	Y26	3200 2600 1600 1000	-
141	3	Y27	AA31	3200 2600 2000 1600 1000	-
142	3	AA27	AA29	3200 2600 2000 1600	-
143	3	AB32	AB29	2600 2000 1000	VREF
144	3	AA28	AC34	3200 1600 1000	-
145	3	Y25	AD34	2600 1600	-
146	3	AB30	AC33	3200 2600 1600 1000	-
147	3	AA26	AC32	2000 1000	-
148	3	AD33	AB28	3200 2600 2000	-
149	3	AE34	AB27	3200 2600 2000 1600 1000	D5
150	3	AE33	AC30	2000 1600 1000	VREF
151	3	AA25	AE32	3200 1600 1000	-
152	3	AE31	AD29	3200 2600 2000 1600 1000	-

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
153	3	AD31	AF33	3200 2600 2000 1600 1000	VREF
154	3	AC28	AF31	3200 2600 1600 1000	-
155	3	AC27	AF32	3200 2600 1600	-
156	3	AE29	AD28	2600 1000	VREF
157	3	AD30	AG32	3200 2600 2000 1600 1000	-
158	3	AC26	AH33	2000 1600	-
159	3	AD26	AF30	3200 2600 2000 1600 1000	VREF
160	3	AC25	AH32	2600 2000 1000	-
161	3	AE28	AL34	3200 2600 2000	-
162	3	AG30	AD27	3200 2600 1600 1000	-
163	3	AF29	AK34	3200 2600 2000 1600 1000	-
164	3	AD25	AE27	3200 2600 2000 1600	-
165	3	AJ33	AH31	2600 2000 1000	VREF
166	3	AE26	AL33	3200 2600 1600 1000	-
167	3	AF28	AL32	2600 1600	-
168	3	AJ31	AF27	3200 2600 1600 1000	VREF
169	3	AG29	AJ32	2600 2000 1000	-
170	3	AK33	AH30	3200 2600 2000	-
171	3	AK32	AK31	3200 2600 2000 1600 1000	INIT

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
172	4	AP31	AK29	3200 2600 2000 1600 1000	-
173	4	AP30	AN31	3200 1600 1000	-
174	4	AH27	AN30	3200 2000 1000	-
175	4	AM30	AK28	3200 2000 1000	VREF
176	4	AG26	AN29	3200 2600 1000	-
177	4	AF25	AM29	3200 2600 2000 1600 1000	-
178	4	AL29	AL28	3200 2600 2000 1600 1000	VREF
179	4	AE24	AN28	2000 1600	-
180	4	AJ27	AH26	3200 1000	-
181	4	AG25	AK27	3200 1000	-
182	4	AM28	AF24	3200 2600	-
183	4	AJ26	AP27	3200 2600 2000 1600 1000	-
184	4	AK26	AN27	3200 2600 2000 1600 1000	VREF
185	4	AE23	AM27	3200 1600	-
186	4	AL26	AP26	3200 2000 1000	-
187	4	AN26	AJ25	3200 2000 1000	VREF
188	4	AG24	AP25	3200 2600	-
189	4	AF23	AM26	3200 2600 2000 1600 1000	-
190	4	AJ24	AN25	3200 2600 2000 1600 1000	VREF
191	4	AE22	AM25	2600 1600 1000	-

Date	Version	Revision
4/2/01	2.0	• Updated numerous values in **Virtex-E Switching Characteristics** tables. • Changed pinout table footnotes from "V_{REF} option only" to "V_{REF} or I/O option only" to improve clarity. • Converted file to modularized format. See the **Virtex-E Data Sheet** section.
7/26/01	2.1	• Changed pinout table footnotes from "V_{REF} or I/O option only" to "V_{REF} or I/O option only; otherwise I/O only" to improve clarity. • Changed designation for pin pair 300 in Table 29 from AO to footnote 9.
10/25/01	2.2	• Changed Table 29 to clarify which devices in the FG1156 package can use each pin pair as an asynchronous output. • Updated references to the XCV3200E device in the FG1156 package.
11/15/01	2.3	• Fixed cosmetic error.
07/17/02	2.4	• Added “VREF” to the description for pin B15 in Table 12. • Changed designation for pin pair 129 in Table 15 from AO to “AO in the XCV1000E, 1600E, 2000E“. • Data sheet designation upgraded from Preliminary to Production.
03/14/03	2.5	• Removed the Virtex-E XCV300E section under **Pinout Differences Between Virtex and Virtex-E Families** (and revised Table 1), since these differences do not exist.

Virtex-E Data Sheet

The Virtex-E Data Sheet contains the following modules:

- DS022-1, Virtex-E 1.8V FPGAs:
  Introduction and Ordering Information (Module 1)
- DS022-2, Virtex-E 1.8V FPGAs:
  Functional Description (Module 2)
- DS022-3, Virtex-E 1.8V FPGAs:
  DC and Switching Characteristics (Module 3)
- DS022-4, Virtex-E 1.8V FPGAs:
  Pinout Tables (Module 4)