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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	1536
Number of Logic Elements/Cells	6912
Total RAM Bits	131072
Number of I/O	176
Number of Gates	411955
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv300e-7fg256c

Table 1: **Virtex-E Field-Programmable Gate Array Family Members**

Device	System Gates	Logic Gates	CLB Array	Logic Cells	Differential I/O Pairs	User I/O	BlockRAM Bits	Distributed RAM Bits
XCV50E	71,693	20,736	16 x 24	1,728	83	176	65,536	24,576
XCV100E	128,236	32,400	20 x 30	2,700	83	196	81,920	38,400
XCV200E	306,393	63,504	28 x 42	5,292	119	284	114,688	75,264
XCV300E	411,955	82,944	32 x 48	6,912	137	316	131,072	98,304
XCV400E	569,952	129,600	40 x 60	10,800	183	404	163,840	153,600
XCV600E	985,882	186,624	48 x 72	15,552	247	512	294,912	221,184
XCV1000E	1,569,178	331,776	64 x 96	27,648	281	660	393,216	393,216
XCV1600E	2,188,742	419,904	72 x 108	34,992	344	724	589,824	497,664
XCV2000E	2,541,952	518,400	80 x 120	43,200	344	804	655,360	614,400
XCV2600E	3,263,755	685,584	92 x 138	57,132	344	804	753,664	812,544
XCV3200E	4,074,387	876,096	104 x 156	73,008	344	804	851,968	1,038,336

Virtex-E Compared to Virtex Devices

The Virtex-E family offers up to 43,200 logic cells in devices up to 30% faster than the Virtex family.

I/O performance is increased to 622 Mb/s using Source Synchronous data transmission architectures and synchronous system performance up to 240 MHz using singled-ended SelectI/O technology. Additional I/O standards are supported, notably LVPECL, LVDS, and BLVDS, which use two pins per signal. Almost all signal pins can be used for these new standards.

Virtex-E devices have up to 640 Kb of faster (250 MHz) block SelectRAM, but the individual RAMs are the same size and structure as in the Virtex family. They also have eight DLLs instead of the four in Virtex devices. Each individual DLL is slightly improved with easier clock mirroring and 4x frequency multiplication.

V_{CCINT}, the supply voltage for the internal logic and memory, is 1.8 V, instead of 2.5 V for Virtex devices. Advanced processing and 0.18 μm design rules have resulted in smaller dice, faster speed, and lower power consumption.

I/O pins are 3 V tolerant, and can be 5 V tolerant with an external 100 Ω resistor. PCI 5 V is not supported. With the addition of appropriate external resistors, any pin can tolerate any voltage desired.

Banking rules are different. With Virtex devices, all input buffers are powered by V_{CCINT}. With Virtex-E devices, the LVTTL, LVCMOS2, and PCI input buffers are powered by the I/O supply voltage V_{CCO}.

The Virtex-E family is not bitstream-compatible with the Virtex family, but Virtex designs can be compiled into equivalent Virtex-E devices.

The same device in the same package for the Virtex-E and Virtex families are pin-compatible with some minor exceptions. See the data sheet pinout section for details.

General Description

The Virtex-E FPGA family delivers high-performance, high-capacity programmable logic solutions. Dramatic increases in silicon efficiency result from optimizing the new architecture for place-and-route efficiency and exploiting an aggressive 6-layer metal 0.18 μm CMOS process. These advances make Virtex-E FPGAs powerful and flexible alternatives to mask-programmed gate arrays. The Virtex-E family includes the nine members in Table 1.

Building on experience gained from Virtex FPGAs, the Virtex-E family is an evolutionary step forward in programmable logic design. Combining a wide variety of programmable system features, a rich hierarchy of fast, flexible interconnect resources, and advanced process technology, the Virtex-E family delivers a high-speed and high-capacity programmable logic solution that enhances design flexibility while reducing time-to-market.

Virtex-E Architecture

Virtex-E devices feature a flexible, regular architecture that comprises an array of configurable logic blocks (CLBs) surrounded by programmable input/output blocks (IOBs), all interconnected by a rich hierarchy of fast, versatile routing resources. The abundance of routing resources permits the Virtex-E family to accommodate even the largest and most complex designs.

Virtex-E FPGAs are SRAM-based, and are customized by loading configuration data into internal memory cells. Configuration data can be read from an external SPROM (master serial mode), or can be written into the FPGA (SelectMAP™, slave serial, and JTAG modes).

The standard Xilinx Foundation Series™ and Alliance Series™ Development systems deliver complete design support for Virtex-E, covering every aspect from behavioral and schematic entry, through simulation, automatic design translation and implementation, to the creation and downloading of a configuration bit stream.

Higher Performance

Virtex-E devices provide better performance than previous generations of FPGAs. Designs can achieve synchronous system clock rates up to 240 MHz including I/O or 622 Mb/s using Source Synchronous data transmission architectures. Virtex-E I/Os comply fully with 3.3 V PCI specifications, and interfaces can be implemented that operate at 33 MHz or 66 MHz.

While performance is design-dependent, many designs operate internally at speeds in excess of 133 MHz and can achieve over 311 MHz. Table 2 shows performance data for representative circuits, using worst-case timing parameters.

Table 2: **Performance for Common Circuit Functions**

Function	Bits	Virtex-E (-7)
Register-to-Register		
Adder	16 64	4.3 ns 6.3 ns
Pipelined Multiplier	8 x 8 16 x 16	4.4 ns 5.1 ns
Address Decoder	16 64	3.8 ns 5.5 ns
16:1 Multiplexer		4.6 ns
Parity Tree	9 18 36	3.5 ns 4.3 ns 5.9 ns
Chip-to-Chip		
HSTL Class IV		
LVTTL,16mA, fast slew		
LVDS		
LVPECL		

Virtex-E Device/Package Combinations and Maximum I/O

Table 3: **Virtex-E Family Maximum User I/O by Device/Package (Excluding Dedicated Clock Pins)**

	XCV 50E	XCV 100E	XCV 200E	XCV 300E	XCV 400E	XCV 600E	XCV 1000E	XCV 1600E	XCV 2000E	XCV 2600E	XCV 3200E
CS144	94	94	94								
PQ240	158	158	158	158	158						
HQ240						158	158				
BG352		196	260	260							
BG432				316	316	316					
BG560					404	404	404	404	404		
FG256	176	176	176	176							
FG456			284	312							
FG676					404	444					
FG680						512	512	512	512		
FG860							660	660	660		
FG900						512	660	700			
FG1156							660	724	804	804	804

Dedicated Routing

Some classes of signal require dedicated routing resources to maximize performance. In the Virtex-E architecture, dedicated routing resources are provided for two classes of signal.

- Horizontal routing resources are provided for on-chip 3-state buses. Four partitionable bus lines are provided per CLB row, permitting multiple buses within a row, as shown in Figure 8.
- Two dedicated nets per CLB propagate carry signals vertically to the adjacent CLB.Global Clock Distribution Network
- DLL Location

Clock Routing

Clock Routing resources distribute clocks and other signals with very high fanout throughout the device. Virtex-E devices include two tiers of clock routing resources referred to as global and local clock routing resources.

- The global routing resources are four dedicated global nets with dedicated input pins that are designed to distribute high-fanout clock signals with minimal skew. Each global clock net can drive all CLB, IOB, and block RAM clock pins. The global nets can be driven only by global buffers. There are four global buffers, one for each global net.
- The local clock routing resources consist of 24 backbone lines, 12 across the top of the chip and 12 across bottom. From these lines, up to 12 unique signals per column can be distributed via the 12 longlines in the column. These local resources are more flexible than the global resources since they are not restricted to routing only to clock pins.

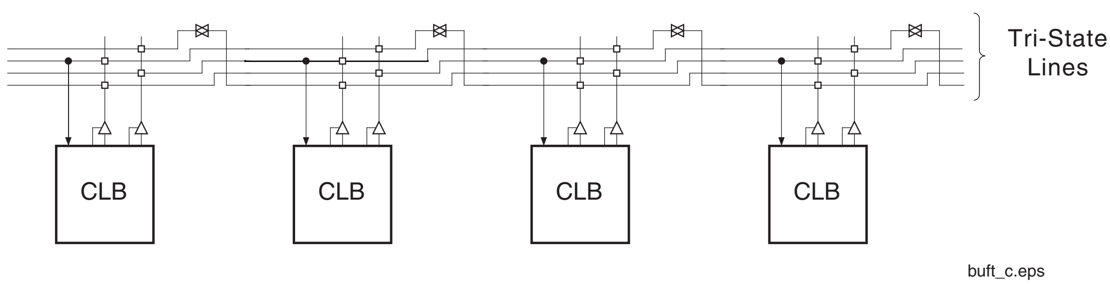

Figure 8: **BUFT Connections to Dedicated Horizontal Bus LInes**

Global Clock Distribution

Virtex-E provides high-speed, low-skew clock distribution through the global routing resources described above. A typical clock distribution net is shown in Figure 9.

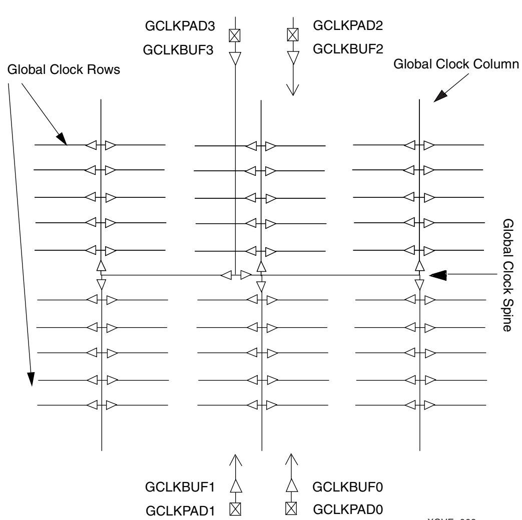

Figure 9: **Global Clock Distribution Network**

Four global buffers are provided, two at the top center of the device and two at the bottom center. These drive the four global nets that in turn drive any clock pin.

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is selected either from these pads or from signals in the general purpose routing.

Digital Delay-Locked Loops

There are eight DLLs (Delay-Locked Loops) per device, with four located at the top and four at the bottom, Figure 10. The DLLs can be used to eliminate skew between the clock input pad and the internal clock input pins throughout the device. Each DLL can drive two global clock networks.The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element. Additional delay is introduced such that clock edges arrive at internal flip-flops synchronized with clock edges arriving at the input.

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock, and can double the clock or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

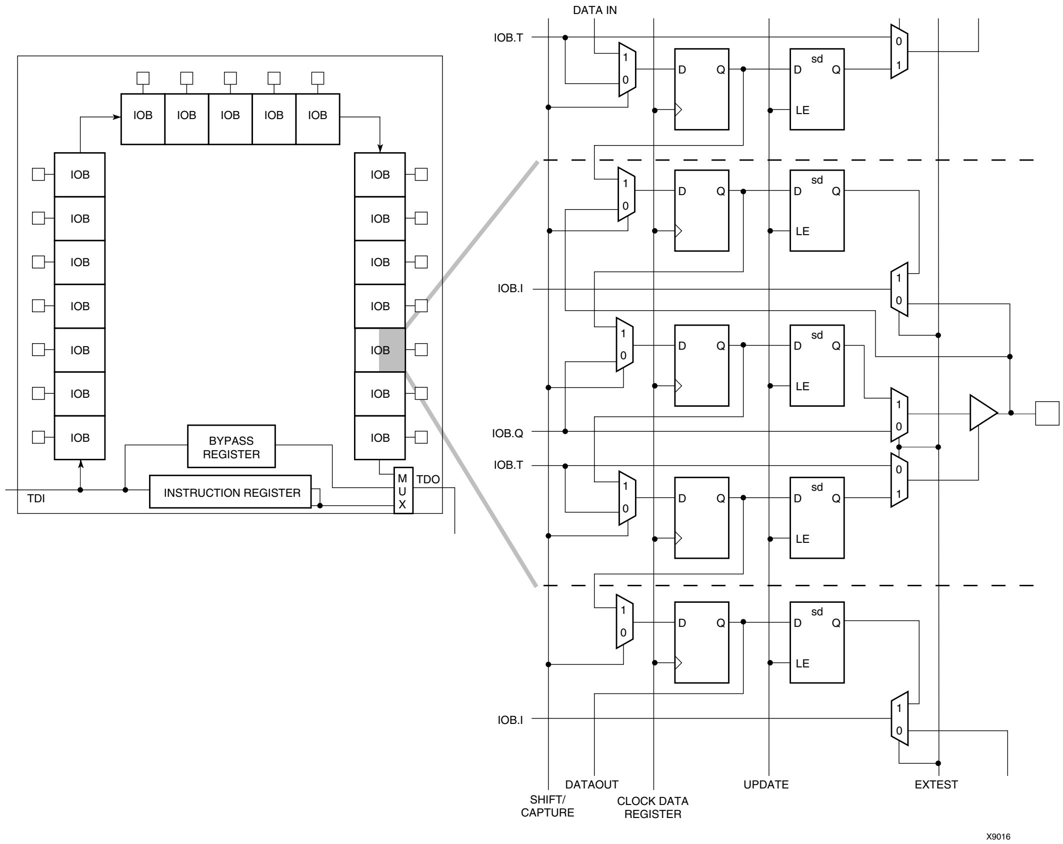

Figure 11: **Virtex-E Family Boundary Scan Logic**

Instruction Set

The Virtex-E series Boundary Scan instruction set also includes instructions to configure the device and read back configuration data (CFG_IN, CFG_OUT, and JSTART). The complete instruction set is coded as shown in Table 6..

Table 6: **Boundary Scan Instructions**

Boundary Scan Command	Binary Code(4:0)	Description
EXTEST	00000	Enables Boundary Scan EXTEST operation
SAMPLE/ PRELOAD	00001	Enables Boundary Scan SAMPLE/PRELOAD operation
USER1	00010	Access user-defined register 1
USER2	00011	Access user-defined register 2
CFG_OUT	00100	Access the configuration bus for read operations.
CFG_IN	00101	Access the configuration bus for write operations.
INTEST	00111	Enables Boundary Scan INTEST operation
USERCODE	01000	Enables shifting out USER code
IDCODE	01001	Enables shifting out of ID Code
HIGHZ	01010	3-states output pins while enabling the Bypass Register
JSTART	01100	Clock the start-up sequence when StartupClk is TCK
BYPASS	11111	Enables BYPASS
RESERVED	All other codes	Xilinx reserved instructions

For in-circuit debugging, an optional download and read-back cable is available. This cable connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can single-step the logic, readback the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be down-loaded into the system in a matter of minutes.

Configuration

Virtex-E devices are configured by loading configuration data into the internal configuration memory. Note that attempting to load an incorrect bitstream causes configuration to fail and can damage the device.

Some of the pins used for configuration are dedicated pins, while others can be re-used as general purpose inputs and outputs once configuration is complete.

The following are dedicated pins:

- Mode pins (M2, M1, M0)
- Configuration clock pin (CCLK)
- $\overline{\text{PROGRAM}}$ pin
- DONE pin
- Boundary Scan pins (TDI, TDO, TMS, TCK)

Depending on the configuration mode chosen, CCLK can be an output generated by the FPGA, or can be generated externally and provided to the FPGA as an input. The $\overline{\text{PROGRAM}}$ pin must be pulled High prior to reconfiguration.

Note that some configuration pins can act as outputs. For correct operation, these pins require a V_{CCO} of 3.3 V or 2.5 V. At 3.3 V the pins operate as LVTTL, and at 2.5 V they operate as LVCMOS. All affected pins fall in banks 2 or 3. The configuration pins needed for SelectMap (CS, Write) are located in bank 1.

Configuration Modes

Virtex-E supports the following four configuration modes.

- Slave-serial mode
- Master-serial mode
- SelectMAP mode
- Boundary Scan mode (JTAG)

The Configuration mode pins (M2, M1, M0) select among these configuration modes with the option in each case of having the IOB pins either pulled up or left floating prior to configuration. The selection codes are listed in Table 8.

Configuration through the Boundary Scan port is always available, independent of the mode selection. Selecting the Boundary Scan mode simply turns off the other modes. The three mode pins have internal pull-up resistors, and default to a logic High if left unconnected. However, it is recommended to drive the configuration mode pins externally.

Table 8: **Configuration Codes**

Configuration Mode	M2(1)	M1	M0	CCLK Direction	Data Width	Serial D_{out}	Configuration Pull-ups(1)
Master-serial mode	0	0	0	Out	1	Yes	No
Boundary Scan mode	1	0	1	N/A	1	No	No
SelectMAP mode	1	1	0	In	8	No	No
Slave-serial mode	1	1	1	In	1	Yes	No
Master-serial mode	1	0	0	Out	1	Yes	Yes
Boundary Scan mode	0	0	1	N/A	1	No	Yes
SelectMAP mode	0	1	0	In	8	No	Yes
Slave-serial mode	0	1	1	In	1	Yes	Yes

Notes:
1. M2 is sampled continuously from power up until the end of the configuration. Toggling M2 while INIT is being held externally Low can cause the configuration pull-up settings to change.

Verilog Initialization Example

```
module MYMEM (CLK, WE, ADDR, DIN, DOUT);
input CLK, WE;
input [8:0] ADDR;
input [7:0] DIN;
output [7:0] DOUT;

wire logic0, logic1;

//synopsys dc_script_begin
//set_attribute ram0 INIT_00
"0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF" -type string
//set_attribute ram0 INIT_01
"FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210" -type string
//synopsys dc_script_end

assign logic0 = 1'b0;
assign logic1 = 1'b1;

RAMB4_S8 ram0 (.WE(WE), .EN(logic1), .RST(logic0), .CLK(CLK), .ADDR(ADDR), .DI(DIN),
.DO(DOUT));
//synopsys translate_off
defparam ram0.INIT_00 =
256h'0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF;
defparam ram0.INIT_01 =
256h'FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210;
//synopsys translate_on
endmodule
```

Using SelectI/O

The Virtex-E FPGA series includes a highly configurable, high-performance I/O resource, called SelectI/O™ to provide support for a wide variety of I/O standards. The SelectI/O resource is a robust set of features including programmable control of output drive strength, slew rate, and input delay and hold time. Taking advantage of the flexibility and SelectI/O features and the design considerations described in this document can improve and simplify system level design.

Introduction

As FPGAs continue to grow in size and capacity, the larger and more complex systems designed for them demand an increased variety of I/O standards. Furthermore, as system clock speeds continue to increase, the need for high performance I/O becomes more important.

While chip-to-chip delays have an increasingly substantial impact on overall system speed, the task of achieving the desired system performance becomes more difficult with the proliferation of low-voltage I/O standards. SelectI/O, the revolutionary input/output resources of Virtex-E devices, resolve this potential problem by providing a highly configurable, high-performance alternative to the I/O resources of more conventional programmable devices. Virtex-E SelectI/O features combine the flexibility and time-to-market advantages of programmable logic with the high performance previously available only with ASICs and custom ICs.

Each SelectI/O block can support up to 20 I/O standards. Supporting such a variety of I/O standards allows the support of a wide variety of applications, from general purpose standard applications to high-speed low-voltage memory buses.

SelectI/O blocks also provide selectable output drive strengths and programmable slew rates for the LVTTL output buffers, as well as an optional, programmable weak pull-up, weak pull-down, or weak "keeper" circuit ideal for use in external bussing applications.

Each Input/Output Block (IOB) includes three registers, one each for the input, output, and 3-state signals within the IOB. These registers are optionally configurable as either a D-type flip-flop or as a level sensitive latch.

The input buffer has an optional delay element used to guarantee a zero hold time requirement for input signals registered within the IOB.

The Virtex-E SelectI/O features also provide dedicated resources for input reference voltage (V_{REF}) and output source voltage (V_{CCO}), along with a convenient banking system that simplifies board design.

By taking advantage of the built-in features and wide variety of I/O standards supported by the SelectI/O features, system-level design and board design can be greatly simplified and improved.

SSTL3_I

A sample circuit illustrating a valid termination technique for SSTL3_I appears in Figure 49. DC voltage specifications appear in Table 28.

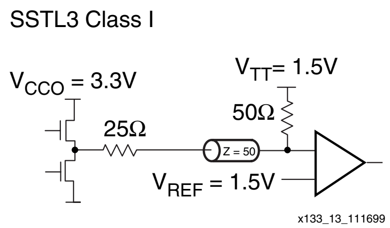

Figure 49: **Terminated SSTL3 Class I**

Table 28: **SSTL3_I Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	**3.0**	**3.3**	**3.6**
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} = V_{REF} + 0.2$	1.5	1.7	3.9(1)
$V_{IL} = V_{REF} - 0.2$	–0.3(2)	1.3	1.5
$V_{OH} = V_{REF} + 0.6$	1.9	-	-
$V_{OL} = V_{REF} - 0.6$	-	-	1.1
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL}at V_{OL} (mA)	8	-	-

Notes:
1. V_{IH} maximum is V_{CCO} + 0.3
2. V_{IL} minimum does not conform to the formula

SSTL3_II

A sample circuit illustrating a valid termination technique for SSTL3_II appears in Figure 50. DC voltage specifications appear in Table 29.

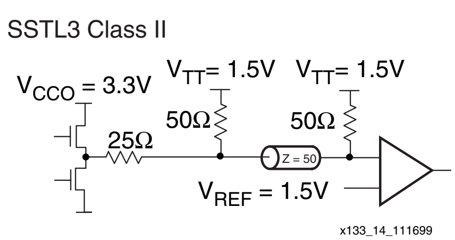

Figure 50: **Terminated SSTL3 Class II**

Table 29: **SSTL3_II Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} = V_{REF} + 0.2$	1.5	1.7	3.9(1)
$V_{IL}= V_{REF} - 0.2$	–0.3(2)	1.3	1.5
$V_{OH} = V_{REF} + 0.8$	2.1	-	-
$V_{OL}= V_{REF} - 0.8$	-	-	0.9
I_{OH} at V_{OH} (mA)	–16	-	-
I_{OL}at V_{OL} (mA)	16	-	-

Notes:
1. V_{IH} maximum is V_{CCO} + 0.3
2. V_{IL} minimum does not conform to the formula

SSTL2_I

A sample circuit illustrating a valid termination technique for SSTL2_I appears in Figure 51. DC voltage specifications appear in Table 30.

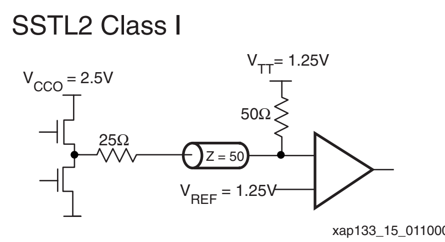

Figure 51: **Terminated SSTL2 Class I**

Table 30: **SSTL2_I Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
$V_{REF} = 0.5 \times V_{CCO}$	1.15	1.25	1.35
$V_{TT} = V_{REF} + N$(1)	1.11	1.25	1.39
$V_{IH} = V_{REF} + 0.18$	1.33	1.43	3.0(2)
$V_{IL} = V_{REF} - 0.18$	–0.3(3)	1.07	1.17
$V_{OH} = V_{REF} + 0.61$	1.76	-	-
$V_{OL}= V_{REF} - 0.61$	-	-	0.74
I_{OH} at V_{OH} (mA)	–7.6	-	-
I_{OL}at V_{OL} (mA)	7.6	-	-

Notes:
1. N must be greater than or equal to -0.04 and less than or equal to 0.04.
2. V_{IH} maximum is V_{CCO} + 0.3.
3. V_{IL} minimum does not conform to the formula.

Table 44: **Bidirectional I/O Library Macros**

Name	Inputs	Bidirectional	Outputs
IOBUFDS_FD_LVDS	D, T, C	IO, IOB	Q
IOBUFDS_FDE_LVDS	D, T, CE, C	IO, IOB	Q
IOBUFDS_FDC_LVDS	D, T, C, CLR	IO, IOB	Q
IOBUFDS_FDCE_LVDS	D, T, CE, C, CLR	IO, IOB	Q
IOBUFDS_FDP_LVDS	D, T, C, PRE	IO, IOB	Q
IOBUFDS_FDPE_LVDS	D, T, CE, C, PRE	IO, IOB	Q
IOBUFDS_FDR_LVDS	D, T, C, R	IO, IOB	Q
IOBUFDS_FDRE_LVDS	D, T, CE, C, R	IO, IOB	Q
IOBUFDS_FDS_LVDS	D, T, C, S	IO, IOB	Q
IOBUFDS_FDSE_LVDS	D, T, CE, C, S	IO, IOB	Q
IOBUFDS_LD_LVDS	D, T, G	IO, IOB	Q
IOBUFDS_LDE_LVDS	D, T, GE, G	IO, IOB	Q
IOBUFDS_LDC_LVDS	D, T, G, CLR	IO, IOB	Q
IOBUFDS_LDCE_LVDS	D, T, GE, G, CLR	IO, IOB	Q
IOBUFDS_LDP_LVDS	D, T, G, PRE	IO, IOB	Q
IOBUFDS_LDPE_LVDS	D, T, GE, G, PRE	IO, IOB	Q

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/7/99	1.0	Initial Xilinx release.
1/10/00	1.1	Re-released with spd.txt v. 1.18, FG860/900/1156 package information, and additional DLL, Select RAM and SelectI/O information.
1/28/00	1.2	Added Delay Measurement Methodology table, updated SelectI/O section, Figures 30, 54, & 55, text explaining Table 5, T_{BYP} values, buffered Hex Line info, p. 8, I/O Timing Measurement notes, notes for Tables 15, 16, and corrected F1156 pinout table footnote references.
2/29/00	1.3	Updated pinout tables, V_{CC} page 20, and corrected Figure 20.
5/23/00	1.4	Correction to table on p. 22.
7/10/00	1.5	• Numerous minor edits. • Data sheet upgraded to Preliminary. • Preview -8 numbers added to **Virtex-E Electrical Characteristics** tables.
8/1/00	1.6	• Reformatted entire document to follow new style guidelines. • Changed speed grade values in tables on pages 35-37.

Virtex-E Electrical Characteristics

Definition of Terms

Electrical and switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance: These speed files are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These speed files are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production: These speed files are released once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. Contact the factory for design considerations requiring more detailed information.

Table 1 correlates the current status of each Virtex-E device with a corresponding speed file designation.

Table 1: **Virtex-E Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	**Preliminary**	**Production**
XCV50E			–8, –7, –6
XCV100E			–8, –7, –6
XCV200E			–8, –7, –6
XCV300E			–8, –7, –6
XCV400E			–8, –7, –6
XCV600E			–8, –7, –6
XCV1000E			–8, –7, –6
XCV1600E			–8, –7, –6
XCV2000E			–8, –7, –6
XCV2600E			–8, –7, –6
XCV3200E			–8, –7, –6

All specifications are subject to change without notice.

IOB Input Switching Characteristics Standard Adjustments

Description	Symbol	Standard	Speed Grade[(1)] Min	-8	-7	-6	Units
Data Input Delay Adjustments							
Standard-specific data input delay adjustments	T_{ILVTTL}	LVTTL	0.0	0.0	0.0	0.0	ns
	$T_{ILVCMOS2}$	LVCMOS2	–0.02	0.0	0.0	0.0	ns
	$T_{ILVCMOS18}$	LVCMOS18	0.12	+0.20	+0.20	+0.20	ns
	T_{ILVDS}	LVDS	0.00	+0.15	+0.15	+0.15	ns
	$T_{ILVPECL}$	LVPECL	0.00	+0.15	+0.15	+0.15	ns
	T_{IPCI33_3}	PCI, 33 MHz, 3.3 V	–0.05	+0.08	+0.08	+0.08	ns
	T_{IPCI66_3}	PCI, 66 MHz, 3.3 V	–0.05	–0.11	–0.11	–0.11	ns
	T_{IGTL}	GTL	+0.10	+0.14	+0.14	+0.14	ns
	$T_{IGTLPLUS}$	GTL+	+0.06	+0.14	+0.14	+0.14	ns
	T_{IHSTL}	HSTL	+0.02	+0.04	+0.04	+0.04	ns
	T_{ISSTL2}	SSTL2	–0.04	+0.04	+0.04	+0.04	ns
	T_{ISSTL3}	SSTL3	–0.02	+0.04	+0.04	+0.04	ns
	T_{ICTT}	CTT	+0.01	+0.10	+0.10	+0.10	ns
	T_{IAGP}	AGP	–0.03	+0.04	+0.04	+0.04	ns

Notes:
1. Input timing i for LVTTL is measured at 1.4 V. For other I/O standards, see Table 4.

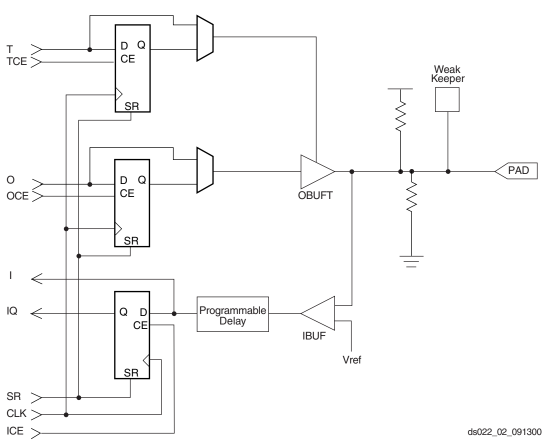

Figure 1: **Virtex-E Input/Output Block (IOB)**

Low Voltage Differential Signals

The Virtex-E family incorporates low-voltage signalling (LVDS and LVPECL). Two pins are utilized for these signals to be connected to a Virtex-E device. These are known as differential pin pairs. Each differential pin pair has a Positive (P) and a Negative (N) pin. These pairs are labeled in the following manner.

IO_L#[P/N]

where

L = LVDS or LVPECL pin
# = Pin Pair Number
P = Positive
N = Negative

I/O pins for differential signals can either be synchronous or asynchronous, input or output. The pin pairs can be used for synchronous input and output signals as well as asynchronous input signals. However, only some of the low-voltage pairs can be used for asynchronous output signals.

DIfferential signals require the pins of a pair to switch almost simultaneously. If the signals driving the pins are from IOB flip-flops, they are synchronous. If the signals driving the pins are from internal logic, they are asynchronous. Table 2 defines the names and function of the different types of low-voltage pin pairs in the Virtex-E family.

Table 2: **LVDS Pin Pairs**

Pin Name	Description
IO_L#[P/N] Example: IO_L22N	Represents a general IO or a synchronous input/output differential signal. When used as a differential signal, N means Negative I/O and P means Positive I/O.
IO_L#[P/N]_Y Example: IO_L22N_Y	Represents a general IO or a synchronous input/output differential signal, or a part-dependent asynchronous output differential signal.
IO_L#[P/N]_YY Example: O_L22N_YY	Represents a general IO or a synchronous input/output differential signal, or an asynchronous output differential signal.
IO_LVDS_DLL_L#[P/N] Example: IO_LVDS_DLL_L16N	Represents a general IO or a synchronous input/output differential signal, a differential clock input signal, or a DLL input. When used as a differential clock input, this pin is paired with the adjacent GCK pin. The GCK pin is always the positive input in the differential clock input configuration.

Virtex-E Package Pinouts

The Virtex-E family of FPGAs is available in 12 popular packages, including chip-scale, plastic and high heat-dissipation quad flat packs, and ball grid and fine-pitch ball grid arrays. Family members have footprint compatibility across devices provided in the same package. The pinout tables in this section indicate function, pin, and bank information for each package/device combination. Following each pinout table is an additional table summarizing information specific to differential pin pairs for all devices provided in that package.

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
4	IO_L104N_YY	AJ12	
4	IO_L105P_Y	AN11	
4	IO_L105N_Y	AK12	
4	IO_L106P_YY	AL12	
4	IO_L106N_YY	AM12	
4	IO_VREF_L107P_YY	AK13	3
4	IO_L107N_YY	AL13	
4	IO_L108P_Y	AM13	
4	IO_L108N_Y	AN13	
4	IO_L109P_YY	AJ14	
4	IO_L109N_YY	AK14	
4	IO_VREF_L110P_YY	AM14	
4	IO_L110N_YY	AN15	
4	IO_L111P_Y	AJ15	
4	IO_L111N_Y	AK15	
4	IO_L112P_Y	AL15	
4	IO_L112N_Y	AM16	
4	IO_VREF_L113P_Y	AL16	
4	IO_L113N_Y	AJ16	
4	IO_L114P_Y	AK16	
4	IO_VREF_L114N_Y	AN17	2
4	IO_LVDS_DLL_L115P	AM17	
5	GCK1	AJ17	
5	IO	AL25	
5	IO	AL28	
5	IO	AL30	
5	IO	AN28	
5	IO_LVDS_DLL_L115N	AM18	
5	IO_VREF	AL18	2
5	IO_L116P_Y	AK18	
5	IO_VREF_L116N_Y	AJ18	
5	IO_L117P_Y	AN19	
5	IO_L117N_Y	AL19	
5	IO_L118P_Y	AK19	
5	IO_L118N_Y	AM20	
5	IO_L119P_YY	AJ19	
5	IO_VREF_L119N_YY	AL20	
5	IO_L120P_YY	AN21	
5	IO_L120N_YY	AL21	
5	IO_L121P_Y	AJ20	
5	IO_L121N_Y	AM22	
5	IO_L122P_YY	AK21	
5	IO_VREF_L122N_YY	AN23	3
5	IO_L123P_YY	AJ21	
5	IO_L123N_YY	AM23	
5	IO_L124P_Y	AK22	
5	IO_L124N_Y	AM24	
5	IO_L125P_YY	AL23	
5	IO_L125N_YY	AJ22	
5	IO_L126P_YY	AK23	
5	IO_VREF_L126N_YY	AL24	
5	IO_L127P_Y	AN26	
5	IO_L127N_Y	AJ23	
5	IO_L128P_Y	AK24	
5	IO_VREF_L128N_Y	AM26	4
5	IO_L129P_Y	AM27	
5	IO_L129N_Y	AJ24	
5	IO_L130P_Y	AL26	
5	IO_VREF_L130N_Y	AK25	1
5	IO_L131P_YY	AN29	
5	IO_VREF_L131N_YY	AJ25	
5	IO_L132P_YY	AK26	
5	IO_L132N_YY	AM29	
5	IO_L133P_Y	AM30	
5	IO_L133N_Y	AJ26	
5	IO_L134P_YY	AK27	
5	IO_VREF_L134N_YY	AL29	
5	IO_L135P_YY	AN31	
5	IO_L135N_YY	AJ27	

Table 15: **BG560 Differential Pin Pair Summary XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
47	2	F4	C1	14	-
48	2	G5	E3	15	VREF
49	2	D2	G4	16	-
50	2	H5	E2	15	-
51	2	H4	G3	√	VREF
52	2	J5	F1	17	VREF
53	2	J4	H3	14	-
54	2	K5	H2	18	VREF
55	2	J3	K4	19	-
56	2	L5	K3	√	D1
57	2	L4	K2	√	D2
58	2	M5	L3	17	-
59	2	L1	M4	14	-
60	2	N5	M2	15	VREF
61	2	N4	N3	16	-
62	2	N2	P5	15	-
63	2	P4	P3	√	D3
64	2	P2	R5	17	-
65	2	R4	R3	14	-
66	2	R1	T4	18	VREF
67	2	T5	T3	19	VREF
68	2	T2	U3	√	-
69	3	U1	U2	19	VREF
70	3	V2	V4	18	VREF
71	3	V5	V3	14	-
72	3	W1	W3	17	-
73	3	W4	W5	√	VREF
74	3	Y3	Y4	15	-
75	3	AA1	Y5	16	-
76	3	AA3	AA4	15	VREF
77	3	AB3	AA5	14	-

Table 15: **BG560 Differential Pin Pair Summary XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
78	3	AC1	AB4	17	-
79	3	AC3	AB5	√	D5
80	3	AC4	AD3	√	VREF
81	3	AE1	AC5	4	-
82	3	AD4	AF1	18	VREF
83	3	AF2	AD5	14	-
84	3	AG2	AE4	20	VREF
85	3	AH1	AE5	√	VREF
86	3	AF4	AJ1	15	-
87	3	AJ2	AF5	14	-
88	3	AG4	AK2	15	VREF
89	3	AJ3	AG5	14	-
90	3	AL1	AH4	14	VREF
91	3	AJ4	AH5	√	INIT
92	4	AL4	AJ6	√	-
93	4	AK5	AN3	8	VREF
94	4	AL5	AJ7	√	-
95	4	AM4	AM5	√	VREF
96	4	AK7	AL6	3	-
97	4	AM6	AN6	√	-
98	4	AL7	AJ9	√	VREF
99	4	AN7	AL8	9	VREF
100	4	AM8	AJ10	7	-
101	4	AL9	AM9	7	VREF
102	4	AK10	AN9	2	-
103	4	AL10	AM10	√	VREF
104	4	AL11	AJ12	√	-
105	4	AN11	AK12	8	-
106	4	AL12	AM12	√	-
107	4	AK13	AL13	√	VREF
108	4	AM13	AN13	3	-

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
5	IO_L76N_Y	W11
5	IO_L77P_YY	V11
5	IO_VREF_L77N_YY	Y10
5	IO_L78P_YY	AB10
5	IO_L78N_YY	W10
5	IO_L79P_Y	V10
5	IO_L79N_Y	Y9
5	IO_L80P_Y	AB9
5	IO_L80N_Y	W9
5	IO_L81P_YY	V9
5	IO_L81N_YY	AA8
5	IO_L82P_YY	Y8
5	IO_VREF_L82N_YY	W8
5	IO_L83P_Y	W7
5	IO_L83N_Y	AA7
5	IO_L84P_Y	AB6
5	IO_L84N_Y	AA6
5	IO_L85P_YY	AB5
5	IO_VREF_L85N_YY	AA5
5	IO_L86P_YY	Y7
5	IO_L86N_YY	W6
5	IO_L87P_YY	AA4
5	IO_VREF_L87N_YY	Y6
5	IO_L88P_YY	V7
5	IO_L88N_YY	AB3
6	IO	M2[1]
6	IO	M5
6	IO	P4
6	IO	R3[1]
6	IO	T2
6	IO	T4
6	IO	U3[1]
6	IO	W2
6	IO	AA1[1]
6	IO_L89N_YY	W3
6	IO_L89P_YY	Y2

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
6	IO_L90N_YY	V4
6	IO_L90P_YY	V3
6	IO_VREF_L91N_YY	Y1
6	IO_L91P_YY	U4
6	IO_L92N_YY	V2
6	IO_L92P_YY	W1
6	IO_VREF_L93N_YY	T3
6	IO_L93P_YY	U2
6	IO_L94N_Y	T5
6	IO_L94P_Y	V1
6	IO_L95N_Y	R5
6	IO_L95P_Y	U1
6	IO_VREF_L96N_Y	R4
6	IO_L96P_Y	T1
6	IO_L97N_YY	R2
6	IO_L97P_YY	P3
6	IO_L98N_YY	P5
6	IO_L98P_YY	R1
6	IO_L99N_YY	P2
6	IO_L99P_YY	N5
6	IO_L100N_Y	P1
6	IO_L100P_Y	N4
6	IO_L101N	N3
6	IO_VREF_L101P	N2
6	IO_L102N_Y	N1
6	IO_L102P_Y	M4
6	IO_L103N_YY	M3
6	IO_L103P_YY	M6
6	IO	M1
7	IO	B1
7	IO	C2[1]
7	IO	D1[1]
7	IO	E4
7	IO	F4
7	IO	G2[1]
7	IO	G4

Table 19: **FG456 Differential Pin Pair Summary XCV200E, XCV300E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
18	1	C14	B14	2	-
19	1	A15	F12	2	-
20	1	C15	B15	√	-
21	1	E14	A16	√	VREF
22	1	C16	D14	2	-
23	1	A17	D15	2	-
24	1	A18	B17	√	VREF
25	1	C17	D16	√	-
26	1	A19	B18	√	VREF
27	1	C18	D17	√	-
28	1	C19	A20	√	CS
29	2	C21	D20	√	DIN, D0
30	2	C22	D21	√	-
31	2	D22	E21	√	VREF
32	2	E22	F18	√	-
33	2	F21	F19	√	VREF
34	2	F22	G19	2	-
35	2	G20	G18	1	-
36	2	H18	H22	2	D1, VREF
37	2	H20	H19	√	D2
38	2	H21	J19	√	-
39	2	J18	J20	√	-
40	2	K18	J21	2	-
41	2	K22	K21	1	VREF
42	2	K19	L22	2	-
43	2	L21	L18	√	-
44	2	L17	L20	√	-
45	3	M18	M20	√	-
46	3	M19	M17	2	-
47	3	N22	N21	2	VREF
48	3	N20	N18	√	-
49	3	N19	P21	√	-
50	3	P20	P19	√	-
51	3	P18	R21	√	D5
52	3	T22	R19	2	VREF

Table 19: **FG456 Differential Pin Pair Summary XCV200E, XCV300E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
53	3	U22	R18	2	-
54	3	T21	V22	√	-
55	3	T20	U21	√	VREF
56	3	W22	T18	√	-
57	3	U19	U20	√	VREF
58	3	W21	AA22	√	-
59	3	Y21	V19	√	INIT
60	4	W18	AA20	√	-
61	4	Y18	V17	NA	-
62	4	AB20	W17	√	VREF
63	4	AA18	V16	NA	-
64	4	AB19	AB18	√	VREF
65	4	W16	AA17	1	-
66	4	Y16	V15	1	-
67	4	AB16	Y15	√	VREF
68	4	AA15	AB15	√	-
69	4	W15	Y14	1	-
70	4	V14	AA14	1	-
71	4	AB14	V13	NA	-
72	4	AA13	AB13	√	VREF
73	4	W13	AA12	2	-
74	4	Y12	V12	2	-
75	5	U12	AA11	NA	IO_LVDS_DLL
76	5	AB11	W11	1	-
77	5	V11	Y10	√	VREF
78	5	AB10	W10	√	-
79	5	V10	Y9	2	-
80	5	AB9	W9	2	-
81	5	V9	AA8	√	-
82	5	Y8	W8	√	VREF
83	5	W7	AA7	2	-
84	5	AB6	AA6	2	-
85	5	AB5	AA5	√	VREF
86	5	Y7	W6	√	-
87	5	AA4	Y6	√	VREF

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
4	IO_VREF_L132P_YY	AV8
4	IO_L132N_YY	AU9
4	IO_L133P_Y	AW8
4	IO_L133N_Y	AT10
4	IO_VREF_L134P_Y	AV9[3]
4	IO_L134N_Y	AU10
4	IO_L135P_YY	AW9
4	IO_L135N_YY	AT11
4	IO_VREF_L136P_YY	AV10
4	IO_L136N_YY	AU11
4	IO_L137P_Y	AW10
4	IO_L137N_Y	AU12
4	IO_L138P_Y	AV11
4	IO_L138N_Y	AT13
4	IO_VREF_L139P_YY	AW11
4	IO_L139N_YY	AU13
4	IO_L140P_YY	AT14
4	IO_L140N_YY	AV12
4	IO_L141P_Y	AU14
4	IO_L141N_Y	AW12
4	IO_L142P_Y	AT15
4	IO_L142N_Y	AV13
4	IO_L143P_YY	AU15
4	IO_L143N_YY	AW13
4	IO_VREF_L144P_YY	AV14[1]
4	IO_L144N_YY	AT16
4	IO_L145P_Y	AW14
4	IO_L145N_Y	AU16
4	IO_L146P_Y	AV15
4	IO_L146N_Y	AR17
4	IO_L147P_YY	AW15
4	IO_L147N_YY	AT17
4	IO_VREF_L148P_YY	AU17
4	IO_L148N_YY	AV16
4	IO_L149P_Y	AR18
4	IO_L149N_Y	AW16
4	IO_L150P_Y	AT18
4	IO_L150N_Y	AV17
4	IO_L151P_YY	AU18
4	IO_L151N_YY	AW17
4	IO_VREF_L152P_YY	AT19
4	IO_L152N_YY	AV18
4	IO_L153P_Y	AU19
4	IO_L153N_Y	AW18
4	IO_VREF_L154P	AU21[2]
4	IO_L154N	AV19
4	IO_LVDS_DLL_L155P	AT21
5	GCK1	AU22
5	IO	AT34
5	IO	AW20
5	IO_LVDS_DLL_L155N	AT22
5	IO_VREF_L156P_Y	AV20[2]
5	IO_L156N_Y	AR22
5	IO_L157P_YY	AV23
5	IO_VREF_L157N_YY	AW21
5	IO_L158P_YY	AU23
5	IO_L158N_YY	AV21
5	IO_L159P_Y	AT23
5	IO_L159N_Y	AW22
5	IO_L160P_Y	AR23
5	IO_L160N_Y	AV22
5	IO_L161P_YY	AV24
5	IO_VREF_L161N_YY	AW23
5	IO_L162P_YY	AW24
5	IO_L162N_YY	AU24
5	IO_L163P_Y	AW25
5	IO_L163N_Y	AT24
5	IO_L164P_Y	AV25
5	IO_L164N_Y	AU25
5	IO_L165P_YY	AW26
5	IO_VREF_L165N_YY	AT25[1]

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
NA	VCCO_1	F15
NA	VCCO_1	F19
NA	VCCO_1	F20
NA	VCCO_1	F7
NA	VCCO_1	F8
NA	VCCO_2	G6
NA	VCCO_2	H6
NA	VCCO_2	L6
NA	VCCO_2	M6
NA	VCCO_2	P6
NA	VCCO_2	R6
NA	VCCO_2	W6
NA	VCCO_2	Y6
NA	VCCO_3	AC6
NA	VCCO_3	AD6
NA	VCCO_3	AH6
NA	VCCO_3	AJ6
NA	VCCO_3	AL6
NA	VCCO_3	AM6
NA	VCCO_3	AR6
NA	VCCO_3	AT6
NA	VCCO_4	AU11
NA	VCCO_4	AU12
NA	VCCO_4	AU14
NA	VCCO_4	AU15
NA	VCCO_4	AU19
NA	VCCO_4	AU20
NA	VCCO_4	AU7
NA	VCCO_4	AU8
NA	VCCO_5	AU23
NA	VCCO_5	AU24
NA	VCCO_5	AU28
NA	VCCO_5	AU29
NA	VCCO_5	AU31
NA	VCCO_5	AU32
NA	VCCO_5	AU35
NA	VCCO_5	AU36

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
NA	VCCO_6	AC37
NA	VCCO_6	AD37
NA	VCCO_6	AH37
NA	VCCO_6	AJ37
NA	VCCO_6	AL37
NA	VCCO_6	AM37
NA	VCCO_6	AR37
NA	VCCO_6	AT37
NA	VCCO_7	G37
NA	VCCO_7	H37
NA	VCCO_7	L37
NA	VCCO_7	M37
NA	VCCO_7	P37
NA	VCCO_7	R37
NA	VCCO_7	W37
NA	VCCO_7	Y37
NA	GND	N6
NA	GND	N5
NA	GND	N38
NA	GND	N37
NA	GND	F6
NA	GND	F37
NA	GND	F30
NA	GND	F22
NA	GND	F21
NA	GND	F13
NA	GND	E5
NA	GND	E38
NA	GND	E30
NA	GND	E22
NA	GND	E21
NA	GND	E13
NA	GND	D42
NA	GND	D4
NA	GND	D39
NA	GND	D1

Table 25: **FG860 Differential Pin Pair Summary XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
256	7	T38	T41	√	-
257	7	T42	R39	1	VREF
258	7	R38	R42	2	-
259	7	P39	R40	4	-
260	7	P38	R41	2	-
261	7	N39	P42	1	-
262	7	M39	P40	3	-
263	7	M38	P41	√	-
264	7	L39	N42	√	VREF
265	7	N41	L38	2	-
266	7	M42	K40	√	-
267	7	K38	M40	√	VREF
268	7	J40	M41	2	-
269	7	L40	J39	5	VREF
270	7	L41	J38	√	-
271	7	H39	K42	√	VREF
272	7	H38	K41	1	-
273	7	G40	J41	2	-
274	7	G39	H42	√	-
275	7	G42	G38	1	VREF
276	7	F40	G41	2	-
277	7	F41	F42	4	-
278	7	E42	F39	2	VREF
279	7	E41	E40	1	-
280	7	D41	E39	3	-

Notes:
1. AO in the XCV1000E, 2000E.
2. AO in the XCV1000E, 1600E.
3. AO in the XCV2000E.
4. AO in the XCV1600E.
5. AO in the XCV1000E.

FG900 Fine-Pitch Ball Grid Array Package

XCV600E, XCV1000E, and XCV1600E devices in the FG900 fine-pitch Ball Grid Array package have footprint compatibility. Pins labeled I0_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 26, see Table 27 for Differential Pair information.

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
0	GCK3	C15
0	IO	A7[4]
0	IO	A13[4]
0	IO	C5[4]
0	IO	C6[4]
0	IO	C14[4]
0	IO	D8[5]
0	IO	D10
0	IO	D13[4]
0	IO	E6
0	IO	E9[5]
0	IO	E14[5]
0	IO	F9[4]
0	IO	F14[5]
0	IO	G15
0	IO	K11[5]
0	IO	K12
0	IO	L13[4]
0	IO_L0N_YY	C4[4]
0	IO_L0P_YY	F7[3]
0	IO_L1N_Y	D5
0	IO_L1P_Y	G8
0	IO_VREF_L2N_Y	A3[1]
0	IO_L2P_Y	H9
0	IO_L3N_Y	B4[4]
0	IO_L3P_Y	J10[4]
0	IO_L4N_YY	A4
0	IO_L4P_YY	D6
0	IO_VREF_L5N_YY	E7
0	IO_L5P_YY	B5

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
2	IO_L99P_YY	N26
2	IO_L99N_YY	P28
2	IO_L100P	P29
2	IO_L100N	N24
2	IO_L101P_YY	P22
2	IO_L101N_YY	R26
2	IO_VREF_L102P_YY	P25
2	IO_L102N_YY	R29
2	IO_L103P_YY	R21[4]
2	IO_L103N_YY	R28[3]
2	IO_VREF_L104P_YY	R25[2]
2	IO_L104N_YY	T30
2	IO_L105P_YY	P24[4]
2	IO_L105N_YY	R27[3]
2	IO_L106P	R24
3	IO	T22[4]
3	IO	T24[4]
3	IO	T26[4]
3	IO	T29[4]
3	IO	U26[5]
3	IO	V23[4]
3	IO	V25[4]
3	IO	V30[5]
3	IO	Y21[4]
3	IO	AA26[4]
3	IO	AA23[4]
3	IO	AB27[4]
3	IO	AB29[4]
3	IO	AC28[5]
3	IO	AD26[4]
3	IO	AD29[5]
3	IO	AE27[5]
3	IO_L106N	U29
3	IO_L107P_YY	R22
3	IO_VREF_L107N_YY	T27[2]
3	IO_L108P_YY	R23

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
3	IO_L108N_YY	T28
3	IO_L109P_YY	T21
3	IO_VREF_L109N_YY	T25
3	IO_L110P_YY	U28
3	IO_L110N_YY	U30
3	IO_L111P	T23
3	IO_L111N	U27
3	IO_L112P_YY	U25
3	IO_L112N_YY	V27
3	IO_D4_L113P_YY	U24
3	IO_VREF_L113N_YY	V29
3	IO_L114P	W30
3	IO_L114N	U22
3	IO_L115P_YY	U21
3	IO_L115N_YY	W29
3	IO_L116P_YY	V26
3	IO_L116N_YY	W27
3	IO_L117P	W26
3	IO_VREF_L117N	Y29[1]
3	IO_L118P_YY	W25
3	IO_L118N_YY	Y30
3	IO_L119P_Y	V24[4]
3	IO_L119N_Y	Y28[4]
3	IO_L120P_YY	AA30
3	IO_L120N_YY	W24
3	IO_L121P	AA29
3	IO_L121N	V20
3	IO_L122P	Y27[4]
3	IO_L122N	W23[4]
3	IO_L123P_YY	Y26
3	IO_D5_L123N_YY	AB30
3	IO_D6_L124P_YY	V21
3	IO_VREF_L124N_YY	AA28
3	IO_L125P_YY	Y25
3	IO_L125N_YY	AA27
3	IO_L126P_YY	W22
3	IO_L126N_YY	Y23

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
270	6	AG2	AE7	2600 2000 1000	-
271	6	AG1	AF6	3200 2600 2000 1600 1000	VREF
272	6	AG4	AC9	2000 1600	-
273	6	AF3	AE6	3200 2600 2000 1600 1000	-
274	6	AF4	AF1	2600 1000	VREF
275	6	AF2	AB10	3200 2600 1600	-
276	6	AE1	AC8	3200 2600 1600 1000	-
277	6	AE3	AD5	3200 2600 2000 1600 1000	VREF
278	6	AD1	AC7	3200 2600 2000 1600 1000	-
279	6	AD2	AD6	3200 1600 1000	-
280	6	AC1	AB8	2000 1600 1000	VREF
281	6	AC2	AC5	3200 2600 2000 1600 1000	-
282	6	AC3	AA9	3200 2600 2000	-
283	6	AD4	AC4	2000 1000	-
284	6	AB6	AA8	3200 2600 1600 1000	-
285	6	Y10	AB1	2600 1600	-
286	6	AA7	AB2	3200 1600 1000	-
287	6	AA1	AA4	2600 2000 1000	VREF
288	6	AB4	Y9	3200 2600 2000 1600	-
289	6	Y8	AA2	3200 2600 2000 1600 1000	-
290	6	AA5	AA6	3200 2600 1600 1000	-
291	6	Y7	AB3	3200 2600 2000	-
292	6	W10	Y1	2600 2000 1000	-
293	6	Y2	Y5	2000 1600 1000	VREF
294	6	W2	W9	2000 1600	-
295	6	Y4	W7	3200 2600 2000 1600 1000	-
296	6	Y6	W1	1000	-
297	6	W3	W6	3200 1600	-
298	6	W4	V9	3200 2600 1600 1000	-
299	6	V1	W5	2000 1600 1000	VREF
300	6	U2	V7	2000 1600 1000	-
301	6	U1	V6	3200 2600 1600 1000	VREF
302	7	U4	U9	3200 2600 2000 1600 1000	-
303	7	U5	U7	3200 2600 1600 1000	VREF
304	7	U6	U3	2000 1600 1000	-
305	7	T6	T3	2000 1600 1000	VREF
306	7	T4	T9	3200 2600 1600 1000	-
307	7	R1	T5	3200 1600	-
308	7	T10	R6	1000	-
309	7	R5	R2	3200 2600 2000 1600 1000	-
310	7	P5	P1	2000 1600 1000	VREF