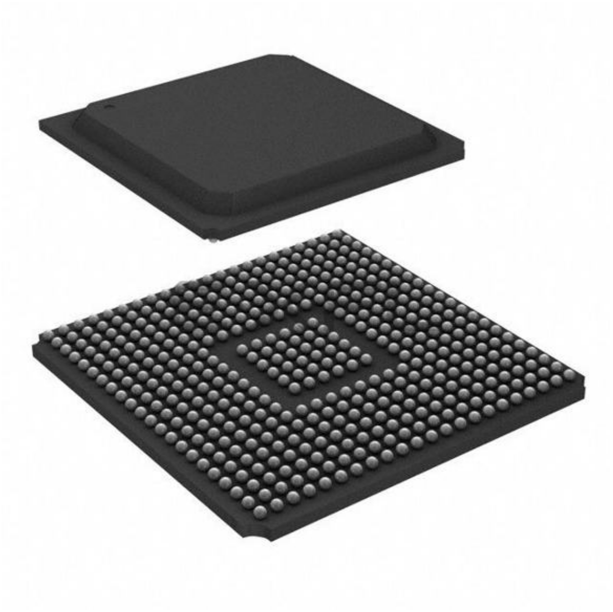

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 1536 |
| Number of Logic Elements/Cells | 6912 |
| Total RAM Bits | 131072 |
| Number of I/O | 312 |
| Number of Gates | 411955 |
| Voltage - Supply | 1.71V ~ 1.89V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 456-BBGA |
| Supplier Device Package | 456-FBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xcv300e-7fg456i |

For in-circuit debugging, an optional download and read-back cable is available. This cable connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can single-step the logic, readback the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.

## Configuration

Virtex-E devices are configured by loading configuration data into the internal configuration memory. Note that attempting to load an incorrect bitstream causes configuration to fail and can damage the device.

Some of the pins used for configuration are dedicated pins, while others can be re-used as general purpose inputs and outputs once configuration is complete.

The following are dedicated pins:

- Mode pins (M2, M1, M0)
- Configuration clock pin (CCLK)
- $\overline{\text{PROGRAM}}$ pin
- DONE pin
- Boundary Scan pins (TDI, TDO, TMS, TCK)

Depending on the configuration mode chosen, CCLK can be an output generated by the FPGA, or can be generated externally and provided to the FPGA as an input. The $\overline{\text{PROGRAM}}$ pin must be pulled High prior to reconfiguration.

Note that some configuration pins can act as outputs. For correct operation, these pins require a $V_{CCO}$ of 3.3 V or 2.5 V. At 3.3 V the pins operate as LVTTL, and at 2.5 V they operate as LVCMOS. All affected pins fall in banks 2 or 3. The configuration pins needed for SelectMap (CS, Write) are located in bank 1.

### Configuration Modes

Virtex-E supports the following four configuration modes.

- Slave-serial mode
- Master-serial mode
- SelectMAP mode
- Boundary Scan mode (JTAG)

The Configuration mode pins (M2, M1, M0) select among these configuration modes with the option in each case of having the IOB pins either pulled up or left floating prior to configuration. The selection codes are listed in Table 8.

Configuration through the Boundary Scan port is always available, independent of the mode selection. Selecting the Boundary Scan mode simply turns off the other modes. The three mode pins have internal pull-up resistors, and default to a logic High if left unconnected. However, it is recommended to drive the configuration mode pins externally.

*Table 8:* **Configuration Codes**

| Configuration Mode | M2(1) | M1 | M0 | CCLK Direction | Data Width | Serial $D_{out}$ | Configuration Pull-ups(1) |
|---|---|---|---|---|---|---|---|
| Master-serial mode | 0 | 0 | 0 | Out | 1 | Yes | No |
| Boundary Scan mode | 1 | 0 | 1 | N/A | 1 | No | No |
| SelectMAP mode | 1 | 1 | 0 | In | 8 | No | No |
| Slave-serial mode | 1 | 1 | 1 | In | 1 | Yes | No |
| Master-serial mode | 1 | 0 | 0 | Out | 1 | Yes | Yes |
| Boundary Scan mode | 0 | 0 | 1 | N/A | 1 | No | Yes |
| SelectMAP mode | 0 | 1 | 0 | In | 8 | No | Yes |
| Slave-serial mode | 0 | 1 | 1 | In | 1 | Yes | Yes |

**Notes:**

1. M2 is sampled continuously from power up until the end of the configuration. Toggling M2 while INIT is being held externally Low can cause the configuration pull-up settings to change.

Configuration through the TAP uses the CFG_IN instruction. This instruction allows data input on TDI to be converted into data packets for the internal configuration bus.

The following steps are required to configure the FPGA through the Boundary Scan port (when using TCK as a start-up clock).

1. Load the CFG_IN instruction into the Boundary Scan instruction register (IR).
2. Enter the Shift-DR (SDR) state.
3. Shift a configuration bitstream into TDI.
4. Return to Run-Test-Idle (RTI).
5. Load the JSTART instruction into IR.
6. Enter the SDR state.
7. Clock TCK through the startup sequence.
8. Return to RTI.

Configuration and readback via the TAP is always available. The Boundary Scan mode is selected by a <101> or <001> on the mode pins (M2, M1, M0). For details on TAP characteristics, refer to XAPP139.

## Configuration Sequence

The configuration of Virtex-E devices is a three-phase process. First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user, as described below. The configuration process can also be initiated by asserting $\overline{\text{PROGRAM}}$. The end of the memory-clearing phase is signalled by $\overline{\text{INIT}}$ going High, and the completion of the entire process is signalled by DONE going High.

The power-up timing of configuration signals is shown in Figure 20.

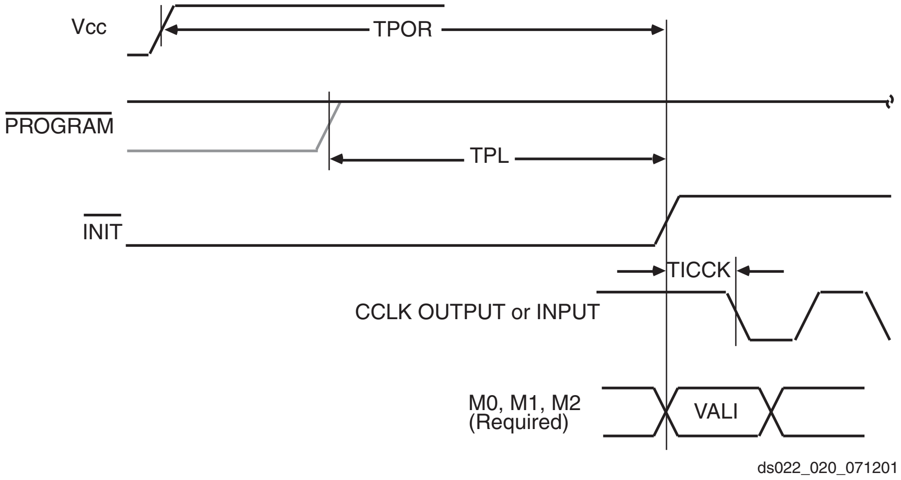

*Figure 20:* **Power-Up Timing Configuration Signals**

The corresponding timing characteristics are listed in Table 12.

*Table 12:* **Power-up Timing Characteristics**

| Description | Symbol | Value | Units |
|---|---|---|---|
| Power-on Reset[1] | $T_{POR}$ | 2.0 | ms, max |
| Program Latency | $T_{PL}$ | 100.0 | µs, max |
| CCLK (output) Delay | $T_{ICCK}$ | 0.5 | µs, min |
| | | 4.0 | µs, max |
| Program Pulse Width | $T_{PROGRAM}$ | 300 | ns, min |

**Notes:**

1. $T_{POR}$ delay is the initialization time required after $V_{CCINT}$ and $V_{CCO}$ in Bank 2 reach the recommended operating voltage.

### *Delaying Configuration*

$\overline{\text{INIT}}$ can be held Low using an open-drain driver. An open-drain is required since $\overline{\text{INIT}}$ is a bidirectional open-drain pin that is held Low by the FPGA while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

### *Start-Up Sequence*

The default Start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary.

One CCLK cycle later, the Global Set/Reset (GSR) and Global Write Enable (GWE) signals are released. This permits

## Verilog Initialization Example

```
module MYMEM (CLK, WE, ADDR, DIN, DOUT);
input CLK, WE;
input [8:0] ADDR;
input [7:0] DIN;
output [7:0] DOUT;

wire logic0, logic1;

//synopsys dc_script_begin
//set_attribute ram0 INIT_00
"0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF" -type string
//set_attribute ram0 INIT_01
"FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210" -type string
//synopsys dc_script_end

assign logic0 = 1'b0;
assign logic1 = 1'b1;

RAMB4_S8 ram0 (.WE(WE), .EN(logic1), .RST(logic0), .CLK(CLK), .ADDR(ADDR), .DI(DIN),
.DO(DOUT));
//synopsys translate_off
defparam ram0.INIT_00 =
256h'0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF;
defparam ram0.INIT_01 =
256h'FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210;
//synopsys translate_on
endmodule
```

# Using SelectI/O

The Virtex-E FPGA series includes a highly configurable, high-performance I/O resource, called SelectI/O™ to provide support for a wide variety of I/O standards. The SelectI/O resource is a robust set of features including programmable control of output drive strength, slew rate, and input delay and hold time. Taking advantage of the flexibility and SelectI/O features and the design considerations described in this document can improve and simplify system level design.

## Introduction

As FPGAs continue to grow in size and capacity, the larger and more complex systems designed for them demand an increased variety of I/O standards. Furthermore, as system clock speeds continue to increase, the need for high performance I/O becomes more important.

While chip-to-chip delays have an increasingly substantial impact on overall system speed, the task of achieving the desired system performance becomes more difficult with the proliferation of low-voltage I/O standards. SelectI/O, the revolutionary input/output resources of Virtex-E devices, resolve this potential problem by providing a highly configurable, high-performance alternative to the I/O resources of more conventional programmable devices. Virtex-E SelectI/O features combine the flexibility and time-to-market advantages of programmable logic with the high performance previously available only with ASICs and custom ICs.

Each SelectI/O block can support up to 20 I/O standards. Supporting such a variety of I/O standards allows the support of a wide variety of applications, from general purpose standard applications to high-speed low-voltage memory buses.

SelectI/O blocks also provide selectable output drive strengths and programmable slew rates for the LVTTL output buffers, as well as an optional, programmable weak pull-up, weak pull-down, or weak “keeper” circuit ideal for use in external bussing applications.

Each Input/Output Block (IOB) includes three registers, one each for the input, output, and 3-state signals within the IOB. These registers are optionally configurable as either a D-type flip-flop or as a level sensitive latch.

The input buffer has an optional delay element used to guarantee a zero hold time requirement for input signals registered within the IOB.

The Virtex-E SelectI/O features also provide dedicated resources for input reference voltage ($V_{REF}$) and output source voltage ($V_{CCO}$), along with a convenient banking system that simplifies board design.

By taking advantage of the built-in features and wide variety of I/O standards supported by the SelectI/O features, system-level design and board design can be greatly simplified and improved.

## Fundamentals

Modern bus applications, pioneered by the largest and most influential companies in the digital electronics industry, are commonly introduced with a new I/O standard tailored specifically to the needs of that application. The bus I/O standards provide specifications to other vendors who create products designed to interface with these applications. Each standard often has its own specifications for current, voltage, I/O buffering, and termination techniques.

The ability to provide the flexibility and time-to-market advantages of programmable logic is increasingly dependent on the capability of the programmable logic device to support an ever increasing variety of I/O standards

The SelectI/O resources feature highly configurable input and output buffers which provide support for a wide variety of I/O standards. As shown in Table 18, each buffer type can support a variety of voltage requirements.

*Table 18:* **Virtex-E Supported I/O Standards**

| I/O Standard | Output $V_{CCO}$ | Input $V_{CCO}$ | Input $V_{REF}$ | Board Termination Voltage ($V_{TT}$) |
|---|---|---|---|---|
| LVTTL | 3.3 | 3.3 | N/A | N/A |
| LVCMOS2 | 2.5 | 2.5 | N/A | N/A |
| LVCMOS18 | 1.8 | 1.8 | N/A | N/A |
| SSTL3 I & II | 3.3 | N/A | 1.50 | 1.50 |
| SSTL2 I & II | 2.5 | N/A | 1.25 | 1.25 |
| GTL | N/A | N/A | 0.80 | 1.20 |
| GTL+ | N/A | N/A | 1.0 | 1.50 |
| HSTL I | 1.5 | N/A | 0.75 | 0.75 |
| HSTL III & IV | 1.5 | N/A | 0.90 | 1.50 |
| CTT | 3.3 | N/A | 1.50 | 1.50 |
| AGP-2X | 3.3 | N/A | 1.32 | N/A |
| PCI33_3 | 3.3 | 3.3 | N/A | N/A |
| PCI66_3 | 3.3 | 3.3 | N/A | N/A |
| BLVDS & LVDS | 2.5 | N/A | N/A | N/A |
| LVPECL | 3.3 | N/A | N/A | N/A |

## Overview of Supported I/O Standards

This section provides a brief overview of the I/O standards supported by all Virtex-E devices.

While most I/O standards specify a range of allowed voltages, this document records typical voltage values only. Detailed information on each specification can be found on the Electronic Industry Alliance Jedec website at:

http://www.jedec.org

### *LVTTL — Low-Voltage TTL*

The Low-Voltage TTL, or LVTTL standard is a general purpose EIA/JESDSA standard for 3.3V applications that uses an LVTTL input buffer and a Push-Pull output buffer. This standard requires a 3.3V output source voltage ($V_{CCO}$), but does not require the use of a reference voltage ($V_{REF}$) or a termination voltage ($V_{TT}$).

### *LVCMOS2 — Low-Voltage CMOS for 2.5 Volts*

The Low-Voltage CMOS for 2.5 Volts or lower, or LVCMOS2 standard is an extension of the LVCMOS standard (JESD 8.-5) used for general purpose 2.5V applications. This standard requires a 2.5V output source voltage ($V_{CCO}$), but does not require the use of a reference voltage ($V_{REF}$) or a board termination voltage ($V_{TT}$).

### *LVCMOS18 — 1.8 V Low Voltage CMOS*

This standard is an extension of the LVCMOS standard. It is used in general purpose 1.8 V applications. The use of a reference voltage ($V_{REF}$) or a board termination voltage ($V_{TT}$) is not required.

### *PCI — Peripheral Component Interface*

The Peripheral Component Interface, or PCI standard specifies support for both 33 MHz and 66 MHz PCI bus applications. It uses a LVTTL input buffer and a Push-Pull output buffer. This standard does not require the use of a reference voltage ($V_{REF}$) or a board termination voltage ($V_{TT}$), however, it does require a 3.3V output source voltage ($V_{CCO}$).

### *GTL — Gunning Transceiver Logic Terminated*

The Gunning Transceiver Logic, or GTL standard is a high-speed bus standard (JESD8.3) invented by Xerox. Xilinx has implemented the terminated variation for this standard. This standard requires a differential amplifier input buffer and a Open Drain output buffer.

### *GTL+ — Gunning Transceiver Logic Plus*

The Gunning Transceiver Logic Plus, or GTL+ standard is a high-speed bus standard (JESD8.3) first used by the Pentium Pro processor.

### *HSTL — High-Speed Transceiver Logic*

The High-Speed Transceiver Logic, or HSTL standard is a general purpose high-speed, 1.5V bus standard sponsored by IBM (EIA/JESD 8-6). This standard has four variations or classes. SelectI/O devices support Class I, III, and IV. This

### SSTL3_I

A sample circuit illustrating a valid termination technique for SSTL3_I appears in Figure 49. DC voltage specifications appear in Table 28.

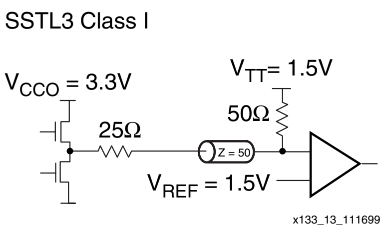

*Figure 49:* **Terminated SSTL3 Class I**

*Table 28:* **SSTL3_I Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | **3.0** | **3.3** | **3.6** |
| $V_{REF} = 0.45 \times V_{CCO}$ | 1.3 | 1.5 | 1.7 |
| $V_{TT} = V_{REF}$ | 1.3 | 1.5 | 1.7 |
| $V_{IH} = V_{REF} + 0.2$ | 1.5 | 1.7 | 3.9(1) |
| $V_{IL} = V_{REF} - 0.2$ | –0.3(2) | 1.3 | 1.5 |
| $V_{OH} = V_{REF} + 0.6$ | 1.9 | - | - |
| $V_{OL} = V_{REF} - 0.6$ | - | - | 1.1 |
| $I_{OH}$ at $V_{OH}$ (mA) | –8 | - | - |
| $I_{OL}$at $V_{OL}$ (mA) | 8 | - | - |

**Notes:**
1. $V_{IH}$ maximum is $V_{CCO}$ + 0.3
2. $V_{IL}$ minimum does not conform to the formula

### SSTL3_II

A sample circuit illustrating a valid termination technique for SSTL3_II appears in Figure 50. DC voltage specifications appear in Table 29.

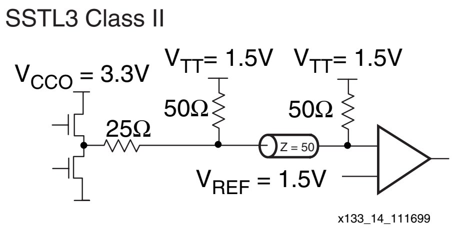

*Figure 50:* **Terminated SSTL3 Class II**

*Table 29:* **SSTL3_II Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 3.0 | 3.3 | 3.6 |
| $V_{REF} = 0.45 \times V_{CCO}$ | 1.3 | 1.5 | 1.7 |
| $V_{TT} = V_{REF}$ | 1.3 | 1.5 | 1.7 |
| $V_{IH} = V_{REF} + 0.2$ | 1.5 | 1.7 | 3.9(1) |
| $V_{IL} = V_{REF} - 0.2$ | –0.3(2) | 1.3 | 1.5 |
| $V_{OH} = V_{REF} + 0.8$ | 2.1 | - | - |
| $V_{OL} = V_{REF} - 0.8$ | - | - | 0.9 |
| $I_{OH}$ at $V_{OH}$ (mA) | –16 | - | - |
| $I_{OL}$at $V_{OL}$ (mA) | 16 | - | - |

**Notes:**
1. $V_{IH}$ maximum is $V_{CCO}$ + 0.3
2. $V_{IL}$ minimum does not conform to the formula

### SSTL2_I

A sample circuit illustrating a valid termination technique for SSTL2_I appears in Figure 51. DC voltage specifications appear in Table 30.

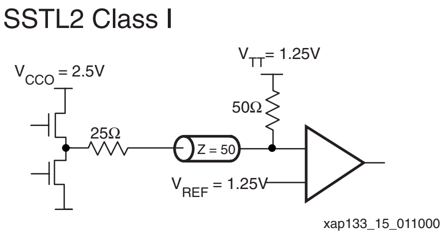

*Figure 51:* **Terminated SSTL2 Class I**

*Table 30:* **SSTL2_I Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 2.3 | 2.5 | 2.7 |
| $V_{REF} = 0.5 \times V_{CCO}$ | 1.15 | 1.25 | 1.35 |
| $V_{TT} = V_{REF} + N$(1) | 1.11 | 1.25 | 1.39 |
| $V_{IH} = V_{REF} + 0.18$ | 1.33 | 1.43 | 3.0(2) |
| $V_{IL} = V_{REF} - 0.18$ | –0.3(3) | 1.07 | 1.17 |
| $V_{OH} = V_{REF} + 0.61$ | 1.76 | - | - |
| $V_{OL} = V_{REF} - 0.61$ | - | - | 0.74 |
| $I_{OH}$ at $V_{OH}$ (mA) | –7.6 | - | - |
| $I_{OL}$at $V_{OL}$ (mA) | 7.6 | - | - |

**Notes:**
1. N must be greater than or equal to -0.04 and less than or equal to 0.04.
2. $V_{IH}$ maximum is $V_{CCO}$ + 0.3.
3. $V_{IL}$ minimum does not conform to the formula.

### LVTTL

LVTTL requires no termination. DC voltage specifications appears in Table 34.

*Table 34:* **LVTTL Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 3.0 | 3.3 | 3.6 |
| $V_{REF}$ | - | - | - |
| $V_{TT}$ | - | - | - |
| $V_{IH}$ | 2.0 | - | 3.6 |
| $V_{IL}$ | –0.5 | - | 0.8 |
| $V_{OH}$ | 2.4 | - | - |
| $V_{OL}$ | - | - | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | –24 | - | - |
| $I_{OL}$at $V_{OL}$ (mA) | 24 | - | - |

**Notes:**

1. Note: $V_{OL}$and $V_{OH}$ for lower drive currents sample tested.

### LVCMOS2

LVCMOS2 requires no termination. DC voltage specifications appear in Table 35.

*Table 35:* **LVCMOS2 Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 2.3 | 2.5 | 2.7 |
| $V_{REF}$ | - | - | - |
| $V_{TT}$ | - | - | - |
| $V_{IH}$ | 1.7 | - | 3.6 |
| $V_{IL}$ | –0.5 | - | 0.7 |
| $V_{OH}$ | 1.9 | - | - |
| $V_{OL}$ | - | - | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | –12 | - | - |
| $I_{OL}$at $V_{OL}$ (mA) | 12 | - | - |

### LVCMOS18

LVCMOS18 does not require termination. Table 36 lists DC voltage specifications.

*Table 36:* **LVCMOS18 Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 1.70 | 1.80 | 1.90 |
| $V_{REF}$ | - | - | - |
| $V_{TT}$ | - | - | - |
| $V_{IH}$ | 0.65 x $V_{CCO}$ | - | 1.95 |
| $V_{IL}$ | – 0.5 | - | 0.2 x $V_{CCO}$ |
| $V_{OH}$ | $V_{CCO}$ – 0.4 | - | - |
| $V_{OL}$ | - | - | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | –8 | - | - |
| $I_{OL}$at $V_{OL}$ (mA) | 8 | - | - |

### AGP-2X

The specification for the AGP-2X standard does not document a recommended termination technique. DC voltage specifications appear in Table 37.

*Table 37:* **AGP-2X Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 3.0 | 3.3 | 3.6 |
| $V_{REF} = N \times V_{CCO}$(1) | 1.17 | 1.32 | 1.48 |
| $V_{TT}$ | - | - | - |
| $V_{IH} = V_{REF} + 0.2$ | 1.37 | 1.52 | - |
| $V_{IL} = V_{REF} - 0.2$ | - | 1.12 | 1.28 |
| $V_{OH} = 0.9 \times V_{CCO}$ | 2.7 | 3.0 | - |
| $V_{OL} = 0.1 \times V_{CCO}$ | - | 0.33 | 0.36 |
| $I_{OH}$ at $V_{OH}$ (mA) | Note 2 | - | - |
| $I_{OL}$at $V_{OL}$ (mA) | Note 2 | - | - |

**Notes:**

1. N must be greater than or equal to 0.39 and less than or equal to 0.41.
2. Tested according to the relevant specification.

| Input/Output Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|
| | **V, Min** | **V, Max** | **V, Min** | **V, Max** | **V, Max** | **V, Min** | **mA** | **mA** |
| CTT | – 0.5 | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 3.6 | $V_{REF}$ – 0.4 | $V_{REF}$ + 0.4 | 8 | –8 |
| AGP | – 0.5 | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 3.6 | 10% $V_{CCO}$ | 90% $V_{CCO}$ | Note 2 | Note 2 |

**Notes:**

1. $V_{OL}$ and $V_{OH}$ for lower drive currents are sample tested.
2. Tested according to the relevant specifications.
3. DC input and output levels for HSTL18 (HSTL I/O standard with $V_{CCO}$ of 1.8 V) are provided in an HSTL white paper on www.xilinx.com.

## LVDS DC Specifications

| DC Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CCO}$ | | 2.375 | 2.5 | 2.625 | V |
| Output High Voltage for Q and $\overline{Q}$ | $V_{OH}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 1.25 | 1.425 | 1.6 | V |
| Output Low Voltage for Q and $\overline{Q}$ | $V_{OL}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 0.9 | 1.075 | 1.25 | V |
| Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High | $V_{ODIFF}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 250 | 350 | 450 | mV |
| Output Common-Mode Voltage | $V_{OCM}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 1.125 | 1.25 | 1.375 | V |
| Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High | $V_{IDIFF}$ | Common-mode input voltage = 1.25 V | 100 | 350 | NA | mV |
| Input Common-Mode Voltage | $V_{ICM}$ | Differential input voltage = ±350 mV | 0.2 | 1.25 | 2.2 | V |

Note: Refer to the Design Consideration section for termination schematics.

## LVPECL DC Specifications

These values are valid at the output of the source termination pack shown under LVPECL, with a 100 Ω differential load only. The $V_{OH}$ levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. The following table summarizes the DC output specifications of LVPECL.

| DC Parameter | Min | Max | Min | Max | Min | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{CCO}$ | **3.0** | | **3.3** | | **3.6** | | **V** |
| $V_{OH}$ | 1.8 | 2.11 | 1.92 | 2.28 | 2.13 | 2.41 | V |
| $V_{OL}$ | 0.96 | 1.27 | 1.06 | 1.43 | 1.30 | 1.57 | V |
| $V_{IH}$ | 1.49 | 2.72 | 1.49 | 2.72 | 1.49 | 2.72 | V |
| $V_{IL}$ | 0.86 | 2.125 | 0.86 | 2.125 | 0.86 | 2.125 | V |
| Differential Input Voltage | 0.3 | - | 0.3 | - | 0.3 | - | V |

## IOB Output Switching Characteristics Standard Adjustments

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

| | | | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| **Description** | **Symbol** | **Standard** | **Min** | **-8** | **-7** | **-6** | |
| **Output Delay Adjustments** | | | | | | | |
| Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl) | $T_{OLVTTL\_S2}$ | LVTTL, Slow, 2 mA | 4.2 | +14.7 | +14.7 | +14.7 | ns |
| | $T_{OLVTTL\_S4}$ | 4 mA | 2.5 | +7.5 | +7.5 | +7.5 | ns |
| | $T_{OLVTTL\_S6}$ | 6 mA | 1.8 | +4.8 | +4.8 | +4.8 | ns |
| | $T_{OLVTTL\_S8}$ | 8 mA | 1.2 | +3.0 | +3.0 | +3.0 | ns |
| | $T_{OLVTTL\_S12}$ | 12 mA | 1.0 | +1.9 | +1.9 | +1.9 | ns |
| | $T_{OLVTTL\_S16}$ | 16 mA | 0.9 | +1.7 | +1.7 | +1.7 | ns |
| | $T_{OLVTTL\_S24}$ | 24 mA | 0.8 | +1.3 | +1.3 | +1.3 | ns |
| | $T_{OLVTTL\_F2}$ | LVTTL, Fast, 2 mA | 1.9 | +13.1 | +13.1 | +13.1 | ns |
| | $T_{OLVTTL\_F4}$ | 4 mA | 0.7 | +5.3 | +5.3 | +5.3 | ns |
| | $T_{OLVTTL\_F6}$ | 6 mA | 0.20 | +3.1 | +3.1 | +3.1 | ns |
| | $T_{OLVTTL\_F8}$ | 8 mA | 0.10 | +1.0 | +1.0 | +1.0 | ns |
| | $T_{OLVTTL\_F12}$ | 12 mA | 0.0 | 0.0 | 0.0 | 0.0 | ns |
| | $T_{OLVTTL\_F16}$ | 16 mA | –0.10 | –0.05 | –0.05 | –0.05 | ns |
| | $T_{OLVTTL\_F24}$ | 24 mA | –0.10 | –0.20 | –0.20 | –0.20 | ns |
| | $T_{OLVCMOS\_2}$ | LVCMOS2 | 0.10 | +0.09 | +0.09 | +0.09 | ns |
| | $T_{OLVCMOS\_18}$ | LVCMOS18 | 0.10 | +0.7 | +0.7 | +0.7 | ns |
| | $T_{OLVDS}$ | LVDS | –0.39 | –1.2 | –1.2 | –1.2 | ns |
| | $T_{OLVPECL}$ | LVPECL | –0.20 | –0.41 | –0.41 | –0.41 | ns |
| | $T_{OPCI33\_3}$ | PCI, 33 MHz, 3.3 V | 0.50 | +2.3 | +2.3 | +2.3 | ns |
| | $T_{OPCI66\_3}$ | PCI, 66 MHz, 3.3 V | 0.10 | –0.41 | –0.41 | –0.41 | ns |
| | $T_{OGTL}$ | GTL | 0.6 | +0.49 | +0.49 | +0.49 | ns |
| | $T_{OGTLP}$ | GTL+ | 0.7 | +0.8 | +0.8 | +0.8 | ns |
| | $T_{OHSTL\_I}$ | HSTL I | 0.10 | –0.51 | –0.51 | –0.51 | ns |
| | $T_{OHSTL\_III}$ | HSTL III | –0.10 | –0.91 | –0.91 | –0.91 | ns |
| | $T_{OHSTL\_IV}$ | HSTL IV | –0.20 | –1.01 | –1.01 | –1.01 | ns |
| | $T_{OSSTL2\_I}$ | SSTL2 I | –0.10 | –0.51 | –0.51 | –0.51 | ns |
| | $T_{OSSTL2\_II}$ | SSTL2 II | –0.20 | –0.91 | –0.91 | –0.91 | ns |
| | $T_{OSSTL3\_I}$ | SSTL3 I | –0.20 | –0.51 | –0.51 | –0.51 | ns |
| | $T_{OSSTL3\_II}$ | SSTL3 II | –0.30 | –1.01 | –1.01 | –1.01 | ns |
| | $T_{OCTT}$ | CTT | 0.0 | –0.61 | –0.61 | –0.61 | ns |
| | $T_{OAGP}$ | AGP | –0.1 | –0.91 | –0.91 | –0.91 | ns |

## CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used, see Figure 2. The values listed below are worst-case. Precise values are provided by the timing analyzer.

| | | Speed Grade(1) | | | | Units |
|---|---|---|---|---|---|---|
| **Description** | **Symbol** | **Min** | **-8** | **-7** | **-6** | |
| **Combinatorial Delays** | | | | | | |
| 4-input function: F/G inputs to X/Y outputs | $T_{ILO}$ | 0.19 | 0.40 | 0.42 | 0.47 | ns, max |
| 5-input function: F/G inputs to F5 output | $T_{IF5}$ | 0.36 | 0.76 | 0.8 | 0.9 | ns, max |
| 5-input function: F/G inputs to X output | $T_{IF5X}$ | 0.35 | 0.74 | 0.8 | 0.9 | ns, max |
| 6-input function: F/G inputs to Y output via F6 MUX | $T_{IF6Y}$ | 0.35 | 0.74 | 0.9 | 1.0 | ns, max |
| 6-input function: F5IN input to Y output | $T_{F5INY}$ | 0.04 | 0.11 | 0.20 | 0.22 | ns, max |
| Incremental delay routing through transparent latch to XQ/YQ outputs | $T_{IFNCTL}$ | 0.27 | 0.63 | 0.7 | 0.8 | ns, max |
| BY input to YB output | $T_{BYYB}$ | 0.19 | 0.38 | 0.46 | 0.51 | ns, max |
| **Sequential Delays** | | | | | | |
| FF Clock CLK to XQ/YQ outputs | $T_{CKO}$ | 0.34 | 0.78 | 0.9 | 1.0 | ns, max |
| Latch Clock CLK to XQ/YQ outputs | $T_{CKLO}$ | 0.40 | 0.77 | 0.9 | 1.0 | ns, max |
| **Setup and Hold Times before/after Clock CLK** | | | | | | |
| 4-input function: F/G Inputs | $T_{ICK}$ / $T_{CKI}$ | 0.39 / 0 | 0.9 / 0 | 1.0 / 0 | 1.1 / 0 | ns, min |
| 5-input function: F/G inputs | $T_{IF5CK}$ / $T_{CKIF5}$ | 0.55 / 0 | 1.3 / 0 | 1.4 / 0 | 1.5 / 0 | ns, min |
| 6-input function: F5IN input | $T_{F5INCK}$ / $T_{CKF5IN}$ | 0.27 / 0 | 0.6 / 0 | 0.8 / 0 | 0.8 / 0 | ns, min |
| 6-input function: F/G inputs via F6 MUX | $T_{IF6CK}$ / $T_{CKIF6}$ | 0.58 / 0 | 1.3 / 0 | 1.5 / 0 | 1.6 / 0 | ns, min |
| BX/BY inputs | $T_{DICK}$ / $T_{CKDI}$ | 0.25 / 0 | 0.6 / 0 | 0.7 / 0 | 0.8 / 0 | ns, min |
| CE input | $T_{CECK}$ / $T_{CKCE}$ | 0.28 / 0 | 0.55 / 0 | 0.7 / 0 | 0.7 / 0 | ns, min |
| SR/BY inputs (synchronous) | $T_{RCK}$ / $T_{CKR}$ | 0.24 / 0 | 0.46 / 0 | 0.52 / 0 | 0.6 / 0 | ns, min |
| **Clock CLK** | | | | | | |
| Minimum Pulse Width, High | $T_{CH}$ | 0.56 | 1.2 | 1.3 | 1.4 | ns, min |
| Minimum Pulse Width, Low | $T_{CL}$ | 0.56 | 1.2 | 1.3 | 1.4 | ns, min |
| **Set/Reset** | | | | | | |
| Minimum Pulse Width, SR/BY inputs | $T_{RPW}$ | 0.94 | 1.9 | 2.1 | 2.4 | ns, min |
| Delay from SR/BY inputs to XQ/YQ outputs (asynchronous) | $T_{RQ}$ | 0.39 | 0.8 | 0.9 | 1.0 | ns, max |
| Toggle Frequency (MHz) (for export control) | $F_{TOG}$ | - | 416 | 400 | 357 | MHz |

**Notes:**

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

*Table 13:* **BG432 Differential Pin Pair Summary XCV300E, XCV400E, XC600E**

| Pair | Bank | P Pin | N Pin | AO | Other Functions |
|---|---|---|---|---|---|
| 48 | 2 | N1 | P4 | √ | D3 |
| 49 | 2 | P3 | P2 | 4 | - |
| 50 | 2 | R3 | R4 | 1 | VREF |
| 51 | 2 | R1 | T3 | √ | - |
| 52 | 3 | U4 | U2 | 1 | VREF |
| 53 | 3 | U1 | V3 | 4 | - |
| 54 | 3 | V4 | V2 | √ | VREF |
| 55 | 3 | W3 | W4 | 1 | - |
| 56 | 3 | Y1 | Y3 | 1 | - |
| 57 | 3 | Y4 | Y2 | 4 | - |
| 58 | 3 | AA3 | AB1 | √ | D5 |
| 59 | 3 | AB3 | AB4 | √ | VREF |
| 60 | 3 | AD1 | AC3 | 1 | VREF |
| 61 | 3 | AC4 | AD2 | 4 | - |
| 62 | 3 | AD3 | AD4 | √ | VREF |
| 63 | 3 | AF2 | AE3 | 1 | - |
| 64 | 3 | AE4 | AG1 | 5 | - |
| 65 | 3 | AG2 | AF3 | 1 | VREF |
| 66 | 3 | AF4 | AH1 | 4 | - |
| 67 | 3 | AH2 | AG3 | 3 | - |
| 68 | 3 | AG4 | AJ2 | √ | INIT |
| 69 | 4 | AJ4 | AK3 | √ | - |
| 70 | 4 | AH5 | AK4 | 1 | - |
| 71 | 4 | AJ5 | AH6 | √ | - |
| 72 | 4 | AL4 | AK5 | √ | VREF |
| 73 | 4 | AJ6 | AH7 | 2 | - |
| 74 | 4 | AL5 | AK6 | √ | - |
| 75 | 4 | AJ7 | AL6 | √ | VREF |
| 76 | 4 | AH9 | AJ8 | 1 | - |
| 77 | 4 | AK8 | AJ9 | 1 | VREF |
| 78 | 4 | AL8 | AK9 | √ | VREF |
| 79 | 4 | AK10 | AL10 | √ | - |
| 80 | 4 | AH12 | AK11 | √ | - |
| 81 | 4 | AJ12 | AK12 | √ | - |
| 82 | 4 | AH13 | AJ13 | √ | - |
| 83 | 4 | AL13 | AK14 | √ | VREF |
| 84 | 4 | AH14 | AJ14 | 1 | - |
| 85 | 4 | AK15 | AJ15 | 1 | VREF |
| 86 | 5 | AH15 | AL17 | NA | IO_LVDS_DLL |
| 87 | 5 | AK17 | AJ17 | 1 | VREF |
| 88 | 5 | AH17 | AK18 | 1 | - |
| 89 | 5 | AL19 | AJ18 | √ | VREF |
| 90 | 5 | AH18 | AL20 | √ | - |
| 91 | 5 | AK20 | AH19 | √ | - |
| 92 | 5 | AJ20 | AK21 | √ | - |
| 93 | 5 | AJ21 | AL22 | √ | - |
| 94 | 5 | AJ22 | AK23 | √ | VREF |
| 95 | 5 | AH22 | AL24 | 1 | VREF |
| 96 | 5 | AK24 | AH23 | 1 | - |
| 97 | 5 | AK25 | AJ25 | √ | VREF |
| 98 | 5 | AL26 | AK26 | √ | - |
| 99 | 5 | AH25 | AL27 | 2 | - |
| 100 | 5 | AJ26 | AK27 | √ | VREF |
| 101 | 5 | AH26 | AL28 | √ | - |
| 102 | 5 | AJ27 | AK28 | 1 | - |
| 103 | 6 | AH30 | AJ30 | √ | - |
| 104 | 6 | AH31 | AG28 | 3 | - |
| 105 | 6 | AG30 | AG29 | 4 | - |
| 106 | 6 | AG31 | AF28 | 1 | VREF |
| 107 | 6 | AF30 | AF29 | 5 | - |
| 108 | 6 | AF31 | AE28 | 1 | - |
| 109 | 6 | AD28 | AE30 | √ | VREF |
| 110 | 6 | AD31 | AD30 | 4 | - |
| 111 | 6 | AC29 | AC28 | 1 | VREF |

*Table 15:* **BG560 Differential Pin Pair Summary XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

| Pair | Bank | P Pin | N Pin | AO | Other Functions |
|---|---|---|---|---|---|
| 171 | 7 | J33 | M29 | √ | - |
| 172 | 7 | K31 | L30 | √ | VREF |
| 173 | 7 | H33 | L29 | 4 | - |
| 174 | 7 | H32 | J31 | 18 | VREF |
| 175 | 7 | H31 | K29 | 14 | - |
| 176 | 7 | G32 | J30 | 20 | VREF |
| 177 | 7 | G31 | J29 | √ | VREF |
| 178 | 7 | E32 | E33 | 15 | - |
| 179 | 7 | F31 | H29 | 14 | - |
| 180 | 7 | E31 | D32 | 15 | VREF |
| 181 | 7 | C33 | G29 | 14 | - |
| 182 | 7 | D31 | F30 | 14 | VREF |

**Notes:**

1. AO in the XCV1600E.
2. AO in the XCV2000E.
3. AO in the XCV1600E, 2000E.
4. AO in the XCV1000E, 1600E.
5. AO in the XCV1000E, 2000E.
6. AO in the XCV1000E.
7. AO in the XCV1000E, 1600E, 2000E.
8. AO in the XCV600E, 1600E.
9. AO in the XCV400E, 600E, 1600E.
10. AO in the XCV400E, 600E, 1000E, 2000E.
11. AO in the XCV400E, 600E, 1000E.
12. AO in the XCV400E, 1000E, 2000E.
13. AO in the XCV400E, 600E, 1000E, 1600E.
14. AO in the XCV400E, 1000E, 1600E.
15. AO in the XCV600E, 1000E, 2000E.
16. AO in the XCV600E, 2000E.
17. AO in the XCV400E, 600E, 1600E, 2000E.
18. AO in the XCV600E, 1000E, 1600E, 2000E.
19. AO in the XCV400E, 600E, 2000E.
20. AO in the XCV400E, 1000E.

## FG256 Fine-Pitch Ball Grid Array Packages

XCV50E, XCV100E, XCV200E, and XCV300E devices in FG256 fine-pitch Ball Grid Array packages have footprint compatibility. Pins labeled I0_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as $V_{REF}$, it can be used as general I/O. Immediately following Table 16, see Table 17 for Differential Pair information.

*Table 16:* **FG256 Package — XCV50E, XCV100E, XCV200E, XCV300E**

| Bank | Pin Description | Pin # |
|---|---|---|
| 0 | GCK3 | B8 |
| 0 | IO | B3 |
| 0 | IO | E7 |
| 0 | IO | D8 |
| 0 | IO_L0N_Y | C5 |
| 0 | IO_VREF_L0P_Y | A3[2] |
| 0 | IO_L1N_YY | D5 |
| 0 | IO_L1P_YY | E6 |
| 0 | IO_VREF_L2N_YY | B4 |
| 0 | IO_L2P_YY | A4 |
| 0 | IO_L3N_Y | D6 |
| 0 | IO_L3P_Y | B5 |
| 0 | IO_VREF_L4N_YY | C6[1] |
| 0 | IO_L4P_YY | A5 |
| 0 | IO_L5N_YY | B6 |
| 0 | IO_L5P_YY | C7 |
| 0 | IO_L6N_Y | D7 |
| 0 | IO_L6P_Y | C8 |
| 0 | IO_VREF_L7N_Y | B7 |
| 0 | IO_L7P_Y | A6 |
| 0 | IO_LVDS_DLL_L8N | A7 |
| | | |
| 1 | GCK2 | C9 |
| 1 | IO | B10 |
| 1 | IO_LVDS_DLL_L8P | A8 |
| 1 | IO_L9N_Y | D9 |
| 1 | IO_L9P_Y | A9 |
| 1 | IO_L10N_Y | E10 |
| 1 | IO_VREF_L10P_Y | B9 |

*Table 18:* **FG456 — XCV200E and XCV300E**

| Bank | Pin Description | Pin # |
|---|---|---|
| NA | GND | M14 |
| NA | GND | M13 |
| NA | GND | M12 |
| NA | GND | M11 |
| NA | GND | M10 |
| NA | GND | M9 |
| NA | GND | L14 |
| NA | GND | L13 |
| NA | GND | L12 |
| NA | GND | L11 |
| NA | GND | L10 |
| NA | GND | L9 |
| NA | GND | K14 |
| NA | GND | K13 |
| NA | GND | K12 |
| NA | GND | K11 |
| NA | GND | K10 |
| NA | GND | K9 |
| NA | GND | J14 |
| NA | GND | J13 |
| NA | GND | J12 |
| NA | GND | J11 |
| NA | GND | J10 |
| NA | GND | J9 |
| NA | GND | C20 |
| NA | GND | C3 |
| NA | GND | B21 |
| NA | GND | B2 |
| NA | GND | A22 |
| NA | GND | A1 |

Note 1: NC in the XCV200E device.

## FG456 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

*Table 19:* **FG456 Differential Pin Pair Summary XCV200E, XCV300E**

| Pair | Bank | P Pin | N Pin | AO | Other Functions |
|---|---|---|---|---|---|
| Global Differential Clock | | | | | |
| 0 | 4 | W12 | U12 | NA | IO_DLL_L75P |
| 1 | 5 | Y11 | AA11 | NA | IO_DLL_L75N |
| 2 | 1 | A11 | D11 | NA | IO_DLL_L13P |
| 3 | 0 | C11 | B11 | NA | IO_DLL_L13N |
| IO LVDS<br>Total Pairs: 119, Asynchronous Output Pairs: 69 | | | | | |
| 0 | 0 | B3 | D5 | NA | - |
| 1 | 0 | E6 | B4 | √ | VREF |
| 2 | 0 | E7 | A4 | NA | - |
| 3 | 0 | D6 | C6 | √ | VREF |
| 4 | 0 | B6 | A5 | 1 | - |
| 5 | 0 | C7 | D7 | 1 | - |
| 6 | 0 | B7 | E8 | √ | VREF |
| 7 | 0 | E9 | A7 | √ | - |
| 8 | 0 | B8 | C8 | 1 | - |
| 9 | 0 | A8 | D9 | 1 | - |
| 10 | 0 | E10 | C9 | NA | - |
| 11 | 0 | C10 | A9 | √ | VREF |
| 12 | 0 | B10 | F11 | 2 | - |
| 13 | 1 | D11 | B11 | NA | IO_LVDS_DLL |
| 14 | 1 | D12 | C12 | 2 | - |
| 15 | 1 | A13 | B12 | 2 | - |
| 16 | 1 | B13 | E12 | √ | VREF |
| 17 | 1 | D13 | C13 | √ | - |

*Table 23:* **FG680 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E, XCV2000E**

*Table 23:* **FG680 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E, XCV2000E**

| Pair | Bank | P Pin | N Pin | AO | Other Functions |
|---|---|---|---|---|---|
| 52 | 1 | B8 | A8 | √ | VREF |
| 53 | 1 | A7 | D9 | √ | - |
| 54 | 1 | B7 | C8 | 3 | - |
| 55 | 1 | A6 | D8 | 3 | - |
| 56 | 1 | B6 | C7 | √ | VREF |
| 57 | 1 | A5 | D7 | √ | - |
| 58 | 1 | B5 | C6 | 5 | VREF |
| 59 | 1 | A4 | D6 | 5 | - |
| 60 | 1 | D5 | B4 | √ | CS |
| 61 | 2 | E3 | C2 | √ | DIN, D0 |
| 62 | 2 | D3 | F3 | 6 | - |
| 63 | 2 | D2 | G4 | 4 | VREF |
| 64 | 2 | G3 | E2 | 4 | - |
| 65 | 2 | H4 | E1 | 6 | VREF |
| 66 | 2 | H3 | F2 | √ | - |
| 67 | 2 | J4 | F1 | 4 | - |
| 68 | 2 | J3 | G2 | 6 | - |
| 69 | 2 | G1 | K4 | √ | VREF |
| 70 | 2 | H2 | K3 | √ | - |
| 71 | 2 | H1 | L4 | 7 | VREF |
| 72 | 2 | J2 | L3 | 4 | - |
| 73 | 2 | J1 | M3 | √ | VREF |
| 74 | 2 | K2 | N4 | √ | - |
| 75 | 2 | K1 | N3 | 4 | - |
| 76 | 2 | L2 | P4 | √ | D1 |
| 77 | 2 | P3 | L1 | √ | D2 |
| 78 | 2 | R4 | M2 | 6 | - |
| 79 | 2 | R3 | M1 | 4 | - |
| 80 | 2 | T4 | N2 | 4 | - |
| 81 | 2 | N1 | T3 | 6 | VREF |
| 82 | 2 | P2 | U5 | √ | - |
| 83 | 2 | P1 | U4 | 4 | - |
| 84 | 2 | R2 | U3 | 6 | - |
| 85 | 2 | V5 | R1 | √ | D3 |
| 86 | 2 | V4 | T2 | √ | - |
| 87 | 2 | V3 | T1 | 7 | - |
| 88 | 2 | W4 | U2 | 4 | - |
| 89 | 2 | W3 | U1 | √ | VREF |
| 90 | 2 | AA3 | V2 | √ | - |
| 91 | 2 | AA4 | V1 | 4 | VREF |
| 92 | 2 | AB2 | W2 | √ | - |
| 93 | 3 | AB4 | W1 | 4 | VREF |
| 94 | 3 | AB5 | Y2 | √ | - |
| 95 | 3 | AC2 | Y1 | √ | VREF |
| 96 | 3 | AC3 | AA1 | 4 | - |
| 97 | 3 | AC4 | AA2 | 7 | - |
| 98 | 3 | AC5 | AB1 | √ | - |
| 99 | 3 | AD3 | AC1 | √ | VREF |
| 100 | 3 | AD1 | AD4 | 6 | - |
| 101 | 3 | AD2 | AE3 | 4 | - |
| 102 | 3 | AE1 | AE4 | √ | - |
| 103 | 3 | AE2 | AF3 | 6 | VREF |
| 104 | 3 | AF4 | AF1 | 4 | - |
| 105 | 3 | AG3 | AF2 | 4 | - |
| 106 | 3 | AG4 | AG1 | 6 | - |
| 107 | 3 | AH3 | AG2 | √ | D5 |
| 108 | 3 | AH1 | AJ2 | √ | VREF |
| 109 | 3 | AH2 | AJ3 | 4 | - |
| 110 | 3 | AJ1 | AJ4 | √ | - |
| 111 | 3 | AK1 | AK3 | √ | VREF |
| 112 | 3 | AK2 | AK4 | 4 | - |
| 113 | 3 | AL1 | AL2 | 7 | VREF |
| 114 | 3 | AM1 | AL3 | √ | - |
| 115 | 3 | AM2 | AL4 | √ | VREF |
| 116 | 3 | AM3 | AN1 | 6 | - |
| 117 | 3 | AM4 | AP1 | 4 | - |
| 118 | 3 | AN2 | AP2 | √ | - |
| 119 | 3 | AN3 | AR1 | 6 | VREF |

*Table 23:* **FG680 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E, XCV2000E**

| Pair | Bank | P Pin | N Pin | AO | Other Functions |
|---|---|---|---|---|---|
| 120 | 3 | AN4 | AT1 | 4 | - |
| 121 | 3 | AR2 | AP4 | 4 | VREF |
| 122 | 3 | AT2 | AR3 | 6 | - |
| 123 | 3 | AR4 | AU2 | √ | INIT |
| 124 | 4 | AU4 | AV5 | √ | - |
| 125 | 4 | AT6 | AV4 | 5 | - |
| 126 | 4 | AU6 | AW4 | 5 | VREF |
| 127 | 4 | AT7 | AW5 | √ | - |
| 128 | 4 | AU7 | AV6 | √ | VREF |
| 129 | 4 | AT8 | AW6 | 3 | - |
| 130 | 4 | AU8 | AV7 | 3 | - |
| 131 | 4 | AT9 | AW7 | √ | - |
| 132 | 4 | AV8 | AU9 | √ | VREF |
| 133 | 4 | AW8 | AT10 | 5 | - |
| 134 | 4 | AV9 | AU10 | 5 | VREF |
| 135 | 4 | AW9 | AT11 | √ | - |
| 136 | 4 | AV10 | AU11 | √ | VREF |
| 137 | 4 | AW10 | AU12 | 2 | - |
| 138 | 4 | AV11 | AT13 | 2 | - |
| 139 | 4 | AW11 | AU13 | √ | VREF |
| 140 | 4 | AT14 | AV12 | √ | - |
| 141 | 4 | AU14 | AW12 | 5 | - |
| 142 | 4 | AT15 | AV13 | 5 | - |
| 143 | 4 | AU15 | AW13 | √ | - |
| 144 | 4 | AV14 | AT16 | √ | VREF |
| 145 | 4 | AW14 | AU16 | 3 | - |
| 146 | 4 | AV15 | AR17 | 3 | - |
| 147 | 4 | AW15 | AT17 | √ | - |
| 148 | 4 | AU17 | AV16 | √ | VREF |
| 149 | 4 | AR18 | AW16 | 5 | - |
| 150 | 4 | AT18 | AV17 | 5 | - |
| 151 | 4 | AU18 | AW17 | √ | - |
| 152 | 4 | AT19 | AV18 | √ | VREF |
| 153 | 4 | AU19 | AW18 | 2 | - |
| 154 | 4 | AU21 | AV19 | 2 | VREF |
| 155 | 5 | AT21 | AT22 | NA | IO_LVDS_DLL |
| 156 | 5 | AV20 | AR22 | 8 | VREF |
| 157 | 5 | AV23 | AW21 | √ | VREF |
| 158 | 5 | AU23 | AV21 | √ | - |
| 159 | 5 | AT23 | AW22 | 5 | - |
| 160 | 5 | AR23 | AV22 | 5 | - |
| 161 | 5 | AV24 | AW23 | √ | VREF |
| 162 | 5 | AW24 | AU24 | √ | - |
| 163 | 5 | AW25 | AT24 | 3 | - |
| 164 | 5 | AV25 | AU25 | 3 | - |
| 165 | 5 | AW26 | AT25 | √ | VREF |
| 166 | 5 | AV26 | AW27 | √ | - |
| 167 | 5 | AU26 | AV27 | 5 | - |
| 168 | 5 | AT26 | AW28 | 5 | - |
| 169 | 5 | AU27 | AV28 | √ | - |
| 170 | 5 | AW29 | AT27 | √ | VREF |
| 171 | 5 | AW30 | AU28 | 2 | - |
| 172 | 5 | AV30 | AV29 | 2 | - |
| 173 | 5 | AW31 | AU29 | √ | VREF |
| 174 | 5 | AV31 | AT29 | √ | - |
| 175 | 5 | AW32 | AU30 | 5 | VREF |
| 176 | 5 | AW33 | AT30 | 5 | - |
| 177 | 5 | AV33 | AU31 | √ | VREF |
| 178 | 5 | AT31 | AW34 | √ | - |
| 179 | 5 | AV32 | AV34 | 3 | - |
| 180 | 5 | AU32 | AW35 | 3 | - |
| 181 | 5 | AT32 | AV35 | √ | VREF |
| 182 | 5 | AU33 | AW36 | √ | - |
| 183 | 5 | AT33 | AV36 | 5 | VREF |
| 184 | 5 | AU34 | AU36 | 5 | - |
| 185 | 6 | AT38 | AR36 | √ | - |
| 186 | 6 | AP36 | AR38 | 6 | - |
| 187 | 6 | AP37 | AT39 | 4 | VREF |

*Table 26:* **FG900 — XCV600E, XCV1000E, XCV1600E**

| Bank | Pin Description | Pin # |
|---|---|---|
| 0 | IO_L6N_Y | A5 |
| 0 | IO_L6P_Y | F8 |
| 0 | IO_L7N_Y | D7 |
| 0 | IO_L7P_Y | N11 |
| 0 | IO_L8N_YY | G9 |
| 0 | IO_L8P_YY | E8 |
| 0 | IO_VREF_L9N_YY | A6 |
| 0 | IO_L9P_YY | J11 |
| 0 | IO_L10N_Y | C7 |
| 0 | IO_L10P_Y | B7 |
| 0 | IO_L11N_Y | C8 |
| 0 | IO_L11P_Y | H10 |
| 0 | IO_L12N_YY | G10 |
| 0 | IO_L12P_YY | F10 |
| 0 | IO_VREF_L13N_YY | A8 |
| 0 | IO_L13P_YY | H11 |
| 0 | IO_L14N | D9[4] |
| 0 | IO_L14P | C9[3] |
| 0 | IO_L15N_YY | B9 |
| 0 | IO_L15P_YY | J12 |
| 0 | IO_L16N | E10[4] |
| 0 | IO_VREF_L16P | A9 |
| 0 | IO_L17N | G11 |
| 0 | IO_L17P | B10 |
| 0 | IO_L18N_YY | H12[4] |
| 0 | IO_L18P_YY | C10[4] |
| 0 | IO_L19N_Y | H13 |
| 0 | IO_L19P_Y | F11 |
| 0 | IO_L20N_Y | E11 |
| 0 | IO_L20P_Y | D11 |
| 0 | IO_L21N_Y | B11[4] |
| 0 | IO_L21P_Y | G12[4] |
| 0 | IO_L22N_YY | F12 |
| 0 | IO_L22P_YY | C11 |
| 0 | IO_VREF_L23N_YY | A10[1] |
| 0 | IO_L23P_YY | D12 |
| 0 | IO_L24N_Y | E12 |
| 0 | IO_L24P_Y | A11 |
| 0 | IO_L25N_Y | G13 |
| 0 | IO_L25P_Y | B12 |
| 0 | IO_L26N_YY | A12 |
| 0 | IO_L26P_YY | K13 |
| 0 | IO_VREF_L27N_YY | F13 |
| 0 | IO_L27P_YY | B13 |
| 0 | IO_L28N_Y | G14 |
| 0 | IO_L28P_Y | E13 |
| 0 | IO_L29N_Y | D14 |
| 0 | IO_L29P_Y | B14 |
| 0 | IO_L30N_YY | A14 |
| 0 | IO_L30P_YY | J14 |
| 0 | IO_VREF_L31N_YY | K14 |
| 0 | IO_L31P_YY | J15 |
| 0 | IO_L32N | B15[4] |
| 0 | IO_L32P | H15[3] |
| 0 | IO_VREF_L33N_YY | F15[2,3] |
| 0 | IO_L33P_YY | D15[4] |
| 0 | IO_LVDS_DLL_L34N | A15 |
| | | |
| 1 | GCK2 | E15 |
| 1 | IO | A25[4] |
| 1 | IO | B17[4] |
| 1 | IO | B18[4] |
| 1 | IO | C23[4] |
| 1 | IO | D16[4] |
| 1 | IO | D17[5] |
| 1 | IO | D23[4] |
| 1 | IO | E19[4] |
| 1 | IO | E24[5] |
| 1 | IO | F22[4] |
| 1 | IO | G17[5] |
| 1 | IO | G20[4] |
| 1 | IO | J16[4] |
| 1 | IO | J17[4] |
| 1 | IO | J19[5] |

*Table 26:* **FG900 — XCV600E, XCV1000E, XCV1600E**

| Bank | Pin Description | Pin # |
|---|---|---|
| 1 | IO | J20[5] |
| 1 | IO | L18[4] |
| 1 | IO_LVDS_DLL_L34P | E16 |
| 1 | IO_L35N_YY | B16 |
| 1 | IO_VREF_L35P_YY | F16[2] |
| 1 | IO_L36N_YY | A16 |
| 1 | IO_L36P_YY | H16 |
| 1 | IO_L37N_YY | C16 |
| 1 | IO_VREF_L37P_YY | K15 |
| 1 | IO_L38N_YY | K16 |
| 1 | IO_L38P_YY | G16 |
| 1 | IO_L39N_Y | A17 |
| 1 | IO_L39P_Y | E17 |
| 1 | IO_L40N_Y | F17 |
| 1 | IO_L40P_Y | C17 |
| 1 | IO_L41N_YY | E18 |
| 1 | IO_VREF_L41P_YY | A18 |
| 1 | IO_L42N_YY | D18 |
| 1 | IO_L42P_YY | A19 |
| 1 | IO_L43N_Y | B19 |
| 1 | IO_L43P_Y | G18 |
| 1 | IO_L44N_Y | D19 |
| 1 | IO_L44P_Y | H18 |
| 1 | IO_L45N_YY | F18 |
| 1 | IO_VREF_L45P_YY | F19[1] |
| 1 | IO_L46N_YY | B20 |
| 1 | IO_L46P_YY | K17 |
| 1 | IO_L47N_Y | D20[4] |
| 1 | IO_L47P_Y | A20[4] |
| 1 | IO_L48N_Y | G19 |
| 1 | IO_L48P_Y | C20 |
| 1 | IO_L49N_Y | K18 |
| 1 | IO_L49P_Y | E20 |
| 1 | IO_L50N_YY | B21[4] |
| 1 | IO_L50P_YY | D21[4] |
| 1 | IO_L51N_YY | F20 |
| 1 | IO_L51P_YY | A21 |
| 1 | IO_L52N_YY | C21 |
| 1 | IO_VREF_L52P_YY | A22 |
| 1 | IO_L53N_YY | H19 |
| 1 | IO_L53P_YY | B22 |
| 1 | IO_L54N_YY | E21 |
| 1 | IO_L54P_YY | D22 |
| 1 | IO_L55N_YY | F21 |
| 1 | IO_VREF_L55P_YY | C22 |
| 1 | IO_L56N_YY | H20 |
| 1 | IO_L56P_YY | E22 |
| 1 | IO_L57N_Y | G21 |
| 1 | IO_L57P_Y | A23 |
| 1 | IO_L58N_Y | A24 |
| 1 | IO_L58P_Y | K19 |
| 1 | IO_L59N_YY | C24 |
| 1 | IO_VREF_L59P_YY | B24 |
| 1 | IO_L60N_YY | H21 |
| 1 | IO_L60P_YY | G22 |
| 1 | IO_L61N_Y | E23 |
| 1 | IO_L61P_Y | C25 |
| 1 | IO_L62N_Y | D24 |
| 1 | IO_L62P_Y | A26 |
| 1 | IO_L63N_YY | B26 |
| 1 | IO_VREF_L63P_YY | K20 |
| 1 | IO_L64N_YY | D25 |
| 1 | IO_L64P_YY | J21 |
| 1 | IO_L65N_Y | C26[4] |
| 1 | IO_L65P_Y | F23[4] |
| 1 | IO_L66N_Y | B27 |
| 1 | IO_VREF_L66P_Y | G23[1] |
| 1 | IO_L67N_Y | A27 |
| 1 | IO_L67P_Y | F24 |
| 1 | IO_L68N_YY | B28[3] |
| 1 | IO_L68P_YY | A28[4] |
| 1 | IO_WRITE_L69N_YY | K21 |
| 1 | IO_CS_L69P_YY | C27 |

*Table 26:* **FG900 — XCV600E, XCV1000E, XCV1600E**

| Bank | Pin Description | Pin # |
|---|---|---|
| 2 | IO_L99P_YY | N26 |
| 2 | IO_L99N_YY | P28 |
| 2 | IO_L100P | P29 |
| 2 | IO_L100N | N24 |
| 2 | IO_L101P_YY | P22 |
| 2 | IO_L101N_YY | R26 |
| 2 | IO_VREF_L102P_YY | P25 |
| 2 | IO_L102N_YY | R29 |
| 2 | IO_L103P_YY | R21[4] |
| 2 | IO_L103N_YY | R28[3] |
| 2 | IO_VREF_L104P_YY | R25[2] |
| 2 | IO_L104N_YY | T30 |
| 2 | IO_L105P_YY | P24[4] |
| 2 | IO_L105N_YY | R27[3] |
| 2 | IO_L106P | R24 |
| | | |
| 3 | IO | T22[4] |
| 3 | IO | T24[4] |
| 3 | IO | T26[4] |
| 3 | IO | T29[4] |
| 3 | IO | U26[5] |
| 3 | IO | V23[4] |
| 3 | IO | V25[4] |
| 3 | IO | V30[5] |
| 3 | IO | Y21[4] |
| 3 | IO | AA26[4] |
| 3 | IO | AA23[4] |
| 3 | IO | AB27[4] |
| 3 | IO | AB29[4] |
| 3 | IO | AC28[5] |
| 3 | IO | AD26[4] |
| 3 | IO | AD29[5] |
| 3 | IO | AE27[5] |
| 3 | IO_L106N | U29 |
| 3 | IO_L107P_YY | R22 |
| 3 | IO_VREF_L107N_YY | T27[2] |
| 3 | IO_L108P_YY | R23 |
| 3 | IO_L108N_YY | T28 |
| 3 | IO_L109P_YY | T21 |
| 3 | IO_VREF_L109N_YY | T25 |
| 3 | IO_L110P_YY | U28 |
| 3 | IO_L110N_YY | U30 |
| 3 | IO_L111P | T23 |
| 3 | IO_L111N | U27 |
| 3 | IO_L112P_YY | U25 |
| 3 | IO_L112N_YY | V27 |
| 3 | IO_D4_L113P_YY | U24 |
| 3 | IO_VREF_L113N_YY | V29 |
| 3 | IO_L114P | W30 |
| 3 | IO_L114N | U22 |
| 3 | IO_L115P_YY | U21 |
| 3 | IO_L115N_YY | W29 |
| 3 | IO_L116P_YY | V26 |
| 3 | IO_L116N_YY | W27 |
| 3 | IO_L117P | W26 |
| 3 | IO_VREF_L117N | Y29[1] |
| 3 | IO_L118P_YY | W25 |
| 3 | IO_L118N_YY | Y30 |
| 3 | IO_L119P_Y | V24[4] |
| 3 | IO_L119N_Y | Y28[4] |
| 3 | IO_L120P_YY | AA30 |
| 3 | IO_L120N_YY | W24 |
| 3 | IO_L121P | AA29 |
| 3 | IO_L121N | V20 |
| 3 | IO_L122P | Y27[4] |
| 3 | IO_L122N | W23[4] |
| 3 | IO_L123P_YY | Y26 |
| 3 | IO_D5_L123N_YY | AB30 |
| 3 | IO_D6_L124P_YY | V21 |
| 3 | IO_VREF_L124N_YY | AA28 |
| 3 | IO_L125P_YY | Y25 |
| 3 | IO_L125N_YY | AA27 |
| 3 | IO_L126P_YY | W22 |
| 3 | IO_L126N_YY | Y23 |

*Table 26:* **FG900 — XCV600E, XCV1000E, XCV1600E**

| Bank | Pin Description | Pin # |
|---|---|---|
| 5 | IO_L182N | AF13 |
| 5 | IO_L183P | AH14 |
| 5 | IO_L183N | AJ14 |
| 5 | IO_L184P_YY | AE14 |
| 5 | IO_VREF_L184N_YY | AG13 |
| 5 | IO_L185P_YY | AK13 |
| 5 | IO_L185N_YY | AD13 |
| 5 | IO_L186P | AE13 |
| 5 | IO_L186N | AF12 |
| 5 | IO_L187P | AC13 |
| 5 | IO_L187N | AA13 |
| 5 | IO_L188P_YY | AA12 |
| 5 | IO_VREF_L188N_YY | AJ12[1] |
| 5 | IO_L189P_YY | AB12 |
| 5 | IO_L189N_YY | AE11 |
| 5 | IO_L190P | AK12[4] |
| 5 | IO_L190N | Y13[4] |
| 5 | IO_L191P | AG11 |
| 5 | IO_L191N | AF11 |
| 5 | IO_L192P | AH11 |
| 5 | IO_L192N | AJ11 |
| 5 | IO_L193P_YY | AE12[4] |
| 5 | IO_L193N_YY | AG10[4] |
| 5 | IO_L194P_YY | AD12 |
| 5 | IO_L194N_YY | AK11 |
| 5 | IO_L195P_YY | AJ10 |
| 5 | IO_VREF_L195N_YY | AC12 |
| 5 | IO_L196P_YY | AK10 |
| 5 | IO_L196N_YY | AD11 |
| 5 | IO_L197P_YY | AJ9 |
| 5 | IO_L197N_YY | AE9 |
| 5 | IO_L198P_YY | AH10 |
| 5 | IO_VREF_L198N_YY | AF9 |
| 5 | IO_L199P_YY | AH9 |
| 5 | IO_L199N_YY | AK9 |
| 5 | IO_L200P | AF8 |
| 5 | IO_L200N | AB11 |
| 5 | IO_L201P | AC11 |
| 5 | IO_L201N | AG8 |
| 5 | IO_L202P_YY | AK8 |
| 5 | IO_VREF_L202N_YY | AF7 |
| 5 | IO_L203P_YY | AG7 |
| 5 | IO_L203N_YY | AK7 |
| 5 | IO_L204P | AJ7 |
| 5 | IO_L204N | AD10 |
| 5 | IO_L205P | AH6 |
| 5 | IO_L205N | AC10 |
| 5 | IO_L206P_YY | AD9 |
| 5 | IO_VREF_L206N_YY | AG6 |
| 5 | IO_L207P_YY | AB10 |
| 5 | IO_L207N_YY | AJ5 |
| 5 | IO_L208P | AD8[4] |
| 5 | IO_L208N | AK5[4] |
| 5 | IO_L209P | AC9 |
| 5 | IO_VREF_L209N | AJ4[1] |
| 5 | IO_L210P | AG5 |
| 5 | IO_L210N | AK4 |
| 5 | IO_L211P_YY | AH5[3] |
| 5 | IO_L211N_YY | AG3[4] |
| | | |
| 6 | IO | T2[4] |
| 6 | IO | T10[4] |
| 6 | IO | U1 |
| 6 | IO | U4[5] |
| 6 | IO | U6[4] |
| 6 | IO | U7[4] |
| 6 | IO | V1[4] |
| 6 | IO | V5[5] |
| 6 | IO | V8 |
| 6 | IO | Y10[4] |
| 6 | IO | AA4[4] |
| 6 | IO | AB5[5] |
| 6 | IO | AB7[4] |
| 6 | IO | AC3[5] |

*Table 26:* **FG900 — XCV600E, XCV1000E, XCV1600E**

| Bank | Pin Description | Pin # |
|---|---|---|
| | | |
| 7 | IO | E3 |
| 7 | IO | F1[4] |
| 7 | IO | G1[5] |
| 7 | IO | G4[5] |
| 7 | IO | H3[5] |
| 7 | IO | J1[4] |
| 7 | IO | J3[4] |
| 7 | IO | J4[4] |
| 7 | IO | J6[4] |
| 7 | IO | L10[4] |
| 7 | IO | N2[4] |
| 7 | IO | N8[4] |
| 7 | IO | N10[4] |
| 7 | IO | P3[5] |
| 7 | IO | P9[4] |
| 7 | IO | R1[5] |
| 7 | IO | T3[4] |
| 7 | IO_L247P | R10 |
| 7 | IO_L248N_YY | R5[3] |
| 7 | IO_L248P_YY | R6[4] |
| 7 | IO_L249N_YY | R8 |
| 7 | IO_VREF_L249P_YY | R4[2] |
| 7 | IO_L250N_YY | R7 |
| 7 | IO_L250P_YY | R3 |
| 7 | IO_L251N_YY | P10 |
| 7 | IO_VREF_L251P_YY | P6 |
| 7 | IO_L252N_YY | P5 |
| 7 | IO_L252P_YY | P2 |
| 7 | IO_L253N | P7 |
| 7 | IO_L253P | P4 |
| 7 | IO_L254N_YY | N4 |
| 7 | IO_L254P_YY | R2 |
| 7 | IO_L255N_YY | N7 |
| 7 | IO_VREF_L255P_YY | P1 |
| 7 | IO_L256N | M6 |

*Table 26:* **FG900 — XCV600E, XCV1000E, XCV1600E**

| Bank | Pin Description | Pin # |
|---|---|---|
| 7 | IO_L256P | N6 |
| 7 | IO_L257N_YY | N5 |
| 7 | IO_L257P_YY | N1 |
| 7 | IO_L258N_YY | M4 |
| 7 | IO_L258P_YY | M5 |
| 7 | IO_L259N | M2 |
| 7 | IO_VREF_L259P | M1[1] |
| 7 | IO_L260N_YY | L4 |
| 7 | IO_L260P_YY | L2 |
| 7 | IO_L261N_Y | M7[4] |
| 7 | IO_L261P_Y | L5[4] |
| 7 | IO_L262N_YY | L1 |
| 7 | IO_L262P_YY | M8 |
| 7 | IO_L263N | K2 |
| 7 | IO_L263P | M9 |
| 7 | IO_L264N | L3[4] |
| 7 | IO_L264P | M10[4] |
| 7 | IO_L265N_YY | K5 |
| 7 | IO_L265P_YY | K1 |
| 7 | IO_L266N_YY | L6 |
| 7 | IO_VREF_L266P_YY | K3 |
| 7 | IO_L267N_YY | L7 |
| 7 | IO_L267P_YY | K4 |
| 7 | IO_L268N_YY | L8 |
| 7 | IO_L268P_YY | J5 |
| 7 | IO_L269N_YY | K6 |
| 7 | IO_VREF_L269P_YY | H4 |
| 7 | IO_L270N_YY | H1 |
| 7 | IO_L270P_YY | K7 |
| 7 | IO_L271N | J7 |
| 7 | IO_L271P | J2 |
| 7 | IO_L272N_YY | H5 |
| 7 | IO_L272P_YY | G2 |
| 7 | IO_L273N_YY | L9 |
| 7 | IO_VREF_L273P_YY | G5 |
| 7 | IO_L274N | F3 |
| 7 | IO_L274P | K8 |

*Table 28:* **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

| Bank | Pin Description | Pin # |
|---|---|---|
| NA | VCCINT | N22 |
| NA | VCCINT | P13 |
| NA | VCCINT | P22 |
| NA | VCCINT | R13 |
| NA | VCCINT | R22 |
| NA | VCCINT | T13 |
| NA | VCCINT | T22 |
| NA | VCCINT | U10 |
| NA | VCCINT | U25 |
| NA | VCCINT | V10 |
| NA | VCCINT | V25 |
| NA | VCCINT | W13 |
| NA | VCCINT | W22 |
| NA | VCCINT | Y13 |
| NA | VCCINT | Y22 |
| NA | VCCINT | AA13 |
| NA | VCCINT | AA22 |
| NA | VCCINT | AB13 |
| NA | VCCINT | AB14 |
| NA | VCCINT | AB15 |
| NA | VCCINT | AB16 |
| NA | VCCINT | AB19 |
| NA | VCCINT | AB20 |
| NA | VCCINT | AB21 |
| NA | VCCINT | AB22 |
| NA | VCCINT | AC12 |
| NA | VCCINT | AC23 |
| NA | VCCINT | AD24 |
| NA | VCCINT | AD11 |
| NA | VCCINT | AE10 |
| NA | VCCINT | AE17 |
| NA | VCCINT | AE18 |
| NA | VCCINT | AE25 |
| NA | VCCO_0 | M17 |
| NA | VCCO_0 | L17 |
| NA | VCCO_0 | L16 |
| NA | VCCO_0 | E10 |
| NA | VCCO_0 | C14 |
| NA | VCCO_0 | A6 |
| NA | VCCO_0 | M13 |
| NA | VCCO_0 | M14 |
| NA | VCCO_0 | M15 |
| NA | VCCO_0 | M16 |
| NA | VCCO_0 | L12 |
| NA | VCCO_0 | L13 |
| NA | VCCO_0 | L14 |
| NA | VCCO_0 | L15 |
| NA | VCCO_1 | M18 |
| NA | VCCO_1 | L18 |
| NA | VCCO_1 | L23 |
| NA | VCCO_1 | E25 |
| NA | VCCO_1 | C21 |
| NA | VCCO_1 | A29 |
| NA | VCCO_1 | M19 |
| NA | VCCO_1 | M20 |
| NA | VCCO_1 | M21 |
| NA | VCCO_1 | M22 |
| NA | VCCO_1 | L19 |
| NA | VCCO_1 | L20 |
| NA | VCCO_1 | L21 |
| NA | VCCO_1 | L22 |
| NA | VCCO_2 | U24 |
| NA | VCCO_2 | U23 |
| NA | VCCO_2 | N24 |
| NA | VCCO_2 | M24 |
| NA | VCCO_2 | K30 |
| NA | VCCO_2 | F34 |