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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	1536
Number of Logic Elements/Cells	6912
Total RAM Bits	131072
Number of I/O	260
Number of Gates	411955
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	352-LBGA Exposed Pad, Metal
Supplier Device Package	352-MBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv300e-8bg352c

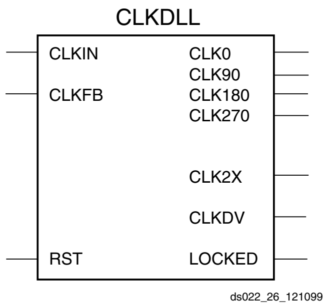

Figure 22: **Standard DLL Symbol CLKDLL**

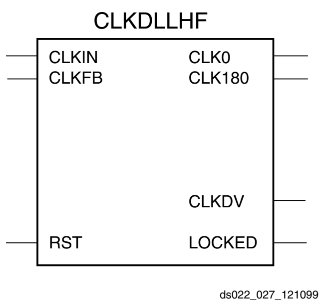

Figure 23: **High Frequency DLL Symbol CLKDLLHF**

BUFGDLL Pin Descriptions

Use the BUFGDLL macro as the simplest way to provide zero propagation delay for a high-fanout on-chip clock from an external input. This macro uses the IBUFG, CLKDLL and BUFG primitives to implement the most basic DLL application as shown in Figure 24.

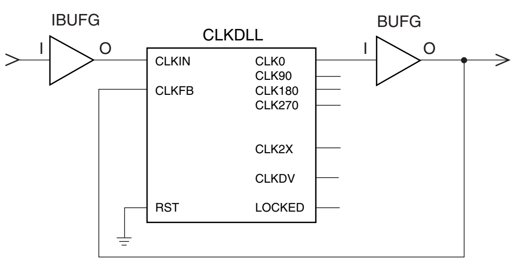

Figure 24: **BUFGDLL Schematic**

This symbol does not provide access to the advanced clock domain controls or to the clock multiplication or clock division features of the DLL. This symbol also does not provide access to the RST, or LOCKED pins of the DLL. For access to these features, a designer must use the library DLL primitives described in the following sections.

Source Clock Input — I

The I pin provides the user source clock, the clock signal on which the DLL operates, to the BUFGDLL. For the BUFGDLL macro the source clock frequency must fall in the low frequency range as specified in the data sheet. The BUFGDLL requires an external signal source clock. Therefore, only an external input port can source the signal that drives the BUFGDLL I pin.

Clock Output — O

The clock output pin O represents a delay-compensated version of the source clock (I) signal. This signal, sourced by a global clock buffer BUFG symbol, takes advantage of the dedicated global clock routing resources of the device.

The output clock has a 50-50 duty cycle unless you deactivate the duty cycle correction property.

CLKDLL Primitive Pin Descriptions

The library CLKDLL primitives provide access to the complete set of DLL features needed when implementing more complex applications with the DLL.

Source Clock Input — CLKIN

The CLKIN pin provides the user source clock (the clock signal on which the DLL operates) to the DLL. The CLKIN frequency must fall in the ranges specified in the data sheet. A global clock buffer (BUFG) driven from another CLKDLL, one of the global clock input buffers (IBUFG), or an IO_LVDS_DLL pin on the same edge of the device (top or bottom) must source this clock signal. There are four IO_LVDS_DLL input pins that can be used as inputs to the DLLs. This makes a total of eight usable input pins for DLLs in the Virtex-E family.

Feedback Clock Input — CLKFB

The DLL requires a reference or feedback signal to provide the delay-compensated output. Connect only the CLK0 or CLK2X DLL outputs to the feedback clock input (CLKFB) pin to provide the necessary feedback to the DLL. The feedback clock input can also be provided through one of the following pins.

IBUFG - Global Clock Input Pad

IO_LVDS_DLL - the pin adjacent to IBUFG

If an IBUFG sources the CLKFB pin, the following special rules apply.

1. An external input port must source the signal that drives the IBUFG I pin.
2. The CLK2X output must feedback to the device if both the CLK0 and CLK2X outputs are driving off chip devices.
3. That signal must directly drive only OBUFs and nothing else.

These rules enable the software determine which DLL clock output sources the CLKFB pin.

Reset Input — RST

When the reset pin RST activates the LOCKED signal deactivates within four source clock cycles. The RST pin, active High, must either connect to a dynamic signal or tied to

Optional N-side

Some designers might prefer to also instantiate the N-side buffer for the global clock buffer. This allows the top-level net list to include net connections for both PCB layout and system-level integration. In this case, only the output P-side IBUFG connection has a net connected to it. Since the N-side IBUFG does not have a connection in the EDIF net list, it is trimmed from the design in MAP.

VHDL Instantiation

```
gclk0_p : IBUFG_LVDS port map
(I=>clk_p_external, O=>clk_internal);

gclk0_n : IBUFG_LVDS port map
(I=>clk_n_external, O=>clk_internal);
```

Verilog Instantiation

```
IBUFG_LVDS gclk0_p (.I(clk_p_external),
.O(clk_internal));

IBUFG_LVDS gclk0_n (.I(clk_n_external),
.O(clk_internal));
```

Location Constraints

All LVDS buffers must be explicitly placed on a device. For the global clock input buffers this can be done with the following constraint in the .ucf or .ncf file.

```
NET clk_p_external LOC = GCLKPAD3;

NET clk_n_external LOC = C17;
```

GCLKPAD3 can also be replaced with the package pin name, such as D17 for the BG432 package.

Creating LVDS Input Buffers

An LVDS input buffer can be placed in a wide number of IOB locations. The exact location is dependent on the package that is used. The Virtex-E package information lists the possible locations as IO_L#P for the P-side and IO_L#N for the N-side where # is the pair number.

HDL Instantiation

Only one input buffer is required to be instantiated in the design and placed on the correct IO_L#P location. The N-side of the buffer is reserved and no other IOB is allowed to be placed on this location. In the physical device, a configuration option is enabled that routes the pad wire from the IO_L#N IOB to the differential input buffer located in the IO_L#P IOB. The output of this buffer then drives the output of the IO_L#P cell or the input register in the IO_L#P IOB. In EPIC it appears that the second buffer is unused. Any attempt to use this location for another purpose leads to a DRC error in the software.

VHDL Instantiation

```
data0_p : IBUF_LVDS port map (I=>data(0),
O=>data_int(0));
```

Verilog Instantiation

```
IBUF_LVDS data0_p (.I(data[0]),
.O(data_int[0]));
```

Location Constraints

All LVDS buffers must be explicitly placed on a device. For the input buffers this can be done with the following constraint in the .ucf or .ncf file.

```
NET data<0> LOC = D28; # IO_L0P
```

Optional N-side

Some designers might prefer to also instantiate the N-side buffer for the input buffer. This allows the top-level net list to include net connections for both PCB layout and system-level integration. In this case, only the output P-side IBUF connection has a net connected to it. Since the N-side IBUF does not have a connection in the EDIF net list, it is trimmed from the design in MAP.

VHDL Instantiation

```
data0_p : IBUF_LVDS port map
(I=>data_p(0), O=>data_int(0));

data0_n : IBUF_LVDS port map
(I=>data_n(0), O=>open);
```

Verilog Instantiation

```
IBUF_LVDS data0_p (.I(data_p[0]),
.O(data_int[0]));

IBUF_LVDS data0_n (.I(data_n[0]), .O());
```

Location Constraints

All LVDS buffers must be explicitly placed on a device. For the global clock input buffers this can be done with the following constraint in the .ucf or .ncf file.

```
NET data_p<0> LOC = D28; # IO_L0P

NET data_n<0> LOC = B29; # IO_L0N
```

Adding an Input Register

All LVDS buffers can have an input register in the IOB. The input register is in the P-side IOB only. All the normal IOB register options are available (FD, FDE, FDC, FDCE, FDP, FDPE, FDR, FDRE, FDS, FDSE, LD, LDE, LDC, LDCE, LDP, LDPE). The register elements can be inferred or explicitly instantiated in the HDL code.

The register elements can be packed in the IOB using the IOB property to TRUE on the register or by using the "map -pr [i|o|b]" where "i" is inputs only, "o" is outputs only and "b" is both inputs and outputs.

To improve design coding times VHDL and Verilog synthesis macro libraries available to explicitly create these structures. The input library macros are listed in Table 42. The I and IB inputs to the macros are the external net connections.

Date	Version	Revision
9/20/00	1.7	• Min values added to **Virtex-E Electrical Characteristics** tables. • XCV2600E and XCV3200E numbers added to **Virtex-E Electrical Characteristics** tables (Module 3). • Corrected user I/O count for XCV100E device in Table 1 (Module 1). • Changed several pins to "No Connect in the XCV100E" and removed duplicate V_{CCINT} pins in Table ~ (Module 4). • Changed pin J10 to "No connect in XCV600E" in Table 74 (Module 4). • Changed pin J30 to "VREF option only in the XCV600E" in Table 74 (Module 4). • Corrected pair 18 in Table 75 (Module 4) to be "AO in the XCV1000E, XCV1600E".
11/20/00	1.8	• Upgraded speed grade -8 numbers in **Virtex-E Electrical Characteristics** tables to Preliminary. • Updated minimums in Table 13 and added notes to Table 14. • Added to note 2 to **Absolute Maximum Ratings**. • Changed speed grade -8 numbers for $T_{SHCKO32}$, T_{REG}, T_{BCCS}, and T_{ICKOF} • Changed all minimum hold times to –0.4 under **Global Clock Set-Up and Hold for LVTTL Standard, with DLL**. • Revised maximum T_{DLLPW} in -6 speed grade for **DLL Timing Parameters**. • Changed GCLK0 to BA22 for FG860 package in Table 46.
2/12/01	1.9	• Revised footnote for Table 14. • Added numbers to **Virtex-E Electrical Characteristics** tables for XCV1000E and XCV2000E devices. • Updated Table 27 and Table 78 to include values for XCV400E and XCV600E devices. • Revised Table 62 to include pinout information for the XCV400E and XCV600E devices in the BG560 package. • Updated footnotes 1 and 2 for Table 76 to include XCV2600E and XCV3200E devices.
4/02/01	2.0	• Updated numerous values in **Virtex-E Switching Characteristics** tables. • Converted data sheet to modularized format. See the **Virtex-E Data Sheet** section.
4/19/01	2.1	• Modified Figure 30 "DLL Generation of 4x Clock in Virtex-E Devices."
07/23/01	2.2	• Made minor edits to text under **Configuration**. • Added CLB column locations for XCV2600E anbd XCV3200E devices in Table 3.
11/09/01	2.3	• Added warning under **Configuration** section that attempting to load an incorrect bitstream causes configuration to fail and can damage the device.
07/17/02	2.4	• Data sheet designation upgraded from Preliminary to Production.
09/10/02	2.5	• Added clarification to the **Input/Output Block**, **Configuration**, **Boundary Scan Mode**, and **Block SelectRAM** sections. Revised Figure 18, Table 11, and Table 36.
11/19/02	2.6	• Added clarification in the **Boundary Scan** section. • Removed last sentence regarding deactivation of duty-cycle correction in **Duty Cycle Correction Property** section.
06/15/04	2.6.1	• Updated clickable web addresses.
01/12/06	2.7	• Updated the **Slave-Serial Mode** and the **Master-Serial Mode** sections.
01/16/06	2.8	• Made minor updates to Table 8.

Virtex-E Electrical Characteristics

Definition of Terms

Electrical and switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance: These speed files are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These speed files are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production: These speed files are released once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. Contact the factory for design considerations requiring more detailed information.

Table 1 correlates the current status of each Virtex-E device with a corresponding speed file designation.

Table 1: **Virtex-E Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XCV50E			–8, –7, –6
XCV100E			–8, –7, –6
XCV200E			–8, –7, –6
XCV300E			–8, –7, –6
XCV400E			–8, –7, –6
XCV600E			–8, –7, –6
XCV1000E			–8, –7, –6
XCV1600E			–8, –7, –6
XCV2000E			–8, –7, –6
XCV2600E			–8, –7, –6
XCV3200E			–8, –7, –6

All specifications are subject to change without notice.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
CTT	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.4	V_{REF} + 0.4	8	–8
AGP	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2

Notes:
1. V_{OL} and V_{OH} for lower drive currents are sample tested.
2. Tested according to the relevant specifications.
3. DC input and output levels for HSTL18 (HSTL I/O standard with V_{CCO} of 1.8 V) are provided in an HSTL white paper on **www.xilinx.com**.

LVDS DC Specifications

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}		2.375	2.5	2.625	V
Output High Voltage for Q and $\overline{Q}$	V_{OH}	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.25	1.425	1.6	V
Output Low Voltage for Q and $\overline{Q}$	V_{OL}	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.9	1.075	1.25	V
Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{ODIFF}	R_T = 100 Ω across Q and $\overline{Q}$ signals	250	350	450	mV
Output Common-Mode Voltage	V_{OCM}	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.25	1.375	V
Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{IDIFF}	Common-mode input voltage = 1.25 V	100	350	NA	mV
Input Common-Mode Voltage	V_{ICM}	Differential input voltage = ±350 mV	0.2	1.25	2.2	V

Note: Refer to the Design Consideration section for termination schematics.

LVPECL DC Specifications

These values are valid at the output of the source termination pack shown under **LVPECL**, with a 100 Ω differential load only. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. The following table summarizes the DC output specifications of LVPECL.

DC Parameter	Min	Max	Min	Max	Min	Max	Units
V_{CCO}	**3.0**		**3.3**		**3.6**		**V**
V_{OH}	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{IH}	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential Input Voltage	0.3	-	0.3	-	0.3	-	V

Virtex-E Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted

Global Clock Set-Up and Hold for LVTTL Standard, *with* DLL

Description[1]	Symbol	Device	Speed Grade[2, 3]				Units
			Min	-8	-7	-6	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in **IOB Input Switching Characteristics Standard Adjustments**, page 8.							
No Delay	T_{PSDLL}/T_{PHDLL}	XCV50E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns
Global Clock and IFF, with DLL		XCV100E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns
		XCV200E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns
		XCV300E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns
		XCV400E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns
		XCV600E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns
		XCV1000E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns
		XCV1600E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns
		XCV2000E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns
		XCV2600E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns
		XCV3200E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. DLL output jitter is already included in the timing calculation.

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P66	IO_VREF_L46P	5
P65	IO_L46N	5
P64	IO_L47P_YY	5
P63	IO_L47N_YY	5
P62	M2	NA
P61	VCCO	5
P60	M0	NA
P59	GND	NA
P58	M1	NA
P57	IO_L48N_YY	6
P56	IO_L48P_YY	6
P55	VCCO	6
P54	IO_VREF	6
P53	IO_L49N_Y	6
P52	IO_L49P_Y	6
P51	GND	NA
P50	IO_VREF_L50N_Y	6
P49	IO_L50P_Y	6
P48	IO_VREF	6
P47	IO_VREF_L51N_Y	6
P46	IO_L51P_Y	6
P45	GND	NA
P44	VCCO	6
P43	VCCINT	NA
P42	IO_L52N_YY	6
P41	IO_L52P_YY	6
P40[1]	IO_VREF	6
P39	IO_L53N_Y	6
P38	IO_L53P_Y	6
P37	GND	NA
P36	IO_VREF_L54N_Y	6
P35	IO_L54P_Y	6
P34	IO_L55N_Y	6
P33	IO_VREF_L55P_Y	6
P32	VCCINT	NA
P31	IO	6

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P30	VCCO	6
P29	GND	NA
P28	IO_L56N_YY	7
P27	IO_L56P_YY	7
P26	IO_VREF	7
P25	VCCO	7
P24	IO_L57N_Y	7
P23	IO_VREF_L57P_Y	7
P22	GND	NA
P21	IO_L58N_Y	7
P20	IO_L58P_Y	7
P19[1]	IO_VREF	7
P18	IO_L59N_YY	7
P17	IO_L59P_YY	7
P16	VCCINT	NA
P15	VCCO	7
P14	GND	NA
P13	IO_L60N_Y	7
P12	IO_VREF_L60P_Y	7
P11	IO_VREF	7
P10	IO_L61N_Y	7
P9	IO_VREF_L61P_Y	7
P8	GND	NA
P7	IO_L62N_Y	7
P6	IO_L62P_Y	7
P5	IO_VREF_L63N_Y	7
P4	IO_L63P_Y	7
P3	IO	7
P2	TMS	NA
P1	GND	NA

Notes:
1. V_{REF} or I/O option only in the XCV1000E; otherwise, I/O option only.

BG352 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A check (√) in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock

Table 11: **BG352 Differential Pin Pair Summary XCV100E, XCV200E, XCV300E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	AE13	AC13	NA	IO LVDS 55
1	5	AF14	AD14	NA	IO LVDS 55
2	1	B14	A13	NA	IO LVDS 9
3	0	D14	A15	NA	IO LVDS 9
IO LVDS Total Outputs: 87, Asynchronous Output Pairs: 43					
0	0	B23	D21	√	VREF_0
1	0	D20	A23	√	-
2	0	B22	C21	√	VREF_0
3	0	A21	B20	2	-
4	0	B19	C19	√	VREF_0
5	0	C18	D17	√	-
6	0	A18	C17	2	-
7	0	C16	B17	√	-
8	0	D15	A16	√	VREF_0
9	1	A13	A15	√	GCLK LVDS 3/2
10	1	A12	C13	2	-
11	1	C12	B12	√	VREF_1
12	1	B11	A11	√	-
13	1	D11	C11	2	-
14	1	C10	B9	√	-
15	1	C9	B8	√	VREF_1
16	1	A7	D9	1	-
17	1	B6	A6	√	VREF_1
18	1	A4	C7	√	-

Table 11: **BG352 Differential Pin Pair Summary XCV100E, XCV200E, XCV300E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
19	1	D6	C6	√	VREF_1
20	1	C4	D5	√	CS
21	2	E4	D3	√	DIN_D0
22	2	D2	C1	√	VREF_2
23	2	G4	F3	√	-
24	2	E2	F2	√	VREF_2
25	2	F1	J4	2	-
26	2	H2	G1	√	D1
27	2	J3	J2	√	D2
28	2	J1	L4	1	-
29	2	L3	L2	√	-
30	2	M4	M3	√	D3
31	2	M2	M1	2	-
32	2	N4	N2	√	-
33	3	R1	R2	2	-
34	3	R3	R4	√	VREF_3
35	3	T2	U2	√	-
36	3	T4	V1	1	-
37	3	U3	U4	√	D5
38	3	V3	V4	√	VREF_3
39	3	Y1	Y2	1	-
40	3	AA2	Y3	√	VREF_3
41	3	AC1	AB2	√	-
42	3	AA4	AC2	√	VREF_3
43	3	AC3	AD2	√	INIT
44	4	AC5	AD4	√	-
45	4	AE4	AF3	√	VREF_4
46	4	AC7	AD6	√	-
47	4	AE5	AE6	√	VREF_4
48	4	AF6	AC9	2	-
49	4	AE8	AF7	√	VREF_4
50	4	AD9	AE9	√	-
51	4	AF9	AC11	2	-
52	4	AD11	AE11	√	-
53	4	AC12	AD12	√	VREF_4
54	4	AE12	AF12	2	-

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
NA	GND	A29	
NA	GND	A32	
NA	GND	A33	
NA	GND	B1	
NA	GND	B6	
NA	GND	B9	
NA	GND	B15	
NA	GND	B23	
NA	GND	B27	
NA	GND	B31	
NA	GND	C2	
NA	GND	E1	
NA	GND	F32	
NA	GND	G2	
NA	GND	G33	
NA	GND	J32	
NA	GND	K1	
NA	GND	L2	
NA	GND	M33	
NA	GND	P1	
NA	GND	P33	
NA	GND	R32	
NA	GND	T1	
NA	GND	V33	
NA	GND	W2	
NA	GND	Y1	
NA	GND	Y33	
NA	GND	AB1	
NA	GND	AC32	
NA	GND	AD33	
NA	GND	AE2	
NA	GND	AG1	
NA	GND	AG32	
NA	GND	AH2	
NA	GND	AJ33	

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
NA	GND	AL32	
NA	GND	AM3	
NA	GND	AM7	
NA	GND	AM11	
NA	GND	AM19	
NA	GND	AM25	
NA	GND	AM28	
NA	GND	AM33	
NA	GND	AN1	
NA	GND	AN2	
NA	GND	AN5	
NA	GND	AN10	
NA	GND	AN14	
NA	GND	AN16	
NA	GND	AN20	
NA	GND	AN22	
NA	GND	AN27	
NA	GND	AN33	

Notes:

1. V_{REF} or I/O option only in the XCV2000E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV1600E & 2000E; otherwise, I/O option only.
3. V_{REF} or I/O option only in the XCV1000E, 1600E, & 2000E; otherwise, I/O option only.
4. V_{REF} or I/O option only in the XCV600E, 1000E, 1600E, & 2000E; otherwise, I/O option only.

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
3	IO	Y26
3	IO	AB25
3	IO	AC25[1]
3	IO	AC26
3	IO_L69P_YY	P21
3	IO_L69N_YY	P23
3	IO_L70P_Y	P22
3	IO_VREF_L70N_Y	R25
3	IO_L71P_Y	P19
3	IO_L71N_Y	P20
3	IO_L72P_YY	R21
3	IO_L72N_YY	R22
3	IO_D4_L73P_YY	R24
3	IO_VREF_L73N_YY	R23
3	IO_L74P_Y	T24
3	IO_L74N_Y	R20
3	IO_L75P_Y	T22
3	IO_L75N_Y	U24
3	IO_L76P_Y	T23
3	IO_L76N_Y	U25
3	IO_L77P_Y	T21
3	IO_L77N_Y	U20
3	IO_L78P_YY	U22
3	IO_L78N_YY	V26
3	IO_L79P_YY	T20
3	IO_D5_L79N_YY	U23
3	IO_D6_L80P_YY	V24
3	IO_VREF_L80N_YY	U21
3	IO_L81P_YY	V23
3	IO_L81N_YY	W24
3	IO_L82P_Y	V22
3	IO_VREF_L82N_Y	W26[2]
3	IO_L83P_Y	Y25
3	IO_L83N_Y	V21
3	IO_L84P_YY	V20
3	IO_L84N_YY	AA26
3	IO_L85P_YY	Y24

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
3	IO_VREF_L85N_YY	W23
3	IO_L86P_Y	AA24
3	IO_L86N_Y	Y23
3	IO_L87P_Y	AB26
3	IO_L87N_Y	W21
3	IO_L88P_Y	Y22
3	IO_VREF_L88N_Y	W22
3	IO_L89P_Y	AA23
3	IO_L89N_Y	AB24
3	IO_L90P_YY	W20
3	IO_L90N_YY	AC24
3	IO_D7_L91P_YY	AB23
3	IO_INIT_L91N_YY	Y21
4	GCK0	AA14
4	IO	AC18
4	IO	AE15[1]
4	IO	AE20
4	IO	AE23
4	IO	AF14[1]
4	IO	AF16[1]
4	IO	AF18[1]
4	IO	AF21
4	IO	AF23[1]
4	IO_L92P_YY	AC22
4	IO_L92N_YY	AD26
4	IO_L93P_Y	AD23
4	IO_L93N_Y	AA20
4	IO_L94P_YY	Y19
4	IO_L94N_YY	AC21
4	IO_VREF_L95P_YY	AD22
4	IO_L95N_YY	AB20
4	IO_L96P	AE22
4	IO_L96N	Y18
4	IO_L97P	AF22
4	IO_L97N	AA19
4	IO_VREF_L98P_YY	AD21

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
4	IO_L98N_YY	AB19
4	IO_L99P_YY	AC20
4	IO_L99N_YY	AA18
4	IO_L100P_Y	AC19
4	IO_L100N_Y	AD20
4	IO_VREF_L101P_Y	AF20[2]
4	IO_L101N_Y	AB18
4	IO_L102P	AD19
4	IO_L102N	Y17
4	IO_L103P	AE19
4	IO_VREF_L103N	AD18
4	IO_L104P_YY	AF19
4	IO_L104N_YY	AA17
4	IO_L105P_Y	AC17
4	IO_L105N_Y	AB17
4	IO_L106P_YY	Y16
4	IO_L106N_YY	AE17
4	IO_L107P_YY	AF17
4	IO_L107N_YY	AA16
4	IO_L108P	AD17
4	IO_L108N	AB16
4	IO_L109P_YY	AC16
4	IO_L109N_YY	AD16
4	IO_VREF_L110P_YY	AC15
4	IO_L110N_YY	Y15
4	IO_L111P_YY	AD15
4	IO_L111N_YY	AA15
4	IO_L112P_Y	W14
4	IO_L112N_Y	AB15
4	IO_VREF_L113P_Y	AF15
4	IO_L113N_Y	Y14
4	IO_L114P	AD14
4	IO_L114N	AB14
4	IO_LVDS_DLL_L115P	AC14
5	GCK1	AB13
5	IO	Y13[1]
5	IO	AD7
5	IO	AD13
5	IO	AE4
5	IO	AE7
5	IO	AE12[1]
5	IO	AF3[1]
5	IO	AF5
5	IO	AF10[1]
5	IO	AF11[1]
5	IO_LVDS_DLL_L115N	AF13
5	IO_L116P_Y	AA13
5	IO_VREF_L116N_Y	AF12
5	IO_L117P_Y	AC13
5	IO_L117N_Y	W13
5	IO_L118P_YY	AA12
5	IO_L118N_YY	AD12
5	IO_L119P_YY	AC12
5	IO_VREF_L119N_YY	AB12
5	IO_L120P_YY	AD11
5	IO_L120N_YY	Y12
5	IO_L121P	AB11
5	IO_L121N	AD10
5	IO_L122P_YY	AC11
5	IO_L122N_YY	AE10
5	IO_L123P_YY	AC10
5	IO_L123N_YY	AA11
5	IO_L124P_Y	Y11
5	IO_L124N_Y	AD9
5	IO_L125P_YY	AB10
5	IO_L125N_YY	AF9
5	IO_L126P_YY	AD8
5	IO_VREF_L126N_YY	AA10
5	IO_L127P_YY	AE8
5	IO_L127N_YY	Y10
5	IO_L128P_Y	AC9
5	IO_VREF_L128N_Y	AF8[2]
5	IO_L129P_Y	AF7

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
1	IO	C5
1	IO_LVDS_DLL_L29P	A19
1	IO_L30N_Y	C21
1	IO_VREF_L30P_Y	B19[2]
1	IO_L31N_Y	C19
1	IO_L31P_Y	A18
1	IO_L32N_YY	D19
1	IO_VREF_L32P_YY	B18
1	IO_L33N_YY	C18
1	IO_L33P_YY	A17
1	IO_L34N_Y	D18
1	IO_L34P_Y	B17
1	IO_L35N_Y	E18
1	IO_L35P_Y	A16
1	IO_L36N_YY	C17
1	IO_VREF_L36P_YY	D17
1	IO_L37N_YY	B16
1	IO_L37P_YY	E17
1	IO_L38N_Y	A15
1	IO_L38P_Y	C16
1	IO_L39N_Y	B15
1	IO_L39P_Y	D16
1	IO_L40N_YY	A14
1	IO_VREF_L40P_YY	B14[1]
1	IO_L41N_YY	C15
1	IO_L41P_YY	A13
1	IO_L42N_Y	D15
1	IO_L42P_Y	B13
1	IO_L43N_Y	C14
1	IO_L43P_Y	A12
1	IO_L44N_YY	D14
1	IO_L44P_YY	C13
1	IO_L45N_YY	B12
1	IO_VREF_L45P_YY	D13
1	IO_L46N_Y	A11
1	IO_L46P_Y	C12

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
1	IO_L47N_Y	B11
1	IO_L47P_Y	C11
1	IO_L48N_YY	A10
1	IO_VREF_L48P_YY	D11
1	IO_L49N_YY	B10
1	IO_L49P_YY	C10
1	IO_L50N_Y	A9
1	IO_VREF_L50P_Y	D10[3]
1	IO_L51N_Y	B9
1	IO_L51P_Y	C9
1	IO_L52N_YY	A8
1	IO_VREF_L52P_YY	B8
1	IO_L53N_YY	D9
1	IO_L53P_YY	A7
1	IO_L54N_Y	C8
1	IO_L54P_Y	B7
1	IO_L55N_Y	D8
1	IO_L55P_Y	A6
1	IO_L56N_YY	C7
1	IO_VREF_L56P_YY	B6
1	IO_L57N_YY	D7
1	IO_L57P_YY	A5
1	IO_L58N_Y	C6
1	IO_VREF_L58P_Y	B5[1]
1	IO_L59N_Y	D6
1	IO_L59P_Y	A4
1	IO_WRITE_L60N_YY	B4
1	IO_CS_L60P_YY	D5
2	IO	D1
2	IO	F4
2	IO_DOUT_BUSY_L61P_YY	E3
2	IO_DIN_D0_L61N_YY	C2
2	IO_L62P_Y	D3
2	IO_L62N_Y	F3
2	IO_VREF_L63P	D2[1]

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
0	VCCO	E34
0	VCCO	E33
0	VCCO	E30
0	VCCO	E29
0	VCCO	E27
0	VCCO	E26
1	VCCO	E10
1	VCCO	E11
1	VCCO	E13
1	VCCO	E14
1	VCCO	E6
1	VCCO	E7
2	VCCO	P5
2	VCCO	N5
2	VCCO	L5
2	VCCO	K5
2	VCCO	G5
2	VCCO	F5
3	VCCO	AP5
3	VCCO	AN5
3	VCCO	AK5
3	VCCO	AJ5
3	VCCO	AG5
3	VCCO	AF5
4	VCCO	AR10
4	VCCO	AR11
4	VCCO	AR13
4	VCCO	AR14
4	VCCO	AR6
4	VCCO	AR7
5	VCCO	AR34
5	VCCO	AR33
5	VCCO	AR30
5	VCCO	AR29
5	VCCO	AR27

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
5	VCCO	AR26
6	VCCO	AP35
6	VCCO	AN35
6	VCCO	AK35
6	VCCO	AJ35
6	VCCO	AG35
6	VCCO	AF35
7	VCCO	P35
7	VCCO	N35
7	VCCO	L35
7	VCCO	K35
7	VCCO	G35
7	VCCO	F35
NA	GND	Y5
NA	GND	Y4
NA	GND	Y37
NA	GND	Y36
NA	GND	Y35
NA	GND	Y3
NA	GND	W5
NA	GND	W35
NA	GND	M5
NA	GND	M4
NA	GND	M36
NA	GND	M35
NA	GND	E5
NA	GND	E35
NA	GND	E28
NA	GND	E21
NA	GND	E20
NA	GND	E19
NA	GND	E12
NA	GND	D4
NA	GND	D36
NA	GND	D28

FG860 Fine-Pitch Ball Grid Array Package

XCV1000E, XCV1600E, and XCV2000E devices in the FG680 fine-pitch Ball Grid Array package have footprint compatibility. Pins labeled I0_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 24, see Table 25 for Differential Pair information.

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
0	GCK3	C22
0	IO	A26
0	IO	B31
0	IO	B34
0	IO	C24
0	IO	C29
0	IO	C34
0	IO	D24
0	IO	D36
0	IO	D40
0	IO	E26
0	IO	E28
0	IO	E35
0	IO_L0N_Y	A38
0	IO_L0P_Y	D38
0	IO_L1N_Y	B37
0	IO_L1P_Y	E37
0	IO_VREF_L2N_Y	A37
0	IO_L2P_Y	C39
0	IO_L3N_Y	B36
0	IO_L3P_Y	C38
0	IO_L4N_YY	A36
0	IO_L4P_YY	B35
0	IO_VREF_L5N_YY	A35
0	IO_L5P_YY	D37
0	IO_L6N_Y	C37
0	IO_L6P_Y	A34
0	IO_L7N_Y	E36
0	IO_L7P_Y	B33
0	IO_L8N_YY	A33
0	IO_L8P_YY	C32
0	IO_VREF_L9N_YY	C36
0	IO_L9P_YY	B32
0	IO_L10N_Y	A32
0	IO_L10P_Y	D35
0	IO_VREF_L11N_Y	C31[2]
0	IO_L11P_Y	C35
0	IO_L12N_YY	E34
0	IO_L12P_YY	A31
0	IO_VREF_L13N_YY	D34
0	IO_L13P_YY	C30
0	IO_L14N_Y	B30
0	IO_L14P_Y	E33
0	IO_L15N_Y	A30
0	IO_L15P_Y	D33
0	IO_VREF_L16N_YY	C33
0	IO_L16P_YY	B29
0	IO_L17N_YY	E32
0	IO_L17P_YY	A29
0	IO_L18N_Y	D32
0	IO_L18P_Y	C28
0	IO_L19N_Y	E31
0	IO_L19P_Y	B28
0	IO_L20N_Y	D31
0	IO_L20P_Y	A28
0	IO_L21N_Y	D30
0	IO_L21P_Y	C27
0	IO_L22N_YY	E29
0	IO_L22P_YY	B27
0	IO_VREF_L23N_YY	D29
0	IO_L23P_YY	A27
0	IO_L24N_Y	C26
0	IO_L24P_Y	D28
0	IO_L25N_Y	B26
0	IO_L25P_Y	F27
0	IO_L26N_YY	E27
0	IO_L26P_YY	C25

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
6	IO	AJ40
6	IO	AL41
6	IO	AN38
6	IO	AN42
6	IO	AP41
6	IO	AR39
6	IO_L211N_YY	AV41
6	IO_L211P_YY	AV42
6	IO_L212N_Y	AW40
6	IO_L212P_Y	AU41
6	IO_L213N_Y	AV39
6	IO_L213P_Y	AU42
6	IO_VREF_L214N_Y	AT41
6	IO_L214P_Y	AU38
6	IO_L215N	AT42
6	IO_L215P	AV40
6	IO_L216N_Y	AR41
6	IO_L216P_Y	AU39
6	IO_VREF_L217N_Y	AR42
6	IO_L217P_Y	AU40
6	IO_L218N_YY	AT38
6	IO_L218P_YY	AP42
6	IO_L219N_Y	AN41
6	IO_L219P_Y	AT39
6	IO_L220N_Y	AT40
6	IO_L220P_Y	AM40
6	IO_VREF_L221N_YY	AR38
6	IO_L221P_YY	AM41
6	IO_L222N_YY	AM42
6	IO_L222P_YY	AR40
6	IO_VREF_L223N_Y	AL40[2]
6	IO_L223P_Y	AP38
6	IO_L224N_Y	AP39
6	IO_L224P_Y	AL42
6	IO_VREF_L225N_YY	AP40
6	IO_L225P_YY	AK40
6	IO_L226N_YY	AK41

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
6	IO_L226P_YY	AN39
6	IO_L227N_Y	AK42
6	IO_L227P_Y	AN40
6	IO_VREF_L228N_YY	AM38
6	IO_L228P_YY	AJ41
6	IO_L229N_YY	AJ42
6	IO_L229P_YY	AM39
6	IO_L230N_Y	AH40
6	IO_L230P_Y	AH41
6	IO_L231N_Y	AL38
6	IO_L231P_Y	AH42
6	IO_L232N_Y	AL39
6	IO_L232P_Y	AG41
6	IO_L233N	AK39
6	IO_L233P	AG40
6	IO_L234N_Y	AJ38
6	IO_L234P_Y	AG42
6	IO_VREF_L235N_Y	AF42
6	IO_L235P_Y	AJ39
6	IO_L236N_YY	AF41
6	IO_L236P_YY	AH38
6	IO_L237N_Y	AE42
6	IO_L237P_Y	AH39
6	IO_L238N_Y	AG38
6	IO_L238P_Y	AE41
6	IO_VREF_L239N_YY	AG39
6	IO_L239P_YY	AD42
6	IO_L240N_YY	AD40
6	IO_L240P_YY	AF39
6	IO_L241N_Y	AD41
6	IO_L241P_Y	AE38
6	IO_L242N_Y	AE39
6	IO_L242P_Y	AC40
6	IO_VREF_L243N_YY	AD38
6	IO_L243P_YY	AC41
6	IO_L244N_YY	AB42
6	IO_L244P_YY	AC38

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
NA	VCCO_1	F15
NA	VCCO_1	F19
NA	VCCO_1	F20
NA	VCCO_1	F7
NA	VCCO_1	F8
NA	VCCO_2	G6
NA	VCCO_2	H6
NA	VCCO_2	L6
NA	VCCO_2	M6
NA	VCCO_2	P6
NA	VCCO_2	R6
NA	VCCO_2	W6
NA	VCCO_2	Y6
NA	VCCO_3	AC6
NA	VCCO_3	AD6
NA	VCCO_3	AH6
NA	VCCO_3	AJ6
NA	VCCO_3	AL6
NA	VCCO_3	AM6
NA	VCCO_3	AR6
NA	VCCO_3	AT6
NA	VCCO_4	AU11
NA	VCCO_4	AU12
NA	VCCO_4	AU14
NA	VCCO_4	AU15
NA	VCCO_4	AU19
NA	VCCO_4	AU20
NA	VCCO_4	AU7
NA	VCCO_4	AU8
NA	VCCO_5	AU23
NA	VCCO_5	AU24
NA	VCCO_5	AU28
NA	VCCO_5	AU29
NA	VCCO_5	AU31
NA	VCCO_5	AU32
NA	VCCO_5	AU35
NA	VCCO_5	AU36
NA	VCCO_6	AC37
NA	VCCO_6	AD37
NA	VCCO_6	AH37
NA	VCCO_6	AJ37
NA	VCCO_6	AL37
NA	VCCO_6	AM37
NA	VCCO_6	AR37
NA	VCCO_6	AT37
NA	VCCO_7	G37
NA	VCCO_7	H37
NA	VCCO_7	L37
NA	VCCO_7	M37
NA	VCCO_7	P37
NA	VCCO_7	R37
NA	VCCO_7	W37
NA	VCCO_7	Y37
NA	GND	N6
NA	GND	N5
NA	GND	N38
NA	GND	N37
NA	GND	F6
NA	GND	F37
NA	GND	F30
NA	GND	F22
NA	GND	F21
NA	GND	F13
NA	GND	E5
NA	GND	E38
NA	GND	E30
NA	GND	E22
NA	GND	E21
NA	GND	E13
NA	GND	D42
NA	GND	D4
NA	GND	D39
NA	GND	D1

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
NA	GND	AG27
NA	GND	D27
NA	GND	AF26
NA	GND	E26
NA	GND	F25
NA	GND	AE25
NA	GND	G24
NA	GND	AJ23
NA	GND	AD24
NA	GND	H23
NA	GND	B23
NA	GND	AC23
NA	GND	AB22
NA	GND	V22
NA	GND	N22
NA	GND	AH18
NA	GND	AB18
NA	GND	J18
NA	GND	C18
NA	GND	U17
NA	GND	T17
NA	GND	R17
NA	GND	P17
NA	GND	U16
NA	GND	T16
NA	GND	R16
NA	GND	P16
NA	GND	U15
NA	GND	T15
NA	GND	R15
NA	GND	P15
NA	GND	U14
NA	GND	T14
NA	GND	R14
NA	GND	P14
NA	GND	AH13
NA	GND	AB13

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
NA	GND	J13
NA	GND	C13
NA	GND	V9
NA	GND	N9
NA	GND	J9
NA	GND	AJ8
NA	GND	AC8
NA	GND	H8
NA	GND	AD7
NA	GND	B8
NA	GND	AE6
NA	GND	G7
NA	GND	F6
NA	GND	AF5
NA	GND	E5
NA	GND	AG4
NA	GND	D4
NA	GND	V3
NA	GND	N3
NA	GND	C3
NA	GND	AK2
NA	GND	AH3
NA	GND	AC2
NA	GND	H2
NA	GND	B2
NA	GND	A2
NA	GND	AK1
NA	GND	AJ2
NA	GND	AJ1
NA	GND	A1
NA	GND	B1

Notes:
1. V_{REF} or I/O option only in the XCV1000E and XCV1600E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV1600E; otherwise, I/O option only.
3. I/O option only in the XCV600E.
4. No Connect in the XCV600E.
5. No Connect in the XCV600E, 1000E.

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
5	IO_L239P_Y	AP9
5	IO_L239N_Y	AK11
5	IO_L240P_YY	AL11
5	IO_VREF_L240N_YY	AL10
5	IO_L241P_YY	AE13
5	IO_L241N_YY	AM9
5	IO_L242P	AF12[5]
5	IO_L242N	AP8[4]
5	IO_L243P_Y	AL9
5	IO_VREF_L243N_Y	AH11[2]
5	IO_L244P_Y	AF11
5	IO_L244N_Y	AN8
5	IO_L245P_Y	AM8[5]
5	IO_L245N_Y	AG11[4]
5	IO_L246P_YY	AL8
5	IO_VREF_L246N_YY	AK9
5	IO_L247P_YY	AH10
5	IO_L247N_YY	AN7
5	IO_L248P	AE12[5]
5	IO_L248N	AJ9[4]
5	IO_L249P_Y	AM7
5	IO_L249N_Y	AL7
5	IO_L250P_Y	AG10
5	IO_L250N_Y	AN6
5	IO_L251P_YY	AK8[5]
5	IO_L251N_YY	AH9[4]
5	IO_L252P_YY	AP5
5	IO_VREF_L252N_YY	AJ8
5	IO_L253P_YY	AE11
5	IO_L253N_YY	AN5
5	IO_L254P_Y	AF10
5	IO_L254N_Y	AM6
5	IO_L255P_Y	AL6
5	IO_VREF_L255N_Y	AG9

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
5	IO_L256P_Y	AH8
5	IO_L256N_Y	AP4
5	IO_L257P_Y	AN4
5	IO_L257N_Y	AJ7
5	IO_L258P_YY	AM5
5	IO_L258N_YY	AK6
6	IO	T1
6	IO	V2
6	IO	V3
6	IO	V5[3]
6	IO	V8[3]
6	IO	AA10[3]
6	IO	AB5[3]
6	IO	AB7[3]
6	IO	AB9[3]
6	IO	AD7[3]
6	IO	AD8[3]
6	IO	AE2
6	IO	AE4
6	IO	AJ4[3]
6	IO	AH5[3]
6	IO_L259N_YY	AH6
6	IO_L259P_YY	AF8
6	IO_L260N_Y	AE9
6	IO_L260P_Y	AK3
6	IO_L261N_Y	AD10
6	IO_L261P_Y	AL2
6	IO_VREF_L262N_Y	AL1
6	IO_L262P_Y	AH4
6	IO_L263N	AG6
6	IO_L263P	AK1
6	IO_L264N_Y	AF7
6	IO_L264P_Y	AK2

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
7	IO_L324P_Y	L4
7	IO_L325N_YY	J1
7	IO_L325P_YY	L5
7	IO_L326N_YY	J2
7	IO_VREF_L326P_YY	K3
7	IO_L327N_Y	L7
7	IO_L327P_Y	J3
7	IO_L328N_Y	M9[5]
7	IO_L328P_Y	H2[4]
7	IO_L329N_Y	J4
7	IO_VREF_L329P_Y	K6[2]
7	IO_L330N_YY	L8
7	IO_L330P_YY	G2
7	IO_L331N_YY	H3[5]
7	IO_L331P_YY	K7[4]
7	IO_L332N_YY	G3
7	IO_VREF_L332P_YY	J5
7	IO_L333N_Y	L9
7	IO_L333P_Y	H5
7	IO_L334N_Y	J6[5]
7	IO_L334P_Y	H4[4]
7	IO_L335N_Y	G4
7	IO_L335P_Y	K8
7	IO_L336N_YY	J7
7	IO_L336P_YY	F2
7	IO_L337N_YY	F3[5]
7	IO_L337P_YY	L10[4]
7	IO_L338N_Y	E1
7	IO_VREF_L338P_Y_Y	H6
7	IO_L339N_Y	G5
7	IO_L339P_Y	E2
7	IO_L340N	K9
7	IO_L340P	D1
7	IO_L341N_Y	E3

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
7	IO_VREF_L341P_Y	J8
7	IO_L342N_Y	E4
7	IO_L342P_Y	D2
7	IO_L343N_Y	F4
7	IO_L343P_Y	D3
2	CCLK	C31
3	DONE	AM31
NA	DXN	AJ5
NA	DXP	AL5
NA	M0	AK4
NA	M1	AG7
NA	M2	AL3
NA	PROGRAM	AG28
NA	TCK	D5
NA	TDI	C30
2	TDO	K26
NA	TMS	C4
NA	VCCINT	K10
NA	VCCINT	K17
NA	VCCINT	K18
NA	VCCINT	K25
NA	VCCINT	L11
NA	VCCINT	L24
NA	VCCINT	M12
NA	VCCINT	M23
NA	VCCINT	N13
NA	VCCINT	N14
NA	VCCINT	N15
NA	VCCINT	N16
NA	VCCINT	N19
NA	VCCINT	N20
NA	VCCINT	N21

FG1156 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. The AO column in Table 29 indicates which devices in this package can use the pin pair as an asynchronous output. The “Other Functions” column indicates alternative function(s) that are not available when the pair is used as a differential pair or differential clock.

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
GCLK LVDS					
3	0	E17	C17	NA	IO_DLL_L 42N
2	1	D17	J18	NA	IO_DLL_L 42P
1	5	AL19	AL17	NA	IO_DLL_L 215N
0	4	AH18	AM18	NA	IO_DLL_L 215P
IO LVDS Total Pairs: 344, Asynchronous Output Pairs: 134					
0	0	H9	F7	3200 1600 1000	-
1	0	J10	C5	3200 2000 1000	-
2	0	D6	E6	3200 2000 1000	VREF
3	0	G8	A4	3200 2600 1000	-
4	0	J11	C6	3200 2600 2000 1600 1000	-
5	0	F8	G9	3200 2600 2000 1600 1000	VREF
6	0	H10	A5	2000 1600	-
7	0	B5	D7	3200 1000	-
8	0	E8	K12	3200 1000	-
9	0	F9	B6	3200 2600	-
10	0	C7	G10	3200 2600 2000 1600 1000	-
11	0	B7	D8	3200 2600 2000 1600 1000	VREF
12	0	C8	H11	3200 1600	-
13	0	B8	E9	3200 2000 1000	-
14	0	G11	K13	3200 2000 1000	VREF
15	0	F10	A8	3200 2600	-
16	0	H12	C9	3200 2600 2000 1600 1000	-
17	0	A9	D10	3200 2600 2000 1600 1000	VREF
18	0	A10	F11	2600 1600 1000	-
19	0	C10	K14	2600 1600 1000	-
20	0	G12	H13	3200 2600 2000 1600 1000	VREF
21	0	B11	A11	3200 2600 2000 1600 1000	-
22	0	D11	E12	3200 1600 1000	-
23	0	C12	G13	3200 2000 1000	-
24	0	A12	K15	3200 2000 1000	-
25	0	H14	B12	3200 2600 1000	-
26	0	F13	D12	3200 2600 2000 1600 1000	-
27	0	B13	A13	3200 2600 2000 1600 1000	VREF
28	0	G14	J15	2000 1600	-
29	0	F14	C13	3200 2600 1000	-
30	0	D13	H15	3200 2600 1000	-
31	0	K16	A14	3200	-