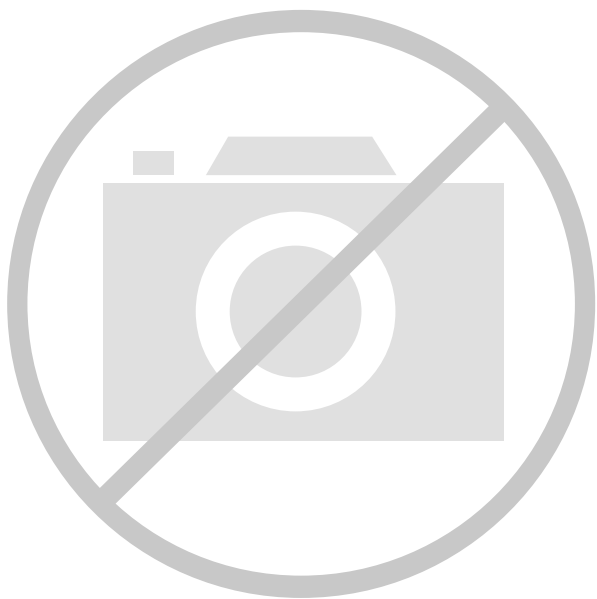




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	1536
Number of Logic Elements/Cells	6912
Total RAM Bits	131072
Number of I/O	316
Number of Gates	411955
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	432-LBGA Exposed Pad, Metal
Supplier Device Package	432-MBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv300e-8bg432c

Table 1: Virtex-E Field-Programmable Gate Array Family Members

Device	System Gates	Logic Gates	CLB Array	Logic Cells	Differential I/O Pairs	User I/O	BlockRAM Bits	Distributed RAM Bits
XCV50E	71,693	20,736	16 x 24	1,728	83	176	65,536	24,576
XCV100E	128,236	32,400	20 x 30	2,700	83	196	81,920	38,400
XCV200E	306,393	63,504	28 x 42	5,292	119	284	114,688	75,264
XCV300E	411,955	82,944	32 x 48	6,912	137	316	131,072	98,304
XCV400E	569,952	129,600	40 x 60	10,800	183	404	163,840	153,600
XCV600E	985,882	186,624	48 x 72	15,552	247	512	294,912	221,184
XCV1000E	1,569,178	331,776	64 x 96	27,648	281	660	393,216	393,216
XCV1600E	2,188,742	419,904	72 x 108	34,992	344	724	589,824	497,664
XCV2000E	2,541,952	518,400	80 x 120	43,200	344	804	655,360	614,400
XCV2600E	3,263,755	685,584	92 x 138	57,132	344	804	753,664	812,544
XCV3200E	4,074,387	876,096	104 x 156	73,008	344	804	851,968	1,038,336

Virtex-E Compared to Virtex Devices

The Virtex-E family offers up to 43,200 logic cells in devices up to 30% faster than the Virtex family.

I/O performance is increased to 622 Mb/s using Source Synchronous data transmission architectures and synchronous system performance up to 240 MHz using singled-ended SelectI/O technology. Additional I/O standards are supported, notably LVPECL, LVDS, and BLVDS, which use two pins per signal. Almost all signal pins can be used for these new standards.

Virtex-E devices have up to 640 Kb of faster (250 MHz) block SelectRAM, but the individual RAMs are the same size and structure as in the Virtex family. They also have eight DLLs instead of the four in Virtex devices. Each individual DLL is slightly improved with easier clock mirroring and 4x frequency multiplication.

V_{CCINT} , the supply voltage for the internal logic and memory, is 1.8 V, instead of 2.5 V for Virtex devices. Advanced processing and 0.18 μ m design rules have resulted in smaller dice, faster speed, and lower power consumption.

I/O pins are 3 V tolerant, and can be 5 V tolerant with an external 100 Ω resistor. PCI 5 V is not supported. With the addition of appropriate external resistors, any pin can tolerate any voltage desired.

Banking rules are different. With Virtex devices, all input buffers are powered by V_{CCINT} . With Virtex-E devices, the LVTTTL, LVCMOS2, and PCI input buffers are powered by the I/O supply voltage V_{CCO} .

The Virtex-E family is not bitstream-compatible with the Virtex family, but Virtex designs can be compiled into equivalent Virtex-E devices.

The same device in the same package for the Virtex-E and Virtex families are pin-compatible with some minor exceptions. See the data sheet pinout section for details.

General Description

The Virtex-E FPGA family delivers high-performance, high-capacity programmable logic solutions. Dramatic increases in silicon efficiency result from optimizing the new architecture for place-and-route efficiency and exploiting an aggressive 6-layer metal 0.18 μ m CMOS process. These advances make Virtex-E FPGAs powerful and flexible alternatives to mask-programmed gate arrays. The Virtex-E family includes the nine members in Table 1.

Building on experience gained from Virtex FPGAs, the Virtex-E family is an evolutionary step forward in programmable logic design. Combining a wide variety of programmable system features, a rich hierarchy of fast, flexible interconnect resources, and advanced process technology, the Virtex-E family delivers a high-speed and high-capacity programmable logic solution that enhances design flexibility while reducing time-to-market.

Virtex-E Architecture

Virtex-E devices feature a flexible, regular architecture that comprises an array of configurable logic blocks (CLBs) surrounded by programmable input/output blocks (IOBs), all interconnected by a rich hierarchy of fast, versatile routing

Architectural Description

Virtex-E Array

The Virtex-E user-programmable gate array, shown in **Figure 1**, comprises two major configurable elements: configurable logic blocks (CLBs) and input/output blocks (IOBs).

- CLBs provide the functional elements for constructing logic
- IOBs provide the interface between the package pins and the CLBs

CLBs interconnect through a general routing matrix (GRM). The GRM comprises an array of routing switches located at the intersections of horizontal and vertical routing channels. Each CLB nests into a VersaBlock™ that also provides local routing resources to connect the CLB to the GRM.

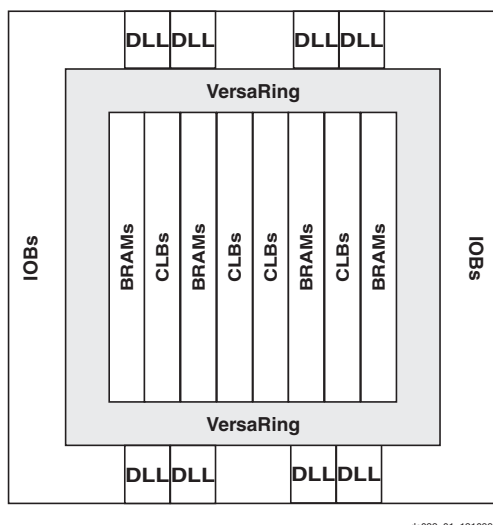


Figure 1: Virtex-E Architecture Overview

The VersaRing™ I/O interface provides additional routing resources around the periphery of the device. This routing improves I/O routability and facilitates pin locking.

The Virtex-E architecture also includes the following circuits that connect to the GRM.

- Dedicated block memories of 4096 bits each
- Clock DLLs for clock-distribution delay compensation and clock domain control
- 3-State buffers (BUFTs) associated with each CLB that drive dedicated segmentable horizontal routing resources

Values stored in static memory cells control the configurable logic elements and interconnect resources. These values load into the memory cells on power-up, and can reload if necessary to change the function of the device.

Input/Output Block

The Virtex-E IOB, **Figure 2**, features SelectI/O+ inputs and outputs that support a wide variety of I/O signalling standards, see **Table 1**.

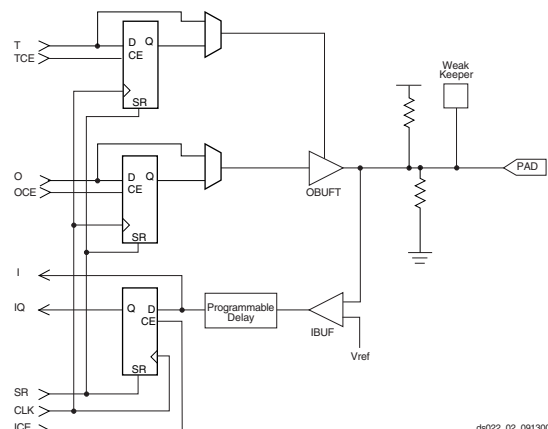


Figure 2: Virtex-E Input/Output Block (IOB)

The three IOB storage elements function either as edge-triggered D-type flip-flops or as level-sensitive latches. Each IOB has a clock signal (CLK) shared by the three flip-flops and independent clock enable signals for each flip-flop.

The DLL also operates as a clock mirror. By driving the output from a DLL off-chip and then back on again, the DLL can be used to deskew a board level clock among multiple devices.

To guarantee that the system clock is operating correctly prior to the FPGA starting up after configuration, the DLL can delay the completion of the configuration process until after it has achieved lock. For more information about DLL functionality, see the Design Consideration section of the data sheet.

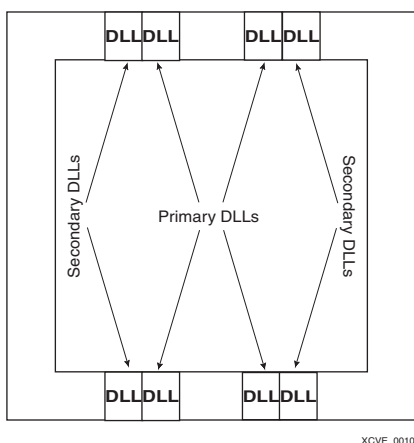


Figure 10: DLL Locations

Boundary Scan

Virtex-E devices support all the mandatory Boundary Scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, INTEST, SAMPLE/PRELOAD, BYPASS, IDCODE, USERCODE, and HIGHZ instructions. The TAP

also supports two internal scan chains and configuration/readback of the device.

The JTAG input pins (TDI, TMS, TCK) do not have a V_{CCO} requirement and operate with either 2.5 V or 3.3 V input signalling levels. The output pin (TDO) is sourced from the V_{CCO} in bank 2, and for proper operation of LVTTTL 3.3 V levels, the bank should be supplied with 3.3 V.

Boundary Scan operation is independent of individual IOB configurations, and unaffected by package type. All IOBs, including un-bonded ones, are treated as independent 3-state bidirectional pins in a single scan chain. Retention of the bidirectional test capability after configuration facilitates the testing of external interconnections, provided the user design or application is turned off.

Table 6 lists the Boundary Scan instructions supported in Virtex-E FPGAs. Internal signals can be captured during EXTEST by connecting them to un-bonded or unused IOBs. They can also be connected to the unused outputs of IOBs defined as unidirectional input pins.

Before the device is configured, all instructions except USER1 and USER2 are available. After configuration, all instructions are available. During configuration, it is recommended that those operations using the Boundary Scan register (SAMPLE/PRELOAD, INTEST, EXTEST) not be performed.

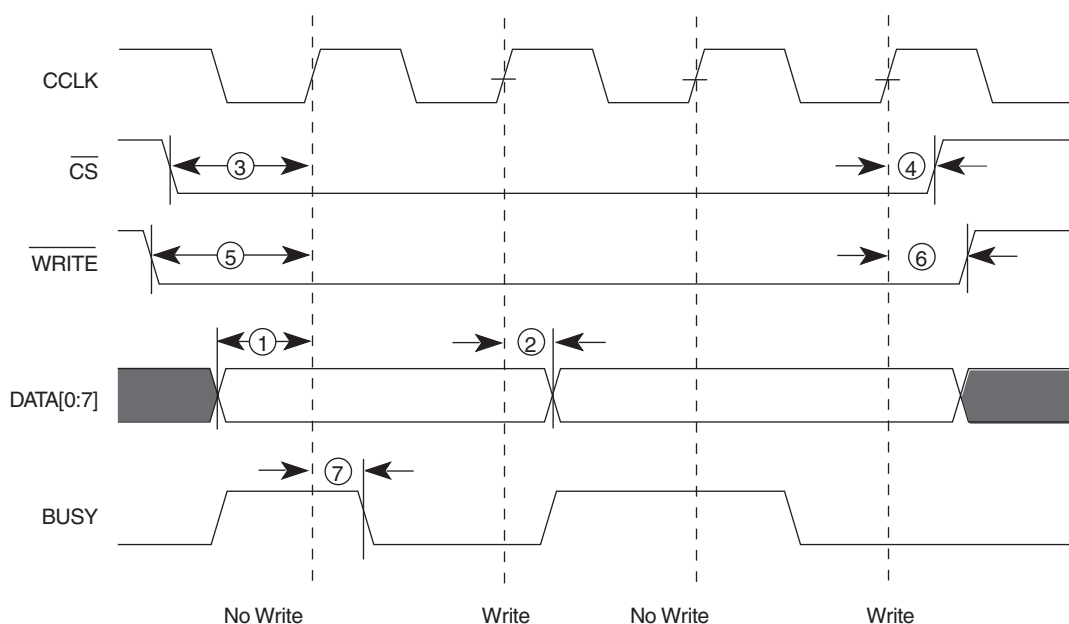
In addition to the test instructions outlined above, the Boundary Scan circuitry can be used to configure the FPGA, and also to read back the configuration data.

Figure 11 is a diagram of the Virtex-E Series Boundary Scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

3. At the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock. If BUSY is High (from a previous write), the data is not accepted. Acceptance instead occurs on the first clock after BUSY goes Low, and the data must be held until this has happened.
4. Repeat steps 2 and 3 until all the data has been sent.
5. De-assert $\overline{\text{CS}}$ and $\overline{\text{WRITE}}$.

Table 11: SelectMAP Write Timing Characteristics

	Description		Symbol		Units
CCLK	D ₀₋₇ Setup/Hold	1/2	T _{SMDC} /T _{SMCCD}	5.0 / 1.7	ns, min
	$\overline{\text{CS}}$ Setup/Hold	3/4	T _{SMCSC} /T _{SMCCCS}	7.0 / 1.7	ns, min
	$\overline{\text{WRITE}}$ Setup/Hold	5/6	T _{SMCCW} /T _{SMWCC}	7.0 / 1.7	ns, min
	BUSY Propagation Delay	7	T _{SMCKBY}	12.0	ns, max
	Maximum Frequency		F _{CC}	66	MHz, max
	Maximum Frequency with no handshake		F _{CCNH}	50	MHz, max



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Figure 17: Write Operations

A flowchart for the write operation is shown in **Figure 18**. Note that if CCLK is slower than f_{CCNH} , the FPGA never asserts BUSY. In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.

Abort

During a given assertion of $\overline{\text{CS}}$, the user cannot switch from a write to a read, or vice-versa. This action causes the cur-

rent packet command to be aborted. The device remains BUSY until the aborted operation has completed. Following an abort, data is assumed to be unaligned to word boundaries, and the FPGA requires a new synchronization word prior to accepting any new packets.

To initiate an abort during a write operation, de-assert $\overline{\text{WRITE}}$. At the rising edge of CCLK, an abort is initiated, as shown in **Figure 19**.

HSTL

A sample circuit illustrating a valid termination technique for HSTL_I appears in [Figure 46](#). A sample circuit illustrating a valid termination technique for HSTL_III appears in [Figure 47](#).

Table 25: HSTL Class I Voltage Specification

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF}	0.68	0.75	0.90
V_{TT}	-	$V_{CCO} \times 0.5$	-
V_{IH}	$V_{REF} + 0.1$	-	-
V_{IL}	-	-	$V_{REF} - 0.1$
V_{OH}	$V_{CCO} - 0.4$	-	-
V_{OL}			0.4
I_{OH} at V_{OH} (mA)	-8	-	-
I_{OL} at V_{OL} (mA)	8	-	-

HSTL Class I

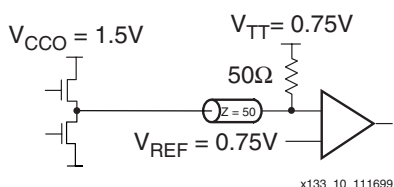


Figure 46: Terminated HSTL Class I

Table 26: HSTL Class III Voltage Specification

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
$V_{REF}^{(1)}$	-	0.90	-
V_{TT}	-	V_{CCO}	-
V_{IH}	$V_{REF} + 0.1$	-	-
V_{IL}	-	-	$V_{REF} - 0.1$
V_{OH}	$V_{CCO} - 0.4$	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	-8	-	-
I_{OL} at V_{OL} (mA)	24	-	-

Note: Per EIA/JESD8-6, "The value of V_{REF} is to be selected by the user to provide optimum noise margin in the use conditions specified by the user."

HSTL Class III

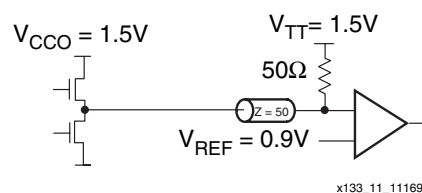


Figure 47: Terminated HSTL Class III

A sample circuit illustrating a valid termination technique for HSTL_IV appears in [Figure 48](#).

Table 27: HSTL Class IV Voltage Specification

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF}	-	0.90	-
V_{TT}	-	V_{CCO}	-
V_{IH}	$V_{REF} + 0.1$	-	-
V_{IL}	-	-	$V_{REF} - 0.1$
V_{OH}	$V_{CCO} - 0.4$	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	-8	-	-
I_{OL} at V_{OL} (mA)	48	-	-

Note: Per EIA/JESD8-6, "The value of V_{REF} is to be selected by the user to provide optimum noise margin in the use conditions specified by the user."

HSTL Class IV

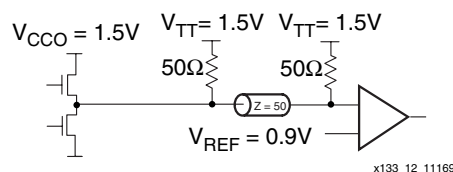


Figure 48: Terminated HSTL Class IV

Table 2: IOB Input Switching Characteristics (Continued)

			Speed Grade ⁽¹⁾				Units
Description ⁽²⁾	Symbol	Device	Min	-8	-7	-6	
Sequential Delays							
Clock CLK							
Minimum Pulse Width, High	T _{CH}	All	0.56	1.2	1.3	1.4	ns, min
Minimum Pulse Width, Low	T _{CL}		0.56	1.2	1.3	1.4	ns, min
Clock CLK to output IQ	T _{IOCKIQ}		0.18	0.4	0.7	0.7	ns, max
Setup and Hold Times with respect to Clock at IOB Input Register							
Pad, no delay	T _{IOPICK} / T _{IOICKP}	All	0.69 / 0	1.3 / 0	1.4 / 0	1.5 / 0	ns, min
Pad, with delay	T _{IOPICKD} / T _{IOICKPD}	XCV50E	1.25 / 0	2.8 / 0	2.9 / 0	2.9 / 0	ns, min
		XCV100E	1.25 / 0	2.8 / 0	2.9 / 0	2.9 / 0	ns, min
		XCV200E	1.33 / 0	3.0 / 0	3.1 / 0	3.1 / 0	ns, min
		XCV300E	1.33 / 0	3.0 / 0	3.1 / 0	3.1 / 0	ns, min
		XCV400E	1.37 / 0	3.1 / 0	3.2 / 0	3.2 / 0	ns, min
		XCV600E	1.49 / 0	3.4 / 0	3.5 / 0	3.5 / 0	ns, min
		XCV1000E	1.49 / 0	3.4 / 0	3.5 / 0	3.5 / 0	ns, min
		XCV1600E	1.53 / 0	3.5 / 0	3.6 / 0	3.6 / 0	ns, min
		XCV2000E	1.53 / 0	3.5 / 0	3.6 / 0	3.6 / 0	ns, min
		XCV2600E	1.53 / 0	3.5 / 0	3.6 / 0	3.6 / 0	ns, min
XCV3200E	1.53 / 0	3.5 / 0	3.6 / 0	3.6 / 0	ns, min		
ICE input	T _{IOICECK} / T _{IOCKICE}	All	0.28 / 0.0	0.55 / 0.01	0.7 / 0.01	0.7 / 0.01	ns, min
SR input (IFF, synchronous)	T _{IOSRCKI}	All	0.38	0.8	0.9	1.0	ns, min
Set/Reset Delays							
SR input to IQ (asynchronous)	T _{IOSRIQ}	All	0.54	1.1	1.2	1.4	ns, max
GSR to output IQ	T _{GSRQ}	All	3.88	7.6	8.5	9.7	ns, max

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. Input timing t_i for LVTTTL is measured at 1.4 V. For other I/O standards, see Table 4.

IOB Output Switching Characteristics, Figure 1

Output delays terminating at a pad are specified for LVTTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 10.

		Speed Grade ⁽¹⁾				Units
Description ⁽²⁾	Symbol	Min	-8	-7	-6	
Propagation Delays						
O input to Pad	T _{IOOP}	1.04	2.5	2.7	2.9	ns, max
O input to Pad via transparent latch	T _{IOOLP}	1.24	2.9	3.1	3.4	ns, max
3-State Delays						
T input to Pad high-impedance (Note 2)	T _{IOTHZ}	0.73	1.5	1.7	1.9	ns, max
T input to valid data on Pad	T _{IOTON}	1.13	2.7	2.9	3.1	ns, max
T input to Pad high-impedance via transparent latch (Note 2)	T _{IOTLPHZ}	0.86	1.8	2.0	2.2	ns, max
T input to valid data on Pad via transparent latch	T _{IOTLPON}	1.26	3.0	3.2	3.4	ns, max
GTS to Pad high impedance (Note 2)	T _{GTS}	1.94	4.1	4.6	4.9	ns, max
Sequential Delays						
Clock CLK						
Minimum Pulse Width, High	T _{CH}	0.56	1.2	1.3	1.4	ns, min
Minimum Pulse Width, Low	T _{CL}	0.56	1.2	1.3	1.4	ns, min
Clock CLK to Pad	T _{IOCKP}	0.97	2.4	2.8	2.9	ns, max
Clock CLK to Pad high-impedance (synchronous) (Note 2)	T _{IOCKHZ}	0.77	1.6	2.0	2.2	ns, max
Clock CLK to valid data on Pad (synchronous)	T _{IOCKON}	1.17	2.8	3.2	3.4	ns, max
Setup and Hold Times before/after Clock CLK						
O input	T _{IOOCK} / T _{IOCKO}	0.43 / 0	0.9 / 0	1.0 / 0	1.1 / 0	ns, min
OCE input	T _{IOOCECK} / T _{IOCKOCE}	0.28 / 0	0.55 / 0.01	0.7 / 0	0.7 / 0	ns, min
SR input (OFF)	T _{IOSRCKO} / T _{IOCKOSR}	0.40 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
3-State Setup Times, T input	T _{IOTCK} / T _{IOCKT}	0.26 / 0	0.51 / 0	0.6 / 0	0.7 / 0	ns, min
3-State Setup Times, TCE input	T _{IOTCECK} / T _{IOCKTCE}	0.30 / 0	0.6 / 0	0.7 / 0	0.8 / 0	ns, min
3-State Setup Times, SR input (TFF)	T _{IOSRCKT} / T _{IOCKTSR}	0.38 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
Set/Reset Delays						
SR input to Pad (asynchronous)	T _{IOSRP}	1.30	3.1	3.3	3.5	ns, max
SR input to Pad high-impedance (asynchronous) (Note 2)	T _{IOSRHZ}	1.08	2.2	2.4	2.7	ns, max
SR input to valid data on Pad (asynchronous)	T _{IOSRON}	1.48	3.4	3.7	3.9	ns, max
GSR to Pad	T _{IOGSRQ}	3.88	7.6	8.5	9.7	ns, max

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. 3-state turn-off delays should not be adjusted.

Table 12: BG432 — XCV300E, XCV400E, XCV600E

Bank	Pin Description	Pin #
2	IO_L41N_Y	H2
2	IO_VREF_L42P_Y	H1 ¹
2	IO_L42N_Y	J4
2	IO_VREF_L43P_YY	J2
2	IO_D1_L43N_YY	K4
2	IO_D2_L44P_YY	K2
2	IO_L44N_YY	K1
2	IO_L45P_Y	L2
2	IO_L45N_Y	M4
2	IO_L46P_Y	M3
2	IO_L46N_Y	M2
2	IO_L47P_Y	N4
2	IO_L47N_Y	N3
2	IO_VREF_L48P_YY	N1
2	IO_D3_L48N_YY	P4
2	IO_L49P_Y	P3
2	IO_L49N_Y	P2
2	IO_VREF_L50P_Y	R3 ²
2	IO_L50N_Y	R4
2	IO_L51P_YY	R1
2	IO_L51N_YY	T3
3	IO	AA2
3	IO	AC2
3	IO	AE2
3	IO	U3
3	IO	W1
3	IO_L52P_Y	U4
3	IO_VREF_L52N_Y	U2 ²
3	IO_L53P_Y	U1
3	IO_L53N_Y	V3
3	IO_D4_L54P_YY	V4
3	IO_VREF_L54N_YY	V2
3	IO_L55P_Y	W3
3	IO_L55N_Y	W4
3	IO_L56P_Y	Y1

Table 12: BG432 — XCV300E, XCV400E, XCV600E

Bank	Pin Description	Pin #
3	IO_L56N_Y	Y3
3	IO_L57P_Y	Y4
3	IO_L57N_Y	Y2
3	IO_L58P_YY	AA3
3	IO_D5_L58N_YY	AB1
3	IO_D6_L59P_YY	AB3
3	IO_VREF_L59N_YY	AB4
3	IO_L60P_Y	AD1
3	IO_VREF_L60N_Y	AC3 ¹
3	IO_L61P_Y	AC4
3	IO_L61N_Y	AD2
3	IO_L62P_YY	AD3
3	IO_VREF_L62N_YY	AD4
3	IO_L63P_Y	AF2
3	IO_L63N_Y	AE3
3	IO_L64P	AE4
3	IO_L64N	AG1
3	IO_L65P_Y	AG2
3	IO_VREF_L65N_Y	AF3
3	IO_L66P_Y	AF4
3	IO_L66N_Y	AH1
3	IO_L67P	AH2
3	IO_L67N	AG3
3	IO_D7_L68P_YY	AG4
3	IO_INIT_L68N_YY	AJ2
3	IO	T2
4	GCK0	AL16
4	IO	AH10
4	IO	AJ11
4	IO	AK7
4	IO	AL12
4	IO	AL15
4	IO_L69P_YY	AJ4
4	IO_L69N_YY	AK3
4	IO_L70P_Y	AH5

BG432 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A ✓ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 13: BG432 Differential Pin Pair Summary
XCV300E, XCV400E, XC600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	AL16	AH15	NA	IO_DLL_L86P
1	5	AK16	AL17	NA	IO_DLL_L86N
2	1	A16	B16	NA	IO_DLL_L16P
3	0	D17	C17	NA	IO_DLL_L16N
IO LVDS					
Total Outputs: 137, Asynchronous Output Pairs: 63					
0	0	D27	B29	1	-
1	0	C27	B28	✓	-
2	0	A28	D26	✓	VREF
3	0	C26	B27	2	-
4	0	A27	D25	✓	-
5	0	C25	D24	✓	VREF
6	0	D23	B25	1	-
7	0	B24	C24	1	VREF
8	0	A24	D22	✓	VREF
9	0	B22	C22	✓	-
10	0	D20	C21	✓	-
11	0	C20	B21	✓	-
12	0	D19	A20	✓	-
13	0	A19	B19	✓	VREF
14	0	D18	B18	1	-
15	0	B17	C18	1	VREF

Table 13: BG432 Differential Pin Pair Summary
XCV300E, XCV400E, XC600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
16	1	B16	C17	NA	IO_LVDS_DLL
17	1	B15	A15	1	VREF
18	1	D15	C15	1	-
19	1	A13	B14	✓	VREF
20	1	D14	B13	✓	-
21	1	B12	C13	✓	-
22	1	C12	D13	✓	-
23	1	C11	D12	✓	-
24	1	C10	B10	✓	VREF
25	1	D10	C9	1	VREF
26	1	B8	A8	1	-
27	1	B7	C8	✓	VREF
28	1	A6	D8	✓	-
29	1	D7	B6	2	-
30	1	C6	A5	✓	VREF
31	1	D6	B5	✓	-
32	1	C5	A4	1	-
33	1	D5	B4	✓	CS, WRITE
34	2	D3	C2	✓	DIN, D0, BUSY
35	2	D2	E4	3	-
36	2	D1	E3	4	-
37	2	E2	F4	1	VREF
38	2	E1	F3	5	-
39	2	F2	G4	1	-
40	2	G3	G2	✓	VREF
41	2	H3	H2	4	-
42	2	H1	J4	1	VREF
43	2	J2	K4	✓	D1
44	2	K2	K1	✓	D2
45	2	L2	M4	4	-
46	2	M3	M2	1	-
47	2	N4	N3	1	-

Table 14: BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin#	See Note
NA	VCCINT	N29	
NA	VCCINT	N33	
NA	VCCINT	U5	
NA	VCCINT	U30	
NA	VCCINT	Y2	
NA	VCCINT	Y31	
NA	VCCINT	AB2	
NA	VCCINT	AB32	
NA	VCCINT	AD2	
NA	VCCINT	AD32	
NA	VCCINT	AG3	
NA	VCCINT	AG31	
NA	VCCINT	AJ13	
NA	VCCINT	AK8	
NA	VCCINT	AK11	
NA	VCCINT	AK17	
NA	VCCINT	AK20	
NA	VCCINT	AL14	
NA	VCCINT	AL22	
NA	VCCINT	AL27	
NA	VCCINT	AN25	
0	VCCO	A22	
0	VCCO	A26	
0	VCCO	A30	
0	VCCO	B19	
0	VCCO	B32	
1	VCCO	A10	
1	VCCO	A16	
1	VCCO	B13	
1	VCCO	C3	
1	VCCO	E5	
2	VCCO	B2	
2	VCCO	D1	
2	VCCO	H1	

Table 14: BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin#	See Note
2	VCCO	M1	
2	VCCO	R2	
3	VCCO	V1	
3	VCCO	AA2	
3	VCCO	AD1	
3	VCCO	AK1	
3	VCCO	AL2	
4	VCCO	AN4	
4	VCCO	AN8	
4	VCCO	AN12	
4	VCCO	AM2	
4	VCCO	AM15	
5	VCCO	AL31	
5	VCCO	AM21	
5	VCCO	AN18	
5	VCCO	AN24	
5	VCCO	AN30	
6	VCCO	W32	
6	VCCO	AB33	
6	VCCO	AF33	
6	VCCO	AK33	
6	VCCO	AM32	
7	VCCO	C32	
7	VCCO	D33	
7	VCCO	K33	
7	VCCO	N32	
7	VCCO	T33	
NA	GND	A1	
NA	GND	A7	
NA	GND	A12	
NA	GND	A14	
NA	GND	A18	
NA	GND	A20	
NA	GND	A24	

Table 16: FG256 Package — XCV50E, XCV100E, XCV200E, XCV300E

Bank	Pin Description	Pin #
7	IO_L74N_Y	G4
7	IO_VREF_L74P_Y	H3
7	IO_L75N_YY	G2
7	IO_L75P_YY	F5
7	IO_L76N	F4
7	IO_L76P	F1
7	IO_L77N_YY	G3
7	IO_L77P_YY	F2
7	IO_L78N_Y	E1
7	IO_VREF_L78P_Y	D1 ¹
7	IO_L79N	E4
7	IO_L79P	E2
7	IO_L80N_Y	F3
7	IO_VREF_L80P_Y	C1
7	IO_L81N_YY	D2
7	IO_L81P_YY	E3
7	IO_VREF_L82N	B1 ²
7	IO_L82P	A2
2	CCLK	D15
3	DONE	R14
NA	DXN	R4
NA	DXP	P4
NA	M0	N3
NA	M1	P2
NA	M2	R3
NA	PROGRAM	P15
NA	TCK	C4
NA	TDI	A15
2	TDO	B14
NA	TMS	D3
NA	VCCINT	C3
NA	VCCINT	C14
NA	VCCINT	D4

Table 16: FG256 Package — XCV50E, XCV100E, XCV200E, XCV300E

Bank	Pin Description	Pin #
NA	VCCINT	D13
NA	VCCINT	E5
NA	VCCINT	E12
NA	VCCINT	M5
NA	VCCINT	M12
NA	VCCINT	N4
NA	VCCINT	N13
NA	VCCINT	P3
NA	VCCINT	P14
0	VCCO	F8
0	VCCO	E8
1	VCCO	F9
1	VCCO	E9
2	VCCO	H12
2	VCCO	H11
3	VCCO	J12
3	VCCO	J11
4	VCCO	M9
4	VCCO	L9
5	VCCO	M8
5	VCCO	L8
6	VCCO	J6
6	VCCO	J5
7	VCCO	H6
7	VCCO	H5
NA	GND	T16
NA	GND	T1
NA	GND	R15
NA	GND	R2
NA	GND	L11
NA	GND	L10
NA	GND	L7
NA	GND	L6

FG680 Fine-Pitch Ball Grid Array Package

XCV600E, XCV1000E, XCV1600E, and XCV2000E devices in the FG680 fine-pitch Ball Grid Array package have footprint compatibility. Pins labeled IO_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF} , it can be used as general I/O. Immediately following Table 22, see Table 23 for Differential Pair information.

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
0	GCK3	A20
0	IO	D35
0	IO	B36
0	IO_L0N_Y	C35
0	IO_L0P_Y	A36
0	IO_VREF_L1N_Y	D34 ¹
0	IO_L1P_Y	B35
0	IO_L2N_YY	C34
0	IO_L2P_YY	A35
0	IO_VREF_L3N_YY	D33
0	IO_L3P_YY	B34
0	IO_L4N	C33
0	IO_L4P	A34
0	IO_L5N_Y	D32
0	IO_L5P_Y	B33
0	IO_L6N_YY	C32
0	IO_L6P_YY	D31
0	IO_VREF_L7N_YY	A33
0	IO_L7P_YY	C31
0	IO_L8N_Y	B32
0	IO_L8P_Y	B31
0	IO_VREF_L9N_Y	A32 ³
0	IO_L9P_Y	D30
0	IO_L10N_YY	A31
0	IO_L10P_YY	C30
0	IO_VREF_L11N_YY	B30
0	IO_L11P_YY	D29
0	IO_L12N_Y	A30
0	IO_L12P_Y	C29

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
0	IO_L13N_Y	A29
0	IO_L13P_Y	B29
0	IO_VREF_L14N_YY	B28
0	IO_L14P_YY	A28
0	IO_L15N_YY	C28
0	IO_L15P_YY	B27
0	IO_L16N_Y	D27
0	IO_L16P_Y	A27
0	IO_L17N_Y	C27
0	IO_L17P_Y	B26
0	IO_L18N_YY	D26
0	IO_L18P_YY	C26
0	IO_VREF_L19N_YY	A26 ¹
0	IO_L19P_YY	D25
0	IO_L20N_Y	B25
0	IO_L20P_Y	C25
0	IO_L21N_Y	A25
0	IO_L21P_Y	D24
0	IO_L22N_YY	A24
0	IO_L22P_YY	B23
0	IO_VREF_L23N_YY	C24
0	IO_L23P_YY	A23
0	IO_L24N_Y	B24
0	IO_L24P_Y	B22
0	IO_L25N_Y	E23
0	IO_L25P_Y	A22
0	IO_L26N_YY	D23
0	IO_L26P_YY	B21
0	IO_VREF_L27N_YY	C23
0	IO_L27P_YY	A21
0	IO_L28N_Y	E22
0	IO_L28P_Y	B20
0	IO_LVDS_DLL_L29N	C22
0	IO_VREF	D22 ²
1	GCK2	D21

FG680 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A ✓ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 23: FG680 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
GCLK LVDS					
3	0	A20	C22	NA	IO_DLL_L29N
2	1	D21	A19	NA	IO_DLL_L29P
1	5	AU22	AT22	NA	IO_DLL_L155N
0	4	AW19	AT21	NA	IO_DLL_L155P
IO LVDS					
Total Pairs: 247, Asynchronous Output Pairs: 111					
0	0	A36	C35	5	-
1	0	B35	D34	5	VREF
2	0	A35	C34	✓	-
3	0	B34	D33	✓	VREF
4	0	A34	C33	3	-
5	0	B33	D32	3	-
6	0	D31	C32	✓	-
7	0	C31	A33	✓	VREF
8	0	B31	B32	5	-
9	0	D30	A32	5	VREF
10	0	C30	A31	✓	-
11	0	D29	B30	✓	VREF
12	0	C29	A30	2	-
13	0	B29	A29	2	-
14	0	A28	B28	✓	VREF
15	0	B27	C28	✓	-
16	0	A27	D27	5	-
17	0	B26	C27	5	-

Table 23: FG680 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
18	0	C26	D26	✓	-
19	0	D25	A26	✓	VREF
20	0	C25	B25	3	-
21	0	D24	A25	3	-
22	0	B23	A24	✓	-
23	0	A23	C24	✓	VREF
24	0	B22	B24	5	-
25	0	A22	E23	5	-
26	0	B21	D23	✓	-
27	0	A21	C23	✓	VREF
28	0	B20	E22	2	-
29	1	A19	C22	NA	IO_LVDS_DLL
30	1	B19	C21	2	VREF
31	1	A18	C19	2	-
32	1	B18	D19	✓	VREF
33	1	A17	C18	✓	-
34	1	B17	D18	5	-
35	1	A16	E18	5	-
36	1	D17	C17	✓	VREF
37	1	E17	B16	✓	-
38	1	C16	A15	3	-
39	1	D16	B15	3	-
40	1	B14	A14	✓	VREF
41	1	A13	C15	✓	-
42	1	B13	D15	5	-
43	1	A12	C14	5	-
44	1	C13	D14	✓	-
45	1	D13	B12	✓	VREF
46	1	C12	A11	2	-
47	1	C11	B11	2	-
48	1	D11	A10	✓	VREF
49	1	C10	B10	✓	-
50	1	D10	A9	5	VREF
51	1	C9	B9	5	-

Table 23: FG680 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
188	6	AP39	AP38	4	-
189	6	AN38	AN36	6	VREF
190	6	AN39	AN37	√	-
191	6	AM38	AM36	4	-
192	6	AL36	AM37	6	-
193	6	AL37	AM39	√	VREF
194	6	AK36	AL38	√	-
195	6	AK37	AL39	7	VREF
196	6	AJ36	AK38	4	-
197	6	AJ37	AK39	√	VREF
198	6	AH37	AJ38	√	-
199	6	AH38	AJ39	4	-
200	6	AG38	AH39	√	VREF
201	6	AG39	AG36	√	-
202	6	AF39	AG37	6	-
203	6	AE38	AF36	4	-
204	6	AF38	AF37	4	-
205	6	AE36	AE39	6	VREF
206	6	AE37	AD38	√	-
207	6	AD36	AD39	4	-
208	6	AC39	AC38	6	-
209	6	AB38	AD37	√	VREF
210	6	AB39	AC35	√	-
211	6	AA38	AC36	7	-
212	6	AA39	AC37	4	-
213	6	Y38	AB35	√	VREF
214	6	Y39	AB36	√	-
215	6	AA36	AB37	4	VREF
216	7	W38	AA37	√	-
217	7	V39	W37	4	VREF
218	7	U39	W36	√	-
219	7	U38	V38	√	VREF
220	7	T39	V37	4	-
221	7	T38	V36	7	-

Table 23: FG680 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
222	7	R39	V35	√	-
223	7	U36	U37	√	VREF
224	7	U35	R38	6	-
225	7	T37	P39	4	-
226	7	T36	P38	√	-
227	7	N38	N39	6	VREF
228	7	M39	R37	4	-
229	7	M38	R36	4	-
230	7	L39	P37	6	-
231	7	N37	P36	√	-
232	7	N36	L38	√	VREF
233	7	M37	K39	4	-
234	7	L37	K38	√	-
235	7	L36	J39	√	VREF
236	7	K37	J38	4	-
237	7	K36	H39	√	VREF
238	7	J37	H38	√	-
239	7	G38	G39	√	VREF
240	7	F39	J36	6	-
241	7	F38	H37	4	-
242	7	E39	H36	√	-
243	7	E38	G37	6	VREF
244	7	D39	G36	4	-
245	7	F36	D38	4	VREF
246	7	E37	D37	6	-

Notes:

1. AO in the XCV1000E, 1600E, 2000E.
2. AO in the XCV600E, 1000E, 1600E.
3. AO in the XCV600E, 1000E.
4. AO in the XCV1000E, 1600E.
5. AO in the XCV1000E, 2000E.
6. AO in the XCV600E, 1000E, 2000E.
7. AO in the XCV1000E.
8. AO in the XCV2000E.

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
2	IO_D1_L87N_YY	P2
2	IO_D2_L88P_YY	P3
2	IO_L88N_YY	L4
2	IO_L89P_Y	P1
2	IO_L89N_Y	R2
2	IO_L90P_Y	M5
2	IO_L90N_Y	R3
2	IO_L91P_Y	M4
2	IO_L91N_Y	R1
2	IO_L92P	N4
2	IO_L92N	T2
2	IO_L93P_Y	P5
2	IO_L93N_Y	T3
2	IO_VREF_L94P_Y	P4
2	IO_L94N_Y	T1
2	IO_L95P_YY	U2
2	IO_L95N_YY	R4
2	IO_L96P_Y	U3
2	IO_L96N_Y	T5
2	IO_L97P_Y	T4
2	IO_L97N_Y	V2
2	IO_VREF_L98P_YY	U5
2	IO_D3_L98N_YY	V3
2	IO_L99P_YY	V1
2	IO_L99N_YY	V5
2	IO_L100P_Y	W2
2	IO_L100N_Y	V4
2	IO_L101P_Y	W5
2	IO_L101N_Y	W1
2	IO_VREF_L102P_YY	Y2
2	IO_L102N_YY	W4
2	IO_L103P_YY	Y1
2	IO_L103N_YY	Y5
2	IO_VREF_L104P_Y	AA1 ¹
2	IO_L104N_Y	Y4
2	IO_L105P_YY	AA4
2	IO_L105N_YY	AA2

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
3	IO	AB4
3	IO	AC2
3	IO	AD1
3	IO	AE3
3	IO	AF4
3	IO	AH5
3	IO	AJ2
3	IO	AL1
3	IO	AM3
3	IO	AP3
3	IO	AR5
3	IO	AU4
3	IO	AB2
3	IO_L106P_Y	AB3
3	IO_VREF_L106N_Y	AC4 ¹
3	IO_L107P_YY	AB1
3	IO_L107N_YY	AC5
3	IO_L108P_YY	AD4
3	IO_VREF_L108N_YY	AC3
3	IO_L109P_Y	AC1
3	IO_L109N_Y	AD5
3	IO_L110P_Y	AE4
3	IO_L110N_Y	AD3
3	IO_L111P_YY	AE5
3	IO_L111N_YY	AD2
3	IO_D4_L112P_YY	AE1
3	IO_VREF_L112N_YY	AF5
3	IO_L113P_Y	AE2
3	IO_L113N_Y	AG4
3	IO_L114P_Y	AG5
3	IO_L114N_Y	AF1
3	IO_L115P_YY	AH4
3	IO_L115N_YY	AF2
3	IO_L116P_Y	AF3
3	IO_VREF_L116N_Y	AJ4
3	IO_L117P_Y	AG1

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
6	IO_VREF_L245N_Y	AB40 ¹
6	IO_L245P_Y	AC39
7	IO	F38
7	IO	H40
7	IO	H41
7	IO	J42
7	IO	K39
7	IO	L42
7	IO	N40
7	IO	T40
7	IO	U40
7	IO	V38
7	IO	W42
7	IO	Y42
7	IO	AA42
7	IO_L246N_YY	AA41
7	IO_L246P_YY	AB39
7	IO_L247N_Y	Y41
7	IO_VREF_L247P_Y	AA39 ¹
7	IO_L248N_YY	Y40
7	IO_L248P_YY	Y39
7	IO_L249N_YY	Y38
7	IO_VREF_L249P_YY	W41
7	IO_L250N_Y	W40
7	IO_L250P_Y	W39
7	IO_L251N_Y	W38
7	IO_L251P_Y	V41
7	IO_L252N_YY	V39
7	IO_L252P_YY	V40
7	IO_L253N_YY	V42
7	IO_VREF_L253P_YY	U39
7	IO_L254N_Y	U41
7	IO_L254P_Y	U38
7	IO_L255N_Y	U42
7	IO_L255P_Y	T39
7	IO_L256N_YY	T41

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
7	IO_L256P_YY	T38
7	IO_L257N_Y	R39
7	IO_VREF_L257P_Y	T42
7	IO_L258N_Y	R42
7	IO_L258P_Y	R38
7	IO_L259N	R40
7	IO_L259P	P39
7	IO_L260N_Y	R41
7	IO_L260P_Y	P38
7	IO_L261N_Y	P42
7	IO_L261P_Y	N39
7	IO_L262N_Y	P40
7	IO_L262P_Y	M39
7	IO_L263N_YY	P41
7	IO_L263P_YY	M38
7	IO_L264N_YY	N42
7	IO_VREF_L264P_YY	L39
7	IO_L265N_Y	L38
7	IO_L265P_Y	N41
7	IO_L266N_YY	K40
7	IO_L266P_YY	M42
7	IO_L267N_YY	M40
7	IO_VREF_L267P_YY	K38
7	IO_L268N_Y	M41
7	IO_L268P_Y	J40
7	IO_L269N_Y	J39
7	IO_VREF_L269P_Y	L40
7	IO_L270N_YY	J38
7	IO_L270P_YY	L41
7	IO_L271N_YY	K42
7	IO_VREF_L271P_YY	H39
7	IO_L272N_Y	K41
7	IO_L272P_Y	H38
7	IO_L273N_Y	J41
7	IO_L273P_Y	G40
7	IO_L274N_YY	H42
7	IO_L274P_YY	G39

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
7	IO_L275N_Y	G38
7	IO_VREF_L275P_Y	G42
7	IO_L276N_Y	G41
7	IO_L276P_Y	F40
7	IO_L277N	F42
7	IO_L277P	F41
7	IO_L278N_Y	F39
7	IO_VREF_L278P_Y	E42
7	IO_L279N_Y	E40
7	IO_L279P_Y	E41
7	IO_L280N_Y	E39
7	IO_L280P_Y	D41
2	CCLK	B4
3	DONE	AW2
NA	DXN	BA38
NA	DXP	AW38
NA	M0	AW41
NA	M1	AV37
NA	M2	BA39
NA	PROGRAM	AV2
NA	TCK	B38
NA	TDI	B5
2	TDO	D5
NA	TMS	B39
NA	VCCINT	F9
NA	VCCINT	F10
NA	VCCINT	F17
NA	VCCINT	F18
NA	VCCINT	F25
NA	VCCINT	F26
NA	VCCINT	F33
NA	VCCINT	F34
NA	VCCINT	J6
NA	VCCINT	J37
NA	VCCINT	K6

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
NA	VCCINT	K37
NA	VCCINT	T6
NA	VCCINT	T37
NA	VCCINT	U6
NA	VCCINT	U37
NA	VCCINT	V6
NA	VCCINT	V37
NA	VCCINT	AE6
NA	VCCINT	AE37
NA	VCCINT	AF6
NA	VCCINT	AF37
NA	VCCINT	AG6
NA	VCCINT	AG37
NA	VCCINT	AN6
NA	VCCINT	AN37
NA	VCCINT	AP6
NA	VCCINT	AP37
NA	VCCINT	AU9
NA	VCCINT	AU10
NA	VCCINT	AU17
NA	VCCINT	AU18
NA	VCCINT	AU25
NA	VCCINT	AU26
NA	VCCINT	AU33
NA	VCCINT	AU34
NA	VCCO_0	F23
NA	VCCO_0	F24
NA	VCCO_0	F28
NA	VCCO_0	F29
NA	VCCO_0	F31
NA	VCCO_0	F32
NA	VCCO_0	F35
NA	VCCO_0	F36
NA	VCCO_1	F11
NA	VCCO_1	F12
NA	VCCO_1	F14

Table 26: FG900 — XCV600E, XCV1000E, XCV1600E

Bank	Pin Description	Pin #
7	IO_L275N_YY	G3
7	IO_L275P_YY	E1
7	IO_L276N_YY	H6
7	IO_L276P_YY	E2
7	IO_L277N	E4
7	IO_VREF_L277P	K9
7	IO_L278N_YY	J8
7	IO_L278P_YY	F4
7	IO_L279N_Y	D1 ³
7	IO_L279P_Y	H7 ⁴
7	IO_L280N_YY	G6
7	IO_VREF_L280P_YY	C2 ¹
7	IO_L281N	D2
7	IO_L281P	F5
7	IO_L282N_YY	D3 ⁴
7	IO_L282P_YY	K10 ³
2	CCLK	F26
3	DONE	AJ28
NA	DXN	AJ3
NA	DXP	AH4
NA	M0	AF4
NA	M1	AC7
NA	M2	AK3
NA	PROGRAM	AG28
NA	TCK	B3
NA	TDI	H22
2	TDO	D26
NA	TMS	C1
NA	VCCINT	L11
NA	VCCINT	L12
NA	VCCINT	L19
NA	VCCINT	L20
NA	VCCINT	M11
NA	VCCINT	M12
NA	VCCINT	M19

Table 26: FG900 — XCV600E, XCV1000E, XCV1600E

Bank	Pin Description	Pin #
NA	VCCINT	M20
NA	VCCINT	N13
NA	VCCINT	N14
NA	VCCINT	N15
NA	VCCINT	N16
NA	VCCINT	N17
NA	VCCINT	N18
NA	VCCINT	P13
NA	VCCINT	P18
NA	VCCINT	R13
NA	VCCINT	R18
NA	VCCINT	T13
NA	VCCINT	T18
NA	VCCINT	U13
NA	VCCINT	U18
NA	VCCINT	V13
NA	VCCINT	V14
NA	VCCINT	V15
NA	VCCINT	V16
NA	VCCINT	V17
NA	VCCINT	V18
NA	VCCINT	W11
NA	VCCINT	W12
NA	VCCINT	W19
NA	VCCINT	W20
NA	VCCINT	Y11
NA	VCCINT	Y12
NA	VCCINT	Y19
NA	VCCINT	Y20
NA	VCCO_0	B6
NA	VCCO_0	M15
NA	VCCO_0	M14
NA	VCCO_0	L15
NA	VCCO_0	L14
NA	VCCO_0	H14
NA	VCCO_0	M13

Table 27: FG900 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
52	1	A22	C21	√	VREF
53	1	B22	H19	4	-
54	1	D22	E21	4	-
55	1	C22	F21	√	VREF
56	1	E22	H20	√	-
57	1	A23	G21	2	-
58	1	K19	A24	2	-
59	1	B24	C24	√	VREF
60	1	G22	H21	√	-
61	1	C25	E23	1	-
62	1	A26	D24	1	-
63	1	K20	B26	√	VREF
64	1	J21	D25	√	-
65	1	F23	C26	2	-
66	1	G23	B27	2	VREF
67	1	F24	A27	2	-
68	1	A28	B28	4	-
69	1	C27	K21	√	CS
70	2	J22	E27	√	DIN, D0
71	2	C29	D28	NA	-
72	2	G25	E25	1	-
73	2	E28	C30	4	VREF
74	2	K22	F27	3	-
75	2	D30	J23	4	-
76	2	L21	F28	1	VREF
77	2	G28	E30	√	-
78	2	G27	E29	4	-
79	2	K23	H26	1	-
80	2	F30	L22	√	VREF
81	2	H27	G29	√	-
82	2	G30	M21	2	-
83	2	J24	J26	4	-
84	2	H30	L23	4	VREF
85	2	K26	J28	4	-

Table 27: FG900 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
86	2	J29	K24	4	-
87	2	K27	J30	4	VREF
88	2	M22	K29	NA	D2
89	2	K28	L25	4	-
90	2	N21	K25	1	-
91	2	L24	L27	4	-
92	2	L29	M23	3	-
93	2	L26	L28	4	-
94	2	L30	M27	1	VREF
95	2	M26	M29	√	-
96	2	N29	M30	4	-
97	2	N25	N27	1	-
98	2	N30	P21	√	D3
99	2	N26	P28	√	-
100	2	P29	N24	2	-
101	2	P22	R26	√	-
102	2	P25	R29	4	VREF
103	2	R21	R28	4	-
104	2	R25	T30	4	VREF
105	2	P24	R27	4	-
106	3	R24	U29	NA	-
107	3	R22	T27	4	VREF
108	3	R23	T28	4	-
109	3	T21	T25	4	VREF
110	3	U28	U30	4	-
111	3	T23	U27	2	-
112	3	U25	V27	√	-
113	3	U24	V29	√	VREF
114	3	W30	U22	1	-
115	3	U21	W29	4	-
116	3	V26	W27	√	-
117	3	W26	Y29	1	VREF
118	3	W25	Y30	4	-
119	3	V24	Y28	3	-

Date	Version	Revision
4/2/01	2.0	- Updated numerous values in Virtex-E Switching Characteristics tables. - Changed pinout table footnotes from "V_{REF} option only" to "V_{REF} or I/O option only" to improve clarity. - Converted file to modularized format. See the Virtex-E Data Sheet section.
7/26/01	2.1	- Changed pinout table footnotes from "V_{REF} or I/O option only" to "V_{REF} or I/O option only; otherwise I/O only" to improve clarity. - Changed designation for pin pair 300 in Table 29 from AO to footnote 9.
10/25/01	2.2	- Changed Table 29 to clarify which devices in the FG1156 package can use each pin pair as an asynchronous output. - Updated references to the XCV3200E device in the FG1156 package.
11/15/01	2.3	Fixed cosmetic error.
07/17/02	2.4	- Added "VREF" to the description for pin B15 in Table 12. - Changed designation for pin pair 129 in Table 15 from AO to "AO in the XCV1000E, 1600E, 2000E". - Data sheet designation upgraded from Preliminary to Production.
03/14/03	2.5	Removed the Virtex-E XCV300E section under Pinout Differences Between Virtex and Virtex-E Families (and revised Table 1), since these differences do not exist.

Virtex-E Data Sheet

The Virtex-E Data Sheet contains the following modules:

- DS022-1, Virtex-E 1.8V FPGAs:
[Introduction and Ordering Information \(Module 1\)](#)
- DS022-2, Virtex-E 1.8V FPGAs:
[Functional Description \(Module 2\)](#)
- DS022-3, Virtex-E 1.8V FPGAs:
[DC and Switching Characteristics \(Module 3\)](#)
- DS022-4, Virtex-E 1.8V FPGAs:
[Pinout Tables \(Module 4\)](#)