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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	2400
Number of Logic Elements/Cells	10800
Total RAM Bits	163840
Number of I/O	158
Number of Gates	569952
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	240-BFQFP
Supplier Device Package	240-PQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv400e-7pq240i

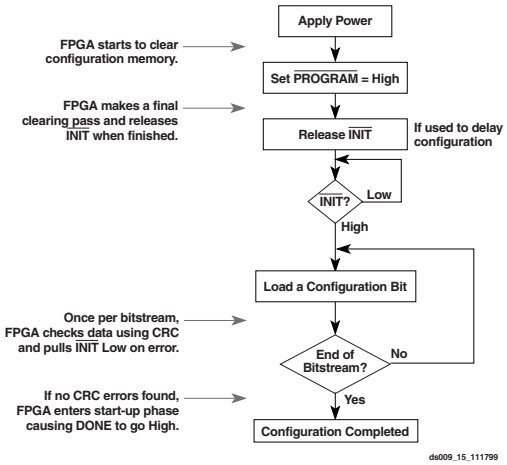

Figure 15: **Serial Configuration Flowchart**

Figure 16 shows the timing of master-serial configuration. Master-serial mode is selected by a <000> or <100> on the mode pins (M2, M1, M0). Table 10 shows the timing information for Figure 16.

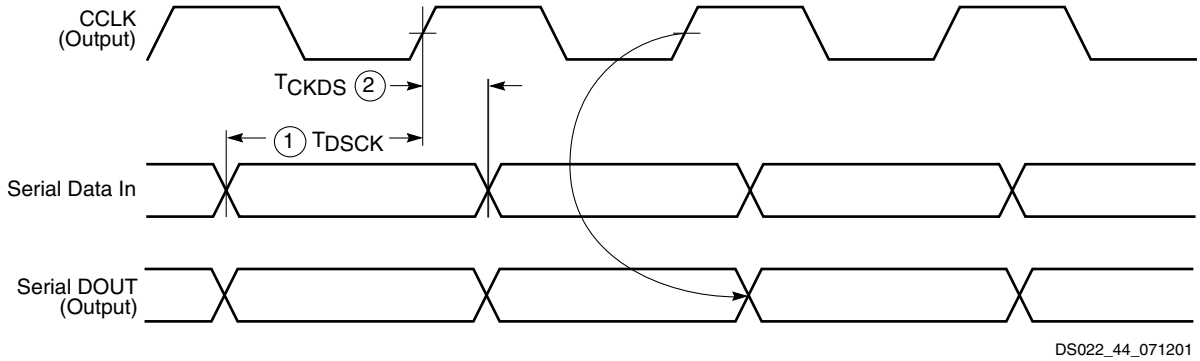

Figure 16: **Master-Serial Mode Programming Switching Characteristics**

At power-up, V_{CC} must rise from 1.0 V to V_{CC} Min in less than 50 ms, otherwise delay configuration by pulling $\overline{\text{PROGRAM}}$ Low until V_{CC} is valid.

SelectMAP Mode

The SelectMAP mode is the fastest configuration option. Byte-wide data is written into the FPGA with a BUSY flag controlling the flow of data.

An external data source provides a byte stream, CCLK, a Chip Select ($\overline{\text{CS}}$) signal and a Write signal ($\overline{\text{WRITE}}$). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low.

Data can also be read using the SelectMAP mode. If $\overline{\text{WRITE}}$ is not asserted, configuration data is read out of the FPGA as part of a readback operation.

After configuration, the pins of the SelectMAP port can be used as additional user I/O. Alternatively, the port can be retained to permit high-speed 8-bit readback.

Retention of the SelectMAP port is selectable on a design-by-design basis when the bitstream is generated. If retention is selected, PROHIBIT constraints are required to prevent the SelectMAP-port pins from being used as user I/O.

Multiple Virtex-E FPGAs can be configured using the SelectMAP mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, $\overline{\text{WRITE}}$, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by asserting the $\overline{\text{CS}}$ pin of each device in turn and writing the appropriate data. See Table 11 for SelectMAP Write Timing Characteristics.

Write

Write operations send packets of configuration data into the FPGA. The sequence of operations for a multi-cycle write operation is shown below. Note that a configuration packet can be split into many such sequences. The packet does not have to complete within one assertion of $\overline{\text{CS}}$, illustrated in Figure 17.

1. Assert $\overline{\text{WRITE}}$ and $\overline{\text{CS}}$ Low. Note that when $\overline{\text{CS}}$ is asserted on successive CCLKs, $\overline{\text{WRITE}}$ must remain either asserted or de-asserted. Otherwise, an abort is initiated, as described below.
2. Drive data onto D[7:0]. Note that to avoid contention, the data source should not be enabled while $\overline{\text{CS}}$ is Low and $\overline{\text{WRITE}}$ is High. Similarly, while $\overline{\text{WRITE}}$ is High, no more that one $\overline{\text{CS}}$ should be asserted.

3. At the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock. If BUSY is High (from a previous write), the data is not accepted. Acceptance instead occurs on the first clock after BUSY goes Low, and the data must be held until this has happened.
4. Repeat steps 2 and 3 until all the data has been sent.
5. De-assert $\overline{CS}$ and $\overline{WRITE}$.

Table 11: **SelectMAP Write Timing Characteristics**

	Description		Symbol		Units
CCLK	D_{0-7} Setup/Hold	1/2	T_{SMDCC}/T_{SMCCD}	5.0 / 1.7	ns, min
	$\overline{CS}$ Setup/Hold	3/4	T_{SMCSCC}/T_{SMCCCS}	7.0 / 1.7	ns, min
	$\overline{WRITE}$ Setup/Hold	5/6	T_{SMCCW}/T_{SMWCC}	7.0 / 1.7	ns, min
	BUSY Propagation Delay	7	T_{SMCKBY}	12.0	ns, max
	Maximum Frequency		F_{CC}	66	MHz, max
	Maximum Frequency with no handshake		F_{CCNH}	50	MHz, max

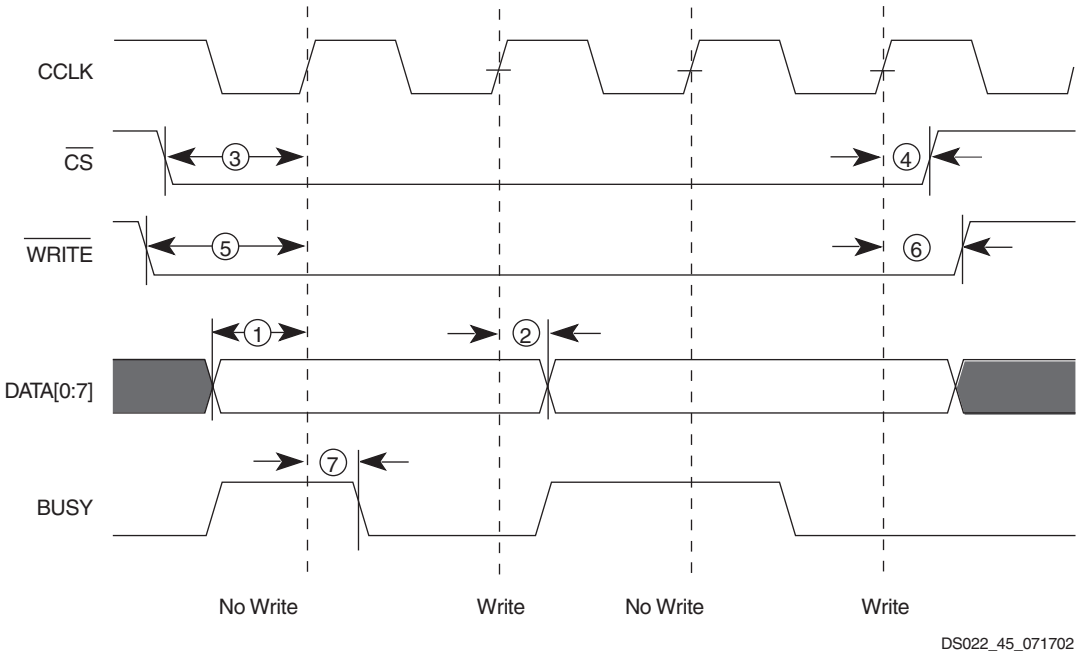

Figure 17: **Write Operations**

A flowchart for the write operation is shown in Figure 18. Note that if CCLK is slower than f_{CCNH}, the FPGA never asserts BUSY, In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.

Abort

During a given assertion of $\overline{CS}$, the user cannot switch from a write to a read, or vice-versa. This action causes the current packet command to be aborted. The device remains BUSY until the aborted operation has completed. Following an abort, data is assumed to be unaligned to word boundaries, and the FPGA requires a new synchronization word prior to accepting any new packets.

To initiate an abort during a write operation, de-assert $\overline{WRITE}$. At the rising edge of CCLK, an abort is initiated, as shown in Figure 19.

VHDL Initialization Example

```
library IEEE;
use IEEE.std_logic_1164.all;

entity MYMEM is
port (CLK, WE:in std_logic;
ADDR: in std_logic_vector(8 downto 0);
DIN: in std_logic_vector(7 downto 0);
DOUT: out std_logic_vector(7 downto 0));
end MYMEM;

architecture BEHAVE of MYMEM is
signal logic0, logic1: std_logic;

component RAMB4_S8
--synopsys translate_off
generic( INIT_00,INIT_01, INIT_02, INIT_03, INIT_04, INIT_05, INIT_06, INIT_07,
INIT_08, INIT_09, INIT_0a, INIT_0b, INIT_0c, INIT_0d, INIT_0e, INIT_0f : BIT_VECTOR(255
downto 0)
:= X"0000000000000000000000000000000000000000000000000000000000000000");
--synopsys translate_on
port (WE, EN, RST, CLK: in STD_LOGIC;
ADDR: in STD_LOGIC_VECTOR(8 downto 0);
DI: in STD_LOGIC_VECTOR(7 downto 0);
DO: out STD_LOGIC_VECTOR(7 downto 0));
end component;

--synopsys dc_script_begin
--set_attribute ram0 INIT_00
"0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF" -type string
--set_attribute ram0 INIT_01
"FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210" -type string
--synopsys dc_script_end

begin
logic0 <='0';
logic1 <='1';

ram0: RAMB4_S8
--synopsys translate_off
generic map (

INIT_00 => X"0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF",
INIT_01 => X"FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210")
--synopsys translate_on
port map (WE=>WE, EN=>logic1, RST=>logic0, CLK=>CLK,ADDR=>ADDR, DI=>DIN, DO=>DOUT);

end BEHAVE;
```

represents a combination of the LVTTL IBUFG and BUFG symbols, such that the output of the BUFGP can connect directly to the clock pins throughout the design.

Unlike previous architectures, the Virtex-E BUFGP symbol can only be placed in a global clock pad location. The LOC property can specify a location for the BUFGP.

OBUF

An OBUF must drive outputs through an external output port. The generic output buffer (OBUF) symbol appears in Figure 40.

The extension to the base name defines which I/O standard the OBUF uses. With no extension specified for the generic OBUF symbol, the assumed standard is slew rate limited LVTTL with 12 mA drive strength.

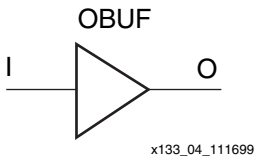

Figure 40: **Virtex-E Output Buffer (OBUF) Symbol**

The LVTTL OBUF additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL output buffers have selectable drive strengths.

The format for LVTTL OBUF symbol names is as follows:

OBUF_<slew_rate>_<drive_strength>

where <slew_rate> is either F (Fast) or S (Slow), and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

The following list details variations of the OBUF symbol.

- OBUF
- OBUF_S_2
- OBUF_S_4
- OBUF_S_6
- OBUF_S_8
- OBUF_S_12
- OBUF_S_16
- OBUF_S_24
- OBUF_F_2
- OBUF_F_4
- OBUF_F_6
- OBUF_F_8
- OBUF_F_12
- OBUF_F_16
- OBUF_F_24
- OBUF_LVCMOS2
- OBUF_PCI33_3
- OBUF_PCI66_3
- OBUF_GTL
- OBUF_GTLP
- OBUF_HSTL_I
- OBUF_HSTL_III
- OBUF_HSTL_IV
- OBUF_SSTL3_I
- OBUF_SSTL3_II
- OBUF_SSTL2_I
- OBUF_SSTL2_II
- OBUF_CTT
- OBUF_AGP
- OBUF_LVCMOS18
- OBUF_LVDS
- OBUF_LVPECL

The Virtex-E series supports eight banks for the HQ and PQ packages. The CS packages support four V_{CCO} banks.

OBUF placement restrictions require that within a given V_{CCO} bank each OBUF share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within any V_{CCO} bank. Table 20 summarizes the Virtex-E output compatibility requirements. The LOC property can specify a location for the OBUF.

Table 20: **Output Standards Compatibility Requirements**

Rule 1	Only outputs with standards that share compatible V_{CCO} can be used within the same bank.
Rule 2	There are no placement restrictions for outputs with standards that do not require a V_{CCO}.
V_{CCO}	Compatible Standards
3.3	LVTTL, SSTL3_I, SSTL3_II, CTT, AGP, GTL, GTL+, PCI33_3, PCI66_3
2.5	SSTL2_I, SSTL2_II, LVCMOS2, GTL, GTL+
1.5	HSTL_I, HSTL_III, HSTL_IV, GTL, GTL+

OBUFT

The generic 3-state output buffer OBUFT (see Figure 41) typically implements 3-state outputs or bidirectional I/O.

The extension to the base name defines which I/O standard OBUFT uses. With no extension specified for the generic OBUFT symbol, the assumed standard is slew rate limited LVTTL with 12 mA drive strength.

The LVTTL OBUFT additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

SSTL3_I

A sample circuit illustrating a valid termination technique for SSTL3_I appears in Figure 49. DC voltage specifications appear in Table 28.

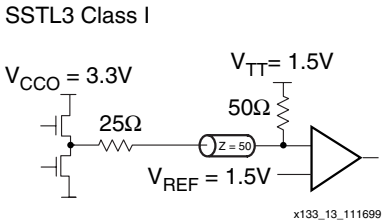

Figure 49: **Terminated SSTL3 Class I**

Table 28: **SSTL3_I Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	**3.0**	**3.3**	**3.6**
V_{REF} = 0.45 × V_{CCO}	1.3	1.5	1.7
V_{TT} = V_{REF}	1.3	1.5	1.7
V_{IH} = V_{REF} + 0.2	1.5	1.7	3.9(1)
V_{IL} = V_{REF} – 0.2	–0.3(2)	1.3	1.5
V_{OH} = V_{REF} + 0.6	1.9	-	-
V_{OL} = V_{REF} – 0.6	-	-	1.1
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL}at V_{OL} (mA)	8	-	-

Notes:
1. V_{IH} maximum is V_{CCO} + 0.3
2. V_{IL} minimum does not conform to the formula

SSTL3_II

A sample circuit illustrating a valid termination technique for SSTL3_II appears in Figure 50. DC voltage specifications appear in Table 29.

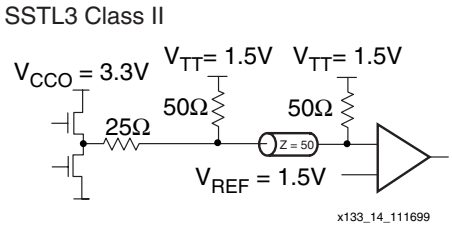

Figure 50: **Terminated SSTL3 Class II**

Table 29: **SSTL3_II Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
V_{REF} = 0.45 × V_{CCO}	1.3	1.5	1.7
V_{TT} = V_{REF}	1.3	1.5	1.7
V_{IH} = V_{REF} + 0.2	1.5	1.7	3.9(1)
V_{IL}= V_{REF} – 0.2	–0.3(2)	1.3	1.5
V_{OH} = V_{REF} + 0.8	2.1	-	-
V_{OL}= V_{REF} – 0.8	-	-	0.9
I_{OH} at V_{OH} (mA)	–16	-	-
I_{OL}at V_{OL} (mA)	16	-	-

Notes:
1. V_{IH} maximum is V_{CCO} + 0.3
2. V_{IL} minimum does not conform to the formula

SSTL2_I

A sample circuit illustrating a valid termination technique for SSTL2_I appears in Figure 51. DC voltage specifications appear in Table 30.

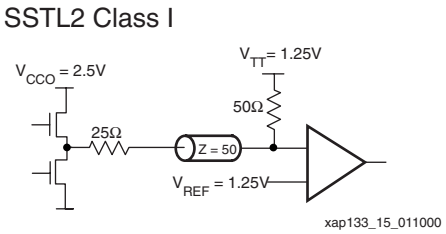

Figure 51: **Terminated SSTL2 Class I**

Table 30: **SSTL2_I Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
V_{REF} = 0.5 × V_{CCO}	1.15	1.25	1.35
V_{TT} = V_{REF} + N(1)	1.11	1.25	1.39
V_{IH} = V_{REF} + 0.18	1.33	1.43	3.0(2)
V_{IL} = V_{REF} – 0.18	–0.3(3)	1.07	1.17
V_{OH} = V_{REF} + 0.61	1.76	-	-
V_{OL}= V_{REF} – 0.61	-	-	0.74
I_{OH} at V_{OH} (mA)	–7.6	-	-
I_{OL}at V_{OL} (mA)	7.6	-	-

Notes:
1. N must be greater than or equal to -0.04 and less than or equal to 0.04.
2. V_{IH} maximum is V_{CCO} + 0.3.
3. V_{IL} minimum does not conform to the formula.

Table 43: **Output Library Macros**

Name	Inputs	Outputs
OBUFDS_FD_LVDS	D, C	O, OB
OBUFDS_FDE_LVDS	DD, CE, C	O, OB
OBUFDS_FDC_LVDS	D, C, CLR	O, OB
OBUFDS_FDCE_LVDS	D, CE, C, CLR	O, OB
OBUFDS_FDP_LVDS	D, C, PRE	O, OB
OBUFDS_FDPE_LVDS	D, CE, C, PRE	O, OB
OBUFDS_FDR_LVDS	D, C, R	O, OB
OBUFDS_FDRE_LVDS	D, CE, C, R	O, OB
OBUFDS_FDS_LVDS	D, C, S	O, OB
OBUFDS_FDSE_LVDS	D, CE, C, S	O, OB
OBUFDS_LD_LVDS	D, G	O, OB
OBUFDS_LDE_LVDS	D, GE, G	O, OB
OBUFDS_LDC_LVDS	D, G, CLR	O, OB
OBUFDS_LDCE_LVDS	D, GE, G, CLR	O, OB
OBUFDS_LDP_LVDS	D, G, PRE	O, OB
OBUFDS_LDPE_LVDS	D, GE, G, PRE	O, OB

Creating LVDS Output 3-State Buffers

LVDS output 3-state buffers can be placed in a wide number of IOB locations. The exact locations are dependent on the package used. The Virtex-E package information lists the possible locations as IO_L#P for the P-side and IO_L#N for the N-side, where # is the pair number.

HDL Instantiation

Both output 3-state buffers are required to be instantiated in the design and placed on the correct IO_L#P and IO_L#N locations. The IOB must have the same net source the following pins, clock (C), set/reset (SR), 3-state (T), 3-state clock enable (TCE), output (O), output clock enable (OCE). In addition, the output (O) pins must be inverted with respect to each other, and if output registers are used, the INIT states must be opposite values (one High and one Low). If 3-state registers are used, they must be initialized to the same state. Failure to follow these rules leads to DRC errors in the software.

VHDL Instantiation

```
data0_p:   OBUFT_LVDS port map
(I=>data_int(0), T=>data_tri,
O=>data_p(0));

data0_inv: INV port map
(I=>data_int(0), O=>data_n_int(0));

data0_n:    OBUFT_LVDS port map
(I=>data_n_int(0), T=>data_tri,
O=>data_n(0));
```

Verilog Instantiation

```
OBUFT_LVDS data0_p   (.I(data_int[0]),
.T(data_tri), .O(data_p[0]));

INV        data0_inv (.I(data_int[0],
.O(data_n_int[0]);

OBUFT_LVDS data0_n   (.I(data_n_int[0]),
.T(data_tri), .O(data_n[0]));
```

Location Constraints

All LVDS buffers must be explicitly placed on a device. For the output buffers this can be done with the following constraint in the .ucf or .ncf file.

```
NET data_p<0> LOC = D28; # IO_L0P

NET data_n<0> LOC = B29; # IO_L0N
```

Synchronous vs. Asynchronous 3-State Outputs

If the outputs are synchronous (registered in the IOB), then any IO_L#PIN pair can be used. If the outputs are asynchronous (no output register), then they must use one of the pairs that are part of the same IOB group at the end of a ROW or COLUMN in the device. This applies for either the 3-state pin or the data out pin.

LVDS pairs that can be used as asynchronous outputs are listed in the Virtex-E pinout tables. Some pairs are marked as “asynchronous capable” for all devices in that package, and others are marked as available only for that device in the package. If the device size might be changed at some point in the product lifetime, then only the common pairs for all packages should be used.

Adding Output and 3-State Registers

All LVDS buffers can have an output register in the IOB. The output registers must be in both the P-side and N-side IOBs. All the normal IOB register options are available (FD, FDE, FDC, FDCE, FDP, FDPE, FDR, FDRE, FDS, FDSE, LD, LDE, LDC, LDCE, LDP, LDPE). The register elements can be inferred or explicitly instantiated in the HDL code.

Special care must be taken to insure that the D pins of the registers are inverted and that the INIT states of the registers are opposite. The 3-state (T), 3-state clock enable (CE), clock pin (C), output clock enable (CE) and set/reset (CLR/PRE or S/R) pins must connect to the same source. Failure to do this leads to a DRC error in the software.

DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Device	Min	Max	Units
V_{DRINT}	Data Retention V_{CCINT} Voltage (below which configuration data might be lost)		All	1.5		V
V_{DRIO}	Data Retention V_{CCO} Voltage (below which configuration data might be lost)		All	1.2		V
I_{CCINTQ}	Quiescent V_{CCINT} supply current (Note 1)		XCV50E		200	mA
			XCV100E		200	mA
			XCV200E		300	mA
			XCV300E		300	mA
			XCV400E		300	mA
			XCV600E		400	mA
			XCV1000E		500	mA
			XCV1600E		500	mA
			XCV2000E		500	mA
			XCV2600E		500	mA
			XCV3200E		500	mA
I_{CCOQ}	Quiescent V_{CCO} supply current (Note 1)		XCV50E		2	mA
			XCV100E		2	mA
			XCV200E		2	mA
			XCV300E		2	mA
			XCV400E		2	mA
			XCV600E		2	mA
			XCV1000E		2	mA
			XCV1600E		2	mA
			XCV2000E		2	mA
			XCV2600E		2	mA
			XCV3200E		2	mA
I_L	Input or output leakage current		All	–10	+10	µA
C_{IN}	Input capacitance (sample tested)	BGA, PQ, HQ, packages	All		8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0 V, V_{CCO} = 3.3 V (sample tested)		All	Note 2	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 3.6 V (sample tested)			Note 2	0.25	mA

Notes:
1. With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating.
2. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.

Virtex-E Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted

Global Clock Set-Up and Hold for LVTTL Standard, *with* DLL

Description[1]	Symbol	Device	Speed Grade[2, 3]				Units
			Min	-8	-7	-6	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in **IOB Input Switching Characteristics Standard Adjustments**, page 8.							
No Delay	T_{PSDLL}/T_{PHDLL}	XCV50E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns
Global Clock and IFF, with DLL		XCV100E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns
		XCV200E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns
		XCV300E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns
		XCV400E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns
		XCV600E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns
		XCV1000E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns
		XCV1600E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns
		XCV2000E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns
		XCV2600E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns
		XCV3200E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. DLL output jitter is already included in the timing calculation.

Table 10: **BG352 — XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
0	IO	C15
0	IO	B15[1]
0	IO_LVDS_DLL_L9N	A15
0	GCK3	D14
1	GCK2	B14
1	IO_LVDS_DLL_L9P	A13
1	IO	B13[1]
1	IO_L10N	C13
1	IO_L10P	A12
1	IO_L11N_Y	B12
1	IO_VREF_1_L11P_Y	C12
1	IO_L12N_Y	A11
1	IO_L12P_Y	B11
1	IO	B10[1]
1	IO_L13N	C11
1	IO_L13P	D11
1	IO	A9[1]
1	IO_L14N_YY	B9
1	IO_L14P_YY	C10
1	IO_L15N_YY	B8
1	IO_VREF_1_L15P_YY	C9
1	IO_L16N _Y	D9
1	IO_L16P _Y	A7
1	IO	B7
1	IO	C8[1]
1	IO	D8[1]
1	IO_L17N_YY	A6
1	IO_VREF_1_L17P_YY	B6
1	IO_L18N_YY	C7
1	IO_L18P_YY	A4
1	IO	B5[1]
1	IO_L19N_YY	C6
1	IO_VREF_1_L19P_YY	D6[2]

Table 10: **BG352 — XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
1	IO	B4
1	IO	C5[1]
1	IO	A3[1]
1	IO_WRITE_L20N_YY	D5
1	IO_CS_L20P_YY	C4
2	IO_DOUT_BUSY_L21P_YY	E4
2	IO_DIN_D0_L21N_YY	D3
2	IO	C2[1]
2	IO	E3[1]
2	IO	F4
2	IO_VREF_2_L22P_YY	D2[2]
2	IO_L22N_YY	C1
2	IO	D1[1]
2	IO_L23P_YY	G4
2	IO_L23N_YY	F3
2	IO_VREF_2_L24P_Y	E2
2	IO_L24N_Y	F2
2	IO	G3[1]
2	IO	G2[1]
2	IO_L25P	F1
2	IO_L25N	J4
2	IO	H3
2	IO_VREF_2_L26P _Y	H2
2	IO_D1_L26N _Y	G1
2	IO_D2_L27P_YY	J3
2	IO_L27N_YY	J2
2	IO	K3[1]
2	IO_L28P	J1
2	IO_L28N	L4
2	IO	K2[1]
2	IO_L29P_YY	L3
2	IO_L29N_YY	L2
2	IO_VREF_2_L30P _Y	M4

Table 10: **BG352 — XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
6	IO_L74P _Y	R25
6	IO_L75N	R26
6	IO_L75P	P24
6	IO	P23[1]
6	IO	N26
7	IO_L76N_YY	N25
7	IO_L76P_YY	N24
7	IO	M26[1]
7	IO_L77N	M25
7	IO_L77P	M24
7	IO_L78N _Y	M23
7	IO_VREF_7_L78P _Y	L26
7	IO_L79N_YY	K25
7	IO_L79P_YY	L24
7	IO	L23[1]
7	IO_L80N	J26
7	IO_L80P	J25
7	IO	K24[1]
7	IO_L81N_YY	K23
7	IO_L81P_YY	H25
7	IO_L82N _Y	J23
7	IO_VREF_7_L82P _Y	G26
7	IO_L83N _Y	G25
7	IO_L83P _Y	H24
7	IO	H23
7	IO	F26[1]
7	IO	F25[1]
7	IO_L84N_Y	G24
7	IO_VREF_7_L84P_Y	D26
7	IO_L85N_YY	E25
7	IO_L85P_YY	F24
7	IO	F23[1]
7	IO_L86N_YY	D25

Table 10: **BG352 — XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
7	IO_VREF_7_L86P_YY	E24[2]
7	IO	C26
7	IO	E23[1]
7	IO	D24[1]
7	IO	C25
NA	TDI	B3
NA	TDO	D4
NA	CCLK	C3
NA	TCK	C24
NA	TMS	D23
NA	PROGRAM	AC4
NA	DONE	AD3
NA	DXN	AD23
NA	DXP	AE24
NA	M2	AC23
NA	M0	AD24
NA	M1	AB23
NA	VCCINT	A20
NA	VCCINT	B16
NA	VCCINT	C14
NA	VCCINT	D12
NA	VCCINT	D10
NA	VCCINT	K4
NA	VCCINT	L1
NA	VCCINT	P2
NA	VCCINT	T1
NA	VCCINT	W2
NA	VCCINT	AC10
NA	VCCINT	AF11
NA	VCCINT	AE14
NA	VCCINT	AF16
NA	VCCINT	AE19

Table 11: **BG352 Differential Pin Pair Summary XCV100E, XCV200E, XCV300E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
55	5	AC13	AD14	√	GCLK LVDS 1/0
56	5	AD15	AC15	√	VREF_5
57	5	AE16	AE17	√	-
58	5	AC16	AF18	2	-
59	5	AD17	AC17	√	-
60	5	AD18	AC18	√	VREF_5
61	5	AF20	AE20	1	-
62	5	AE21	AD20	√	VREF_5
63	5	AF23	AE22	√	-
64	5	AC21	AE23	√	VREF_5
65	6	AD25	AC24	√	-
66	6	AC26	AD26	√	VREF_6
67	6	AB25	AA24	√	-
68	6	Y24	AA25	√	VREF_6
69	6	W24	V23	2	-
70	6	U23	Y26	√	VREF_6
71	6	U24	V25	√	-
72	6	U25	T23	1	-
73	6	T26	T25	√	-
74	6	R25	R24	√	VREF_6
75	6	P24	R26	2	-
76	7	N24	N25	√	-
77	7	M24	M25	2	-
78	7	L26	M23	√	VREF_7
79	7	L24	K25	√	-
80	7	J25	J26	1	-
81	7	H25	K23	√	-
82	7	G26	J23	√	VREF_7
83	7	H24	G25	1	-
84	7	D26	G24	√	VREF_7
85	7	F24	E25	√	-
86	7	E24	D25	√	VREF_7

Notes:
1. AO in the XCV100E.
2. AO in the XCV200E.

BG432 Ball Grid Array Packages

XCV300E, XCV400E, and XCV600E devices in BG432 Ball Grid Array packages have footprint compatibility. Pins labeled I0_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 12, see Table 13 for Differential Pair information.

Table 12: **BG432 — XCV300E, XCV400E, XCV600E**

Bank	Pin Description	Pin #
0	GCK3	D17
0	IO	A22
0	IO	A26
0	IO	B20
0	IO	C23
0	IO	C28
0	IO_L0N_Y	B29
0	IO_L0P_Y	D27
0	IO_L1N_YY	B28
0	IO_L1P_YY	C27
0	IO_VREF_L2N_YY	D26
0	IO_L2P_YY	A28
0	IO_L3N_Y	B27
0	IO_L3P_Y	C26
0	IO_L4N_YY	D25
0	IO_L4P_YY	A27
0	IO_VREF_L5N_YY	D24
0	IO_L5P_YY	C25
0	IO_L6N_Y	B25
0	IO_L6P_Y	D23
0	IO_VREF_L7N_Y	C24[1]
0	IO_L7P_Y	B24
0	IO_VREF_L8N_YY	D22
0	IO_L8P_YY	A24
0	IO_L9N_YY	C22
0	IO_L9P_YY	B22
0	IO_L10N_YY	C21
0	IO_L10P_YY	D20
0	IO_L11N_YY	B21
0	IO_L11P_YY	C20

Table 12: **BG432 — XCV300E, XCV400E, XCV600E**

Bank	Pin Description	Pin #
6	IO	AA30
6	IO	AC30
6	IO	AD29
6	IO	U31
6	IO	W28
6	IO_L103N_YY	AJ30
6	IO_L103P_YY	AH30
6	IO_L104N	AG28
6	IO_L104P	AH31
6	IO_L105N_Y	AG29
6	IO_L105P_Y	AG30
6	IO_VREF_L106N_Y	AF28
6	IO_L106P_Y	AG31
6	IO_L107N	AF29
6	IO_L107P	AF30
6	IO_L108N_Y	AE28
6	IO_L108P_Y	AF31
6	IO_VREF_L109N_YY	AE30
6	IO_L109P_YY	AD28
6	IO_L110N_Y	AD30
6	IO_L110P_Y	AD31
6	IO_VREF_L111N_Y	AC28[1]
6	IO_L111P_Y	AC29
6	IO_VREF_L112N_YY	AB28
6	IO_L112P_YY	AB29
6	IO_L113N_YY	AB31
6	IO_L113P_YY	AA29
6	IO_L114N_Y	Y28
6	IO_L114P_Y	Y29
6	IO_L115N_Y	Y30
6	IO_L115P_Y	Y31
6	IO_L116N_Y	W29
6	IO_L116P_Y	W30
6	IO_VREF_L117N_YY	V28
6	IO_L117P_YY	V29
6	IO_L118N_Y	V30

Table 12: **BG432 — XCV300E, XCV400E, XCV600E**

Bank	Pin Description	Pin #
6	IO_L118P_Y	U29
6	IO_VREF_L119N_Y	U28[2]
6	IO_L119P_Y	U30
6	IO	T30
7	IO	C30
7	IO	H29
7	IO	H31
7	IO	L29
7	IO	M31
7	IO	R28
7	IO_L120N_YY	T31
7	IO_L120P_YY	R29
7	IO_L121N_Y	R30
7	IO_VREF_L121P_Y	R31[2]
7	IO_L122N_Y	P29
7	IO_L122P_Y	P28
7	IO_L123N_YY	P30
7	IO_VREF_L123P_YY	N30
7	IO_L124N_Y	N28
7	IO_L124P_Y	N31
7	IO_L125N_Y	M29
7	IO_L125P_Y	M28
7	IO_L126N_Y	M30
7	IO_L126P_Y	L30
7	IO_L127N_YY	K31
7	IO_L127P_YY	K30
7	IO_L128N_YY	K28
7	IO_VREF_L128P_YY	J30
7	IO_L129N_Y	J29
7	IO_VREF_L129P_Y	J28[1]
7	IO_L130N_Y	H30
7	IO_L130P_Y	G30
7	IO_L131N_YY	H28
7	IO_VREF_L131P_YY	F31
7	IO_L132N_Y	G29

FG676 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 21: **FG676 Differential Pin Pair Summary XCV400E, XCV600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
3	0	E13	B13	NA	IO_DLL_L21N
2	1	C13	F14	NA	IO_DLL_L21P
1	5	AB13	AF13	NA	IO_DLL_L115N
0	4	AA14	AC14	NA	IO_DLL_L115P
IOLVDS Total Pairs: 183, Asynchronous Output Pairs: 97					
0	0	F7	C4	1	-
1	0	C5	G8	√	-
2	0	E7	D6	√	VREF
3	0	F8	A4	NA	-
4	0	D7	B5	NA	-
5	0	G9	E8	√	VREF
6	0	F9	A5	√	-
7	0	C7	D8	1	-
8	0	E9	B7	1	VREF
9	0	D9	A7	NA	-
10	0	G10	B8	NA	VREF
11	0	F10	C9	√	-
12	0	E10	A8	1	-
13	0	D10	G11	√	-
14	0	F11	B10	√	-
15	0	E11	C10	NA	-
16	0	D11	G12	√	-
17	0	F12	C11	√	VREF

Table 21: **FG676 Differential Pin Pair Summary XCV400E, XCV600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
18	0	E12	A11	√	-
19	0	C12	D12	1	-
20	0	H13	A12	1	VREF
21	1	F14	B13	NA	IO_LVDS_DLL
22	1	F13	E14	NA	-
23	1	A14	D14	1	VREF
24	1	H14	C14	1	-
25	1	C15	G14	√	-
26	1	D15	E15	√	VREF
27	1	F15	C16	√	-
28	1	D16	G15	-	-
29	1	A17	E16	√	-
30	1	E17	C17	√	-
31	1	D17	F16	1	-
32	1	C18	F17	√	-
33	1	G16	A18	√	VREF
34	1	G17	C19	√	-
35	1	B19	D18	1	VREF
36	1	E18	D19	1	-
37	1	B20	F18	√	-
38	1	C20	G19	√	VREF
39	1	E19	G18	√	-
40	1	D20	A21	√	-
41	1	C21	F19	√	VREF
42	1	E20	B22	√	-
43	1	D21	A23	2	-
44	1	E21	C22	√	CS
45	2	E23	F22	√	DIN, D0
46	2	E24	F20	√	-
47	2	G21	G22	2	-
48	2	F24	H20	1	VREF
49	2	E25	H21	1	-
50	2	F23	G23	√	-
51	2	H23	J20	√	VREF

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
2	IO_L63N	G4
2	IO_L64P	G3
2	IO_L64N	E2
2	IO_VREF_L65P_Y	H4
2	IO_L65N_Y	E1
2	IO_L66P_YY	H3
2	IO_L66N_YY	F2
2	IO_L67P	J4
2	IO_L67N	F1
2	IO_L68P_Y	J3
2	IO_L68N_Y	G2
2	IO_VREF_L69P_YY	G1
2	IO_L69N_YY	K4
2	IO_L70P_YY	H2
2	IO_L70N_YY	K3
2	IO_VREF_L71P	H1[3]
2	IO_L71N	L4
2	IO_L72P	J2
2	IO_L72N	L3
2	IO_VREF_L73P_YY	J1
2	IO_L73N_YY	M3
2	IO_L74P_YY	K2
2	IO_L74N_YY	N4
2	IO_L75P	K1
2	IO_L75N	N3
2	IO_VREF_L76P_YY	L2
2	IO_D1_L76N_YY	P4
2	IO_D2_L77P_YY	P3
2	IO_L77N_YY	L1
2	IO_L78P_Y	R4
2	IO_L78N_Y	M2
2	IO_L79P	R3
2	IO_L79N	M1
2	IO_L80P	T4
2	IO_L80N	N2
2	IO_VREF_L81P_Y	N1[1]

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
2	IO_L81N_Y	T3
2	IO_L82P_YY	P2
2	IO_L82N_YY	U5
2	IO_L83P	P1
2	IO_L83N	U4
2	IO_L84P_Y	R2
2	IO_L84N_Y	U3
2	IO_VREF_L85P_YY	V5
2	IO_D3_L85N_YY	R1
2	IO_L86P_YY	V4
2	IO_L86N_YY	T2
2	IO_L87P	V3
2	IO_L87N	T1
2	IO_L88P	W4
2	IO_L88N	U2
2	IO_VREF_L89P_YY	W3
2	IO_L89N_YY	U1
2	IO_L90P_YY	AA3
2	IO_L90N_YY	V2
2	IO_VREF_L91P	AA4[2]
2	IO_L91N	V1
2	IO_L92P_YY	AB2
2	IO_L92N_YY	W2
3	IO	AP3
3	IO	AT3
3	IO	AB3
3	IO_L93P	AB4
3	IO_VREF_L93N	W1[2]
3	IO_L94P_YY	AB5
3	IO_L94N_YY	Y2
3	IO_L95P_YY	AC2
3	IO_VREF_L95N_YY	Y1
3	IO_L96P	AC3
3	IO_L96N	AA1
3	IO_L97P	AC4

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
NA	GND	D20
NA	GND	D12
NA	GND	C39
NA	GND	C37
NA	GND	C3
NA	GND	C20
NA	GND	C1
NA	GND	B39
NA	GND	B38
NA	GND	B2
NA	GND	B1
NA	GND	AW39
NA	GND	AW38
NA	GND	AW37
NA	GND	AW3
NA	GND	AW2
NA	GND	AW1
NA	GND	AV39
NA	GND	AV38
NA	GND	AV2
NA	GND	AV1
NA	GND	AU39
NA	GND	AU37
NA	GND	AU3
NA	GND	AU20
NA	GND	AU1
NA	GND	AT4
NA	GND	AT36
NA	GND	AT28
NA	GND	AT20
NA	GND	AT12
NA	GND	AR5
NA	GND	AR35
NA	GND	AR28
NA	GND	AR21
NA	GND	AR20

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
NA	GND	AR19
NA	GND	AR12
NA	GND	AH5
NA	GND	AH4
NA	GND	AH36
NA	GND	AH35
NA	GND	AA5
NA	GND	AA35
NA	GND	A39
NA	GND	A38
NA	GND	A37
NA	GND	A3
NA	GND	A2
NA	GND	A1

Notes:
1. V_{REF} or I/O option only in the XCV1000E, 1600E, 2000E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV1600E, 2000E; otherwise, I/O option only.
3. V_{REF} or I/O option only in the XCV2000E; otherwise, I/O option only.

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
0	IO_L6N_Y	A5
0	IO_L6P_Y	F8
0	IO_L7N_Y	D7
0	IO_L7P_Y	N11
0	IO_L8N_YY	G9
0	IO_L8P_YY	E8
0	IO_VREF_L9N_YY	A6
0	IO_L9P_YY	J11
0	IO_L10N_Y	C7
0	IO_L10P_Y	B7
0	IO_L11N_Y	C8
0	IO_L11P_Y	H10
0	IO_L12N_YY	G10
0	IO_L12P_YY	F10
0	IO_VREF_L13N_YY	A8
0	IO_L13P_YY	H11
0	IO_L14N	D9[4]
0	IO_L14P	C9[3]
0	IO_L15N_YY	B9
0	IO_L15P_YY	J12
0	IO_L16N	E10[4]
0	IO_VREF_L16P	A9
0	IO_L17N	G11
0	IO_L17P	B10
0	IO_L18N_YY	H12[4]
0	IO_L18P_YY	C10[4]
0	IO_L19N_Y	H13
0	IO_L19P_Y	F11
0	IO_L20N_Y	E11
0	IO_L20P_Y	D11
0	IO_L21N_Y	B11[4]
0	IO_L21P_Y	G12[4]
0	IO_L22N_YY	F12
0	IO_L22P_YY	C11
0	IO_VREF_L23N_YY	A10[1]
0	IO_L23P_YY	D12
0	IO_L24N_Y	E12

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
0	IO_L24P_Y	A11
0	IO_L25N_Y	G13
0	IO_L25P_Y	B12
0	IO_L26N_YY	A12
0	IO_L26P_YY	K13
0	IO_VREF_L27N_YY	F13
0	IO_L27P_YY	B13
0	IO_L28N_Y	G14
0	IO_L28P_Y	E13
0	IO_L29N_Y	D14
0	IO_L29P_Y	B14
0	IO_L30N_YY	A14
0	IO_L30P_YY	J14
0	IO_VREF_L31N_YY	K14
0	IO_L31P_YY	J15
0	IO_L32N	B15[4]
0	IO_L32P	H15[3]
0	IO_VREF_L33N_YY	F15[2,3]
0	IO_L33P_YY	D15[4]
0	IO_LVDS_DLL_L34N	A15
1	GCK2	E15
1	IO	A25[4]
1	IO	B17[4]
1	IO	B18[4]
1	IO	C23[4]
1	IO	D16[4]
1	IO	D17[5]
1	IO	D23[4]
1	IO	E19[4]
1	IO	E24[5]
1	IO	F22[4]
1	IO	G17[5]
1	IO	G20[4]
1	IO	J16[4]
1	IO	J17[4]
1	IO	J19[5]

Table 27: **FG900 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
120	3	AA30	W24	4	-
121	3	AA29	V20	1	-
122	3	Y27	W23	NA	-
123	3	Y26	AB30	√	D5
124	3	V21	AA28	√	VREF
125	3	Y25	AA27	4	-
126	3	W22	Y23	4	-
127	3	Y24	AB28	4	VREF
128	3	AC30	AA25	√	-
129	3	W21	AA24	2	-
130	3	AB26	AD30	√	-
131	3	Y22	AC27	√	VREF
132	3	AD28	AB25	2	-
133	3	AC26	AE30	4	-
134	3	AD27	AF30	√	-
135	3	AF29	AB24	1	VREF
136	3	AB23	AE28	4	-
137	3	AG30	AC25	3	-
138	3	AE26	AG29	4	VREF
139	3	AH30	AC24	1	-
140	3	AF28	AD25	NA	-
141	3	AH29	AA22	√	INIT
142	4	AF27	AK28	√	-
143	4	AG26	AH27	4	-
144	4	AD23	AJ27	2	-
145	4	AB21	AF25	2	VREF
146	4	AC22	AH26	2	-
147	4	AA21	AG25	√	-
148	4	AJ26	AD22	√	VREF
149	4	AA20	AH25	1	-
150	4	AC21	AF24	1	-
151	4	AG24	AK26	√	-
152	4	AJ24	AF23	√	VREF
153	4	AE23	AB20	2	-

Table 27: **FG900 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
154	4	AC20	AG23	2	-
155	4	AF22	AE22	√	-
156	4	AJ22	AG22	√	VREF
157	4	AK24	AD20	NA	-
158	4	AA19	AF21	4	-
159	4	AH22	AA18	NA	VREF
160	4	AG21	AK23	NA	-
161	4	AH21	AD19	4	-
162	4	AE20	AJ21	2	-
163	4	AG20	AF20	2	-
164	4	AC18	AF19	2	-
165	4	AJ20	AE19	√	-
166	4	AK22	AH20	√	VREF
167	4	AG19	AB17	1	-
168	4	AJ19	AD17	1	-
169	4	AA16	AA17	√	-
170	4	AK21	AB16	√	VREF
171	4	AG18	AK20	2	-
172	4	AK19	AD16	2	-
173	4	AE16	AE17	√	-
174	4	AG17	AJ17	√	VREF
175	4	AD15	AH17	NA	-
176	4	AG16	AK17	4	VREF
177	5	AF16	AH16	NA	IO_ LVDS_DLL
178	5	AC15	AG15	4	VREF
179	5	AB15	AF15	√	-
180	5	AA15	AF14	√	VREF
181	5	AH15	AK15	√	-
182	5	AB14	AF13	2	-
183	5	AH14	AJ14	2	-
184	5	AE14	AG13	√	VREF
185	5	AK13	AD13	√	-
186	5	AE13	AF12	1	-
187	5	AC13	AA13	1	-

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
6	IO_VREF_L299N_YY	W5
6	IO_L299P_YY	V1
6	IO_L300N_YY	V7
6	IO_L300P_YY	U2
6	IO_VREF_L301N_Y	V6[1]
6	IO_L301P_Y	U1
7	IO	F5
7	IO	G6[3]
7	IO	H1
7	IO	H7[3]
7	IO	K2[3]
7	IO	K4[3]
7	IO	L6[3]
7	IO	M5[3]
7	IO	M10[3]
7	IO	N5[3]
7	IO	N10
7	IO	R7[4]
7	IO	T2
7	IO	T7[3]
7	IO	U8
7	IO	V4[3]
7	IO_L302N_YY	U9
7	IO_L302P_YY	U4
7	IO_L303N_Y	U7
7	IO_VREF_L303P_Y	U5[1]
7	IO_L304N_YY	U3
7	IO_L304P_YY	U6
7	IO_L305N_YY	T3
7	IO_VREF_L305P_YY	T6
7	IO_L306N_Y	T9
7	IO_L306P_Y	T4
7	IO_L307N_Y	T5[5]

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
7	IO_L307P_Y	R1[4]
7	IO_L308N_Y	R6
7	IO_L308P_Y	T10
7	IO_L309N_YY	R2
7	IO_L309P_YY	R5
7	IO_L310N_YY	P1
7	IO_VREF_L310P_YY	P5
7	IO_L311N_Y	R8
7	IO_L311P_Y	P2
7	IO_L312N_Y	R9[5]
7	IO_L312P_Y	N1[4]
7	IO_L313N_Y	P4
7	IO_L313P_Y	R10
7	IO_L314N_YY	P8
7	IO_L314P_YY	N2
7	IO_L315N_YY	P6[5]
7	IO_L315P_YY	P7[4]
7	IO_L316N_Y	M1
7	IO_VREF_L316P_Y	N4
7	IO_L317N_Y	N6
7	IO_L317P_Y	N3
7	IO_L318N	P9
7	IO_L318P	M2
7	IO_L319N_Y	N7
7	IO_L319P_Y	M3
7	IO_L320N_Y	P10
7	IO_L320P_Y	M4
7	IO_L321N_Y	L1
7	IO_L321P_Y	N8
7	IO_L322N_YY	L2
7	IO_L322P_YY	N9
7	IO_L323N_YY	M7
7	IO_VREF_L323P_YY	K1
7	IO_L324N_Y	M8

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
153	3	AD31	AF33	3200 2600 2000 1600 1000	VREF
154	3	AC28	AF31	3200 2600 1600 1000	-
155	3	AC27	AF32	3200 2600 1600	-
156	3	AE29	AD28	2600 1000	VREF
157	3	AD30	AG32	3200 2600 2000 1600 1000	-
158	3	AC26	AH33	2000 1600	-
159	3	AD26	AF30	3200 2600 2000 1600 1000	VREF
160	3	AC25	AH32	2600 2000 1000	-
161	3	AE28	AL34	3200 2600 2000	-
162	3	AG30	AD27	3200 2600 1600 1000	-
163	3	AF29	AK34	3200 2600 2000 1600 1000	-
164	3	AD25	AE27	3200 2600 2000 1600	-
165	3	AJ33	AH31	2600 2000 1000	VREF
166	3	AE26	AL33	3200 2600 1600 1000	-
167	3	AF28	AL32	2600 1600	-
168	3	AJ31	AF27	3200 2600 1600 1000	VREF
169	3	AG29	AJ32	2600 2000 1000	-
170	3	AK33	AH30	3200 2600 2000	-
171	3	AK32	AK31	3200 2600 2000 1600 1000	INIT

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
172	4	AP31	AK29	3200 2600 2000 1600 1000	-
173	4	AP30	AN31	3200 1600 1000	-
174	4	AH27	AN30	3200 2000 1000	-
175	4	AM30	AK28	3200 2000 1000	VREF
176	4	AG26	AN29	3200 2600 1000	-
177	4	AF25	AM29	3200 2600 2000 1600 1000	-
178	4	AL29	AL28	3200 2600 2000 1600 1000	VREF
179	4	AE24	AN28	2000 1600	-
180	4	AJ27	AH26	3200 1000	-
181	4	AG25	AK27	3200 1000	-
182	4	AM28	AF24	3200 2600	-
183	4	AJ26	AP27	3200 2600 2000 1600 1000	-
184	4	AK26	AN27	3200 2600 2000 1600 1000	VREF
185	4	AE23	AM27	3200 1600	-
186	4	AL26	AP26	3200 2000 1000	-
187	4	AN26	AJ25	3200 2000 1000	VREF
188	4	AG24	AP25	3200 2600	-
189	4	AF23	AM26	3200 2600 2000 1600 1000	-
190	4	AJ24	AN25	3200 2600 2000 1600 1000	VREF
191	4	AE22	AM25	2600 1600 1000	-

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
231	5	AH14	AP12	3200 2600 2000 1600 1000	-
232	5	AJ14	AL14	3200 2600 1000	-
233	5	AF13	AN12	3200 2000 1000	-
234	5	AF14	AP11	3200 2000 1000	-
235	5	AN11	AH13	3200 1600 1000	-
236	5	AM12	AL12	3200 2600 2000 1600 1000	-
237	5	AJ13	AP10	3200 2600 2000 1600 1000	VREF
238	5	AK12	AM10	2600 1600 1000	-
239	5	AP9	AK11	2600 1600 1000	-
240	5	AL11	AL10	3200 2600 2000 1600 1000	VREF
241	5	AE13	AM9	3200 2600 2000 1600 1000	-
242	5	AF12	AP8	3200 2600	-
243	5	AL9	AH11	3200 2000 1000	VREF
244	5	AF11	AN8	3200 2000 1000	-
245	5	AM8	AG11	3200 1600	-
246	5	AL8	AK9	3200 2600 2000 1600 1000	VREF
247	5	AH10	AN7	3200 2600 2000 1600 1000	-
248	5	AE12	AJ9	3200 2600	-
249	5	AM7	AL7	3200 1000	-
250	5	AG10	AN6	3200 1000	-

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
251	5	AK8	AH9	2000 1600	-
252	5	AP5	AJ8	3200 2600 2000 1600 1000	VREF
253	5	AE11	AN5	3200 2600 2000 1600 1000	-
254	5	AF10	AM6	3200 2600 1000	-
255	5	AL6	AG9	3200 2000 1000	VREF
256	5	AH8	AP4	3200 2000 1000	-
257	5	AN4	AJ7	3200 1600 1000	-
258	5	AM5	AK6	3200 2600 2000 1600 1000	-
259	6	AF8	AH6	3200 2600 2000 1600 1000	-
260	6	AK3	AE9	3200 2600 2000	-
261	6	AL2	AD10	2600 2000 1000	-
262	6	AH4	AL1	3200 2600 1600 1000	VREF
263	6	AK1	AG6	2600 1600	-
264	6	AK2	AF7	3200 2600 1600 1000	-
265	6	AG5	AJ3	2600 2000 1000	VREF
266	6	AJ2	AD9	3200 2600 2000 1600	-
267	6	AH2	AC10	3200 2600 2000 1600 1000	-
268	6	AF5	AH3	3200 2600 1600 1000	-
269	6	AG3	AE8	3200 2600 2000	-