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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	384
Number of Logic Elements/Cells	1728
Total RAM Bits	65536
Number of I/O	176
Number of Gates	71693
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv50e-6fg256c

Initialization in Verilog and Synopsys

The block SelectRAM+ structures can be initialized in Verilog for both simulation and synthesis for inclusion in the EDIF output file. The simulation of the Verilog code uses a defparam to pass the initialization. The Synopsys FPGA compiler does not presently support defparam. The initialization values instead attach as attributes to the RAM by a built-in Synopsys dc_script. The translate_off statement stops synthesis translation of the defparam statements. The following code illustrates a module that employs these techniques.

Design Examples

Creating a 32-bit Single-Port RAM

The true dual-read/write port functionality of the block SelectRAM+ memory allows a single port, 128 deep by 32-bit wide RAM to be created using a single block SelectRAM+ cell as shown in Figure 35.

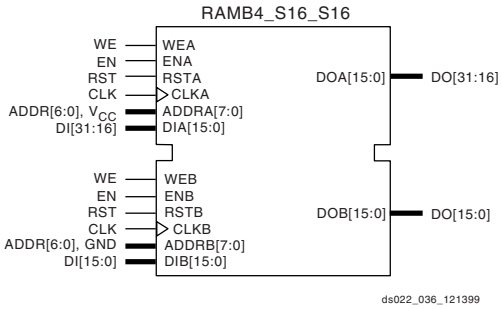


Figure 35: **Single Port 128 x 32 RAM**

Interleaving the memory space, setting the LSB of the address bus of Port A to 1 (V_{CC}), and the LSB of the address bus of Port B to 0 (GND), allows a 32-bit wide single port RAM to be created.

Creating Two Single-Port RAMs

The true dual-read/write port functionality of the block SelectRAM+ memory allows a single RAM to be split into two single port memories of 2K bits each as shown in Figure 36.

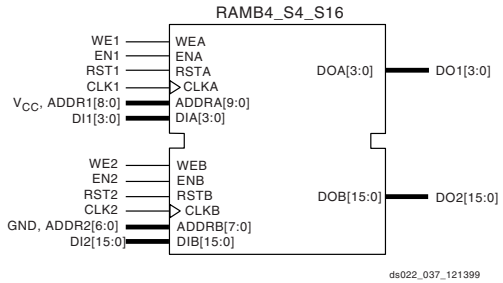


Figure 36: **512 x 4 RAM and 128 x 16 RAM**

In this example, a 512K x 4 RAM (Port A) and a 128 x 16 RAM (Port B) are created out of a single block SelectRAM+. The address space for the RAM is split by fixing the MSB of Port A to 1 (V_{CC}) for the upper 2K bits and the MSB of Port B to 0 (GND) for the lower 2K bits.

Block Memory Generation

The CoreGen program generates memory structures using the block SelectRAM+ features. This program outputs VHDL or Verilog simulation code templates and an EDIF file for inclusion in a design.

Virtex-E Electrical Characteristics

Definition of Terms

Electrical and switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance: These speed files are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These speed files are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production: These speed files are released once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. Contact the factory for design considerations requiring more detailed information.

Table 1 correlates the current status of each Virtex-E device with a corresponding speed file designation.

Table 1: **Virtex-E Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XCV50E			–8, –7, –6
XCV100E			–8, –7, –6
XCV200E			–8, –7, –6
XCV300E			–8, –7, –6
XCV400E			–8, –7, –6
XCV600E			–8, –7, –6
XCV1000E			–8, –7, –6
XCV1600E			–8, –7, –6
XCV2000E			–8, –7, –6
XCV2600E			–8, –7, –6
XCV3200E			–8, –7, –6

All specifications are subject to change without notice.

DC Characteristics

Absolute Maximum Ratings

Symbol	Description[1]			Units
V_{CCINT}	Internal Supply voltage relative to GND		–0.5 to 2.0	V
V_{CCO}	Supply voltage relative to GND		–0.5 to 4.0	V
V_{REF}	Input Reference Voltage		–0.5 to 4.0	V
V_{IN} [3]	Input voltage relative to GND		–0.5 to V_{CCO} +0.5	V
V_{TS}	Voltage applied to 3-state output		–0.5 to 4.0	V
V_{CC}	Longest Supply Voltage Rise Time from 0 V - 1.71 V		50	ms
T_{STG}	Storage temperature (ambient)		–65 to +150	°C
T_J	Junction temperature [2]	Plastic packages	+125	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time can affect device reliability.
2. For soldering guidelines and thermal considerations, see the device packaging information on www.xilinx.com.
3. Inputs configured as PCI are fully PCI compliant. This statement takes precedence over any specification that would imply that the device is not PCI compliant.

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CCINT}	Internal Supply voltage relative to GND, T_J = 0 °C to +85 °C	Commercial	1.8 – 5%	1.8 + 5%	V
	Internal Supply voltage relative to GND, T_J = –40 °C to +100 °C	Industrial	1.8 – 5%	1.8 + 5%	V
V_{CCO}	Supply voltage relative to GND, T_J = 0 °C to +85 °C	Commercial	1.2	3.6	V
	Supply voltage relative to GND, T_J = –40 °C to +100 °C	Industrial	1.2	3.6	V
T_{IN}	Input signal transition time			250	ns

Calculation of T_{ioop} as a Function of Capacitance

T_{ioop} is the propagation delay from the O Input of the IOB to the pad. The values for T_{ioop} are based on the standard capacitive load (C_{sl}) for each I/O standard as listed in Table 3.

Table 3: **Constants for Use in Calculation of T_{ioop}**

Standard	Csl (pF)	fl (ns/pF)
LVTTL Fast Slew Rate, 2mA drive	35	0.41
LVTTL Fast Slew Rate, 4mA drive	35	0.20
LVTTL Fast Slew Rate, 6mA drive	35	0.13
LVTTL Fast Slew Rate, 8mA drive	35	0.079
LVTTL Fast Slew Rate, 12mA drive	35	0.044
LVTTL Fast Slew Rate, 16mA drive	35	0.043
LVTTL Fast Slew Rate, 24mA drive	35	0.033
LVTTL Slow Slew Rate, 2mA drive	35	0.41
LVTTL Slow Slew Rate, 4mA drive	35	0.20
LVTTL Slow Slew Rate, 6mA drive	35	0.10
LVTTL Slow Slew Rate, 8mA drive	35	0.086
LVTTL Slow Slew Rate, 12mA drive	35	0.058
LVTTL Slow Slew Rate, 16mA drive	35	0.050
LVTTL Slow Slew Rate, 24mA drive	35	0.048
LVCMOS2	35	0.041
LVCMOS18	35	0.050
PCI 33 MHZ 3.3 V	10	0.050
PCI 66 MHz 3.3 V	10	0.033
GTL	0	0.014
GTL+	0	0.017
HSTL Class I	20	0.022
HSTL Class III	20	0.016
HSTL Class IV	20	0.014
SSTL2 Class I	30	0.028
SSTL2 Class II	30	0.016
SSTL3 Class I	30	0.029
SSTL3 Class II	30	0.016
CTT	20	0.035
AGP	10	0.037

Notes:
1. I/O parameter measurements are made with the capacitance values shown above. See the application examples (in Module 2 of this data sheet) for appropriate terminations.
2. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

For other capacitive loads, use the formulas below to calculate the corresponding T_{ioop}:

$$T_{ioop} = T_{ioop} + T_{opadjust} + (C_{load} - C_{sl}) * fl$$

where:

$T_{opadjust}$ is reported above in the Output Delay Adjustment section.

C_{load} is the capacitive load for the design.

Table 4: **Delay Measurement Methodology**

Standard	V_L[1]	V_H[1]	Meas. Point	V_{REF} (Typ)[2]
LVTTL	0	3	1.4	-
LVCMOS2	0	2.5	1.125	-
PCI33_3	Per PCI Spec			-
PCI66_3	Per PCI Spec			-
GTL	V_{REF} –0.2	V_{REF} +0.2	V_{REF}	0.80
GTL+	V_{REF} –0.2	V_{REF} +0.2	V_{REF}	1.0
HSTL Class I	V_{REF} –0.5	V_{REF} +0.5	V_{REF}	0.75
HSTL Class III	V_{REF} –0.5	V_{REF} +0.5	V_{REF}	0.90
HSTL Class IV	V_{REF} –0.5	V_{REF} +0.5	V_{REF}	0.90
SSTL3 I & II	V_{REF} –1.0	V_{REF} +1.0	V_{REF}	1.5
SSTL2 I & II	V_{REF} –0.75	V_{REF} +0.75	V_{REF}	1.25
CTT	V_{REF} –0.2	V_{REF} +0.2	V_{REF}	1.5
AGP	V_{REF} – (0.2xV_{CCO})	V_{REF} + (0.2xV_{CCO})	V_{REF}	Per AGP Spec
LVDS	1.2 –0.125	1.2 + 0.125	1.2	
LVPECL	1.6 –0.3	1.6 + 0.3	1.6	

Notes:
1. Input waveform switches between V_L and V_H.
2. Measurements are made at V_{REF} (Typ), Maximum, and Minimum. Worst-case values are reported.

   I/O parameter measurements are made with the capacitance values shown in Table 3. See the application examples (in Module 2 of this data sheet) for appropriate terminations.

   I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

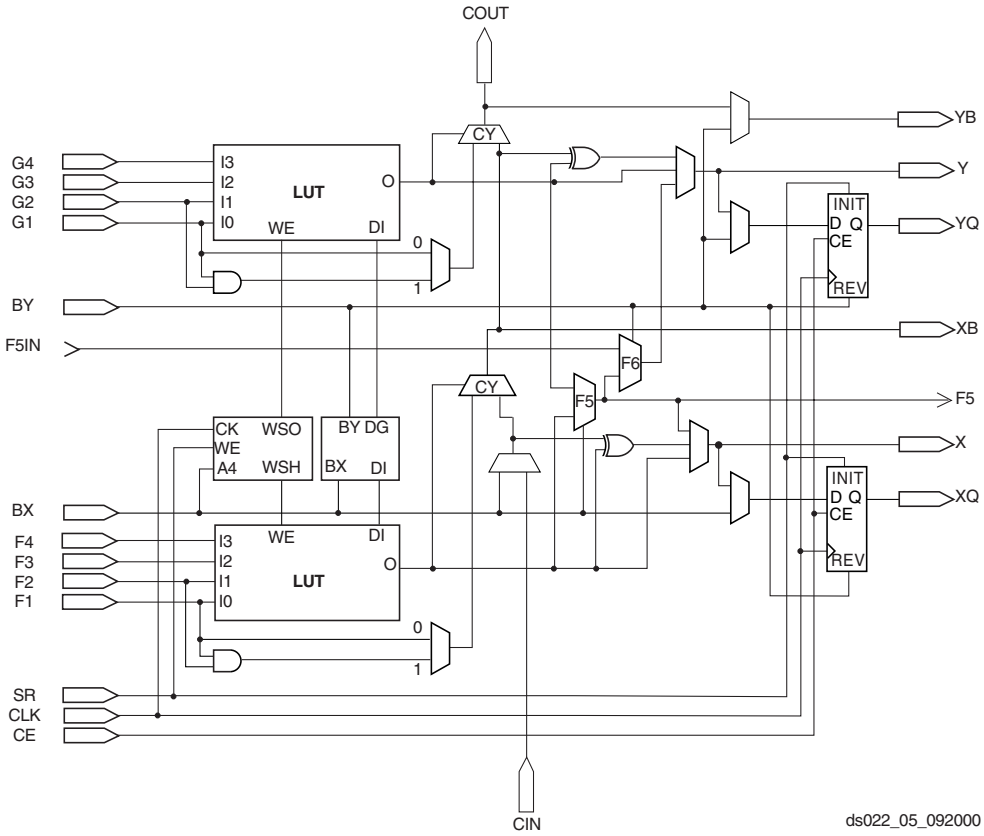


Figure 2: **Detailed View of Virtex-E Slice**

Virtex-E Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted

Global Clock Set-Up and Hold for LVTTL Standard, *with* DLL

Description[1]	Symbol	Device	Speed Grade[2, 3]				Units
			Min	-8	-7	-6	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in **IOB Input Switching Characteristics Standard Adjustments**, page 8.							
No Delay	T_{PSDLL}/T_{PHDLL}	XCV50E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns
Global Clock and IFF, with DLL		XCV100E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns
		XCV200E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns
		XCV300E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns
		XCV400E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns
		XCV600E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns
		XCV1000E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns
		XCV1600E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns
		XCV2000E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns
		XCV2600E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns
		XCV3200E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns

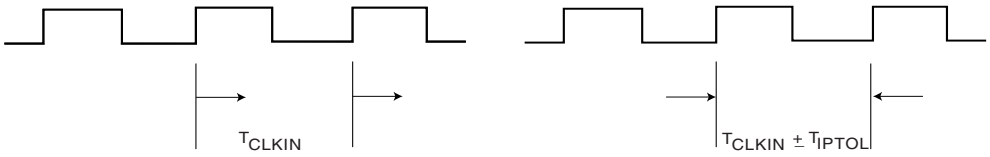
Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. DLL output jitter is already included in the timing calculation.

DLL Timing Parameters

All devices are 100 percent functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

Description	Symbol	F_{CLKIN}	Speed Grade						Units
			-8		-7		-6		
			Min	Max	Min	Max	Min	Max	
Input Clock Frequency (CLKDLLHF)	FCLKINHF		60	350	60	320	60	275	MHz
Input Clock Frequency (CLKDLL)	FCLKINLF		25	160	25	160	25	135	MHz
Input Clock Low/High Pulse Width	T_{DLLPW}	≥2□5 MHz	5.0		5.0		5.0		ns
		≥□50 MHz	3.0		3.0		3.0		ns
		≥100 MHz	2.4		2.4		2.4		ns
		≥□150 MHz	2.0		2.0		2.0		ns
		≥□200 MHz	1.8		1.8		1.8		ns
		≥□250 MHz	1.5		1.5		1.5		ns
		≥□300 MHz	1.3		1.3		NA		ns

Period Tolerance: the allowed input clock period change in nanoseconds.



Output Jitter: the difference between an ideal reference clock edge and the actual design.

Phase Offset and Maximum Phase Difference

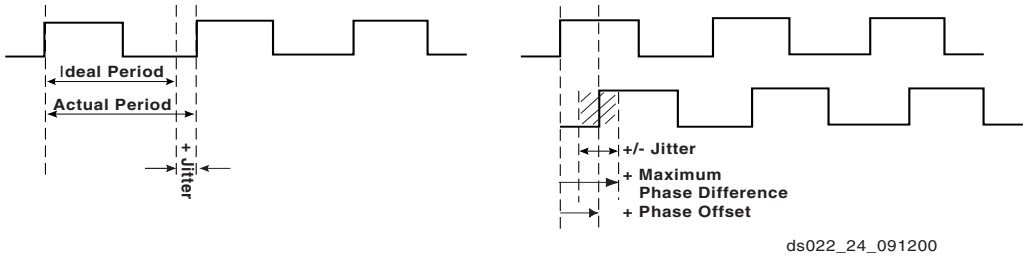


Figure 4: **DLL Timing Waveforms**

PQ240 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 7: **PQ240 Differential Pin Pair Summary XCV50E, XCV100E, XCV200E, XCV300E, XCV400E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	P92	P93	NA	IO_DLL_L40P
1	5	P89	P87	NA	IO_DLL_L40N
2	1	P210	P209	NA	IO_DLL_L6P
3	0	P213	P215	NA	IO_DLL_L6N
IO LVDS Total Pairs: 64, Asynchronous Outputs Pairs: 27					
0	0	P236	P237	1	VREF
1	0	P234	P235	√	-
2	0	P228	P229	√	VREF
3	0	P223	P224	√	-
4	0	P220	P221	3	-
5	0	P217	P218	3	VREF
6	1	P209	P215	NA	IO_LVDS_DLL
7	1	P205	P206	3	VREF
8	1	P202	P203	3	-
9	1	P199	P200	√	-
10	1	P194	P195	√	VREF
11	1	P191	P192	√	VREF
12	1	P188	P189	√	-
13	1	P186	P187	1	VREF
14	1	P184	P185	√	CS
15	2	P178	P177	√	DIN, D0
16	2	P174	P173	2	-
17	2	P171	P170	3	VREF
18	2	P168	P167	4	D1, VREF
19	2	P163	P162	√	D2
20	2	P160	P159	2	-
21	2	P157	P156	4	D3, VREF
22	2	P155	P154	5	VREF
23	2	P153	P152	√	-
24	3	P145	P144	4	D4, VREF
25	3	P142	P141	2	-
26	3	P139	P138	√	D5
27	3	P134	P133	4	VREF
28	3	P131	P130	3	VREF
29	3	P128	P127	2	-
30	3	P126	P125	6	VREF
31	3	P124	P123	√	INIT
32	4	P118	P117	√	-
33	4	P114	P113	√	-
34	4	P111	P110	√	VREF
35	4	P108	P107	√	VREF
36	4	P103	P102	√	-
37	4	P100	P99	3	-
38	4	P97	P96	3	VREF
39	4	P95	P94	7	VREF
40	5	P93	P87	NA	IO_LVDS_DLL
41	5	P84	P82	8	VREF
42	5	P79	P78	√	-
43	5	P74	P73	√	VREF
44	5	P71	P70	√	VREF
45	5	P68	P67	√	-
46	5	P66	P65	1	VREF
47	5	P64	P63	√	-

Table 12: **BG432 — XCV300E, XCV400E, XCV600E**

Bank	Pin Description	Pin #
6	VCCO	AL31
7	VCCO	A31
7	VCCO	L28
7	VCCO	L31
NA	GND	A2
NA	GND	A3
NA	GND	A7
NA	GND	A9
NA	GND	A14
NA	GND	A18
NA	GND	A23
NA	GND	A25
NA	GND	A29
NA	GND	A30
NA	GND	B1
NA	GND	B2
NA	GND	B30
NA	GND	B31
NA	GND	C1
NA	GND	C31
NA	GND	D16
NA	GND	G1
NA	GND	G31
NA	GND	J1
NA	GND	J31
NA	GND	P1
NA	GND	P31
NA	GND	T4
NA	GND	T28
NA	GND	V1
NA	GND	V31
NA	GND	AC1
NA	GND	AC31
NA	GND	AE1
NA	GND	AE31

Table 12: **BG432 — XCV300E, XCV400E, XCV600E**

Bank	Pin Description	Pin #
NA	GND	AH16
NA	GND	AJ1
NA	GND	AJ31
NA	GND	AK1
NA	GND	AK2
NA	GND	AK30
NA	GND	AK31
NA	GND	AL2
NA	GND	AL3
NA	GND	AL7
NA	GND	AL9
NA	GND	AL14
NA	GND	AL18
NA	GND	AL23
NA	GND	AL25
NA	GND	AL29
NA	GND	AL30

Notes:

1. V_{REF} or I/O option only in the XCV600E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV400E, XCV600E; otherwise, I/O option only.

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
1	IO_L23P_Y	A17
1	IO_L24N_YY	B17
1	IO_VREF_L24P_YY	A18
1	IO_L25N_YY	D16
1	IO_L25P_YY	C17
1	IO_L26N_YY	B18
1	IO_VREF_L26P_YY	A19
1	IO_L27N_YY	D17
1	IO_L27P_YY	C18
1	IO_WRITE_L28N_YY	A20
1	IO_CS_L28P_YY	C19
2	IO	D18[1]
2	IO	E19[1]
2	IO	E20
2	IO	F20
2	IO	G21
2	IO	G22[1]
2	IO	J22
2	IO	L19[1]
2	IO_D3	K20
2	IO_DOUT_BUSY_L29P_YY	C21
2	IO_DIN_D0_L29N_YY	D20
2	IO_L30P_YY	C22
2	IO_L30N_YY	D21
2	IO_VREF_L31P_YY	D22
2	IO_L31N_YY	E21
2	IO_L32P_YY	E22
2	IO_L32N_YY	F18
2	IO_VREF_L33P_YY	F21
2	IO_L33N_YY	F19
2	IO_L34P_Y	F22
2	IO_L34N_Y	G19
2	IO_L35P_Y	G20
2	IO_L35N_Y	G18
2	IO_VREF_L36P_Y	H18
2	IO_D1_L36N_Y	H22

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
2	IO_D2_L37P_YY	H20
2	IO_L37N_YY	H19
2	IO_L38P_YY	H21
2	IO_L38N_YY	J19
2	IO_L39P_YY	J18
2	IO_L39N_YY	J20
2	IO_L40P_Y	K18
2	IO_L40N_Y	J21
2	IO_L41P	K22
2	IO_VREF_L41N	K21
2	IO_L42P_Y	K19
2	IO_L42N_Y	L22
2	IO_L43P_YY	L21
2	IO_L43N_YY	L18
2	IO_L44P_YY	L17
2	IO_L44N_YY	L20
3	IO	M21[1]
3	IO	P22
3	IO	R20[1]
3	IO	R22
3	IO	T19
3	IO	U18[1]
3	IO	V20
3	IO	V21
3	IO	Y22[1]
3	IO_L45P_YY	M18
3	IO_L45N_YY	M20
3	IO_L46P_Y	M19
3	IO_L46N_Y	M17
3	IO_D4_L47P_Y	N22
3	IO_VREF_L47N_Y	N21
3	IO_L48P_YY	N20
3	IO_L48N_YY	N18
3	IO_L49P_YY	N19
3	IO_L49N_YY	P21
3	IO_L50P_YY	P20

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
7	IO	J1
7	IO	J4
7	IO	L2[1]
7	IO_L104N_YY	L3
7	IO_L104P_YY	L4
7	IO_L105N_YY	L5
7	IO_L105P_YY	L1
7	IO_L106N_Y	L6
7	IO_L106P_Y	K2
7	IO_L107N_Y	K4
7	IO_VREF_L107P_Y	K3
7	IO_L108N_YY	K1
7	IO_L108P_YY	K5
7	IO_L109N_YY	J3
7	IO_L109P_YY	J2
7	IO_L110N_YY	J5
7	IO_L110P_YY	H1
7	IO_L111N_YY	H2
7	IO_L111P_YY	H3
7	IO_L112N_Y	G1
7	IO_VREF_L112P_Y	H4
7	IO_L113N_Y	F1
7	IO_L113P_Y	F2
7	IO_L114N_YY	H5
7	IO_L114P_YY	G3
7	IO_L115N_YY	E1
7	IO_VREF_L115P_YY	E2
7	IO_L116N_YY	F3
7	IO_L116P_YY	G5
7	IO_L117N_YY	E3
7	IO_VREF_L117P_YY	D2
7	IO_L118N_YY	F5
7	IO_L118P_YY	C1
2	CCLK	B22
3	DONE	Y19
NA	DXN	Y5

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
NA	DXP	V6
NA	M0	AB2
NA	M1	U5
NA	M2	Y4
NA	PROGRAM	W20
NA	TCK	C4
NA	TDI	B20
2	TDO	A21
NA	TMS	D3
NA	NC	W19
NA	NC	W4
NA	NC	D19
NA	NC	D4
NA	VCCINT	E5
NA	VCCINT	E18
NA	VCCINT	F6
NA	VCCINT	F17
NA	VCCINT	G7
NA	VCCINT	G8
NA	VCCINT	G9
NA	VCCINT	G14
NA	VCCINT	G15
NA	VCCINT	H7
NA	VCCINT	G16
NA	VCCINT	H16
NA	VCCINT	J7
NA	VCCINT	J16
NA	VCCINT	P7
NA	VCCINT	P16
NA	VCCINT	R7
NA	VCCINT	R16
NA	VCCINT	T7
NA	VCCINT	T8
NA	VCCINT	T9
NA	VCCINT	T14

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
0	IO_L9N	A7
0	IO_L9P	D9
0	IO_L10N	B8
0	IO_VREF_L10P	G10
0	IO_L11N_YY	C9
0	IO_L11P_YY	F10
0	IO_L12N_Y	A8
0	IO_L12P_Y	E10
0	IO_L13N_YY	G11
0	IO_L13P_YY	D10
0	IO_L14N_YY	B10
0	IO_L14P_YY	F11
0	IO_L15N	C10
0	IO_L15P	E11
0	IO_L16N_YY	G12
0	IO_L16P_YY	D11
0	IO_VREF_L17N_YY	C11
0	IO_L17P_YY	F12
0	IO_L18N_YY	A11
0	IO_L18P_YY	E12
0	IO_L19N_Y	D12
0	IO_L19P_Y	C12
0	IO_VREF_L20N_Y	A12
0	IO_L20P_Y	H13
0	IO_LVDS_DLL_L21N	B13
1	GCK2	C13
1	IO	A13[1]
1	IO	A16[1]
1	IO	A19
1	IO	A20
1	IO	A22
1	IO	A24[1]
1	IO	B15[1]
1	IO	B17[1]
1	IO	B23
1	IO_LVDS_DLL_L21P	F14

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
1	IO_L22N	E14
1	IO_L22P	F13
1	IO_L23N_Y	D14
1	IO_VREF_L23P_Y	A14
1	IO_L24N_Y	C14
1	IO_L24P_Y	H14
1	IO_L25N_YY	G14
1	IO_L25P_YY	C15
1	IO_L26N_YY	E15
1	IO_VREF_L26P_YY	D15
1	IO_L27N_YY	C16
1	IO_L27P_YY	F15
1	IO_L28N	G15
1	IO_L28P	D16
1	IO_L29N_YY	E16
1	IO_L29P_YY	A17
1	IO_L30N_YY	C17
1	IO_L30P_YY	E17
1	IO_L31N_Y	F16
1	IO_L31P_Y	D17
1	IO_L32N_YY	F17
1	IO_L32P_YY	C18
1	IO_L33N_YY	A18
1	IO_VREF_L33P_YY	G16
1	IO_L34N_YY	C19
1	IO_L34P_YY	G17
1	IO_L35N_Y	D18
1	IO_VREF_L35P_Y	B19[2]
1	IO_L36N_Y	D19
1	IO_L36P_Y	E18
1	IO_L37N_YY	F18
1	IO_L37P_YY	B20
1	IO_L38N_YY	G19
1	IO_VREF_L38P_YY	C20
1	IO_L39N_YY	G18
1	IO_L39P_YY	E19
1	IO_L40N_YY	A21

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
4	IO_L98N_YY	AB19
4	IO_L99P_YY	AC20
4	IO_L99N_YY	AA18
4	IO_L100P_Y	AC19
4	IO_L100N_Y	AD20
4	IO_VREF_L101P_Y	AF20[2]
4	IO_L101N_Y	AB18
4	IO_L102P	AD19
4	IO_L102N	Y17
4	IO_L103P	AE19
4	IO_VREF_L103N	AD18
4	IO_L104P_YY	AF19
4	IO_L104N_YY	AA17
4	IO_L105P_Y	AC17
4	IO_L105N_Y	AB17
4	IO_L106P_YY	Y16
4	IO_L106N_YY	AE17
4	IO_L107P_YY	AF17
4	IO_L107N_YY	AA16
4	IO_L108P	AD17
4	IO_L108N	AB16
4	IO_L109P_YY	AC16
4	IO_L109N_YY	AD16
4	IO_VREF_L110P_YY	AC15
4	IO_L110N_YY	Y15
4	IO_L111P_YY	AD15
4	IO_L111N_YY	AA15
4	IO_L112P_Y	W14
4	IO_L112N_Y	AB15
4	IO_VREF_L113P_Y	AF15
4	IO_L113N_Y	Y14
4	IO_L114P	AD14
4	IO_L114N	AB14
4	IO_LVDS_DLL_L115P	AC14
5	GCK1	AB13
5	IO	Y13[1]

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
5	IO	AD7
5	IO	AD13
5	IO	AE4
5	IO	AE7
5	IO	AE12[1]
5	IO	AF3[1]
5	IO	AF5
5	IO	AF10[1]
5	IO	AF11[1]
5	IO_LVDS_DLL_L115N	AF13
5	IO_L116P_Y	AA13
5	IO_VREF_L116N_Y	AF12
5	IO_L117P_Y	AC13
5	IO_L117N_Y	W13
5	IO_L118P_YY	AA12
5	IO_L118N_YY	AD12
5	IO_L119P_YY	AC12
5	IO_VREF_L119N_YY	AB12
5	IO_L120P_YY	AD11
5	IO_L120N_YY	Y12
5	IO_L121P	AB11
5	IO_L121N	AD10
5	IO_L122P_YY	AC11
5	IO_L122N_YY	AE10
5	IO_L123P_YY	AC10
5	IO_L123N_YY	AA11
5	IO_L124P_Y	Y11
5	IO_L124N_Y	AD9
5	IO_L125P_YY	AB10
5	IO_L125N_YY	AF9
5	IO_L126P_YY	AD8
5	IO_VREF_L126N_YY	AA10
5	IO_L127P_YY	AE8
5	IO_L127N_YY	Y10
5	IO_L128P_Y	AC9
5	IO_VREF_L128N_Y	AF8[2]
5	IO_L129P_Y	AF7

Table 23: **FG680 Differential Pin Pair Summary**
XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
188	6	AP39	AP38	4	-
189	6	AN38	AN36	6	VREF
190	6	AN39	AN37	√	-
191	6	AM38	AM36	4	-
192	6	AL36	AM37	6	-
193	6	AL37	AM39	√	VREF
194	6	AK36	AL38	√	-
195	6	AK37	AL39	7	VREF
196	6	AJ36	AK38	4	-
197	6	AJ37	AK39	√	VREF
198	6	AH37	AJ38	√	-
199	6	AH38	AJ39	4	-
200	6	AG38	AH39	√	VREF
201	6	AG39	AG36	√	-
202	6	AF39	AG37	6	-
203	6	AE38	AF36	4	-
204	6	AF38	AF37	4	-
205	6	AE36	AE39	6	VREF
206	6	AE37	AD38	√	-
207	6	AD36	AD39	4	-
208	6	AC39	AC38	6	-
209	6	AB38	AD37	√	VREF
210	6	AB39	AC35	√	-
211	6	AA38	AC36	7	-
212	6	AA39	AC37	4	-
213	6	Y38	AB35	√	VREF
214	6	Y39	AB36	√	-
215	6	AA36	AB37	4	VREF
216	7	W38	AA37	√	-
217	7	V39	W37	4	VREF
218	7	U39	W36	√	-
219	7	U38	V38	√	VREF
220	7	T39	V37	4	-
221	7	T38	V36	7	-

Table 23: **FG680 Differential Pin Pair Summary**
XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
222	7	R39	V35	√	-
223	7	U36	U37	√	VREF
224	7	U35	R38	6	-
225	7	T37	P39	4	-
226	7	T36	P38	√	-
227	7	N38	N39	6	VREF
228	7	M39	R37	4	-
229	7	M38	R36	4	-
230	7	L39	P37	6	-
231	7	N37	P36	√	-
232	7	N36	L38	√	VREF
233	7	M37	K39	4	-
234	7	L37	K38	√	-
235	7	L36	J39	√	VREF
236	7	K37	J38	4	-
237	7	K36	H39	√	VREF
238	7	J37	H38	√	-
239	7	G38	G39	√	VREF
240	7	F39	J36	6	-
241	7	F38	H37	4	-
242	7	E39	H36	√	-
243	7	E38	G37	6	VREF
244	7	D39	G36	4	-
245	7	F36	D38	4	VREF
246	7	E37	D37	6	-

Notes:
1. AO in the XCV1000E, 1600E, 2000E.
2. AO in the XCV600E, 1000E, 1600E.
3. AO in the XCV600E, 1000E.
4. AO in the XCV1000E, 1600E.
5. AO in the XCV1000E, 2000E.
6. AO in the XCV600E, 1000E, 2000E.
7. AO in the XCV1000E.
8. AO in the XCV2000E.

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
2	IO_D1_L87N_YY	P2
2	IO_D2_L88P_YY	P3
2	IO_L88N_YY	L4
2	IO_L89P_Y	P1
2	IO_L89N_Y	R2
2	IO_L90P_Y	M5
2	IO_L90N_Y	R3
2	IO_L91P_Y	M4
2	IO_L91N_Y	R1
2	IO_L92P	N4
2	IO_L92N	T2
2	IO_L93P_Y	P5
2	IO_L93N_Y	T3
2	IO_VREF_L94P_Y	P4
2	IO_L94N_Y	T1
2	IO_L95P_YY	U2
2	IO_L95N_YY	R4
2	IO_L96P_Y	U3
2	IO_L96N_Y	T5
2	IO_L97P_Y	T4
2	IO_L97N_Y	V2
2	IO_VREF_L98P_YY	U5
2	IO_D3_L98N_YY	V3
2	IO_L99P_YY	V1
2	IO_L99N_YY	V5
2	IO_L100P_Y	W2
2	IO_L100N_Y	V4
2	IO_L101P_Y	W5
2	IO_L101N_Y	W1
2	IO_VREF_L102P_YY	Y2
2	IO_L102N_YY	W4
2	IO_L103P_YY	Y1
2	IO_L103N_YY	Y5
2	IO_VREF_L104P_Y	AA1[1]
2	IO_L104N_Y	Y4
2	IO_L105P_YY	AA4
2	IO_L105N_YY	AA2

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
3	IO	AB4
3	IO	AC2
3	IO	AD1
3	IO	AE3
3	IO	AF4
3	IO	AH5
3	IO	AJ2
3	IO	AL1
3	IO	AM3
3	IO	AP3
3	IO	AR5
3	IO	AU4
3	IO	AB2
3	IO_L106P_Y	AB3
3	IO_VREF_L106N_Y	AC4[1]
3	IO_L107P_YY	AB1
3	IO_L107N_YY	AC5
3	IO_L108P_YY	AD4
3	IO_VREF_L108N_YY	AC3
3	IO_L109P_Y	AC1
3	IO_L109N_Y	AD5
3	IO_L110P_Y	AE4
3	IO_L110N_Y	AD3
3	IO_L111P_YY	AE5
3	IO_L111N_YY	AD2
3	IO_D4_L112P_YY	AE1
3	IO_VREF_L112N_YY	AF5
3	IO_L113P_Y	AE2
3	IO_L113N_Y	AG4
3	IO_L114P_Y	AG5
3	IO_L114N_Y	AF1
3	IO_L115P_YY	AH4
3	IO_L115N_YY	AF2
3	IO_L116P_Y	AF3
3	IO_VREF_L116N_Y	AJ4
3	IO_L117P_Y	AG1

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
3	IO_L117N_Y	AJ5
3	IO_L118P	AG2
3	IO_L118N	AK4
3	IO_L119P_Y	AG3
3	IO_L119N_Y	AL4
3	IO_L120P_Y	AH1
3	IO_L120N_Y	AL5
3	IO_L121P_Y	AH2
3	IO_L121N_Y	AM4
3	IO_L122P_YY	AH3
3	IO_D5_L122N_YY	AM5
3	IO_D6_L123P_YY	AJ1
3	IO_VREF_L123N_YY	AN3
3	IO_L124P_Y	AN4
3	IO_L124N_Y	AJ3
3	IO_L125P_YY	AN5
3	IO_L125N_YY	AK1
3	IO_L126P_YY	AK2
3	IO_VREF_L126N_YY	AP4
3	IO_L127P_Y	AK3
3	IO_L127N_Y	AP5
3	IO_L128P_Y	AR3
3	IO_VREF_L128N_Y	AL2[2]
3	IO_L129P_YY	AR4
3	IO_L129N_YY	AL3
3	IO_L130P_YY	AM1
3	IO_VREF_L130N_YY	AT3
3	IO_L131P_Y	AM2
3	IO_L131N_Y	AT4
3	IO_L132P_Y	AT5
3	IO_L132N_Y	AN1
3	IO_L133P_YY	AU3
3	IO_L133N_YY	AN2
3	IO_L134P_Y	AP1
3	IO_VREF_L134N_Y	AP2
3	IO_L135P_Y	AR1
3	IO_L135N_Y	AV3

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
3	IO_L136P	AR2
3	IO_L136N	AT1
3	IO_L137P_Y	AV4
3	IO_VREF_L137N_Y	AT2
3	IO_L138P_Y	AU1
3	IO_L138N_Y	AU5
3	IO_L139P_Y	AU2
3	IO_L139N_Y	AW3
3	IO_D7_L140P_YY	AV1
3	IO_INIT_L140N_YY	AW5
4	GCK0	BA22
4	IO	AV17
4	IO	AY11
4	IO	AY12
4	IO	AY13
4	IO	AY14
4	IO	BA8
4	IO	BA17
4	IO	BA19
4	IO	BA20
4	IO	BA21
4	IO	BB9
4	IO	BB18
4	IO_L141P_YY	AV6
4	IO_L141N_YY	BA4
4	IO_L142P_Y	AY4
4	IO_L142N_Y	BA5
4	IO_L143P_Y	AW6
4	IO_L143N_Y	BB5
4	IO_VREF_L144P_Y	BA6
4	IO_L144N_Y	AY5
4	IO_L145P_Y	BB6
4	IO_L145N_Y	AY6
4	IO_L146P_YY	BA7
4	IO_L146N_YY	AV7
4	IO_VREF_L147P_YY	BB7

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
0	IO_L6P_YY	H10[5]
0	IO_L7N_Y	D7
0	IO_L7P_Y	B5
0	IO_L8N_Y	K12
0	IO_L8P_Y	E8
0	IO_L9N	B6[4]
0	IO_L9P	F9[5]
0	IO_L10N_YY	G10
0	IO_L10P_YY	C7
0	IO_VREF_L11N_YY	D8
0	IO_L11P_YY	B7
0	IO_L12N	H11[4]
0	IO_L12P	C8[5]
0	IO_L13N_Y	E9
0	IO_L13P_Y	B8
0	IO_VREF_L14N_Y	K13[2]
0	IO_L14P_Y	G11
0	IO_L15N	A8[4]
0	IO_L15P	F10[5]
0	IO_L16N_YY	C9
0	IO_L16P_YY	H12
0	IO_VREF_L17N_YY	D10
0	IO_L17P_YY	A9
0	IO_L18N_Y	F11
0	IO_L18P_Y	A10
0	IO_L19N_Y	K14
0	IO_L19P_Y	C10
0	IO_VREF_L20N_YY	H13
0	IO_L20P_YY	G12
0	IO_L21N_YY	A11
0	IO_L21P_YY	B11
0	IO_L22N_Y	E12
0	IO_L22P_Y	D11
0	IO_L23N_Y	G13

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
0	IO_L23P_Y	C12
0	IO_L24N_Y	K15
0	IO_L24P_Y	A12
0	IO_L25N_Y	B12
0	IO_L25P_Y	H14
0	IO_L26N_YY	D12
0	IO_L26P_YY	F13
0	IO_VREF_L27N_YY	A13
0	IO_L27P_YY	B13
0	IO_L28N_YY	J15[4]
0	IO_L28P_YY	G14[5]
0	IO_L29N_Y	C13
0	IO_L29P_Y	F14
0	IO_L30N_Y	H15
0	IO_L30P_Y	D13
0	IO_L31N	A14[4]
0	IO_L31P	K16[5]
0	IO_L32N_YY	E14
0	IO_L32P_YY	B14
0	IO_VREF_L33N_YY	G15
0	IO_L33P_YY	D14
0	IO_L34N	J16[4]
0	IO_L34P	D15[5]
0	IO_L35N_Y	F15
0	IO_L35P_Y	B15
0	IO_L36N_Y	A15
0	IO_L36P_Y	E15
0	IO_L37N	G16[4]
0	IO_L37P	A16[5]
0	IO_L38N_YY	F16
0	IO_L38P_YY	J17
0	IO_VREF_L39N_YY	C16
0	IO_L39P_YY	B16
0	IO_L40N_Y	H17

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
2	IO_L92N_Y	H29
2	IO_L93P_YY	J28[4]
2	IO_L93N_YY	E33[5]
2	IO_L94P_YY	H28
2	IO_L94N_YY	H30
2	IO_L95P_Y	H32
2	IO_L95N_Y	K28
2	IO_L96P_Y	L27[4]
2	IO_L96N_Y	F33[5]
2	IO_L97P_Y	M26
2	IO_L97N_Y	E34
2	IO_VREF_L98P_YY	H31
2	IO_L98N_YY	G32
2	IO_L99P_YY	N25[4]
2	IO_L99N_YY	J31[5]
2	IO_L100P_YY	J30
2	IO_L100N_YY	G33
2	IO_VREF_L101P_Y	H34[2]
2	IO_L101N_Y	J29
2	IO_L102P	M27[4]
2	IO_L102N	H33[5]
2	IO_L103P_Y	K29
2	IO_L103N_Y	J34
2	IO_VREF_L104P_YY	L29
2	IO_L104N_YY	J33
2	IO_L105P_YY	M28
2	IO_L105N_YY	K34
2	IO_L106P_Y	N27
2	IO_L106N_Y	L34
2	IO_VREF_L107P_YY	K33
2	IO_D1_L107N_YY	P26
2	IO_L108P_Y	R25
2	IO_L108N_Y	M34
2	IO_L109P_Y	L31

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
2	IO_L109N_Y	L33
2	IO_L110P_Y	P27
2	IO_L110N_Y	M33
2	IO_L111P	M31
2	IO_L111N	R26
2	IO_L112P_Y	N30
2	IO_L112N_Y	P28
2	IO_VREF_L113P_Y	N29
2	IO_L113N_Y	N33
2	IO_L114P_YY	T25[4]
2	IO_L114N_YY	N34[5]
2	IO_L115P_YY	P34
2	IO_L115N_YY	R27
2	IO_L116P_Y	P29
2	IO_L116N_Y	P31
2	IO_L117P_Y	P33[4]
2	IO_L117N_Y	T26[5]
2	IO_L118P_Y	R34
2	IO_L118N_Y	R28
2	IO_VREF_L119P_YY	N31
2	IO_D3_L119N_YY	N32
2	IO_L120P_YY	P30[4]
2	IO_L120N_YY	R33[5]
2	IO_L121P_YY	R29
2	IO_L121N_YY	T34
2	IO_L122P_Y	R30
2	IO_L122N_Y	T30
2	IO_L123P	T28[4]
2	IO_L123N	R31[5]
2	IO_L124P_Y	T29
2	IO_L124N_Y	U27
2	IO_VREF_L125P_YY	T31
2	IO_L125N_YY	T33
2	IO_L126P_YY	U28

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
4	IO_L212N_YY	AP18
4	IO_L213P_Y	AF18
4	IO_L213N_Y	AP17
4	IO_VREF_L214P_Y	AJ18[1]
4	IO_L214N_Y	AL18
4	IO_LVDS_DLL_L215P	AM18
5	GCK1	AL19
5	IO	AF17[3]
5	IO	AG12[3]
5	IO	AH12
5	IO	AJ10[3]
5	IO	AJ11[3]
5	IO	AK7[3]
5	IO	AK13[3]
5	IO	AL13[3]
5	IO	AM4[3]
5	IO	AN9
5	IO	AN10[3]
5	IO	AN16
5	IO	AN17[3]
5	IO_LVDS_DLL_L215N	AL17
5	IO_L216P_Y	AH17
5	IO_VREF_L216N_Y	AM17[1]
5	IO_L217P_Y	AJ17
5	IO_L217N_Y	AG17
5	IO_L218P_YY	AP16
5	IO_VREF_L218N_YY	AL16
5	IO_L219P_YY	AJ16
5	IO_L219N_YY	AM16
5	IO_L220P	AK16[5]
5	IO_L220N	AP15[4]
5	IO_L221P_Y	AL15
5	IO_L221N_Y	AH16

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
5	IO_L222P_Y	AN15
5	IO_L222N_Y	AF16
5	IO_L223P_Y	AP14[5]
5	IO_L223N_Y	AE16[4]
5	IO_L224P_YY	AK15
5	IO_VREF_L224N_YY	AJ15
5	IO_L225P_YY	AH15
5	IO_L225N_YY	AN14
5	IO_L226P	AK14[5]
5	IO_L226N	AG15[4]
5	IO_L227P_Y	AM13
5	IO_L227N_Y	AF15
5	IO_L228P_Y	AG14
5	IO_L228N_Y	AP13
5	IO_L229P_YY	AE14[5]
5	IO_L229N_YY	AE15[4]
5	IO_L230P_YY	AN13
5	IO_VREF_L230N_YY	AG13
5	IO_L231P_YY	AH14
5	IO_L231N_YY	AP12
5	IO_L232P_Y	AJ14
5	IO_L232N_Y	AL14
5	IO_L233P_Y	AF13
5	IO_L233N_Y	AN12
5	IO_L234P_Y	AF14
5	IO_L234N_Y	AP11
5	IO_L235P_Y	AN11
5	IO_L235N_Y	AH13
5	IO_L236P_YY	AM12
5	IO_L236N_YY	AL12
5	IO_L237P_YY	AJ13
5	IO_VREF_L237N_YY	AP10
5	IO_L238P_Y	AK12
5	IO_L238N_Y	AM10

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
270	6	AG2	AE7	2600 2000 1000	-
271	6	AG1	AF6	3200 2600 2000 1600 1000	VREF
272	6	AG4	AC9	2000 1600	-
273	6	AF3	AE6	3200 2600 2000 1600 1000	-
274	6	AF4	AF1	2600 1000	VREF
275	6	AF2	AB10	3200 2600 1600	-
276	6	AE1	AC8	3200 2600 1600 1000	-
277	6	AE3	AD5	3200 2600 2000 1600 1000	VREF
278	6	AD1	AC7	3200 2600 2000 1600 1000	-
279	6	AD2	AD6	3200 1600 1000	-
280	6	AC1	AB8	2000 1600 1000	VREF
281	6	AC2	AC5	3200 2600 2000 1600 1000	-
282	6	AC3	AA9	3200 2600 2000	-
283	6	AD4	AC4	2000 1000	-
284	6	AB6	AA8	3200 2600 1600 1000	-
285	6	Y10	AB1	2600 1600	-
286	6	AA7	AB2	3200 1600 1000	-
287	6	AA1	AA4	2600 2000 1000	VREF
288	6	AB4	Y9	3200 2600 2000 1600	-
289	6	Y8	AA2	3200 2600 2000 1600 1000	-

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
290	6	AA5	AA6	3200 2600 1600 1000	-
291	6	Y7	AB3	3200 2600 2000	-
292	6	W10	Y1	2600 2000 1000	-
293	6	Y2	Y5	2000 1600 1000	VREF
294	6	W2	W9	2000 1600	-
295	6	Y4	W7	3200 2600 2000 1600 1000	-
296	6	Y6	W1	1000	-
297	6	W3	W6	3200 1600	-
298	6	W4	V9	3200 2600 1600 1000	-
299	6	V1	W5	2000 1600 1000	VREF
300	6	U2	V7	2000 1600 1000	-
301	6	U1	V6	3200 2600 1600 1000	VREF
302	7	U4	U9	3200 2600 2000 1600 1000	-
303	7	U5	U7	3200 2600 1600 1000	VREF
304	7	U6	U3	2000 1600 1000	-
305	7	T6	T3	2000 1600 1000	VREF
306	7	T4	T9	3200 2600 1600 1000	-
307	7	R1	T5	3200 1600	-
308	7	T10	R6	1000	-
309	7	R5	R2	3200 2600 2000 1600 1000	-
310	7	P5	P1	2000 1600 1000	VREF