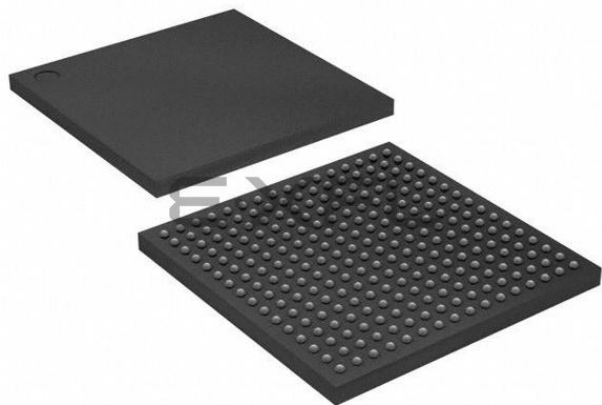




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	384
Number of Logic Elements/Cells	1728
Total RAM Bits	65536
Number of I/O	176
Number of Gates	71693
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv50e-6fg256i

DLL Properties

Properties provide access to some of the Virtex-E series DLL features, (for example, clock division and duty cycle correction).

Duty Cycle Correction Property

The 1x clock outputs, CLK0, CLK90, CLK180, and CLK270, use the duty-cycle corrected default, exhibiting a 50/50 duty cycle. The DUTY_CYCLE_CORRECTION property (by default TRUE) controls this feature. To deactivate the DLL duty-cycle correction for the 1x clock outputs, attach the DUTY_CYCLE_CORRECTION=FALSE property to the DLL symbol.

Clock Divide Property

The CLKDV_DIVIDE property specifies how the signal on the CLKDV pin is frequency divided with respect to the CLK0 pin. The values allowed for this property are 1.5, 2, 2.5, 3, 4, 5, 8, or 16; the default value is 2.

Startup Delay Property

This property, STARTUP_WAIT, takes on a value of TRUE or FALSE (the default value). When TRUE the device configuration DONE signal waits until the DLL locks before going to High.

Virtex-E DLL Location Constraints

As shown in [Figure 26](#), there are four additional DLLs in the Virtex-E devices, for a total of eight per Virtex-E device. These DLLs are located in silicon, at the top and bottom of the two innermost block SelectRAM columns. The location constraint LOC, attached to the DLL symbol with the identifier DLL0S, DLL0P, DLL1S, DLL1P, DLL2S, DLL2P, DLL3S, or DLL3P, controls the DLL location.

The LOC property uses the following form:

LOC = DLL0P

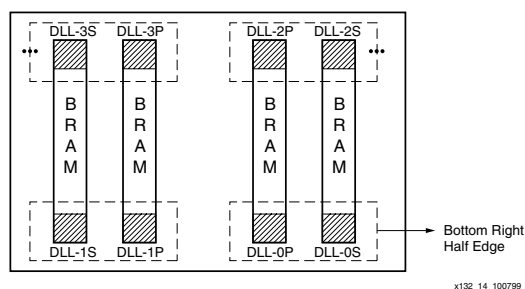


Figure 26: Virtex Series DLLs

Design Factors

Use the following design considerations to avoid pitfalls and improve success designing with Xilinx devices.

Input Clock

The output clock signal of a DLL, essentially a delayed version of the input clock signal, reflects any instability on the input clock in the output waveform. For this reason the quality of the DLL input clock relates directly to the quality of the output clock waveforms generated by the DLL. The DLL input clock requirements are specified in the data sheet.

In most systems a crystal oscillator generates the system clock. The DLL can be used with any commercially available quartz crystal oscillator. For example, most crystal oscillators produce an output waveform with a frequency tolerance of 100 PPM, meaning 0.01 percent change in the clock period. The DLL operates reliably on an input waveform with a frequency drift of up to 1 ns — orders of magnitude in excess of that needed to support any crystal oscillator in the industry. However, the cycle-to-cycle jitter must be kept to less than 300 ps in the low frequencies and 150 ps for the high frequencies.

Input Clock Changes

Changing the period of the input clock beyond the maximum drift amount requires a manual reset of the CLKDLL. Failure to reset the DLL produces an unreliable lock signal and output clock.

It is possible to stop the input clock with little impact to the DLL. Stopping the clock should be limited to less than 100 μ s to keep device cooling to a minimum. The clock should be stopped during a Low phase, and when restored the full High period should be seen. During this time, LOCKED stays High and remains High when the clock is restored.

When the clock is stopped, one to four more clocks are still observed as the delay line is flushed. When the clock is restarted, the output clocks are not observed for one to four clocks as the delay line is filled. The most common case is two or three clocks.

In a similar manner, a phase shift of the input clock is also possible. The phase shift propagates to the output one to four clocks after the original shift, with no disruption to the CLKDLL control.

Output Clocks

As mentioned earlier in the DLL pin descriptions, some restrictions apply regarding the connectivity of the output pins. The DLL clock outputs can drive an OBUF, a global clock buffer BUFG, or they can route directly to destination clock pins. The only BUFGs that the DLL clock outputs can drive are the two on the same edge of the device (top or bottom). In addition, the CLK2X output of the secondary DLL can connect directly to the CLKIN of the primary DLL in the same quadrant.

Do not use the DLL output clock signals until after activation of the LOCKED signal. Prior to the activation of the LOCKED signal, the DLL output clocks are not valid and can exhibit glitches, spikes, or other spurious movement.

Table 2: IOB Input Switching Characteristics (Continued)

			Speed Grade ⁽¹⁾				Units
Description ⁽²⁾	Symbol	Device	Min	-8	-7	-6	
Sequential Delays							
Clock CLK							
Minimum Pulse Width, High	T _{CH}	All	0.56	1.2	1.3	1.4	ns, min
Minimum Pulse Width, Low	T _{CL}		0.56	1.2	1.3	1.4	ns, min
Clock CLK to output IQ	T _{IOCKIQ}		0.18	0.4	0.7	0.7	ns, max
Setup and Hold Times with respect to Clock at IOB Input Register							
Pad, no delay	T _{IOPICK} / T _{IOICKP}	All	0.69 / 0	1.3 / 0	1.4 / 0	1.5 / 0	ns, min
Pad, with delay	T _{IOPICKD} / T _{IOICKPD}	XCV50E	1.25 / 0	2.8 / 0	2.9 / 0	2.9 / 0	ns, min
		XCV100E	1.25 / 0	2.8 / 0	2.9 / 0	2.9 / 0	ns, min
		XCV200E	1.33 / 0	3.0 / 0	3.1 / 0	3.1 / 0	ns, min
		XCV300E	1.33 / 0	3.0 / 0	3.1 / 0	3.1 / 0	ns, min
		XCV400E	1.37 / 0	3.1 / 0	3.2 / 0	3.2 / 0	ns, min
		XCV600E	1.49 / 0	3.4 / 0	3.5 / 0	3.5 / 0	ns, min
		XCV1000E	1.49 / 0	3.4 / 0	3.5 / 0	3.5 / 0	ns, min
		XCV1600E	1.53 / 0	3.5 / 0	3.6 / 0	3.6 / 0	ns, min
		XCV2000E	1.53 / 0	3.5 / 0	3.6 / 0	3.6 / 0	ns, min
		XCV2600E	1.53 / 0	3.5 / 0	3.6 / 0	3.6 / 0	ns, min
XCV3200E	1.53 / 0	3.5 / 0	3.6 / 0	3.6 / 0	ns, min		
ICE input	T _{IOICECK} / T _{IOCKICE}	All	0.28 / 0.0	0.55 / 0.01	0.7 / 0.01	0.7 / 0.01	ns, min
SR input (IFF, synchronous)	T _{IOSRCKI}	All	0.38	0.8	0.9	1.0	ns, min
Set/Reset Delays							
SR input to IQ (asynchronous)	T _{IOSRIQ}	All	0.54	1.1	1.2	1.4	ns, max
GSR to output IQ	T _{GSRQ}	All	3.88	7.6	8.5	9.7	ns, max

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. Input timing t_i for LVTTTL is measured at 1.4 V. For other I/O standards, see Table 4.

IOB Output Switching Characteristics, Figure 1

Output delays terminating at a pad are specified for LVTTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 10.

		Speed Grade ⁽¹⁾				Units
Description ⁽²⁾	Symbol	Min	-8	-7	-6	
Propagation Delays						
O input to Pad	T _{ILOOP}	1.04	2.5	2.7	2.9	ns, max
O input to Pad via transparent latch	T _{IOOLP}	1.24	2.9	3.1	3.4	ns, max
3-State Delays						
T input to Pad high-impedance (Note 2)	T _{IOTHZ}	0.73	1.5	1.7	1.9	ns, max
T input to valid data on Pad	T _{IOTON}	1.13	2.7	2.9	3.1	ns, max
T input to Pad high-impedance via transparent latch (Note 2)	T _{IOTLPHZ}	0.86	1.8	2.0	2.2	ns, max
T input to valid data on Pad via transparent latch	T _{IOTLPON}	1.26	3.0	3.2	3.4	ns, max
GTS to Pad high impedance (Note 2)	T _{GTS}	1.94	4.1	4.6	4.9	ns, max
Sequential Delays						
Clock CLK						
Minimum Pulse Width, High	T _{CH}	0.56	1.2	1.3	1.4	ns, min
Minimum Pulse Width, Low	T _{CL}	0.56	1.2	1.3	1.4	ns, min
Clock CLK to Pad	T _{IOCKP}	0.97	2.4	2.8	2.9	ns, max
Clock CLK to Pad high-impedance (synchronous) (Note 2)	T _{IOCKHZ}	0.77	1.6	2.0	2.2	ns, max
Clock CLK to valid data on Pad (synchronous)	T _{IOCKON}	1.17	2.8	3.2	3.4	ns, max
Setup and Hold Times before/after Clock CLK						
O input	T _{IOOCK} / T _{IOCKO}	0.43 / 0	0.9 / 0	1.0 / 0	1.1 / 0	ns, min
OCE input	T _{IOOCECK} / T _{IOCKOCE}	0.28 / 0	0.55 / 0.01	0.7 / 0	0.7 / 0	ns, min
SR input (OFF)	T _{IOSRCKO} / T _{IOCKOSR}	0.40 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
3-State Setup Times, T input	T _{IOTCK} / T _{IOCKT}	0.26 / 0	0.51 / 0	0.6 / 0	0.7 / 0	ns, min
3-State Setup Times, TCE input	T _{IOTCECK} / T _{IOCKTCE}	0.30 / 0	0.6 / 0	0.7 / 0	0.8 / 0	ns, min
3-State Setup Times, SR input (TFF)	T _{IOSRCKT} / T _{IOCKTSR}	0.38 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
Set/Reset Delays						
SR input to Pad (asynchronous)	T _{IOSRP}	1.30	3.1	3.3	3.5	ns, max
SR input to Pad high-impedance (asynchronous) (Note 2)	T _{IOSRHZ}	1.08	2.2	2.4	2.7	ns, max
SR input to valid data on Pad (asynchronous)	T _{IOSRON}	1.48	3.4	3.7	3.9	ns, max
GSR to Pad	T _{IOGSRQ}	3.88	7.6	8.5	9.7	ns, max

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. 3-state turn-off delays should not be adjusted.

Low Voltage Differential Signals

The Virtex-E family incorporates low-voltage signalling (LVDS and LVPECL). Two pins are utilized for these signals to be connected to a Virtex-E device. These are known as differential pin pairs. Each differential pin pair has a Positive (P) and a Negative (N) pin. These pairs are labeled in the following manner.

IO_L#[P/N]

where

L = LVDS or LVPECL pin

= Pin Pair Number

P = Positive

N = Negative

I/O pins for differential signals can either be synchronous or asynchronous, input or output. The pin pairs can be used for synchronous input and output signals as well as asynchronous input signals. However, only some of the low-voltage pairs can be used for asynchronous output signals.

Differential signals require the pins of a pair to switch almost simultaneously. If the signals driving the pins are from IOB flip-flops, they are synchronous. If the signals driving the pins are from internal logic, they are asynchronous. **Table 2** defines the names and function of the different types of low-voltage pin pairs in the Virtex-E family.

Table 2: LVDS Pin Pairs

Pin Name	Description
IO_L#[P/N] Example: IO_L22N	Represents a general IO or a synchronous input/output differential signal. When used as a differential signal, N means Negative I/O and P means Positive I/O.
IO_L#[P/N]_Y Example: IO_L22N_Y	Represents a general IO or a synchronous input/output differential signal, or a part-dependent asynchronous output differential signal.
IO_L#[P/N]_YY Example: O_L22N_YY	Represents a general IO or a synchronous input/output differential signal, or an asynchronous output differential signal.
IO_LVDS_DLL_L#[P/N] Example: IO_LVDS_DLL_L16N	Represents a general IO or a synchronous input/output differential signal, a differential clock input signal, or a DLL input. When used as a differential clock input, this pin is paired with the adjacent GCK pin. The GCK pin is always the positive input in the differential clock input configuration.

Virtex-E Package Pinouts

The Virtex-E family of FPGAs is available in 12 popular packages, including chip-scale, plastic and high heat-dissipation quad flat packs, and ball grid and fine-pitch ball grid arrays. Family members have footprint compatibility across devices provided in the same package. The pinout tables in

this section indicate function, pin, and bank information for each package/device combination. Following each pinout table is an additional table summarizing information specific to differential pin pairs for all devices provided in that package.

BG352 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A check (✓) in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock

Table 11: BG352 Differential Pin Pair Summary
XCV100E, XCV200E, XCV300E

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	AE13	AC13	NA	IO LVDS 55
1	5	AF14	AD14	NA	IO LVDS 55
2	1	B14	A13	NA	IO LVDS 9
3	0	D14	A15	NA	IO LVDS 9
IO LVDS					
Total Outputs: 87, Asynchronous Output Pairs: 43					
0	0	B23	D21	✓	VREF_0
1	0	D20	A23	✓	-
2	0	B22	C21	✓	VREF_0
3	0	A21	B20	2	-
4	0	B19	C19	✓	VREF_0
5	0	C18	D17	✓	-
6	0	A18	C17	2	-
7	0	C16	B17	✓	-
8	0	D15	A16	✓	VREF_0
9	1	A13	A15	✓	GCLK LVDS 3/2
10	1	A12	C13	2	-
11	1	C12	B12	✓	VREF_1
12	1	B11	A11	✓	-
13	1	D11	C11	2	-
14	1	C10	B9	✓	-
15	1	C9	B8	✓	VREF_1
16	1	A7	D9	1	-
17	1	B6	A6	✓	VREF_1
18	1	A4	C7	✓	-

Table 11: BG352 Differential Pin Pair Summary
XCV100E, XCV200E, XCV300E

Pair	Bank	P Pin	N Pin	AO	Other Functions
19	1	D6	C6	✓	VREF_1
20	1	C4	D5	✓	CS
21	2	E4	D3	✓	DIN_D0
22	2	D2	C1	✓	VREF_2
23	2	G4	F3	✓	-
24	2	E2	F2	✓	VREF_2
25	2	F1	J4	2	-
26	2	H2	G1	✓	D1
27	2	J3	J2	✓	D2
28	2	J1	L4	1	-
29	2	L3	L2	✓	-
30	2	M4	M3	✓	D3
31	2	M2	M1	2	-
32	2	N4	N2	✓	-
33	3	R1	R2	2	-
34	3	R3	R4	✓	VREF_3
35	3	T2	U2	✓	-
36	3	T4	V1	1	-
37	3	U3	U4	✓	D5
38	3	V3	V4	✓	VREF_3
39	3	Y1	Y2	1	-
40	3	AA2	Y3	✓	VREF_3
41	3	AC1	AB2	✓	-
42	3	AA4	AC2	✓	VREF_3
43	3	AC3	AD2	✓	INIT
44	4	AC5	AD4	✓	-
45	4	AE4	AF3	✓	VREF_4
46	4	AC7	AD6	✓	-
47	4	AE5	AE6	✓	VREF_4
48	4	AF6	AC9	2	-
49	4	AE8	AF7	✓	VREF_4
50	4	AD9	AE9	✓	-
51	4	AF9	AC11	2	-
52	4	AD11	AE11	✓	-
53	4	AC12	AD12	✓	VREF_4
54	4	AE12	AF12	2	-

Table 16: FG256 Package — XCV50E, XCV100E, XCV200E, XCV300E

Bank	Pin Description	Pin #
7	IO_L74N_Y	G4
7	IO_VREF_L74P_Y	H3
7	IO_L75N_YY	G2
7	IO_L75P_YY	F5
7	IO_L76N	F4
7	IO_L76P	F1
7	IO_L77N_YY	G3
7	IO_L77P_YY	F2
7	IO_L78N_Y	E1
7	IO_VREF_L78P_Y	D1 ¹
7	IO_L79N	E4
7	IO_L79P	E2
7	IO_L80N_Y	F3
7	IO_VREF_L80P_Y	C1
7	IO_L81N_YY	D2
7	IO_L81P_YY	E3
7	IO_VREF_L82N	B1 ²
7	IO_L82P	A2
2	CCLK	D15
3	DONE	R14
NA	DXN	R4
NA	DXP	P4
NA	M0	N3
NA	M1	P2
NA	M2	R3
NA	PROGRAM	P15
NA	TCK	C4
NA	TDI	A15
2	TDO	B14
NA	TMS	D3
NA	VCCINT	C3
NA	VCCINT	C14
NA	VCCINT	D4

Table 16: FG256 Package — XCV50E, XCV100E, XCV200E, XCV300E

Bank	Pin Description	Pin #
NA	VCCINT	D13
NA	VCCINT	E5
NA	VCCINT	E12
NA	VCCINT	M5
NA	VCCINT	M12
NA	VCCINT	N4
NA	VCCINT	N13
NA	VCCINT	P3
NA	VCCINT	P14
0	VCCO	F8
0	VCCO	E8
1	VCCO	F9
1	VCCO	E9
2	VCCO	H12
2	VCCO	H11
3	VCCO	J12
3	VCCO	J11
4	VCCO	M9
4	VCCO	L9
5	VCCO	M8
5	VCCO	L8
6	VCCO	J6
6	VCCO	J5
7	VCCO	H6
7	VCCO	H5
NA	GND	T16
NA	GND	T1
NA	GND	R15
NA	GND	R2
NA	GND	L11
NA	GND	L10
NA	GND	L7
NA	GND	L6

Table 17: FG256 Differential Pin Pair Summary
XCV50E, XCV100E, XCV200E, XCV300E

Pair	Bank	P Pin	N Pin	AO	Other Functions
19	2	C15	D14	√	DIN, D0
20	2	B16	E13	6	VREF
21	2	C16	E14	√	-
22	2	F13	E15	1	VREF
23	2	F12	D16	5	-
24	2	F14	E16	3	D1
25	2	F15	G13	√	D2
26	2	F16	G12	6	-
27	2	G15	G14	√	-
28	2	H13	G16	3	D3
29	2	J13	H15	4	-
30	2	H14	H16	√	-
31	3	K15	J14	4	-
32	3	J16	K16	3	VREF
33	3	K12	L15	√	-
34	3	K13	L16	6	-
35	3	K14	M16	√	D5
36	3	N16	L13	3	VREF
37	3	P16	L12	5	-
38	3	M15	L14	1	VREF
39	3	M14	R16	√	-
40	3	M13	T15	6	VREF
41	3	N14	N15	√	INIT
42	4	T14	P13	√	-
43	4	P12	R13	7	VREF
44	4	N12	T13	√	-
45	4	T12	P11	√	VREF
46	4	R12	N11	2	-
47	4	T11	M11	√	VREF
48	4	R11	T10	√	-
49	4	R10	M10	1	-
50	4	P9	T9	1	VREF
51	4	N10	R9	1	-
52	5	N9	T8	NA	IO_LVDS_DLL
53	5	R7	P8	1	VREF
54	5	P7	T6	1	-

Table 17: FG256 Differential Pin Pair Summary
XCV50E, XCV100E, XCV200E, XCV300E

Pair	Bank	P Pin	N Pin	AO	Other Functions
55	5	M7	R6	√	-
56	5	P6	R5	√	VREF
57	5	N6	T5	2	-
58	5	M6	T4	√	VREF
59	5	T3	P5	√	-
60	5	T2	N5	7	VREF
61	6	R1	M3	√	-
62	6	N2	M4	6	VREF
63	6	P1	L5	√	-
64	6	L3	N1	1	VREF
65	6	L4	M2	5	-
66	6	K4	M1	3	VREF
67	6	L1	L2	√	-
68	6	K1	K3	6	-
69	6	K5	K2	√	-
70	6	J1	J3	3	VREF
71	6	H1	J4	4	-
72	7	H4	G1	√	-
73	7	H2	G5	4	-
74	7	H3	G4	3	VREF
75	7	F5	G2	√	-
76	7	F1	F4	6	-
77	7	F2	G3	√	-
78	7	D1	E1	3	VREF
79	7	E2	E4	5	-
80	7	C1	F3	1	VREF
81	7	E3	D2	√	-
82	7	A2	B1	6	VREF

Notes:

1. AO in the XCV50E, 200E, 300E.
2. AO in the XCV50E, 200E.
3. AO in the XCV50E, 300E.
4. AO in the XCV100E, 200E.
5. AO in the XCV200E.
6. AO in the XCV100E.
7. AO in the XCV50E.

Table 18: FG456 — XCV200E and XCV300E

Bank	Pin Description	Pin #
NA	GND	M14
NA	GND	M13
NA	GND	M12
NA	GND	M11
NA	GND	M10
NA	GND	M9
NA	GND	L14
NA	GND	L13
NA	GND	L12
NA	GND	L11
NA	GND	L10
NA	GND	L9
NA	GND	K14
NA	GND	K13
NA	GND	K12
NA	GND	K11
NA	GND	K10
NA	GND	K9
NA	GND	J14
NA	GND	J13
NA	GND	J12
NA	GND	J11
NA	GND	J10
NA	GND	J9
NA	GND	C20
NA	GND	C3
NA	GND	B21
NA	GND	B2
NA	GND	A22
NA	GND	A1

Note 1: NC in the XCV200E device.

FG456 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 19: FG456 Differential Pin Pair Summary
XCV200E, XCV300E

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	W12	U12	NA	IO_DLL_L75P
1	5	Y11	AA11	NA	IO_DLL_L75N
2	1	A11	D11	NA	IO_DLL_L13P
3	0	C11	B11	NA	IO_DLL_L13N
IO LVDS					
Total Pairs: 119, Asynchronous Output Pairs: 69					
0	0	B3	D5	NA	-
1	0	E6	B4	√	VREF
2	0	E7	A4	NA	-
3	0	D6	C6	√	VREF
4	0	B6	A5	1	-
5	0	C7	D7	1	-
6	0	B7	E8	√	VREF
7	0	E9	A7	√	-
8	0	B8	C8	1	-
9	0	A8	D9	1	-
10	0	E10	C9	NA	-
11	0	C10	A9	√	VREF
12	0	B10	F11	2	-
13	1	D11	B11	NA	IO_LVDS_DLL
14	1	D12	C12	2	-
15	1	A13	B12	2	-
16	1	B13	E12	√	VREF
17	1	D13	C13	√	-

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
0	IO_L9N	A7
0	IO_L9P	D9
0	IO_L10N	B8
0	IO_VREF_L10P	G10
0	IO_L11N_YY	C9
0	IO_L11P_YY	F10
0	IO_L12N_Y	A8
0	IO_L12P_Y	E10
0	IO_L13N_YY	G11
0	IO_L13P_YY	D10
0	IO_L14N_YY	B10
0	IO_L14P_YY	F11
0	IO_L15N	C10
0	IO_L15P	E11
0	IO_L16N_YY	G12
0	IO_L16P_YY	D11
0	IO_VREF_L17N_YY	C11
0	IO_L17P_YY	F12
0	IO_L18N_YY	A11
0	IO_L18P_YY	E12
0	IO_L19N_Y	D12
0	IO_L19P_Y	C12
0	IO_VREF_L20N_Y	A12
0	IO_L20P_Y	H13
0	IO_LVDS_DLL_L21N	B13
1	GCK2	C13
1	IO	A13 ¹
1	IO	A16 ¹
1	IO	A19
1	IO	A20
1	IO	A22
1	IO	A24 ¹
1	IO	B15 ¹
1	IO	B17 ¹
1	IO	B23
1	IO_LVDS_DLL_L21P	F14

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
1	IO_L22N	E14
1	IO_L22P	F13
1	IO_L23N_Y	D14
1	IO_VREF_L23P_Y	A14
1	IO_L24N_Y	C14
1	IO_L24P_Y	H14
1	IO_L25N_YY	G14
1	IO_L25P_YY	C15
1	IO_L26N_YY	E15
1	IO_VREF_L26P_YY	D15
1	IO_L27N_YY	C16
1	IO_L27P_YY	F15
1	IO_L28N	G15
1	IO_L28P	D16
1	IO_L29N_YY	E16
1	IO_L29P_YY	A17
1	IO_L30N_YY	C17
1	IO_L30P_YY	E17
1	IO_L31N_Y	F16
1	IO_L31P_Y	D17
1	IO_L32N_YY	F17
1	IO_L32P_YY	C18
1	IO_L33N_YY	A18
1	IO_VREF_L33P_YY	G16
1	IO_L34N_YY	C19
1	IO_L34P_YY	G17
1	IO_L35N_Y	D18
1	IO_VREF_L35P_Y	B19 ²
1	IO_L36N_Y	D19
1	IO_L36P_Y	E18
1	IO_L37N_YY	F18
1	IO_L37P_YY	B20
1	IO_L38N_YY	G19
1	IO_VREF_L38P_YY	C20
1	IO_L39N_YY	G18
1	IO_L39P_YY	E19
1	IO_L40N_YY	A21

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
1	IO_L40P_YY	D20
1	IO_L41N_YY	F19
1	IO_VREF_L41P_YY	C21
1	IO_L42N_YY	B22
1	IO_L42P_YY	E20
1	IO_L43N_Y	A23
1	IO_L43P_Y	D21
1	IO_WRITE_L44N_YY	C22
1	IO_CS_L44P_YY	E21
2	IO	D25 ¹
2	IO	D26
2	IO	E26
2	IO	F26
2	IO	H26 ¹
2	IO	K26 ¹
2	IO	M25 ¹
2	IO	N26 ¹
2	IO_D1	K24
2	IO_DOUT_BUSY_L45P_YY	E23
2	IO_DIN_D0_L45N_YY	F22
2	IO_L46P_YY	E24
2	IO_L46N_YY	F20
2	IO_L47P_Y	G21
2	IO_L47N_Y	G22
2	IO_VREF_L48P_Y	F24
2	IO_L48N_Y	H20
2	IO_L49P_Y	E25
2	IO_L49N_Y	H21
2	IO_L50P_YY	F23
2	IO_L50N_YY	G23
2	IO_VREF_L51P_YY	H23
2	IO_L51N_YY	J20
2	IO_L52P_YY	G24
2	IO_L52N_YY	H22
2	IO_L53P_Y	J21
2	IO_L53N_Y	G25

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
2	IO_VREF_L54P_Y	G26 ²
2	IO_L54N_Y	J22
2	IO_L55P_YY	H24
2	IO_L55N_YY	J23
2	IO_L56P_YY	J24
2	IO_VREF_L56N_YY	K20
2	IO_D2_L57P_YY	K22
2	IO_L57N_YY	K21
2	IO_L58P_YY	H25
2	IO_L58N_YY	K23
2	IO_L59P_Y	L20
2	IO_L59N_Y	J26
2	IO_L60P_Y	K25
2	IO_L60N_Y	L22
2	IO_L61P_Y	L21
2	IO_L61N_Y	L23
2	IO_L62P_Y	M20
2	IO_L62N_Y	L24
2	IO_VREF_L63P_YY	M23
2	IO_D3_L63N_YY	M22
2	IO_L64P_YY	L26
2	IO_L64N_YY	M21
2	IO_L65P_Y	N19
2	IO_L65N_Y	M24
2	IO_VREF_L66P_Y	M26
2	IO_L66N_Y	N20
2	IO_L67P_YY	N24
2	IO_L67N_YY	N21
2	IO_L68P_YY	N23
2	IO_L68N_YY	N22
3	IO	P24
3	IO	P26 ¹
3	IO	R26 ¹
3	IO	T26 ¹
3	IO	U26 ¹
3	IO	W25

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
7	IO	D2
7	IO	D3
7	IO	E1
7	IO	G1
7	IO	H2
7	IO	J1 ¹
7	IO	L1 ¹
7	IO	M1 ¹
7	IO	N1 ¹
7	IO_L160N_YY	N5
7	IO_L160P_YY	N8
7	IO_L161N_YY	N6
7	IO_L161P_YY	N3
7	IO_L162N_Y	N4
7	IO_VREF_L162P_Y	M2
7	IO_L163N_Y	N7
7	IO_L163P_Y	M7
7	IO_L164N_YY	M6
7	IO_L164P_YY	M3
7	IO_L165N_YY	M4
7	IO_VREF_L165P_YY	M5
7	IO_L166N_Y	L3
7	IO_L166P_Y	L7
7	IO_L167N_Y	L6
7	IO_L167P_Y	K2
7	IO_L168N_Y	L4
7	IO_L168P_Y	K1
7	IO_L169N_Y	K3
7	IO_L169P_Y	L5
7	IO_L170N_YY	K5
7	IO_L170P_YY	J3
7	IO_L171N_YY	K4
7	IO_L171P_YY	J4
7	IO_L172N_YY	H3
7	IO_VREF_L172P_YY	K6
7	IO_L173N_YY	K7
7	IO_L173P_YY	G3

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
7	IO_L174N_Y	J5
7	IO_VREF_L174P_Y	H1 ²
7	IO_L175N_Y	G2
7	IO_L175P_Y	J6
7	IO_L176N_YY	J7
7	IO_L176P_YY	F1
7	IO_L177N_YY	H4
7	IO_VREF_L177P_YY	G4
7	IO_L178N_Y	F3
7	IO_L178P_Y	H5
7	IO_L179N_Y	E2
7	IO_L179P_Y	H6
7	IO_L180N_Y	G5
7	IO_VREF_L180P_Y	F4
7	IO_L181N_Y	H7
7	IO_L181P_Y	G6
7	IO_L182N_YY	E3
7	IO_L182P_YY	E4
2	CCLK	D24
3	DONE	AB21
NA	DXN	AB7
NA	DXP	Y8
NA	M0	AD4
NA	M1	W7
NA	M2	AB6
NA	PROGRAM	AA22
NA	TCK	E6
NA	TDI	D22
2	TDO	C23
NA	TMS	F5
NA	NC	T25
NA	NC	T2
NA	NC	P2
NA	NC	N25
NA	NC	L25

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
0	VCCO	H10
1	VCCO	J15
1	VCCO	J14
1	VCCO	H18
1	VCCO	H17
1	VCCO	H16
1	VCCO	H15
2	VCCO	N18
2	VCCO	M19
2	VCCO	M18
2	VCCO	L19
2	VCCO	K19
2	VCCO	J19
3	VCCO	V19
3	VCCO	U19
3	VCCO	T19
3	VCCO	R19
3	VCCO	R18
3	VCCO	P18
4	VCCO	W18
4	VCCO	W17
4	VCCO	W16
4	VCCO	W15
4	VCCO	V15
4	VCCO	V14
5	VCCO	W9
5	VCCO	W12
5	VCCO	W11
5	VCCO	W10
5	VCCO	V13
5	VCCO	V12
6	VCCO	V8
6	VCCO	U8
6	VCCO	T8
6	VCCO	R9
6	VCCO	R8
6	VCCO	P9

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
7	VCCO	N9
7	VCCO	M9
7	VCCO	M8
7	VCCO	L8
7	VCCO	K8
7	VCCO	J8
NA	GND	V25
NA	GND	V2
NA	GND	U17
NA	GND	U16
NA	GND	U15
NA	GND	U14
NA	GND	U13
NA	GND	U12
NA	GND	U11
NA	GND	U10
NA	GND	T17
NA	GND	T16
NA	GND	T15
NA	GND	T14
NA	GND	T13
NA	GND	T12
NA	GND	T11
NA	GND	T10
NA	GND	R17
NA	GND	R16
NA	GND	R15
NA	GND	R14
NA	GND	R13
NA	GND	R12
NA	GND	R11
NA	GND	R10
NA	GND	P25
NA	GND	P17
NA	GND	P16
NA	GND	P15

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
NA	GND	P14
NA	GND	P13
NA	GND	P12
NA	GND	P11
NA	GND	P10
NA	GND	N2
NA	GND	N17
NA	GND	N16
NA	GND	N15
NA	GND	N14
NA	GND	N13
NA	GND	N12
NA	GND	N11
NA	GND	N10
NA	GND	M17
NA	GND	M16
NA	GND	M15
NA	GND	M14
NA	GND	M13
NA	GND	M12
NA	GND	M11
NA	GND	M10
NA	GND	L17
NA	GND	L16
NA	GND	L15
NA	GND	L14
NA	GND	L13
NA	GND	L12
NA	GND	L11
NA	GND	L10
NA	GND	K17
NA	GND	K16
NA	GND	K15
NA	GND	K14
NA	GND	K13
NA	GND	K12
NA	GND	K11

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
NA	GND	K10
NA	GND	J25
NA	GND	J2
NA	GND	E5
NA	GND	E22
NA	GND	D4
NA	GND	D23
NA	GND	C3
NA	GND	C24
NA	GND	B9
NA	GND	B25
NA	GND	B2
NA	GND	B18
NA	GND	B14
NA	GND	AF26
NA	GND	AF1
NA	GND	AE9
NA	GND	AE25
NA	GND	AE2
NA	GND	AE18
NA	GND	AE13
NA	GND	AD3
NA	GND	AD24
NA	GND	AC4
NA	GND	AC23
NA	GND	AB5
NA	GND	AB22
NA	GND	A26
NA	GND	A1

Notes:

1. NC in the XCV400E.
2. V_{REF} or I/O option only in the XCV600E; otherwise, I/O option only.

FG676 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A $\checkmark$ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 21: FG676 Differential Pin Pair Summary
XCV400E, XCV600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
3	0	E13	B13	NA	IO_DLL_L21N
2	1	C13	F14	NA	IO_DLL_L21P
1	5	AB13	AF13	NA	IO_DLL_L115N
0	4	AA14	AC14	NA	IO_DLL_L115P
IOLVDS					
Total Pairs: 183, Asynchronous Output Pairs: 97					
0	0	F7	C4	1	-
1	0	C5	G8	$\checkmark$	-
2	0	E7	D6	$\checkmark$	VREF
3	0	F8	A4	NA	-
4	0	D7	B5	NA	-
5	0	G9	E8	$\checkmark$	VREF
6	0	F9	A5	$\checkmark$	-
7	0	C7	D8	1	-
8	0	E9	B7	1	VREF
9	0	D9	A7	NA	-
10	0	G10	B8	NA	VREF
11	0	F10	C9	$\checkmark$	-
12	0	E10	A8	1	-
13	0	D10	G11	$\checkmark$	-
14	0	F11	B10	$\checkmark$	-
15	0	E11	C10	NA	-
16	0	D11	G12	$\checkmark$	-
17	0	F12	C11	$\checkmark$	VREF

Table 21: FG676 Differential Pin Pair Summary
XCV400E, XCV600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
18	0	E12	A11	$\checkmark$	-
19	0	C12	D12	1	-
20	0	H13	A12	1	VREF
21	1	F14	B13	NA	IO_LVDS_DLL
22	1	F13	E14	NA	-
23	1	A14	D14	1	VREF
24	1	H14	C14	1	-
25	1	C15	G14	$\checkmark$	-
26	1	D15	E15	$\checkmark$	VREF
27	1	F15	C16	$\checkmark$	-
28	1	D16	G15	-	-
29	1	A17	E16	$\checkmark$	-
30	1	E17	C17	$\checkmark$	-
31	1	D17	F16	1	-
32	1	C18	F17	$\checkmark$	-
33	1	G16	A18	$\checkmark$	VREF
34	1	G17	C19	$\checkmark$	-
35	1	B19	D18	1	VREF
36	1	E18	D19	1	-
37	1	B20	F18	$\checkmark$	-
38	1	C20	G19	$\checkmark$	VREF
39	1	E19	G18	$\checkmark$	-
40	1	D20	A21	$\checkmark$	-
41	1	C21	F19	$\checkmark$	VREF
42	1	E20	B22	$\checkmark$	-
43	1	D21	A23	2	-
44	1	E21	C22	$\checkmark$	CS
45	2	E23	F22	$\checkmark$	DIN, D0
46	2	E24	F20	$\checkmark$	-
47	2	G21	G22	2	-
48	2	F24	H20	1	VREF
49	2	E25	H21	1	-
50	2	F23	G23	$\checkmark$	-
51	2	H23	J20	$\checkmark$	VREF

Table 21: FG676 Differential Pin Pair Summary
XCV400E, XCV600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
52	2	G24	H22	√	-
53	2	J21	G25	2	-
54	2	G26	J22	1	VREF
55	2	H24	J23	√	-
56	2	J24	K20	√	VREF
57	2	K22	K21	√	D2
58	2	H25	K23	√	-
59	2	L20	J26	2	-
60	2	K25	L22	1	-
61	2	L21	L23	1	-
62	2	M20	L24	1	-
63	2	M23	M22	√	D3
64	2	L26	M21	√	-
65	2	N19	M24	2	-
66	2	M26	N20	1	VREF
67	2	N24	N21	√	-
68	2	N23	N22	√	-
69	3	P21	P23	√	-
70	3	P22	R25	1	VREF
71	3	P19	P20	2	-
72	3	R21	R22	√	-
73	3	R24	R23	√	VREF
74	3	T24	R20	1	-
75	3	T22	U24	1	-
76	3	T23	U25	1	-
77	3	T21	U20	2	-
78	3	U22	V26	√	-
79	3	T20	U23	√	D5
80	3	V24	U21	√	VREF
81	3	V23	W24	√	-
82	3	V22	W26	1	VREF
83	3	Y25	V21	2	-
84	3	V20	AA26	√	-
85	3	Y24	W23	√	VREF

Table 21: FG676 Differential Pin Pair Summary
XCV400E, XCV600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
86	3	AA24	Y23	1	-
87	3	AB26	W21	2	-
88	3	Y22	W22	1	VREF
89	3	AA23	AB24	2	-
90	3	W20	AC24	√	-
91	3	AB23	Y21	√	INIT
92	4	AC22	AD26	√	-
93	4	AD23	AA20	1	-
94	4	Y19	AC21	√	-
95	4	AD22	AB20	√	VREF
96	4	AE22	Y18	NA	-
97	4	AF22	AA19	NA	-
98	4	AD21	AB19	√	VREF
99	4	AC20	AA18	√	-
100	4	AC19	AD20	1	-
101	4	AF20	AB18	1	VREF
102	4	AD19	Y17	NA	-
103	4	AE19	AD18	NA	VREF
104	4	AF19	AA17	√	-
105	4	AC17	AB17	1	-
106	4	Y16	AE17	√	-
107	4	AF17	AA16	√	-
108	4	AD17	AB16	NA	-
109	4	AC16	AD16	√	-
110	4	AC15	Y15	√	VREF
111	4	AD15	AA15	√	-
112	4	W14	AB15	1	-
113	4	AF15	Y14	1	VREF
114	4	AD14	AB14	NA	-
115	5	AC14	AF13	NA	IO_LVDS_DLL
116	5	AA13	AF12	1	VREF
117	5	AC13	W13	1	-
118	5	AA12	AD12	√	-
119	5	AC12	AB12	√	VREF

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
3	IO_L97N	AA2
3	IO_L98P_YY	AC5
3	IO_L98N_YY	AB1
3	IO_D4_L99P_YY	AD3
3	IO_VREF_L99N_YY	AC1
3	IO_L100P_Y	AD1
3	IO_L100N_Y	AD4
3	IO_L101P	AD2
3	IO_L101N	AE3
3	IO_L102P_YY	AE1
3	IO_L102N_YY	AE4
3	IO_L103P_Y	AE2
3	IO_VREF_L103N_Y	AF3 ¹
3	IO_L104P	AF4
3	IO_L104N	AF1
3	IO_L105P	AG3
3	IO_L105N	AF2
3	IO_L106P_Y	AG4
3	IO_L106N_Y	AG1
3	IO_L107P_YY	AH3
3	IO_D5_L107N_YY	AG2
3	IO_D6_L108P_YY	AH1
3	IO_VREF_L108N_YY	AJ2
3	IO_L109P	AH2
3	IO_L109N	AJ3
3	IO_L110P_YY	AJ1
3	IO_L110N_YY	AJ4
3	IO_L111P_YY	AK1
3	IO_VREF_L111N_YY	AK3
3	IO_L112P	AK2
3	IO_L112N	AK4
3	IO_L113P	AL1
3	IO_VREF_L113N	AL2 ³
3	IO_L114P_YY	AM1
3	IO_L114N_YY	AL3
3	IO_L115P_YY	AM2

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
3	IO_VREF_L115N_YY	AL4
3	IO_L116P_Y	AM3
3	IO_L116N_Y	AN1
3	IO_L117P	AM4
3	IO_L117N	AP1
3	IO_L118P_YY	AN2
3	IO_L118N_YY	AP2
3	IO_L119P_Y	AN3
3	IO_VREF_L119N_Y	AR1
3	IO_L120P	AN4
3	IO_L120N	AT1
3	IO_L121P	AR2
3	IO_VREF_L121N	AP4 ¹
3	IO_L122P_Y	AT2
3	IO_L122N_Y	AR3
3	IO_D7_L123P_YY	AR4
3	IO_INIT_L123N_YY	AU2
4	GCK0	AW19
4	IO	AV3
4	IO_L124P_YY	AU4
4	IO_L124N_YY	AV5
4	IO_L125P_Y	AT6
4	IO_L125N_Y	AV4
4	IO_VREF_L126P_Y	AU6 ¹
4	IO_L126N_Y	AW4
4	IO_L127P_YY	AT7
4	IO_L127N_YY	AW5
4	IO_VREF_L128P_YY	AU7
4	IO_L128N_YY	AV6
4	IO_L129P_Y	AT8
4	IO_L129N_Y	AW6
4	IO_L130P_Y	AU8
4	IO_L130N_Y	AV7
4	IO_L131P_YY	AT9
4	IO_L131N_YY	AW7

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
0	IO_VREF_L27N_YY	D27
0	IO_L27P_YY	B25
0	IO_L28N_Y	A25
0	IO_L28P_Y	D26
0	IO_L29N_Y	A24
0	IO_L29P_Y	E25
0	IO_L30N_YY	D25
0	IO_L30P_YY	B24
0	IO_VREF_L31N_YY	E24
0	IO_L31P_YY	A23
0	IO_L32N_Y	C23
0	IO_L32P_Y	E23
0	IO_VREF_L33N_Y	B23 ¹
0	IO_L33P_Y	D23
0	IO_LVDS_DLL_L34N	A22
1	GCK2	B22
1	IO	A14
1	IO	A20
1	IO	B11
1	IO	B13
1	IO	C8
1	IO	C18
1	IO	C21
1	IO	D7
1	IO	D10
1	IO	D15
1	IO	D17
1	IO	E20
1	IO_LVDS_DLL_L34P	D22
1	IO_L35N_Y	D21
1	IO_VREF_L35P_Y	B21 ¹
1	IO_L36N_Y	D20
1	IO_L36P_Y	A21
1	IO_L37N_YY	C20
1	IO_VREF_L37P_YY	D19
1	IO_L38N_YY	B20

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
1	IO_L38P_YY	E19
1	IO_L39N_Y	D18
1	IO_L39P_Y	A19
1	IO_L40N_Y	E18
1	IO_L40P_Y	C19
1	IO_L41N_YY	B19
1	IO_VREF_L41P_YY	E17
1	IO_L42N_YY	A18
1	IO_L42P_YY	D16
1	IO_L43N_Y	E16
1	IO_L43P_Y	B18
1	IO_L44N_Y	F16
1	IO_L44P_Y	A17
1	IO_L45N_YY	C17
1	IO_VREF_L45P_YY	E15
1	IO_L46N_YY	B17
1	IO_L46P_YY	D14
1	IO_L47N_Y	A16
1	IO_L47P_Y	E14
1	IO_L48N_Y	C16
1	IO_L48P_Y	D13
1	IO_L49N_Y	B16
1	IO_L49P_Y	D12
1	IO_L50N_Y	A15
1	IO_L50P_Y	E12
1	IO_L51N_YY	C15
1	IO_L51P_YY	C11
1	IO_L52N_YY	B15
1	IO_VREF_L52P_YY	D11
1	IO_L53N_Y	E11
1	IO_L53P_Y	C14
1	IO_L54N_Y	C10
1	IO_L54P_Y	B14
1	IO_L55N_YY	A13
1	IO_VREF_L55P_YY	E10
1	IO_L56N_YY	C13
1	IO_L56P_YY	C9

Table 27: FG900 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
188	5	AA12	AJ12	√	VREF
189	5	AB12	AE11	√	-
190	5	AK12	Y13	2	-
191	5	AG11	AF11	2	-
192	5	AH11	AJ11	2	-
193	5	AE12	AG10	4	-
194	5	AD12	AK11	√	-
195	5	AJ10	AC12	√	VREF
196	5	AK10	AD11	4	-
197	5	AJ9	AE9	4	-
198	5	AH10	AF9	√	VREF
199	5	AH9	AK9	√	-
200	5	AF8	AB11	2	-
201	5	AC11	AG8	2	-
202	5	AK8	AF7	√	VREF
203	5	AG7	AK7	√	-
204	5	AJ7	AD10	1	-
205	5	AH6	AC10	1	-
206	5	AD9	AG6	√	VREF
207	5	AB10	AJ5	√	-
208	5	AD8	AK5	2	-
209	5	AC9	AJ4	2	VREF
210	5	AG5	AK4	2	-
211	5	AH5	AG3	4	-
212	6	AC6	AF3	√	-
213	6	AG2	AH2	NA	-
214	6	AE4	AB9	1	-
215	6	AH1	AE3	4	VREF
216	6	AD6	AB8	3	-
217	6	AA10	AG1	4	-
218	6	AD4	AA9	1	VREF
219	6	AD2	AD5	√	-
220	6	AF2	AD3	4	-
221	6	AA7	AA8	1	-

Table 27: FG900 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
222	6	Y9	AF1	√	VREF
223	6	AC4	AB6	√	-
224	6	W8	AE1	2	-
225	6	AB4	Y8	4	-
226	6	W9	AB3	4	VREF
227	6	W10	AA5	4	-
228	6	V10	AB1	4	-
229	6	AC1	Y7	4	VREF
230	6	AA3	V11	NA	-
231	6	U10	AA2	4	-
232	6	AA6	W7	1	-
233	6	Y4	Y6	4	-
234	6	V7	AA1	3	-
235	6	Y2	Y3	4	-
236	6	W5	Y5	1	VREF
237	6	W6	W4	√	-
238	6	W2	V6	4	-
239	6	V4	U9	1	-
240	6	T8	AB2	√	VREF
241	6	W1	U5	√	-
242	6	T9	Y1	2	-
243	6	U3	T7	4	-
244	6	V2	T5	4	VREF
245	6	T6	R9	4	-
246	6	U2	T4	4	VREF
247	7	R10	T1	NA	-
248	7	R6	R5	4	-
249	7	R4	R8	4	VREF
250	7	R3	R7	4	-
251	7	P6	P10	4	VREF
252	7	P2	P5	4	-
253	7	P4	P7	2	-
254	7	R2	N4	√	-
255	7	P1	N7	√	VREF

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
2	IO_L92N_Y	H29
2	IO_L93P_YY	J28 ⁴
2	IO_L93N_YY	E33 ⁵
2	IO_L94P_YY	H28
2	IO_L94N_YY	H30
2	IO_L95P_Y	H32
2	IO_L95N_Y	K28
2	IO_L96P_Y	L27 ⁴
2	IO_L96N_Y	F33 ⁵
2	IO_L97P_Y	M26
2	IO_L97N_Y	E34
2	IO_VREF_L98P_YY	H31
2	IO_L98N_YY	G32
2	IO_L99P_YY	N25 ⁴
2	IO_L99N_YY	J31 ⁵
2	IO_L100P_YY	J30
2	IO_L100N_YY	G33
2	IO_VREF_L101P_Y	H34 ²
2	IO_L101N_Y	J29
2	IO_L102P	M27 ⁴
2	IO_L102N	H33 ⁵
2	IO_L103P_Y	K29
2	IO_L103N_Y	J34
2	IO_VREF_L104P_YY	L29
2	IO_L104N_YY	J33
2	IO_L105P_YY	M28
2	IO_L105N_YY	K34
2	IO_L106P_Y	N27
2	IO_L106N_Y	L34
2	IO_VREF_L107P_YY	K33
2	IO_D1_L107N_YY	P26
2	IO_L108P_Y	R25
2	IO_L108N_Y	M34
2	IO_L109P_Y	L31

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
2	IO_L109N_Y	L33
2	IO_L110P_Y	P27
2	IO_L110N_Y	M33
2	IO_L111P	M31
2	IO_L111N	R26
2	IO_L112P_Y	N30
2	IO_L112N_Y	P28
2	IO_VREF_L113P_Y	N29
2	IO_L113N_Y	N33
2	IO_L114P_YY	T25 ⁴
2	IO_L114N_YY	N34 ⁵
2	IO_L115P_YY	P34
2	IO_L115N_YY	R27
2	IO_L116P_Y	P29
2	IO_L116N_Y	P31
2	IO_L117P_Y	P33 ⁴
2	IO_L117N_Y	T26 ⁵
2	IO_L118P_Y	R34
2	IO_L118N_Y	R28
2	IO_VREF_L119P_YY	N31
2	IO_D3_L119N_YY	N32
2	IO_L120P_YY	P30 ⁴
2	IO_L120N_YY	R33 ⁵
2	IO_L121P_YY	R29
2	IO_L121N_YY	T34
2	IO_L122P_Y	R30
2	IO_L122N_Y	T30
2	IO_L123P	T28 ⁴
2	IO_L123N	R31 ⁵
2	IO_L124P_Y	T29
2	IO_L124N_Y	U27
2	IO_VREF_L125P_YY	T31
2	IO_L125N_YY	T33
2	IO_L126P_YY	U28

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
231	5	AH14	AP12	3200 2600 2000 1600 1000	-
232	5	AJ14	AL14	3200 2600 1000	-
233	5	AF13	AN12	3200 2000 1000	-
234	5	AF14	AP11	3200 2000 1000	-
235	5	AN11	AH13	3200 1600 1000	-
236	5	AM12	AL12	3200 2600 2000 1600 1000	-
237	5	AJ13	AP10	3200 2600 2000 1600 1000	VREF
238	5	AK12	AM10	2600 1600 1000	-
239	5	AP9	AK11	2600 1600 1000	-
240	5	AL11	AL10	3200 2600 2000 1600 1000	VREF
241	5	AE13	AM9	3200 2600 2000 1600 1000	-
242	5	AF12	AP8	3200 2600	-
243	5	AL9	AH11	3200 2000 1000	VREF
244	5	AF11	AN8	3200 2000 1000	-
245	5	AM8	AG11	3200 1600	-
246	5	AL8	AK9	3200 2600 2000 1600 1000	VREF
247	5	AH10	AN7	3200 2600 2000 1600 1000	-
248	5	AE12	AJ9	3200 2600	-
249	5	AM7	AL7	3200 1000	-
250	5	AG10	AN6	3200 1000	-

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
251	5	AK8	AH9	2000 1600	-
252	5	AP5	AJ8	3200 2600 2000 1600 1000	VREF
253	5	AE11	AN5	3200 2600 2000 1600 1000	-
254	5	AF10	AM6	3200 2600 1000	-
255	5	AL6	AG9	3200 2000 1000	VREF
256	5	AH8	AP4	3200 2000 1000	-
257	5	AN4	AJ7	3200 1600 1000	-
258	5	AM5	AK6	3200 2600 2000 1600 1000	-
259	6	AF8	AH6	3200 2600 2000 1600 1000	-
260	6	AK3	AE9	3200 2600 2000	-
261	6	AL2	AD10	2600 2000 1000	-
262	6	AH4	AL1	3200 2600 1600 1000	VREF
263	6	AK1	AG6	2600 1600	-
264	6	AK2	AF7	3200 2600 1600 1000	-
265	6	AG5	AJ3	2600 2000 1000	VREF
266	6	AJ2	AD9	3200 2600 2000 1600	-
267	6	AH2	AC10	3200 2600 2000 1600 1000	-
268	6	AF5	AH3	3200 2600 1600 1000	-
269	6	AG3	AE8	3200 2600 2000	-