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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	384
Number of Logic Elements/Cells	1728
Total RAM Bits	65536
Number of I/O	176
Number of Gates	71693
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv50e-7fg256c

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Eight I/O banks result from separating each edge of the FPGA into two banks, as shown in Figure 3. Each bank has multiple V_{CCO} pins, all of which must be connected to the same voltage. This voltage is determined by the output standards in use.

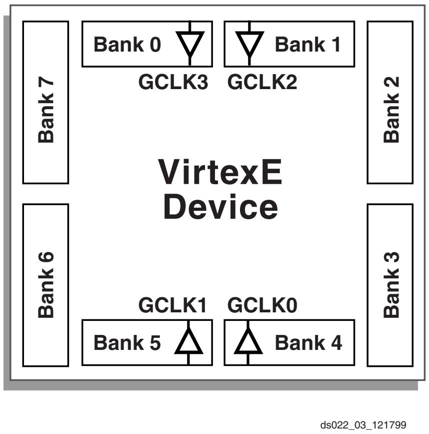

Figure 3: **Virtex-E I/O Banks**

Within a bank, output standards can be mixed only if they use the same V_{CCO}. Compatible standards are shown in Table 2. GTL and GTL+ appear under all voltages because their open-drain outputs do not depend on V_{CCO}.

Table 2: **Compatible Output Standards**

V_{CCO}	Compatible Standards
3.3 V	PCI, LVTTL, SSTL3 I, SSTL3 II, CTT, AGP, GTL, GTL+, LVPECL
2.5 V	SSTL2 I, SSTL2 II, LVCMOS2, GTL, GTL+, BLVDS, LVDS
1.8 V	LVCMOS18, GTL, GTL+
1.5 V	HSTL I, HSTL III, HSTL IV, GTL, GTL+

Some input standards require a user-supplied threshold voltage, V_{REF}. In this case, certain user-I/O pins are automatically configured as inputs for the V_{REF} voltage. Approximately one in six of the I/O pins in the bank assume this role.

The V_{REF} pins within a bank are interconnected internally and consequently only one V_{REF} voltage can be used within each bank. All V_{REF} pins in the bank, however, must be connected to the external voltage source for correct operation.

Within a bank, inputs that require V_{REF} can be mixed with those that do not. However, only one V_{REF} voltage can be used within a bank.

In Virtex-E, input buffers with LVTTL, LVCMOS2, LVCMOS18, PCI33_3, PCI66_3 standards are supplied by V_{CCO} rather than V_{CCINT}. For these standards, only input and output buffers that have the same V_{CCO} can be mixed together.

The V_{CCO} and V_{REF} pins for each bank appear in the device pin-out tables and diagrams. The diagrams also show the bank affiliation of each I/O.

Within a given package, the number of V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices, more I/O pins convert to V_{REF} pins. Since these are always a super set of the V_{REF} pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device if necessary. All the V_{REF} pins for the largest device anticipated must be connected to the V_{REF} voltage, and not used for I/O.

In smaller devices, some V_{CCO} pins used in larger devices do not connect within the package. These unconnected pins can be left unconnected externally, or can be connected to the V_{CCO} voltage to permit migration to a larger device if necessary.

Configurable Logic Blocks

The basic building block of the Virtex-E CLB is the logic cell (LC). An LC includes a 4-input function generator, carry logic, and a storage element. The output from the function generator in each LC drives both the CLB output and the D input of the flip-flop. Each Virtex-E CLB contains four LCs, organized in two similar slices, as shown in Figure 4. Figure 5 shows a more detailed view of a single slice.

In addition to the four basic LCs, the Virtex-E CLB contains logic that combines function generators to provide functions of five or six inputs. Consequently, when estimating the number of system gates provided by a given device, each CLB counts as 4.5 LCs.

Look-Up Tables

Virtex-E function generators are implemented as 4-input look-up tables (LUTs). In addition to operating as a function generator, each LUT can provide a 16 x 1-bit synchronous RAM. Furthermore, the two LUTs within a slice can be combined to create a 16 x 2-bit or 32 x 1-bit synchronous RAM, or a 16 x 1-bit dual-port synchronous RAM.

The Virtex-E LUT can also provide a 16-bit shift register that is ideal for capturing high-speed or burst-mode data. This mode can also be used to store data in applications such as Digital Signal Processing.

The DLL also operates as a clock mirror. By driving the output from a DLL off-chip and then back on again, the DLL can be used to deskew a board level clock among multiple devices.

To guarantee that the system clock is operating correctly prior to the FPGA starting up after configuration, the DLL can delay the completion of the configuration process until after it has achieved lock. For more information about DLL functionality, see the Design Consideration section of the data sheet.

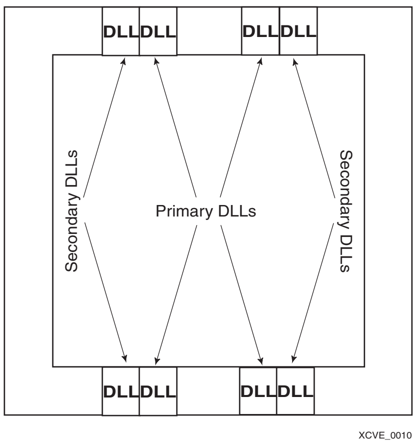

Figure 10: **DLL Locations**

Boundary Scan

Virtex-E devices support all the mandatory Boundary Scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, INTEST, SAMPLE/PRELOAD, BYPASS, IDCODE, USERCODE, and HIGHZ instructions. The TAP also supports two internal scan chains and configuration/readback of the device.

The JTAG input pins (TDI, TMS, TCK) do not have a V_{CCO} requirement and operate with either 2.5 V or 3.3 V input signalling levels. The output pin (TDO) is sourced from the V_{CCO} in bank 2, and for proper operation of LVTTL 3.3 V levels, the bank should be supplied with 3.3 V.

Boundary Scan operation is independent of individual IOB configurations, and unaffected by package type. All IOBs, including un-bonded ones, are treated as independent 3-state bidirectional pins in a single scan chain. Retention of the bidirectional test capability after configuration facilitates the testing of external interconnections, provided the user design or application is turned off.

Table 6 lists the Boundary Scan instructions supported in Virtex-E FPGAs. Internal signals can be captured during EXTEST by connecting them to un-bonded or unused IOBs. They can also be connected to the unused outputs of IOBs defined as unidirectional input pins.

Before the device is configured, all instructions except USER1 and USER2 are available. After configuration, all instructions are available. During configuration, it is recommended that those operations using the Boundary Scan register (SAMPLE/PRELOAD, INTEST, EXTEST) not be performed.

In addition to the test instructions outlined above, the Boundary Scan circuitry can be used to configure the FPGA, and also to read back the configuration data.

Figure 11 is a diagram of the Virtex-E Series Boundary Scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

Data Registers

The primary data register is the Boundary Scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out, and 3-State Control. Non-IOB pins have appropriate partial bit population if input-only or output-only. Each EXTEST CAPTURED-OR state captures all In, Out, and 3-state pins.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream Boundary Scan device.

The FPGA supports up to two additional internal scan chains that can be specified using the BSCAN macro. The macro provides two user pins (SEL1 and SEL2) which are decodes of the USER1 and USER2 instructions respectively. For these instructions, two corresponding pins (T DO1 and TDO2) allow user scan data to be shifted out of TDO.

Likewise, there are individual clock pins (DRCK1 and DRCK2) for each user register. There is a common input pin (TDI) and shared output pins that represent the state of the TAP controller (RESET, SHIFT, and UPDATE).

Bit Sequence

The order within each IOB is: In, Out, 3-State. The input-only pins contribute only the In bit to the Boundary Scan I/O data register, while the output-only pins contributes all three bits.

From a cavity-up view of the chip (as shown in EPIC), starting in the upper right chip corner, the Boundary Scan data-register bits are ordered as shown in Figure 12.

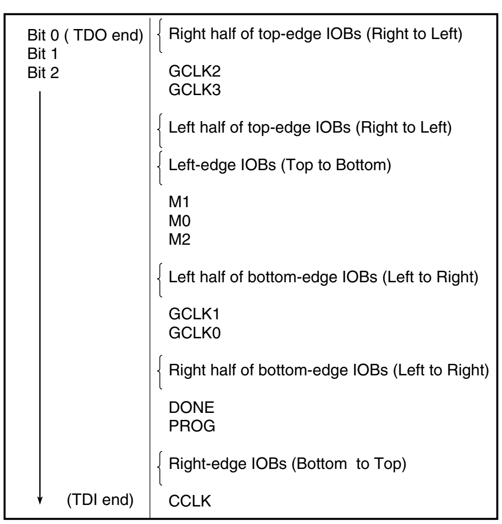

Figure 12: **Boundary Scan Bit Sequence**

BSDL (Boundary Scan Description Language) files for Virtex-E Series devices are available on the Xilinx web site in the File Download area.

Identification Registers

The IDCODE register is supported. By using the IDCODE, the device connected to the JTAG port can be determined.

The IDCODE register has the following binary format:

vvvv:ffff:fffa:aaaa:aaaa:cccc:cccc:ccc1

where

v = the die version number

f = the family code (05 for Virtex-E family)

a = the number of CLB rows (ranges from 16 for

XCV50E to 104 for XCV3200E)

c = the company code (49h for Xilinx)

The USERCODE register is supported. By using the USERCODE, a user-programmable identification code can be loaded and shifted out for examination. The identification code (see Table 7) is embedded in the bitstream during bitstream generation and is valid only after configuration.

Table 7: **IDCODEs Assigned to Virtex-E FPGAs**

FPGA	IDCODE
XCV50E	v0A10093h
XCV100E	v0A14093h
XCV200E	v0A1C093h
XCV300E	v0A20093h
XCV400E	v0A28093h
XCV600E	v0A30093h
XCV1000E	v0A40093h
XCV1600E	v0A48093h
XCV2000E	v0A50093h
XCV2600E	v0A5C093h
XCV3200E	v0A68093h

Note:

Attempting to load an incorrect bitstream causes configuration to fail and can damage the device.

Including Boundary Scan in a Design

Since the Boundary Scan pins are dedicated, no special element needs to be added to the design unless an internal data register (USER1 or USER2) is desired.

If an internal data register is used, insert the Boundary Scan symbol and connect the necessary pins as appropriate.

Development System

Virtex-E FPGAs are supported by the Xilinx Foundation and Alliance Series CAE tools. The basic methodology for Virtex-E design consists of three interrelated steps: design entry, implementation, and verification. Industry-standard tools are used for design entry and simulation (for example, Synopsys FPGA Express), while Xilinx provides proprietary architecture-specific tools for implementation.

The Xilinx development system is integrated under the Xilinx Design Manager (XDM™) software, providing designers with a common user interface regardless of their choice of entry and verification tools. The XDM software simplifies the selection of implementation options with pull-down menus and on-line help.

Application programs ranging from schematic capture to Placement and Routing (PAR) can be accessed through the XDM software. The program command sequence is generated prior to execution, and stored for documentation.

Several advanced software features facilitate Virtex-E design. RPMs, for example, are schematic-based macros with relative location constraints to guide their placement. They help ensure optimal implementation of common functions.

For HDL design entry, the Xilinx FPGA Foundation development system provides interfaces to the following synthesis design environments.

- Synopsys (FPGA Compiler, FPGA Express)
- Exemplar (Spectrum)
- Synplicity (Synplify)

For schematic design entry, the Xilinx FPGA Foundation and Alliance development system provides interfaces to the following schematic-capture design environments.

- Mentor Graphics V8 (Design Architect, QuickSim II)
- Viewlogic Systems (Viewdraw)

Third-party vendors support many other environments.

A standard interface-file specification, Electronic Design Interchange Format (EDIF), simplifies file transfers into and out of the development system.

Virtex-E FPGAs are supported by a unified library of standard functions. This library contains over 400 primitives and macros, ranging from 2-input AND gates to 16-bit accumulators, and includes arithmetic functions, comparators, counters, data registers, decoders, encoders, I/O functions, latches, Boolean functions, multiplexers, shift registers, and barrel shifters.

The “soft macro” portion of the library contains detailed descriptions of common logic functions, but does not contain any partitioning or placement information. The performance of these macros depends, therefore, on the partitioning and placement obtained during implementation.

RPMs, on the other hand, do contain predetermined partitioning and placement information that permits optimal implementation of these functions. Users can create their own library of soft macros or RPMs based on the macros and primitives in the standard library.

The design environment supports hierarchical design entry, with high-level schematics that comprise major functional blocks, while lower-level schematics define the logic in these blocks. These hierarchical design elements are automatically combined by the implementation tools. Different design entry tools can be combined within a hierarchical design, thus allowing the most convenient entry method to be used for each portion of the design.

Design Implementation

The place-and-route tools (PAR) automatically provide the implementation flow described in this section. The partitioner takes the EDIF net list for the design and maps the logic into the architectural resources of the FPGA (CLBs and IOBs, for example). The placer then determines the best locations for these blocks based on their interconnections and the desired performance. Finally, the router interconnects the blocks.

The PAR algorithms support fully automatic implementation of most designs. For demanding applications, however, the user can exercise various degrees of control over the process. User partitioning, placement, and routing information is optionally specified during the design-entry process. The implementation of highly structured designs can benefit greatly from basic floor planning.

The implementation software incorporates Timing Wizard® timing-driven placement and routing. Designers specify timing requirements along entire paths during design entry. The timing path analysis routines in PAR then recognize these user-specified requirements and accommodate them.

Timing requirements are entered on a schematic in a form directly relating to the system requirements, such as the targeted clock frequency, or the maximum allowable delay between two registers. In this way, the overall performance of the system along entire signal paths is automatically tailored to user-generated specifications. Specific timing information for individual nets is unnecessary.

Design Verification

In addition to conventional software simulation, FPGA users can use in-circuit debugging techniques. Because Xilinx devices are infinitely reprogrammable, designs can be verified in real time without the need for extensive sets of software simulation vectors.

The development system supports both software simulation and in-circuit debugging techniques. For simulation, the system extracts the post-layout timing information from the design database, and back-annotates this information into the net list for use by the simulator. Alternatively, the user can verify timing-critical portions of the design using the TRCE® static timing analyzer.

Because any single DLL can access only two BUFGs at most, any additional output clock signals must be routed from the DLL in this example on the high speed backbone routing.

The dll_2x files in the xapp132.zip file show the VHDL and Verilog implementation of this circuit.

Virtex-E 4x Clock

Two DLLs located in the same half-edge (top-left, top-right, bottom-right, bottom-left) can be connected together, without using a BUFG between the CLKDLLs, to generate a 4x clock as shown in Figure 30. Virtex-E devices, like the Virtex devices, have four clock networks that are available for internal deskewing of the clock. Each of the eight DLLs have access to two of the four clock networks. Although all the DLLs can be used for internal deskewing, the presence of two GCLKBUFs on the top and two on the bottom indicate that only two of the four DLLs on the top (and two of the four DLLs on the bottom) can be used for this purpose.

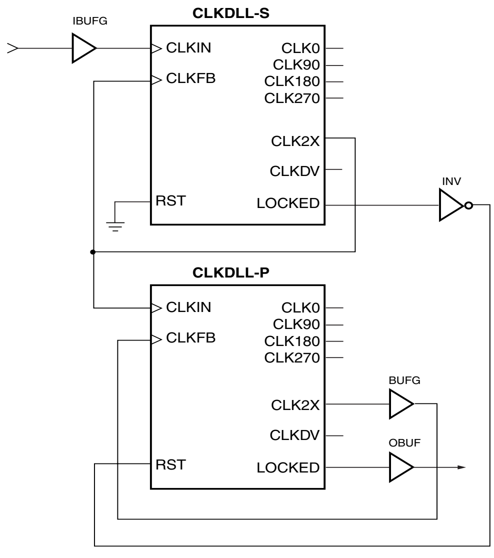

Figure 30: **DLL Generation of 4x Clock in Virtex-E Devices**

The dll_4xe files in the xapp132.zip file show the DLL implementation in Verilog for Virtex-E devices. These files can be found at:

ftp://ftp.xilinx.com/pub/applications/xapp/xapp132.zip

Using Block SelectRAM+ Features

The Virtex FPGA Series provides dedicated blocks of on-chip, true dual-read/write port synchronous RAM, with 4096 memory cells. Each port of the block SelectRAM+ memory can be independently configured as a read/write port, a read port, a write port, and can be configured to a specific data width. The block SelectRAM+ memory offers new capabilities allowing the FPGA designer to simplify designs.

Operating Modes

VIrtex-E block SelectRAM+ memory supports two operating modes:

- Read Through
- Write Back

Read Through (one clock edge)

The read address is registered on the read port clock edge and data appears on the output after the RAM access time. Some memories might place the latch/register at the outputs, depending on whether a faster clock-to-out versus set-up time is desired. This is generally considered to be an inferior solution, since it changes the read operation to an asynchronous function with the possibility of missing an address/control line transition during the generation of the read pulse clock.

Write Back (one clock edge)

The write address is registered on the write port clock edge and the data input is written to the memory and mirrored on the output.

Block SelectRAM+ Characteristics

- All inputs are registered with the port clock and have a set-up to clock timing specification.
- All outputs have a read through or write back function depending on the state of the port WE pin. The outputs relative to the port clock are available after the clock-to-out timing specification.
- The block SelectRAMs are true SRAM memories and do not have a combinatorial path from the address to the output. The LUT SelectRAM+ cells in the CLBs are still available with this function.
- The ports are completely independent from each other (*i.e.,* clocking, control, address, read/write function, and data width) without arbitration.
- A write operation requires only one clock edge.
- A read operation requires only one clock edge.

The output ports are latched with a self timed circuit to guarantee a glitch free read. The state of the output port does not change until the port executes another read or write operation.

Library Primitives

Figure 31 and Figure 32 show the two generic library block SelectRAM+ primitives. Table 14 describes all of the available primitives for synthesis and simulation.

The voltage reference signal is "banked" within the Virtex-E device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 38 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

IBUF placement restrictions require that any differential amplifier input signals within a bank be of the same standard. How to specify a specific location for the IBUF via the LOC property is described below. Table 19 summarizes the Virtex-E input standards compatibility requirements.

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element by default activates to ensure a zero hold-time requirement. The NODELAY=TRUE property overrides this default.

When the IBUF does not drive a flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

Table 19: **Xilinx Input Standards Compatibility Requirements**

Rule 1	Standards with the same input V_{CCO}, output V_{CCO}, and V_{REF} can be placed within the same bank.

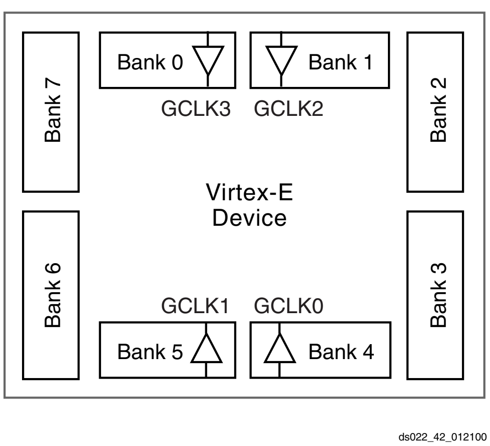

Figure 38: **Virtex-E I/O Banks**

IBUFG

Signals used as high fanout clock inputs to the Virtex-E device should drive a global clock input buffer (IBUFG) via an external input port in order to take advantage of one of the four dedicated global clock distribution networks. The output of the IBUFG should only drive a CLKDLL, CLKDLLHF, or BUFG symbol. The generic Virtex-E IBUFG symbol appears in Figure 39.

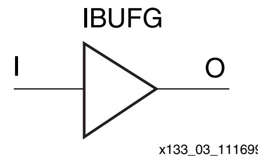

Figure 39: **Virtex-E Global Clock Input Buffer (IBUFG) Symbol**

The extension to the base name determines which I/O standard is used by the IBUFG. With no extension specified for the generic IBUFG symbol, the assumed standard is LVTTL.

The following list details variations of the IBUFG symbol.

- IBUFG
- IBUFG_LVCMOS2
- IBUFG_PCI33_3
- IBUFG_PCI66_3
- IBUFG_GTL
- IBUFG_GTLP
- IBUFG_HSTL_I
- IBUFG_HSTL_III
- IBUFG_HSTL_IV
- IBUFG_SSTL3_I
- IBUFG_SSTL3_II
- IBUFG_SSTL2_I
- IBUFG_SSTL2_II
- IBUFG_CTT
- IBUFG_AGP
- IBUFG_LVCMOS18
- IBUFG_LVDS
- IBUFG_LVPECL

When the IBUFG symbol supports an I/O standard that requires a differential amplifier input, the IBUFG automatically configures as a differential amplifier input buffer. The low-voltage I/O standards with a differential amplifier input require an external reference voltage input V_{REF}.

The voltage reference signal is "banked" within the Virtex-E device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 38 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

IBUFG placement restrictions require any differential amplifier input signals within a bank be of the same standard. The LOC property can specify a location for the IBUFG.

As an added convenience, the BUFGP can be used to instantiate a high fanout clock input. The BUFGP symbol

The register elements can be packed in the IOB using the IOB property to TRUE on the register or by using the “map -pr [i|o|b]” where “i” is inputs only, “o” is outputs only and “b” is both inputs and outputs.

To improve design coding times VHDL and Verilog synthesis macro libraries have been developed to explicitly create these structures. The input library macros are listed below. The 3-state is configured to be 3-stated at GSR and when the PRE,CLR,S or R is asserted and shares it's clock enable with the output register. If this is not desirable then the library can be updated by the user for the desired functionality. The O and OB inputs to the macros are the external net connections.

Creating a LVDS Bidirectional Buffer

LVDS bidirectional buffers can be placed in a wide number of IOB locations. The exact locations are dependent on the package used. The Virtex-E package information lists the possible locations as IO_L#P for the P-side and IO_L#N for the N-side, where # is the pair number.

HDL Instantiation

Both bidirectional buffers are required to be instantiated in the design and placed on the correct IO_L#P and IO_L#N locations. The IOB must have the same net source the following pins, clock (C), set/reset (SR), 3-state (T), 3-state clock enable (TCE), output (O), output clock enable (OCE). In addition, the output (O) pins must be inverted with respect to each other, and if output registers are used, the INIT states must be opposite values (one HIGH and one LOW). If 3-state registers are used, they must be initialized to the same state. Failure to follow these rules leads to DRC errors in the software.

VHDL Instantiation

```
data0_p:   IOBUF_LVDS port map
(I=>data_out(0), T=>data_tri,
IO=>data_p(0), O=>data_int(0));

data0_inv: INV         port map
(I=>data_out(0),   O=>data_n_out(0));

data0_n   : IOBUF_LVDS port map
(I=>data_n_out(0), T=>data_tri,
IO=>data_n(0), O=>open);
```

Verilog Instantiation

```
IOBUF_LVDS data0_p(.I(data_out[0]),
.T(data_tri), .IO(data_p[0]),
.O(data_int[0]);

INV        data0_inv (.I(data_out[0],
.O(data_n_out[0]);

IOBUF_LVDS
data0_n(.I(data_n_out[0]),.T(data_tri),.
IO(data_n[0]).O());
```

Location Constraints

All LVDS buffers must be explicitly placed on a device. For the output buffers this can be done with the following constraint in the .ucf or .ncf file.

```
NET data_p<0> LOC = D28; # IO_L0P

NET data_n<0> LOC = B29; # IO_L0N
```

Synchronous vs. Asynchronous Bidirectional Buffers

If the output side of the bidirectional buffers are synchronous (registered in the IOB), then any IO_L#P|N pair can be used. If the output side of the bidirectional buffers are asynchronous (no output register), then they must use one of the pairs that is a part of the asynchronous LVDS IOB group. This applies for either the 3-state pin or the data out pin.

The LVDS pairs that can be used as asynchronous bidirectional buffers are listed in the Virtex-E pinout tables. Some pairs are marked as asynchronous capable for all devices in that package, and others are marked as available only for that device in the package. If the device size might change at some point in the product's lifetime, then only the common pairs for all packages should be used.

Adding Output and 3-State Registers

All LVDS buffers can have an output and input registers in the IOB. The output registers must be in both the P-side and N-side IOBs, the input register is only in the P-side. All the normal IOB register options are available (FD, FDE, FDC, FDCE, FDP, FDPE, FDR, FDRE, FDS, FDSE, LD, LDE, LDC, LDCE, LDP, LDPE). The register elements can be inferred or explicitly instantiated in the HDL code. Special care must be taken to insure that the D pins of the registers are inverted and that the INIT states of the registers are opposite. The 3-state (T), 3-state clock enable (CE), clock pin (C), output clock enable (CE), and set/reset (CLR/PRE or S/R) pins must connect to the same source. Failure to do this leads to a DRC error in the software.

The register elements can be packed in the IOB using the IOB property to TRUE on the register or by using the “map -pr [i|o|b]” where “i” is inputs only, “o” is outputs only and “b” is both inputs and outputs. To improve design coding times VHDL and Verilog synthesis macro libraries have been developed to explicitly create these structures. The bidirectional I/O library macros are listed in Table 44. The 3-state is configured to be 3-stated at GSR and when the PRE,CLR,S or R is asserted and shares its clock enable with the output and input register. If this is not desirable then the library can be updated be the user for the desired functionality. The I/O and IOB inputs to the macros are the external net connections.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply. This is the time required to reach the nominal power supply voltage of the device[1] from 0V. The fastest ramp rate is 0V to nominal voltage in 2 ms, and the slowest allowed ramp rate is 0V to nominal voltage in 50 ms. For more details on power supply requirements, see XAPP158 on www.xilinx.com.

Product (Commercial Grade)	Description[(2)]	Current Requirement[(3)]
XCV50E - XCV600E	Minimum required current supply	500 mA
XCV812E - XCV2000E	Minimum required current supply	1 A
XCV2600E - XCV3200E	Minimum required current supply	1.2 A
Virtex-E Family, Industrial Grade	Minimum required current supply	2 A

Notes:
1. Ramp rate used for this specification is from 0 - 1.8 V DC. Peak current occurs on or near the internal power-on reset threshold and lasts for less than 3 ms.
2. Devices are guaranteed to initialize properly with the minimum current available from the power supply as noted above.
3. Larger currents might result if ramp rates are forced to be faster.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTL[(1)]	– 0.5	0.8	2.0	3.6	0.4	2.4	24	– 24
LVCMOS2	– 0.5	0.7	1.7	2.7	0.4	1.9	12	– 12
LVCMOS18	– 0.5	35% V_{CCO}	65% V_{CCO}	1.95	0.4	V_{CCO} – 0.4	8	– 8
PCI, 3.3 V	– 0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
GTL	– 0.5	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	n/a	40	n/a
GTL+	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	n/a	36	n/a
HSTL I[(3)]	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	8	–8
HSTL III	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	24	–8
HSTL IV	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	48	–8
SSTL3 I	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.6	V_{REF} + 0.6	8	–8
SSTL3 II	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.8	V_{REF} + 0.8	16	–16
SSTL2 I	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.61	V_{REF} + 0.61	7.6	–7.6
SSTL2 II	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.80	V_{REF} + 0.80	15.2	–15.2

Table 7: **PQ240 Differential Pin Pair Summary XCV50E, XCV100E, XCV200E, XCV300E, XCV400E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
48	6	P56	P57	√	-
49	6	P52	P53	2	-
50	6	P49	P50	3	VREF
51	6	P46	P47	4	VREF
52	6	P41	P42	√	-
53	6	P38	P39	2	-
54	6	P35	P36	4	VREF
55	6	P33	P34	5	VREF
56	7	P27	P28	√	-
57	7	P23	P24	4	VREF
58	7	P20	P21	2	-
59	7	P17	P18	√	-
60	7	P12	P13	4	VREF
61	7	P9	P10	3	VREF
62	7	P6	P7	2	-
63	7	P4	P5	6	VREF

Notes:
1. AO in the XCV50E.
2. AO in the XCV50E, 100E, 200E, 300E.
3. AO in the XCV50E, 200E, 300E, 400E.
4. AO in the XCV50E, 300E, 400E.
5. AO in the XCV100E, 200E, 400E.
6. AO in the XCV100E, 400E.
7. AO in the XCV50E, 200E, 400E.
8. AO in the XCV100E.

HQ240 High-Heat Quad Flat-Pack Packages

XCV600E and XCV1000E devices in High-heat dissipation Quad Flat-pack packages have footprint compatibility. Pins labeled I0_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 8, see Table 9 for Differential Pair information.

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P240	VCCO	7
P239	TCK	NA
P238	IO	0
P237	IO_L0N	0
P236	IO_VREF_L0P	0
P235	IO_L1N_YY	0
P234	IO_L1P_YY	0
P233	GND	NA
P232	VCCO	0
P231	IO_VREF	0
P230	IO_VREF	0
P229	IO_VREF_L2N_YY	0
P228	IO_L2P_YY	0
P227	GND	NA
P226	VCCO	0
P225	VCCINT	NA
P224	IO_L3N_YY	0
P223	IO_L3P_YY	0
P222	IO_VREF	0[1]
P221	IO_L4N_Y	0
P220	IO_L4P_Y	0
P219	GND	NA
P218	IO_VREF_L5N_Y	0
P217	IO_L5P_Y	0
P216	IO_VREF	0
P215	IO_LVDS_DLL_L6N	0
P214	VCCINT	NA
P213	GCK3	0
P212	VCCO	0
P211	GND	NA

Table 10: **BG352 — XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
4	IO_VREF_4_L53P_Y	AC12
4	IO_L53N_Y	AD12
4	IO_L54P	AE12
4	IO_L54N	AF12
4	IO	AD13[1]
4	IO_LVDS_DLL_L55P	AC13
4	GCK0	AE13
5	GCK1	AF14
5	IO_LVDS_DLL_L55N	AD14
5	IO	AF15[1]
5	IO	AE15
5	IO_L56P_Y	AD15
5	IO_VREF_5_L56N_Y	AC15
5	IO_L57P_Y	AE16
5	IO_L57N_Y	AE17
5	IO	AD16[1]
5	IO_L58P	AC16
5	IO_L58N	AF18
5	IO	AE18[1]
5	IO_L59P_YY	AD17
5	IO_L59N_YY	AC17
5	IO_L60P_YY	AD18
5	IO_VREF_5_L60N_YY	AC18
5	IO_L61P _Y	AF20
5	IO_L61N _Y	AE20
5	IO	AD19
5	IO	AC19[1]
5	IO	AF21[1]
5	IO_L62P_YY	AE21
5	IO_VREF_5_L62N_YY	AD20
5	IO_L63P_YY	AF23
5	IO_L63N_YY	AE22
5	IO	AD21[1]

Table 10: **BG352 — XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
5	IO_L64P_YY	AC21
5	IO_VREF_5_L64N_YY	AE23[2]
5	IO	AD22
5	IO	AF24[1]
5	IO	AC22[1]
6	IO_L65N_YY	AC24
6	IO_L65P_YY	AD25
6	IO	AB24[1]
6	IO	AA23[1]
6	IO	AC25
6	IO_VREF_6_L66N_YY	AD26[2]
6	IO_L66P_YY	AC26
6	IO	Y23[1]
6	IO_L67N_YY	AA24
6	IO_L67P_YY	AB25
6	IO_VREF_6_L68N_Y	AA25
6	IO_L68P_Y	Y24
6	IO	Y25[1]
6	IO	AA26[1]
6	IO_L69N	V23
6	IO_L69P	W24
6	IO	W25
6	IO_VREF_6_L70N _Y	Y26
6	IO_L70P _Y	U23
6	IO_L71N_YY	V25
6	IO_L71P_YY	U24
6	IO	V26[1]
6	IO_L72N	T23
6	IO_L72P	U25
6	IO	T24[1]
6	IO_L73N_YY	T25
6	IO_L73P_YY	T26
6	IO_VREF_6_L74N _Y	R24

Table 13: **BG432 Differential Pin Pair Summary XCV300E, XCV400E, XC600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
112	6	AB29	AB28	√	VREF
113	6	AA29	AB31	√	-
114	6	Y29	Y28	4	-
115	6	Y31	Y30	1	-
116	6	W30	W29	1	-
117	6	V29	V28	√	VREF
118	6	U29	V30	4	-
119	6	U30	U28	1	VREF
120	7	R29	T31	√	-
121	7	R31	R30	1	VREF
122	7	P28	P29	4	-
123	7	N30	P30	√	VREF
124	7	N31	N28	1	-
125	7	M28	M29	1	-
126	7	L30	M30	4	-
127	7	K30	K31	√	-
128	7	J30	K28	√	VREF
129	7	J28	J29	1	VREF
130	7	G30	H30	4	-
131	7	F31	H28	√	VREF
132	7	G28	G29	1	-
133	7	E30	E31	5	-
134	7	F28	F29	1	VREF
135	7	D30	D31	4	-
136	7	E28	E29	3	-

Notes:
1. AO in the XCV300E, 600E.
2. AO in the XCV300E.
3. AO in the XCV400E, 600E.
4. AO in the XCV300E, 400E.
5. AO in the XCV600E.

BG560 Ball Grid Array Packages

XCV1000E, XCV1600E, and XCV2000E devices in BG560 Ball Grid Array packages have footprint compatibility. Pins labeled I0_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 14, see Table 15 for Differential Pair information.

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
0	GCK3	A17	
0	IO	A27	
0	IO	B25	
0	IO	C28	
0	IO	C30	
0	IO	D30	
0	IO_L0N	E28	
0	IO_VREF_L0P	D29	3
0	IO_L1N_YY	D28	
0	IO_L1P_YY	A31	
0	IO_VREF_L2N_YY	E27	
0	IO_L2P_YY	C29	
0	IO_L3N_Y	B30	
0	IO_L3P_Y	D27	
0	IO_L4N_YY	E26	
0	IO_L4P_YY	B29	
0	IO_VREF_L5N_YY	D26	
0	IO_L5P_YY	C27	
0	IO_L6N_Y	E25	
0	IO_VREF_L6P_Y	A28	1
0	IO_L7N_Y	D25	
0	IO_L7P_Y	C26	
0	IO_VREF_L8N_Y	E24	4
0	IO_L8P_Y	B26	
0	IO_L9N_Y	C25	
0	IO_L9P_Y	D24	
0	IO_VREF_L10N_YY	E23	
0	IO_L10P_YY	A25	
0	IO_L11N_YY	D23	

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
4	IO_L104N_YY	AJ12	
4	IO_L105P_Y	AN11	
4	IO_L105N_Y	AK12	
4	IO_L106P_YY	AL12	
4	IO_L106N_YY	AM12	
4	IO_VREF_L107P_YY	AK13	3
4	IO_L107N_YY	AL13	
4	IO_L108P_Y	AM13	
4	IO_L108N_Y	AN13	
4	IO_L109P_YY	AJ14	
4	IO_L109N_YY	AK14	
4	IO_VREF_L110P_YY	AM14	
4	IO_L110N_YY	AN15	
4	IO_L111P_Y	AJ15	
4	IO_L111N_Y	AK15	
4	IO_L112P_Y	AL15	
4	IO_L112N_Y	AM16	
4	IO_VREF_L113P_Y	AL16	
4	IO_L113N_Y	AJ16	
4	IO_L114P_Y	AK16	
4	IO_VREF_L114N_Y	AN17	2
4	IO_LVDS_DLL_L115P	AM17	
5	GCK1	AJ17	
5	IO	AL25	
5	IO	AL28	
5	IO	AL30	
5	IO	AN28	
5	IO_LVDS_DLL_L115N	AM18	
5	IO_VREF	AL18	2
5	IO_L116P_Y	AK18	
5	IO_VREF_L116N_Y	AJ18	
5	IO_L117P_Y	AN19	
5	IO_L117N_Y	AL19	
5	IO_L118P_Y	AK19	
5	IO_L118N_Y	AM20	
5	IO_L119P_YY	AJ19	
5	IO_VREF_L119N_YY	AL20	
5	IO_L120P_YY	AN21	
5	IO_L120N_YY	AL21	
5	IO_L121P_Y	AJ20	
5	IO_L121N_Y	AM22	
5	IO_L122P_YY	AK21	
5	IO_VREF_L122N_YY	AN23	3
5	IO_L123P_YY	AJ21	
5	IO_L123N_YY	AM23	
5	IO_L124P_Y	AK22	
5	IO_L124N_Y	AM24	
5	IO_L125P_YY	AL23	
5	IO_L125N_YY	AJ22	
5	IO_L126P_YY	AK23	
5	IO_VREF_L126N_YY	AL24	
5	IO_L127P_Y	AN26	
5	IO_L127N_Y	AJ23	
5	IO_L128P_Y	AK24	
5	IO_VREF_L128N_Y	AM26	4
5	IO_L129P_Y	AM27	
5	IO_L129N_Y	AJ24	
5	IO_L130P_Y	AL26	
5	IO_VREF_L130N_Y	AK25	1
5	IO_L131P_YY	AN29	
5	IO_VREF_L131N_YY	AJ25	
5	IO_L132P_YY	AK26	
5	IO_L132N_YY	AM29	
5	IO_L133P_Y	AM30	
5	IO_L133N_Y	AJ26	
5	IO_L134P_YY	AK27	
5	IO_VREF_L134N_YY	AL29	
5	IO_L135P_YY	AN31	
5	IO_L135N_YY	AJ27	

BG560 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 15: **BG560 Differential Pin Pair Summary XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	AL17	AM17	NA	IO_DLL_L15P
1	5	AJ17	AM18	NA	IO_DLL_L15N
2	1	D17	E17	NA	IO_DLL_L21P
3	0	A17	C18	NA	IO_DLL_L21N
IO LVDS Total Outputs: 183, Asynchronous Outputs: 87					
0	0	D29	E28	8	VREF
1	0	A31	D28	√	-
2	0	C29	E27	√	VREF
3	0	D27	B30	3	-
4	0	B29	E26	√	-
5	0	C27	D26	√	VREF
6	0	A28	E25	9	VREF
7	0	C26	D25	7	-
8	0	B26	E24	7	VREF
9	0	D24	C25	2	-
10	0	A25	E23	√	VREF
11	0	B24	D23	√	-
12	0	C23	E22	8	-
13	0	D22	A23	√	-
14	0	B22	E21	√	VREF
15	0	C21	D21	3	-

Table 15: **BG560 Differential Pin Pair Summary XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
16	0	E20	B21	√	-
17	0	C20	D20	√	VREF
18	0	E19	B20	9	-
19	0	C19	D19	7	-
20	0	D18	A19	7	VREF
21	1	E17	C18	NA	IO_LVDS_DLL
22	1	B17	C17	2	VREF
23	1	D16	B16	7	VREF
24	1	C16	E16	7	-
25	1	C15	A15	9	-
26	1	E15	D15	√	VREF
27	1	D14	C14	√	-
28	1	E14	A13	3	-
29	1	D13	C13	√	VREF
30	1	E13	C12	√	-
31	1	D12	A11	8	-
32	1	C11	B11	√	-
33	1	D11	B10	√	VREF
34	1	A9	C10	10	-
35	1	D10	C9	7	VREF
36	1	B8	A8	7	-
37	1	C8	E10	5	VREF
38	1	A6	B7	√	VREF
39	1	D8	C7	√	-
40	1	B5	A5	11	-
41	1	D7	C6	√	VREF
42	1	B4	A4	√	-
43	1	E7	C5	12	VREF
44	1	A2	D6	√	CS
45	2	D4	E4	√	DIN, D0
46	2	F5	B3	17	VREF

Table 15: **BG560 Differential Pin Pair Summary XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
47	2	F4	C1	14	-
48	2	G5	E3	15	VREF
49	2	D2	G4	16	-
50	2	H5	E2	15	-
51	2	H4	G3	√	VREF
52	2	J5	F1	17	VREF
53	2	J4	H3	14	-
54	2	K5	H2	18	VREF
55	2	J3	K4	19	-
56	2	L5	K3	√	D1
57	2	L4	K2	√	D2
58	2	M5	L3	17	-
59	2	L1	M4	14	-
60	2	N5	M2	15	VREF
61	2	N4	N3	16	-
62	2	N2	P5	15	-
63	2	P4	P3	√	D3
64	2	P2	R5	17	-
65	2	R4	R3	14	-
66	2	R1	T4	18	VREF
67	2	T5	T3	19	VREF
68	2	T2	U3	√	-
69	3	U1	U2	19	VREF
70	3	V2	V4	18	VREF
71	3	V5	V3	14	-
72	3	W1	W3	17	-
73	3	W4	W5	√	VREF
74	3	Y3	Y4	15	-
75	3	AA1	Y5	16	-
76	3	AA3	AA4	15	VREF
77	3	AB3	AA5	14	-

Table 15: **BG560 Differential Pin Pair Summary XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
78	3	AC1	AB4	17	-
79	3	AC3	AB5	√	D5
80	3	AC4	AD3	√	VREF
81	3	AE1	AC5	4	-
82	3	AD4	AF1	18	VREF
83	3	AF2	AD5	14	-
84	3	AG2	AE4	20	VREF
85	3	AH1	AE5	√	VREF
86	3	AF4	AJ1	15	-
87	3	AJ2	AF5	14	-
88	3	AG4	AK2	15	VREF
89	3	AJ3	AG5	14	-
90	3	AL1	AH4	14	VREF
91	3	AJ4	AH5	√	INIT
92	4	AL4	AJ6	√	-
93	4	AK5	AN3	8	VREF
94	4	AL5	AJ7	√	-
95	4	AM4	AM5	√	VREF
96	4	AK7	AL6	3	-
97	4	AM6	AN6	√	-
98	4	AL7	AJ9	√	VREF
99	4	AN7	AL8	9	VREF
100	4	AM8	AJ10	7	-
101	4	AL9	AM9	7	VREF
102	4	AK10	AN9	2	-
103	4	AL10	AM10	√	VREF
104	4	AL11	AJ12	√	-
105	4	AN11	AK12	8	-
106	4	AL12	AM12	√	-
107	4	AK13	AL13	√	VREF
108	4	AM13	AN13	3	-

Table 19: **FG456 Differential Pin Pair Summary XCV200E, XCV300E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
18	1	C14	B14	2	-
19	1	A15	F12	2	-
20	1	C15	B15	√	-
21	1	E14	A16	√	VREF
22	1	C16	D14	2	-
23	1	A17	D15	2	-
24	1	A18	B17	√	VREF
25	1	C17	D16	√	-
26	1	A19	B18	√	VREF
27	1	C18	D17	√	-
28	1	C19	A20	√	CS
29	2	C21	D20	√	DIN, D0
30	2	C22	D21	√	-
31	2	D22	E21	√	VREF
32	2	E22	F18	√	-
33	2	F21	F19	√	VREF
34	2	F22	G19	2	-
35	2	G20	G18	1	-
36	2	H18	H22	2	D1, VREF
37	2	H20	H19	√	D2
38	2	H21	J19	√	-
39	2	J18	J20	√	-
40	2	K18	J21	2	-
41	2	K22	K21	1	VREF
42	2	K19	L22	2	-
43	2	L21	L18	√	-
44	2	L17	L20	√	-
45	3	M18	M20	√	-
46	3	M19	M17	2	-
47	3	N22	N21	2	VREF
48	3	N20	N18	√	-
49	3	N19	P21	√	-
50	3	P20	P19	√	-
51	3	P18	R21	√	D5
52	3	T22	R19	2	VREF
53	3	U22	R18	2	-
54	3	T21	V22	√	-
55	3	T20	U21	√	VREF
56	3	W22	T18	√	-
57	3	U19	U20	√	VREF
58	3	W21	AA22	√	-
59	3	Y21	V19	√	INIT
60	4	W18	AA20	√	-
61	4	Y18	V17	NA	-
62	4	AB20	W17	√	VREF
63	4	AA18	V16	NA	-
64	4	AB19	AB18	√	VREF
65	4	W16	AA17	1	-
66	4	Y16	V15	1	-
67	4	AB16	Y15	√	VREF
68	4	AA15	AB15	√	-
69	4	W15	Y14	1	-
70	4	V14	AA14	1	-
71	4	AB14	V13	NA	-
72	4	AA13	AB13	√	VREF
73	4	W13	AA12	2	-
74	4	Y12	V12	2	-
75	5	U12	AA11	NA	IO_LVDS_DLL
76	5	AB11	W11	1	-
77	5	V11	Y10	√	VREF
78	5	AB10	W10	√	-
79	5	V10	Y9	2	-
80	5	AB9	W9	2	-
81	5	V9	AA8	√	-
82	5	Y8	W8	√	VREF
83	5	W7	AA7	2	-
84	5	AB6	AA6	2	-
85	5	AB5	AA5	√	VREF
86	5	Y7	W6	√	-
87	5	AA4	Y6	√	VREF

FG680 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 23: **FG680 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
GCLK LVDS					
3	0	A20	C22	NA	IO_DLL_L29N
2	1	D21	A19	NA	IO_DLL_L29P
1	5	AU22	AT22	NA	IO_DLL_L155N
0	4	AW19	AT21	NA	IO_DLL_L155P
IO LVDS Total Pairs: 247, Asynchronous Output Pairs: 111					
0	0	A36	C35	5	-
1	0	B35	D34	5	VREF
2	0	A35	C34	√	-
3	0	B34	D33	√	VREF
4	0	A34	C33	3	-
5	0	B33	D32	3	-
6	0	D31	C32	√	-
7	0	C31	A33	√	VREF
8	0	B31	B32	5	-
9	0	D30	A32	5	VREF
10	0	C30	A31	√	-
11	0	D29	B30	√	VREF
12	0	C29	A30	2	-
13	0	B29	A29	2	-
14	0	A28	B28	√	VREF
15	0	B27	C28	√	-
16	0	A27	D27	5	-
17	0	B26	C27	5	-

Table 23: **FG680 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
18	0	C26	D26	√	-
19	0	D25	A26	√	VREF
20	0	C25	B25	3	-
21	0	D24	A25	3	-
22	0	B23	A24	√	-
23	0	A23	C24	√	VREF
24	0	B22	B24	5	-
25	0	A22	E23	5	-
26	0	B21	D23	√	-
27	0	A21	C23	√	VREF
28	0	B20	E22	2	-
29	1	A19	C22	NA	IO_LVDS_DLL
30	1	B19	C21	2	VREF
31	1	A18	C19	2	-
32	1	B18	D19	√	VREF
33	1	A17	C18	√	-
34	1	B17	D18	5	-
35	1	A16	E18	5	-
36	1	D17	C17	√	VREF
37	1	E17	B16	√	-
38	1	C16	A15	3	-
39	1	D16	B15	3	-
40	1	B14	A14	√	VREF
41	1	A13	C15	√	-
42	1	B13	D15	5	-
43	1	A12	C14	5	-
44	1	C13	D14	√	-
45	1	D13	B12	√	VREF
46	1	C12	A11	2	-
47	1	C11	B11	2	-
48	1	D11	A10	√	VREF
49	1	C10	B10	√	-
50	1	D10	A9	5	VREF
51	1	C9	B9	5	-

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
0	IO_VREF_L27N_YY	D27
0	IO_L27P_YY	B25
0	IO_L28N_Y	A25
0	IO_L28P_Y	D26
0	IO_L29N_Y	A24
0	IO_L29P_Y	E25
0	IO_L30N_YY	D25
0	IO_L30P_YY	B24
0	IO_VREF_L31N_YY	E24
0	IO_L31P_YY	A23
0	IO_L32N_Y	C23
0	IO_L32P_Y	E23
0	IO_VREF_L33N_Y	B23[1]
0	IO_L33P_Y	D23
0	IO_LVDS_DLL_L34N	A22
1	GCK2	B22
1	IO	A14
1	IO	A20
1	IO	B11
1	IO	B13
1	IO	C8
1	IO	C18
1	IO	C21
1	IO	D7
1	IO	D10
1	IO	D15
1	IO	D17
1	IO	E20
1	IO_LVDS_DLL_L34P	D22
1	IO_L35N_Y	D21
1	IO_VREF_L35P_Y	B21[1]
1	IO_L36N_Y	D20
1	IO_L36P_Y	A21
1	IO_L37N_YY	C20
1	IO_VREF_L37P_YY	D19
1	IO_L38N_YY	B20

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
1	IO_L38P_YY	E19
1	IO_L39N_Y	D18
1	IO_L39P_Y	A19
1	IO_L40N_Y	E18
1	IO_L40P_Y	C19
1	IO_L41N_YY	B19
1	IO_VREF_L41P_YY	E17
1	IO_L42N_YY	A18
1	IO_L42P_YY	D16
1	IO_L43N_Y	E16
1	IO_L43P_Y	B18
1	IO_L44N_Y	F16
1	IO_L44P_Y	A17
1	IO_L45N_YY	C17
1	IO_VREF_L45P_YY	E15
1	IO_L46N_YY	B17
1	IO_L46P_YY	D14
1	IO_L47N_Y	A16
1	IO_L47P_Y	E14
1	IO_L48N_Y	C16
1	IO_L48P_Y	D13
1	IO_L49N_Y	B16
1	IO_L49P_Y	D12
1	IO_L50N_Y	A15
1	IO_L50P_Y	E12
1	IO_L51N_YY	C15
1	IO_L51P_YY	C11
1	IO_L52N_YY	B15
1	IO_VREF_L52P_YY	D11
1	IO_L53N_Y	E11
1	IO_L53P_Y	C14
1	IO_L54N_Y	C10
1	IO_L54P_Y	B14
1	IO_L55N_YY	A13
1	IO_VREF_L55P_YY	E10
1	IO_L56N_YY	C13
1	IO_L56P_YY	C9

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
NA	GND	AG27
NA	GND	D27
NA	GND	AF26
NA	GND	E26
NA	GND	F25
NA	GND	AE25
NA	GND	G24
NA	GND	AJ23
NA	GND	AD24
NA	GND	H23
NA	GND	B23
NA	GND	AC23
NA	GND	AB22
NA	GND	V22
NA	GND	N22
NA	GND	AH18
NA	GND	AB18
NA	GND	J18
NA	GND	C18
NA	GND	U17
NA	GND	T17
NA	GND	R17
NA	GND	P17
NA	GND	U16
NA	GND	T16
NA	GND	R16
NA	GND	P16
NA	GND	U15
NA	GND	T15
NA	GND	R15
NA	GND	P15
NA	GND	U14
NA	GND	T14
NA	GND	R14
NA	GND	P14
NA	GND	AH13
NA	GND	AB13

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
NA	GND	J13
NA	GND	C13
NA	GND	V9
NA	GND	N9
NA	GND	J9
NA	GND	AJ8
NA	GND	AC8
NA	GND	H8
NA	GND	AD7
NA	GND	B8
NA	GND	AE6
NA	GND	G7
NA	GND	F6
NA	GND	AF5
NA	GND	E5
NA	GND	AG4
NA	GND	D4
NA	GND	V3
NA	GND	N3
NA	GND	C3
NA	GND	AK2
NA	GND	AH3
NA	GND	AC2
NA	GND	H2
NA	GND	B2
NA	GND	A2
NA	GND	AK1
NA	GND	AJ2
NA	GND	AJ1
NA	GND	A1
NA	GND	B1

Notes:
1. V_{REF} or I/O option only in the XCV1000E and XCV1600E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV1600E; otherwise, I/O option only.
3. I/O option only in the XCV600E.
4. No Connect in the XCV600E.
5. No Connect in the XCV600E, 1000E.

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
NA	VCCINT	N22
NA	VCCINT	P13
NA	VCCINT	P22
NA	VCCINT	R13
NA	VCCINT	R22
NA	VCCINT	T13
NA	VCCINT	T22
NA	VCCINT	U10
NA	VCCINT	U25
NA	VCCINT	V10
NA	VCCINT	V25
NA	VCCINT	W13
NA	VCCINT	W22
NA	VCCINT	Y13
NA	VCCINT	Y22
NA	VCCINT	AA13
NA	VCCINT	AA22
NA	VCCINT	AB13
NA	VCCINT	AB14
NA	VCCINT	AB15
NA	VCCINT	AB16
NA	VCCINT	AB19
NA	VCCINT	AB20
NA	VCCINT	AB21
NA	VCCINT	AB22
NA	VCCINT	AC12
NA	VCCINT	AC23
NA	VCCINT	AD24
NA	VCCINT	AD11
NA	VCCINT	AE10
NA	VCCINT	AE17
NA	VCCINT	AE18
NA	VCCINT	AE25

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
NA	VCCO_0	M17
NA	VCCO_0	L17
NA	VCCO_0	L16
NA	VCCO_0	E10
NA	VCCO_0	C14
NA	VCCO_0	A6
NA	VCCO_0	M13
NA	VCCO_0	M14
NA	VCCO_0	M15
NA	VCCO_0	M16
NA	VCCO_0	L12
NA	VCCO_0	L13
NA	VCCO_0	L14
NA	VCCO_0	L15
NA	VCCO_1	M18
NA	VCCO_1	L18
NA	VCCO_1	L23
NA	VCCO_1	E25
NA	VCCO_1	C21
NA	VCCO_1	A29
NA	VCCO_1	M19
NA	VCCO_1	M20
NA	VCCO_1	M21
NA	VCCO_1	M22
NA	VCCO_1	L19
NA	VCCO_1	L20
NA	VCCO_1	L21
NA	VCCO_1	L22
NA	VCCO_2	U24
NA	VCCO_2	U23
NA	VCCO_2	N24
NA	VCCO_2	M24
NA	VCCO_2	K30
NA	VCCO_2	F34

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
111	2	M31	R26	2600 1600	-
112	2	N30	P28	3200 1600 1000	-
113	2	N29	N33	2600 2000 1000	VREF
114	2	T25	N34	3200 2600 2000 1600	-
115	2	P34	R27	3200 2600 2000 1600 1000	-
116	2	P29	P31	3200 2600 1600 1000	-
117	2	P33	T26	3200 2600 2000	-
118	2	R34	R28	2600 2000 1000	-
119	2	N31	N32	2000 1600 1000	D3
120	2	P30	R33	2000 1600	-
121	2	R29	T34	3200 2600 2000 1600 1000	-
122	2	R30	T30	1000	-
123	2	T28	R31	3200 1600	-
124	2	T29	U27	3200 2600 1600 1000	-
125	2	T31	T33	2000 1600 1000	VREF
126	2	U28	T32	2000 1600 1000	-
127	2	U29	U33	3200 2600 1600 1000	VREF
128	2	V33	U31	3200 2600 2000 1600 1000	-
129	3	V26	V30	3200 2600 1600 1000	VREF
130	3	W34	V28	2000 1600 1000	-
131	3	W32	W30	2000 1600 1000	VREF

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
132	3	V29	Y34	3200 2600 1600 1000	-
133	3	W29	Y33	3200 1600	-
134	3	W26	W28	1000	-
135	3	Y31	Y30	3200 2600 2000 1600 1000	-
136	3	AA34	W31	2000 1600	-
137	3	AA33	Y29	2000 1600 1000	VREF
138	3	W25	AB34	2600 2000 1000	-
139	3	Y28	AB33	3200 2600 2000	-
140	3	AA30	Y26	3200 2600 1600 1000	-
141	3	Y27	AA31	3200 2600 2000 1600 1000	-
142	3	AA27	AA29	3200 2600 2000 1600	-
143	3	AB32	AB29	2600 2000 1000	VREF
144	3	AA28	AC34	3200 1600 1000	-
145	3	Y25	AD34	2600 1600	-
146	3	AB30	AC33	3200 2600 1600 1000	-
147	3	AA26	AC32	2000 1000	-
148	3	AD33	AB28	3200 2600 2000	-
149	3	AE34	AB27	3200 2600 2000 1600 1000	D5
150	3	AE33	AC30	2000 1600 1000	VREF
151	3	AA25	AE32	3200 1600 1000	-
152	3	AE31	AD29	3200 2600 2000 1600 1000	-