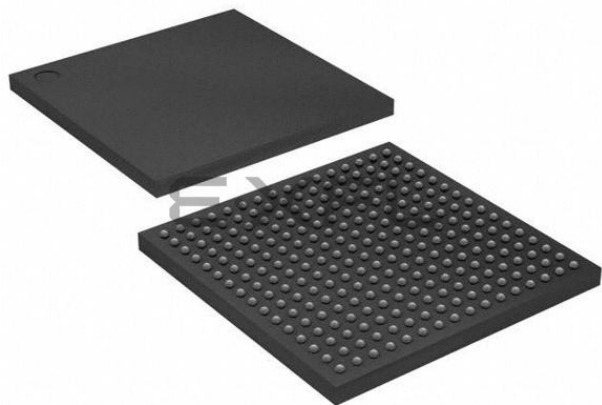




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

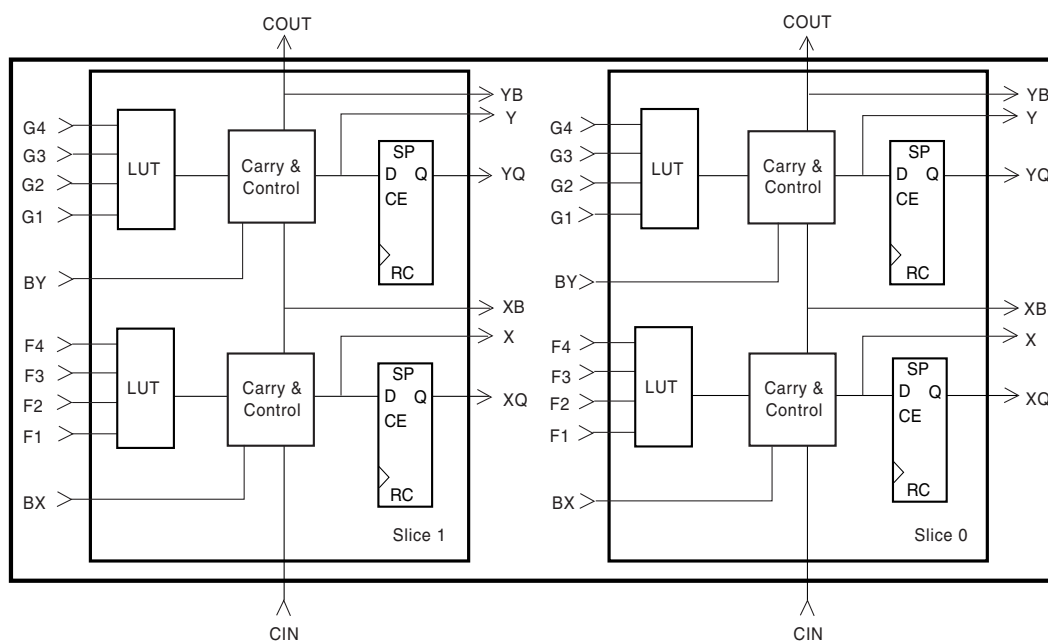
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

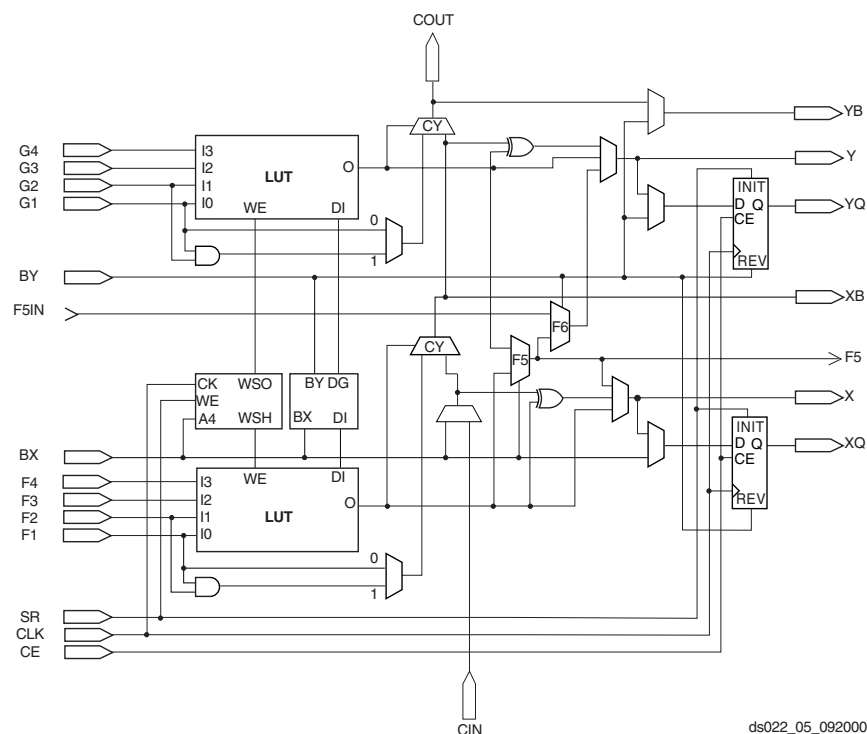
Details

Product Status	Obsolete
Number of LABs/CLBs	384
Number of Logic Elements/Cells	1728
Total RAM Bits	65536
Number of I/O	176
Number of Gates	71693
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv50e-7fg256i



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Figure 4: 2-Slice Virtex-E CLB



ds022_05_092000

Figure 5: Detailed View of Virtex-E Slice

Storage Elements

The storage elements in the Virtex-E slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by

the function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each Slice has synchronous set and reset signals (SR and BY). SR

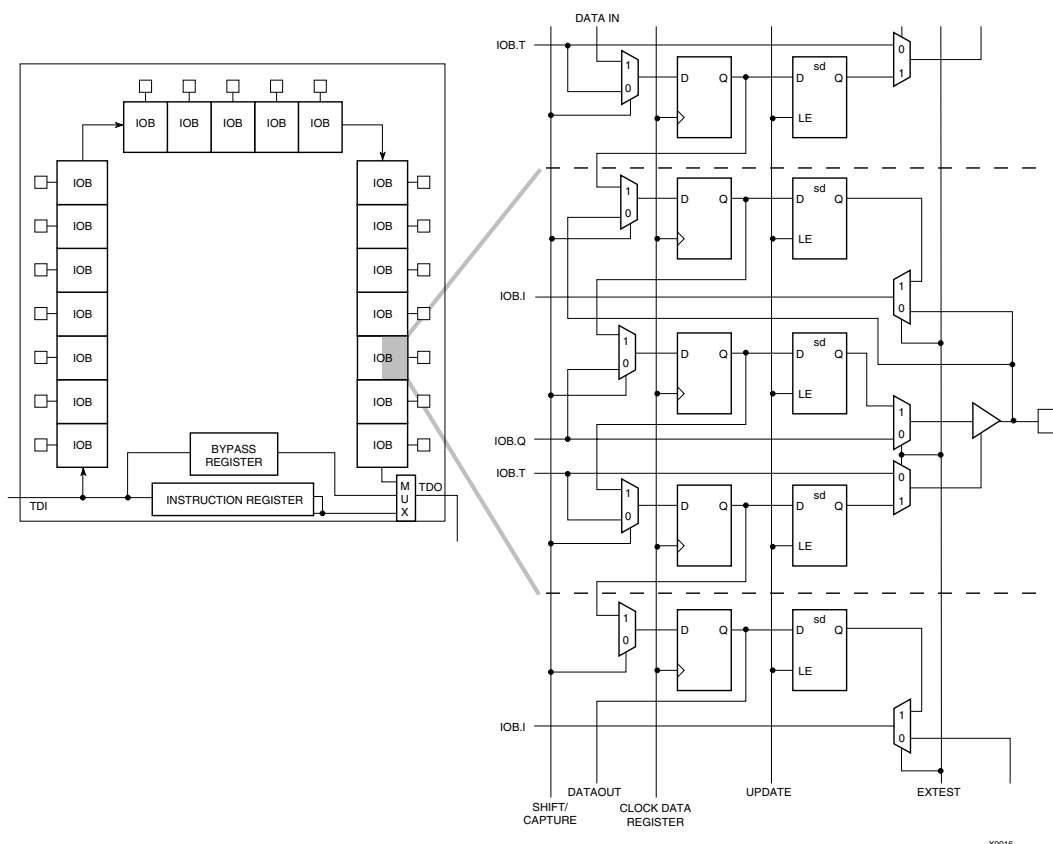


Figure 11: Virtex-E Family Boundary Scan Logic

Instruction Set

The Virtex-E series Boundary Scan instruction set also includes instructions to configure the device and read back configuration data (CFG_IN, CFG_OUT, and JSTART). The complete instruction set is coded as shown in Table 6..

Table 6: Boundary Scan Instructions

Boundary Scan Command	Binary Code(4:0)	Description
EXTEST	00000	Enables Boundary Scan EXTEST operation
SAMPLE/PRELOAD	00001	Enables Boundary Scan SAMPLE/PRELOAD operation
USER1	00010	Access user-defined register 1
USER2	00011	Access user-defined register 2
CFG_OUT	00100	Access the configuration bus for read operations.

Table 6: Boundary Scan Instructions (Continued)

Boundary Scan Command	Binary Code(4:0)	Description
CFG_IN	00101	Access the configuration bus for write operations.
INTEST	00111	Enables Boundary Scan INTEST operation
USERCODE	01000	Enables shifting out USER code
IDCODE	01001	Enables shifting out of ID Code
HIGHZ	01010	3-states output pins while enabling the Bypass Register
JSTART	01100	Clock the start-up sequence when StartupClk is TCK
BYPASS	11111	Enables BYPASS
RESERVED	All other codes	Xilinx reserved instructions

Verilog Initialization Example

```

module MYMEM (CLK, WE, ADDR, DIN, DOUT);
input CLK, WE;
input [8:0] ADDR;
input [7:0] DIN;
output [7:0] DOUT;

wire logic0, logic1;

//synopsys dc_script_begin
//set_attribute ram0 INIT_00
"0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF" -type string
//set_attribute ram0 INIT_01
"FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210" -type string
//synopsys dc_script_end

assign logic0 = 1'b0;
assign logic1 = 1'b1;

RAMB4_S8 ram0 (.WE(WE), .EN(logic1), .RST(logic0), .CLK(CLK), .ADDR(ADDR), .DI(DIN),
.DO(DOUT));
//synopsys translate_off
defparam ram0.INIT_00 =
256h'0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF;
defparam ram0.INIT_01 =
256h'FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210;
//synopsys translate_on
endmodule

```

Using SelectI/O

The Virtex-E FPGA series includes a highly configurable, high-performance I/O resource, called SelectI/O™ to provide support for a wide variety of I/O standards. The SelectI/O resource is a robust set of features including programmable control of output drive strength, slew rate, and input delay and hold time. Taking advantage of the flexibility and SelectI/O features and the design considerations described in this document can improve and simplify system level design.

Introduction

As FPGAs continue to grow in size and capacity, the larger and more complex systems designed for them demand an increased variety of I/O standards. Furthermore, as system clock speeds continue to increase, the need for high performance I/O becomes more important.

While chip-to-chip delays have an increasingly substantial impact on overall system speed, the task of achieving the desired system performance becomes more difficult with the proliferation of low-voltage I/O standards. SelectI/O, the revolutionary input/output resources of Virtex-E devices, resolve this potential problem by providing a highly configurable, high-performance alternative to the I/O resources of more conventional programmable devices. Virtex-E SelectI/O features combine the flexibility and time-to-market advantages of programmable logic with the high performance previously available only with ASICs and custom ICs.

Each SelectI/O block can support up to 20 I/O standards. Supporting such a variety of I/O standards allows the support of a wide variety of applications, from general purpose standard applications to high-speed low-voltage memory buses.

SelectI/O blocks also provide selectable output drive strengths and programmable slew rates for the LVTTTL output buffers, as well as an optional, programmable weak pull-up, weak pull-down, or weak “keeper” circuit ideal for use in external bussing applications.

Each Input/Output Block (IOB) includes three registers, one each for the input, output, and 3-state signals within the IOB. These registers are optionally configurable as either a D-type flip-flop or as a level sensitive latch.

The input buffer has an optional delay element used to guarantee a zero hold time requirement for input signals registered within the IOB.

The Virtex-E SelectI/O features also provide dedicated resources for input reference voltage (V_{REF}) and output source voltage (V_{CCO}), along with a convenient banking system that simplifies board design.

By taking advantage of the built-in features and wide variety of I/O standards supported by the SelectI/O features, system-level design and board design can be greatly simplified and improved.

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used, see [Figure 2](#). The values listed below are worst-case. Precise values are provided by the timing analyzer.

		Speed Grade ⁽¹⁾				Units
Description	Symbol	Min	-8	-7	-6	
Combinatorial Delays						
4-input function: F/G inputs to X/Y outputs	T _{ILO}	0.19	0.40	0.42	0.47	ns, max
5-input function: F/G inputs to F5 output	T _{IF5}	0.36	0.76	0.8	0.9	ns, max
5-input function: F/G inputs to X output	T _{IF5X}	0.35	0.74	0.8	0.9	ns, max
6-input function: F/G inputs to Y output via F6 MUX	T _{IF6Y}	0.35	0.74	0.9	1.0	ns, max
6-input function: F5IN input to Y output	T _{F5INY}	0.04	0.11	0.20	0.22	ns, max
Incremental delay routing through transparent latch to XQ/YQ outputs	T _{IFNCTL}	0.27	0.63	0.7	0.8	ns, max
BY input to YB output	T _{BYYB}	0.19	0.38	0.46	0.51	ns, max
Sequential Delays						
FF Clock CLK to XQ/YQ outputs	T _{CKO}	0.34	0.78	0.9	1.0	ns, max
Latch Clock CLK to XQ/YQ outputs	T _{CKLO}	0.40	0.77	0.9	1.0	ns, max
Setup and Hold Times before/after Clock CLK						
4-input function: F/G Inputs	T _{ICK} / T _{CKI}	0.39 / 0	0.9 / 0	1.0 / 0	1.1 / 0	ns, min
5-input function: F/G inputs	T _{IF5CK} / T _{CKIF5}	0.55 / 0	1.3 / 0	1.4 / 0	1.5 / 0	ns, min
6-input function: F5IN input	T _{F5INCK} / T _{CKF5IN}	0.27 / 0	0.6 / 0	0.8 / 0	0.8 / 0	ns, min
6-input function: F/G inputs via F6 MUX	T _{IF6CK} / T _{CKIF6}	0.58 / 0	1.3 / 0	1.5 / 0	1.6 / 0	ns, min
BX/BY inputs	T _{DICK} / T _{CKDI}	0.25 / 0	0.6 / 0	0.7 / 0	0.8 / 0	ns, min
CE input	T _{CECK} / T _{CKCE}	0.28 / 0	0.55 / 0	0.7 / 0	0.7 / 0	ns, min
SR/BY inputs (synchronous)	T _{RCK} / T _{CKR}	0.24 / 0	0.46 / 0	0.52 / 0	0.6 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T _{CH}	0.56	1.2	1.3	1.4	ns, min
Minimum Pulse Width, Low	T _{CL}	0.56	1.2	1.3	1.4	ns, min
Set/Reset						
Minimum Pulse Width, SR/BY inputs	T _{RPW}	0.94	1.9	2.1	2.4	ns, min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T _{RQ}	0.39	0.8	0.9	1.0	ns, max
Toggle Frequency (MHz) (for export control)	F _{TOG}	-	416	400	357	MHz

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

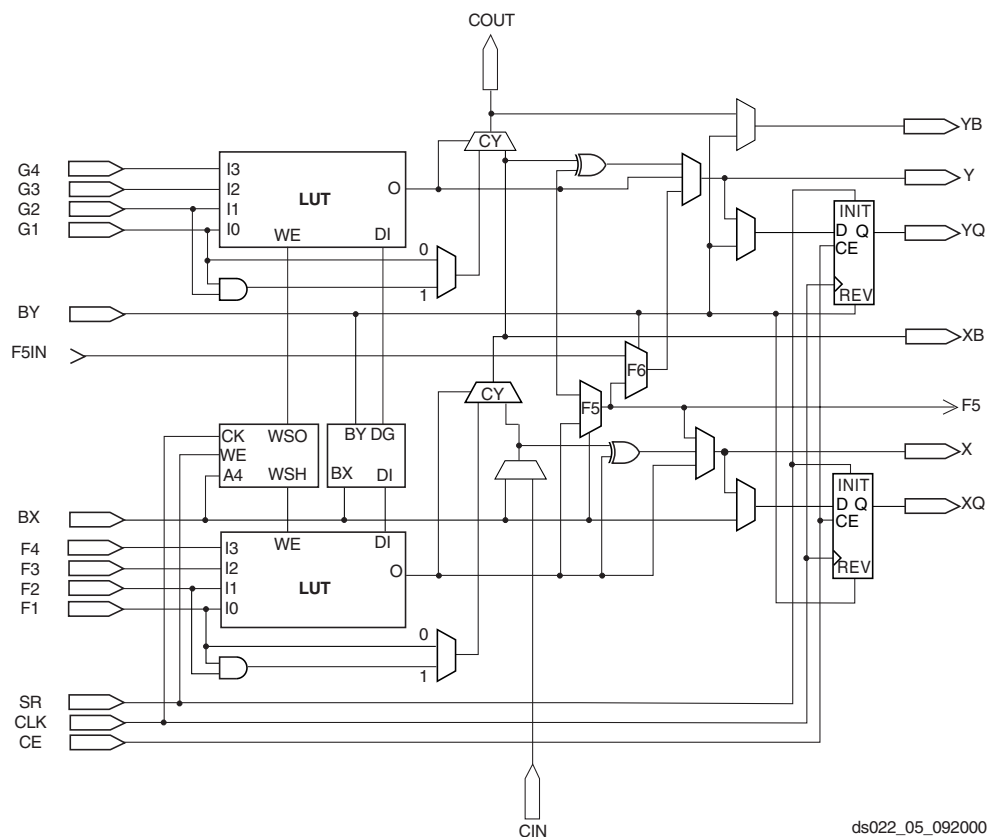


Figure 2: Detailed View of Virtex-E Slice

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Virtex-E Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *with* DLL

Description ⁽¹⁾	Symbol	Device	Speed Grade ^(2, 3)				Units
			Min	-8	-7	-6	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, <i>with</i> DLL. For data <i>output</i> with different standards, adjust the delays with the values shown in IOB Output Switching Characteristics Standard Adjustments , page 10.	T _{ICKOFDLL}	XCV50E	1.0	3.1	3.1	3.1	ns
		XCV100E	1.0	3.1	3.1	3.1	ns
		XCV200E	1.0	3.1	3.1	3.1	ns
		XCV300E	1.0	3.1	3.1	3.1	ns
		XCV400E	1.0	3.1	3.1	3.1	ns
		XCV600E	1.0	3.1	3.1	3.1	ns
		XCV1000E	1.0	3.1	3.1	3.1	ns
		XCV1600E	1.0	3.1	3.1	3.1	ns
		XCV2000E	1.0	3.1	3.1	3.1	ns
		XCV2600E	1.0	3.1	3.1	3.1	ns
		XCV3200E	1.0	3.1	3.1	3.1	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For other I/O standards and different loads, see [Table 3](#) and [Table 4](#).
3. DLL output jitter is already included in the timing calculation.

Table 6: PQ240 — XCV50E, XCV100E, XCV200E, XCV300E, XCV400E

Pin #	Pin Description	Bank
P137	VCCINT	NA
P104	VCCINT	NA
P88	VCCINT	NA
P77	VCCINT	NA
P43	VCCINT	NA
P32	VCCINT	NA
P16	VCCINT	NA
P240	VCCO	7
P232	VCCO	0
P226	VCCO	0
P212	VCCO	0
P207	VCCO	1
P197	VCCO	1
P180	VCCO	1
P176	VCCO	2
P165	VCCO	2
P150	VCCO	2
P146	VCCO	3
P136	VCCO	3
P121	VCCO	3
P116	VCCO	4
P105	VCCO	4
P90	VCCO	4
P85	VCCO	5
P76	VCCO	5
P61	VCCO	5
P55	VCCO	6
P44	VCCO	6
P30	VCCO	6
P25	VCCO	7
P15	VCCO	7
P233	GND	NA
P227	GND	NA

Table 6: PQ240 — XCV50E, XCV100E, XCV200E, XCV300E, XCV400E

Pin #	Pin Description	Bank
P219	GND	NA
P211	GND	NA
P204	GND	NA
P196	GND	NA
P190	GND	NA
P182	GND	NA
P172	GND	NA
P166	GND	NA
P158	GND	NA
P151	GND	NA
P143	GND	NA
P135	GND	NA
P129	GND	NA
P119	GND	NA
P112	GND	NA
P106	GND	NA
P98	GND	NA
P91	GND	NA
P83	GND	NA
P75	GND	NA
P69	GND	NA
P59	GND	NA
P51	GND	NA
P45	GND	NA
P37	GND	NA
P29	GND	NA
P22	GND	NA
P14	GND	NA
P8	GND	NA
P1	GND	NA

Notes:

1. V_{REF} or I/O option only in the XCV100E, 200E, 300E, 400E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV200E, 300E, 400E; otherwise, I/O option only.
3. V_{REF} or I/O option only in the XCV400E; otherwise, I/O option only.

Table 7: PQ240 Differential Pin Pair Summary
XCV50E, XCV100E, XCV200E, XCV300E, XCV400E

Pair	Bank	P Pin	N Pin	AO	Other Functions
48	6	P56	P57	√	-
49	6	P52	P53	2	-
50	6	P49	P50	3	VREF
51	6	P46	P47	4	VREF
52	6	P41	P42	√	-
53	6	P38	P39	2	-
54	6	P35	P36	4	VREF
55	6	P33	P34	5	VREF
56	7	P27	P28	√	-
57	7	P23	P24	4	VREF
58	7	P20	P21	2	-
59	7	P17	P18	√	-
60	7	P12	P13	4	VREF
61	7	P9	P10	3	VREF
62	7	P6	P7	2	-
63	7	P4	P5	6	VREF

Notes:

1. AO in the XCV50E.
2. AO in the XCV50E, 100E, 200E, 300E.
3. AO in the XCV50E, 200E, 300E, 400E.
4. AO in the XCV50E, 300E, 400E.
5. AO in the XCV100E, 200E, 400E.
6. AO in the XCV100E, 400E.
7. AO in the XCV50E, 200E, 400E.
8. AO in the XCV100E.

HQ240 High-Heat Quad Flat-Pack Packages

XCV600E and XCV1000E devices in High-heat dissipation Quad Flat-pack packages have footprint compatibility. Pins labeled IO_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF} it can be used as general I/O. Immediately following Table 8, see Table 9 for Differential Pair information.

Table 8: HQ240 — XCV600E, XCV1000E

Pin #	Pin Description	Bank
P240	VCCO	7
P239	TCK	NA
P238	IO	0
P237	IO_L0N	0
P236	IO_VREF_L0P	0
P235	IO_L1N_YY	0
P234	IO_L1P_YY	0
P233	GND	NA
P232	VCCO	0
P231	IO_VREF	0
P230	IO_VREF	0
P229	IO_VREF_L2N_YY	0
P228	IO_L2P_YY	0
P227	GND	NA
P226	VCCO	0
P225	VCCINT	NA
P224	IO_L3N_YY	0
P223	IO_L3P_YY	0
P222	IO_VREF	0 ¹
P221	IO_L4N_Y	0
P220	IO_L4P_Y	0
P219	GND	NA
P218	IO_VREF_L5N_Y	0
P217	IO_L5P_Y	0
P216	IO_VREF	0
P215	IO_LVDS_DLL_L6N	0
P214	VCCINT	NA
P213	GCK3	0
P212	VCCO	0
P211	GND	NA

Table 8: HQ240 — XCV600E, XCV1000E

Pin #	Pin Description	Bank
P66	IO_VREF_L46P	5
P65	IO_L46N	5
P64	IO_L47P_YY	5
P63	IO_L47N_YY	5
P62	M2	NA
P61	VCCO	5
P60	M0	NA
P59	GND	NA
P58	M1	NA
P57	IO_L48N_YY	6
P56	IO_L48P_YY	6
P55	VCCO	6
P54	IO_VREF	6
P53	IO_L49N_Y	6
P52	IO_L49P_Y	6
P51	GND	NA
P50	IO_VREF_L50N_Y	6
P49	IO_L50P_Y	6
P48	IO_VREF	6
P47	IO_VREF_L51N_Y	6
P46	IO_L51P_Y	6
P45	GND	NA
P44	VCCO	6
P43	VCCINT	NA
P42	IO_L52N_YY	6
P41	IO_L52P_YY	6
P40 ¹	IO_VREF	6
P39	IO_L53N_Y	6
P38	IO_L53P_Y	6
P37	GND	NA
P36	IO_VREF_L54N_Y	6
P35	IO_L54P_Y	6
P34	IO_L55N_Y	6
P33	IO_VREF_L55P_Y	6
P32	VCCINT	NA
P31	IO	6

Table 8: HQ240 — XCV600E, XCV1000E

Pin #	Pin Description	Bank
P30	VCCO	6
P29	GND	NA
P28	IO_L56N_YY	7
P27	IO_L56P_YY	7
P26	IO_VREF	7
P25	VCCO	7
P24	IO_L57N_Y	7
P23	IO_VREF_L57P_Y	7
P22	GND	NA
P21	IO_L58N_Y	7
P20	IO_L58P_Y	7
P19 ¹	IO_VREF	7
P18	IO_L59N_YY	7
P17	IO_L59P_YY	7
P16	VCCINT	NA
P15	VCCO	7
P14	GND	NA
P13	IO_L60N_Y	7
P12	IO_VREF_L60P_Y	7
P11	IO_VREF	7
P10	IO_L61N_Y	7
P9	IO_VREF_L61P_Y	7
P8	GND	NA
P7	IO_L62N_Y	7
P6	IO_L62P_Y	7
P5	IO_VREF_L63N_Y	7
P4	IO_L63P_Y	7
P3	IO	7
P2	TMS	NA
P1	GND	NA

Notes:

1. V_{REF} or I/O option only in the XCV1000E; otherwise, I/O option only.

Table 10: BG352 — XCV100E, XCV200E, XCV300E

Bank	Pin Description	Pin #
2	IO_D3_L30N_Y	M3
2	IO_L31P	M2
2	IO_L31N	M1
2	IO	N3 ¹
2	IO_L32P_YY	N4
2	IO_L32N_YY	N2
3	IO	P1
3	IO	P3 ¹
3	IO_L33P	R1
3	IO_L33N	R2
3	IO_D4_L34P_Y	R3
3	IO_VREF_3_L34N_Y	R4
3	IO_L35P_YY	T2
3	IO_L35N_YY	U2
3	IO	T3 ¹
3	IO_L36P	T4
3	IO_L36N	V1
3	IO	V2 ¹
3	IO_L37P_YY	U3
3	IO_D5_L37N_YY	U4
3	IO_D6_L38P_Y	V3
3	IO_VREF_3_L38N_Y	V4
3	IO_L39P_Y	Y1
3	IO_L39N_Y	Y2
3	IO	W3
3	IO	W4 ¹
3	IO	AA1 ¹
3	IO_L40P_Y	AA2
3	IO_VREF_3_L40N_Y	Y3
3	IO_L41P_YY	AC1
3	IO_L41N_YY	AB2
3	IO	AA3 ¹
3	IO_L42P_YY	AA4

Table 10: BG352 — XCV100E, XCV200E, XCV300E

Bank	Pin Description	Pin #
3	IO_VREF_3_L42N_YY	AC2 ²
3	IO	AB3
3	IO	AD1 ¹
3	IO	AB4 ¹
3	IO_D7_L43P_YY	AC3
3	IO_INIT_L43N_YY	AD2
4	IO_L44P_YY	AC5
4	IO_L44N_YY	AD4
4	IO	AE3 ¹
4	IO	AD5 ¹
4	IO	AC6
4	IO_VREF_4_L45P_YY	AE4 ²
4	IO_L45N_YY	AF3
4	IO	AF4 ¹
4	IO_L46P_YY	AC7
4	IO_L46N_YY	AD6
4	IO_VREF_4_L47P_YY	AE5
4	IO_L47N_YY	AE6
4	IO	AD7 ¹
4	IO	AE7 ¹
4	IO_L48P	AF6
4	IO_L48N	AC9
4	IO	AD8
4	IO_VREF_4_L49P_YY	AE8
4	IO_L49N_YY	AF7
4	IO_L50P_YY	AD9
4	IO_L50N_YY	AE9
4	IO	AD10 ¹
4	IO_L51P	AF9
4	IO_L51N	AC11
4	IO	AE10 ¹
4	IO_L52P_Y	AD11
4	IO_L52N_Y	AE11

Table 12: BG432 — XCV300E, XCV400E, XCV600E

Bank	Pin Description	Pin #
2	IO_L41N_Y	H2
2	IO_VREF_L42P_Y	H1 ¹
2	IO_L42N_Y	J4
2	IO_VREF_L43P_YY	J2
2	IO_D1_L43N_YY	K4
2	IO_D2_L44P_YY	K2
2	IO_L44N_YY	K1
2	IO_L45P_Y	L2
2	IO_L45N_Y	M4
2	IO_L46P_Y	M3
2	IO_L46N_Y	M2
2	IO_L47P_Y	N4
2	IO_L47N_Y	N3
2	IO_VREF_L48P_YY	N1
2	IO_D3_L48N_YY	P4
2	IO_L49P_Y	P3
2	IO_L49N_Y	P2
2	IO_VREF_L50P_Y	R3 ²
2	IO_L50N_Y	R4
2	IO_L51P_YY	R1
2	IO_L51N_YY	T3
3	IO	AA2
3	IO	AC2
3	IO	AE2
3	IO	U3
3	IO	W1
3	IO_L52P_Y	U4
3	IO_VREF_L52N_Y	U2 ²
3	IO_L53P_Y	U1
3	IO_L53N_Y	V3
3	IO_D4_L54P_YY	V4
3	IO_VREF_L54N_YY	V2
3	IO_L55P_Y	W3
3	IO_L55N_Y	W4
3	IO_L56P_Y	Y1

Table 12: BG432 — XCV300E, XCV400E, XCV600E

Bank	Pin Description	Pin #
3	IO_L56N_Y	Y3
3	IO_L57P_Y	Y4
3	IO_L57N_Y	Y2
3	IO_L58P_YY	AA3
3	IO_D5_L58N_YY	AB1
3	IO_D6_L59P_YY	AB3
3	IO_VREF_L59N_YY	AB4
3	IO_L60P_Y	AD1
3	IO_VREF_L60N_Y	AC3 ¹
3	IO_L61P_Y	AC4
3	IO_L61N_Y	AD2
3	IO_L62P_YY	AD3
3	IO_VREF_L62N_YY	AD4
3	IO_L63P_Y	AF2
3	IO_L63N_Y	AE3
3	IO_L64P	AE4
3	IO_L64N	AG1
3	IO_L65P_Y	AG2
3	IO_VREF_L65N_Y	AF3
3	IO_L66P_Y	AF4
3	IO_L66N_Y	AH1
3	IO_L67P	AH2
3	IO_L67N	AG3
3	IO_D7_L68P_YY	AG4
3	IO_INIT_L68N_YY	AJ2
3	IO	T2
4	GCK0	AL16
4	IO	AH10
4	IO	AJ11
4	IO	AK7
4	IO	AL12
4	IO	AL15
4	IO_L69P_YY	AJ4
4	IO_L69N_YY	AK3
4	IO_L70P_Y	AH5

Table 14: BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin#	See Note
0	IO_L11P_YY	B24	
0	IO_L12N_Y	E22	
0	IO_L12P_Y	C23	
0	IO_L13N_YY	A23	
0	IO_L13P_YY	D22	
0	IO_VREF_L14N_YY	E21	3
0	IO_L14P_YY	B22	
0	IO_L15N_Y	D21	
0	IO_L15P_Y	C21	
0	IO_L16N_YY	B21	
0	IO_L16P_YY	E20	
0	IO_VREF_L17N_YY	D20	
0	IO_L17P_YY	C20	
0	IO_L18N_Y	B20	
0	IO_L18P_Y	E19	
0	IO_L19N_Y	D19	
0	IO_L19P_Y	C19	
0	IO_VREF_L20N_Y	A19	
0	IO_L20P_Y	D18	
0	IO_LVDS_DLL_L21N	C18	
0	IO_VREF	E18	2
1	GCK2	D17	
1	IO	A3	
1	IO	D9	
1	IO	E8	
1	IO	E11	
1	IO_LVDS_DLL_L21P	E17	
1	IO_VREF_L22N_Y	C17	2
1	IO_L22P_Y	B17	
1	IO_L23N_Y	B16	
1	IO_VREF_L23P_Y	D16	
1	IO_L24N_Y	E16	
1	IO_L24P_Y	C16	
1	IO_L25N_Y	A15	

Table 14: BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin#	See Note
1	IO_L25P_Y	C15	
1	IO_L26N_YY	D15	
1	IO_VREF_L26P_YY	E15	
1	IO_L27N_YY	C14	
1	IO_L27P_YY	D14	
1	IO_L28N_Y	A13	
1	IO_L28P_Y	E14	
1	IO_L29N_YY	C13	
1	IO_VREF_L29P_YY	D13	3
1	IO_L30N_YY	C12	
1	IO_L30P_YY	E13	
1	IO_L31N_Y	A11	
1	IO_L31P_Y	D12	
1	IO_L32N_YY	B11	
1	IO_L32P_YY	C11	
1	IO_L33N_YY	B10	
1	IO_VREF_L33P_YY	D11	
1	IO_L34N_Y	C10	
1	IO_L34P_Y	A9	
1	IO_L35N_Y	C9	
1	IO_VREF_L35P_Y	D10	4
1	IO_L36N_Y	A8	
1	IO_L36P_Y	B8	
1	IO_L37N_Y	E10	
1	IO_VREF_L37P_Y	C8	1
1	IO_L38N_YY	B7	
1	IO_VREF_L38P_YY	A6	
1	IO_L39N_YY	C7	
1	IO_L39P_YY	D8	
1	IO_L40N_Y	A5	
1	IO_L40P_Y	B5	
1	IO_L41N_YY	C6	
1	IO_VREF_L41P_YY	D7	
1	IO_L42N_YY	A4	
1	IO_L42P_YY	B4	

Table 16: FG256 Package — XCV50E, XCV100E, XCV200E, XCV300E

Bank	Pin Description	Pin #
7	IO_L74N_Y	G4
7	IO_VREF_L74P_Y	H3
7	IO_L75N_YY	G2
7	IO_L75P_YY	F5
7	IO_L76N	F4
7	IO_L76P	F1
7	IO_L77N_YY	G3
7	IO_L77P_YY	F2
7	IO_L78N_Y	E1
7	IO_VREF_L78P_Y	D1 ¹
7	IO_L79N	E4
7	IO_L79P	E2
7	IO_L80N_Y	F3
7	IO_VREF_L80P_Y	C1
7	IO_L81N_YY	D2
7	IO_L81P_YY	E3
7	IO_VREF_L82N	B1 ²
7	IO_L82P	A2
2	CCLK	D15
3	DONE	R14
NA	DXN	R4
NA	DXP	P4
NA	M0	N3
NA	M1	P2
NA	M2	R3
NA	PROGRAM	P15
NA	TCK	C4
NA	TDI	A15
2	TDO	B14
NA	TMS	D3
NA	VCCINT	C3
NA	VCCINT	C14
NA	VCCINT	D4

Table 16: FG256 Package — XCV50E, XCV100E, XCV200E, XCV300E

Bank	Pin Description	Pin #
NA	VCCINT	D13
NA	VCCINT	E5
NA	VCCINT	E12
NA	VCCINT	M5
NA	VCCINT	M12
NA	VCCINT	N4
NA	VCCINT	N13
NA	VCCINT	P3
NA	VCCINT	P14
0	VCCO	F8
0	VCCO	E8
1	VCCO	F9
1	VCCO	E9
2	VCCO	H12
2	VCCO	H11
3	VCCO	J12
3	VCCO	J11
4	VCCO	M9
4	VCCO	L9
5	VCCO	M8
5	VCCO	L8
6	VCCO	J6
6	VCCO	J5
7	VCCO	H6
7	VCCO	H5
NA	GND	T16
NA	GND	T1
NA	GND	R15
NA	GND	R2
NA	GND	L11
NA	GND	L10
NA	GND	L7
NA	GND	L6

Table 17: FG256 Differential Pin Pair Summary
XCV50E, XCV100E, XCV200E, XCV300E

Pair	Bank	P Pin	N Pin	AO	Other Functions
19	2	C15	D14	√	DIN, D0
20	2	B16	E13	6	VREF
21	2	C16	E14	√	-
22	2	F13	E15	1	VREF
23	2	F12	D16	5	-
24	2	F14	E16	3	D1
25	2	F15	G13	√	D2
26	2	F16	G12	6	-
27	2	G15	G14	√	-
28	2	H13	G16	3	D3
29	2	J13	H15	4	-
30	2	H14	H16	√	-
31	3	K15	J14	4	-
32	3	J16	K16	3	VREF
33	3	K12	L15	√	-
34	3	K13	L16	6	-
35	3	K14	M16	√	D5
36	3	N16	L13	3	VREF
37	3	P16	L12	5	-
38	3	M15	L14	1	VREF
39	3	M14	R16	√	-
40	3	M13	T15	6	VREF
41	3	N14	N15	√	INIT
42	4	T14	P13	√	-
43	4	P12	R13	7	VREF
44	4	N12	T13	√	-
45	4	T12	P11	√	VREF
46	4	R12	N11	2	-
47	4	T11	M11	√	VREF
48	4	R11	T10	√	-
49	4	R10	M10	1	-
50	4	P9	T9	1	VREF
51	4	N10	R9	1	-
52	5	N9	T8	NA	IO_LVDS_DLL
53	5	R7	P8	1	VREF
54	5	P7	T6	1	-

Table 17: FG256 Differential Pin Pair Summary
XCV50E, XCV100E, XCV200E, XCV300E

Pair	Bank	P Pin	N Pin	AO	Other Functions
55	5	M7	R6	√	-
56	5	P6	R5	√	VREF
57	5	N6	T5	2	-
58	5	M6	T4	√	VREF
59	5	T3	P5	√	-
60	5	T2	N5	7	VREF
61	6	R1	M3	√	-
62	6	N2	M4	6	VREF
63	6	P1	L5	√	-
64	6	L3	N1	1	VREF
65	6	L4	M2	5	-
66	6	K4	M1	3	VREF
67	6	L1	L2	√	-
68	6	K1	K3	6	-
69	6	K5	K2	√	-
70	6	J1	J3	3	VREF
71	6	H1	J4	4	-
72	7	H4	G1	√	-
73	7	H2	G5	4	-
74	7	H3	G4	3	VREF
75	7	F5	G2	√	-
76	7	F1	F4	6	-
77	7	F2	G3	√	-
78	7	D1	E1	3	VREF
79	7	E2	E4	5	-
80	7	C1	F3	1	VREF
81	7	E3	D2	√	-
82	7	A2	B1	6	VREF

Notes:

1. AO in the XCV50E, 200E, 300E.
2. AO in the XCV50E, 200E.
3. AO in the XCV50E, 300E.
4. AO in the XCV100E, 200E.
5. AO in the XCV200E.
6. AO in the XCV100E.
7. AO in the XCV50E.

Table 19: FG456 Differential Pin Pair Summary
XCV200E, XCV300E

Pair	Bank	P Pin	N Pin	AO	Other Functions
18	1	C14	B14	2	-
19	1	A15	F12	2	-
20	1	C15	B15	√	-
21	1	E14	A16	√	VREF
22	1	C16	D14	2	-
23	1	A17	D15	2	-
24	1	A18	B17	√	VREF
25	1	C17	D16	√	-
26	1	A19	B18	√	VREF
27	1	C18	D17	√	-
28	1	C19	A20	√	CS
29	2	C21	D20	√	DIN, D0
30	2	C22	D21	√	-
31	2	D22	E21	√	VREF
32	2	E22	F18	√	-
33	2	F21	F19	√	VREF
34	2	F22	G19	2	-
35	2	G20	G18	1	-
36	2	H18	H22	2	D1, VREF
37	2	H20	H19	√	D2
38	2	H21	J19	√	-
39	2	J18	J20	√	-
40	2	K18	J21	2	-
41	2	K22	K21	1	VREF
42	2	K19	L22	2	-
43	2	L21	L18	√	-
44	2	L17	L20	√	-
45	3	M18	M20	√	-
46	3	M19	M17	2	-
47	3	N22	N21	2	VREF
48	3	N20	N18	√	-
49	3	N19	P21	√	-
50	3	P20	P19	√	-
51	3	P18	R21	√	D5
52	3	T22	R19	2	VREF

Table 19: FG456 Differential Pin Pair Summary
XCV200E, XCV300E

Pair	Bank	P Pin	N Pin	AO	Other Functions
53	3	U22	R18	2	-
54	3	T21	V22	√	-
55	3	T20	U21	√	VREF
56	3	W22	T18	√	-
57	3	U19	U20	√	VREF
58	3	W21	AA22	√	-
59	3	Y21	V19	√	INIT
60	4	W18	AA20	√	-
61	4	Y18	V17	NA	-
62	4	AB20	W17	√	VREF
63	4	AA18	V16	NA	-
64	4	AB19	AB18	√	VREF
65	4	W16	AA17	1	-
66	4	Y16	V15	1	-
67	4	AB16	Y15	√	VREF
68	4	AA15	AB15	√	-
69	4	W15	Y14	1	-
70	4	V14	AA14	1	-
71	4	AB14	V13	NA	-
72	4	AA13	AB13	√	VREF
73	4	W13	AA12	2	-
74	4	Y12	V12	2	-
75	5	U12	AA11	NA	IO_LVDS_DLL
76	5	AB11	W11	1	-
77	5	V11	Y10	√	VREF
78	5	AB10	W10	√	-
79	5	V10	Y9	2	-
80	5	AB9	W9	2	-
81	5	V9	AA8	√	-
82	5	Y8	W8	√	VREF
83	5	W7	AA7	2	-
84	5	AB6	AA6	2	-
85	5	AB5	AA5	√	VREF
86	5	Y7	W6	√	-
87	5	AA4	Y6	√	VREF

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
4	IO_L98N_YY	AB19
4	IO_L99P_YY	AC20
4	IO_L99N_YY	AA18
4	IO_L100P_Y	AC19
4	IO_L100N_Y	AD20
4	IO_VREF_L101P_Y	AF20 ²
4	IO_L101N_Y	AB18
4	IO_L102P	AD19
4	IO_L102N	Y17
4	IO_L103P	AE19
4	IO_VREF_L103N	AD18
4	IO_L104P_YY	AF19
4	IO_L104N_YY	AA17
4	IO_L105P_Y	AC17
4	IO_L105N_Y	AB17
4	IO_L106P_YY	Y16
4	IO_L106N_YY	AE17
4	IO_L107P_YY	AF17
4	IO_L107N_YY	AA16
4	IO_L108P	AD17
4	IO_L108N	AB16
4	IO_L109P_YY	AC16
4	IO_L109N_YY	AD16
4	IO_VREF_L110P_YY	AC15
4	IO_L110N_YY	Y15
4	IO_L111P_YY	AD15
4	IO_L111N_YY	AA15
4	IO_L112P_Y	W14
4	IO_L112N_Y	AB15
4	IO_VREF_L113P_Y	AF15
4	IO_L113N_Y	Y14
4	IO_L114P	AD14
4	IO_L114N	AB14
4	IO_LVDS_DLL_L115P	AC14
5	GCK1	AB13
5	IO	Y13 ¹

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
5	IO	AD7
5	IO	AD13
5	IO	AE4
5	IO	AE7
5	IO	AE12 ¹
5	IO	AF3 ¹
5	IO	AF5
5	IO	AF10 ¹
5	IO	AF11 ¹
5	IO_LVDS_DLL_L115N	AF13
5	IO_L116P_Y	AA13
5	IO_VREF_L116N_Y	AF12
5	IO_L117P_Y	AC13
5	IO_L117N_Y	W13
5	IO_L118P_YY	AA12
5	IO_L118N_YY	AD12
5	IO_L119P_YY	AC12
5	IO_VREF_L119N_YY	AB12
5	IO_L120P_YY	AD11
5	IO_L120N_YY	Y12
5	IO_L121P	AB11
5	IO_L121N	AD10
5	IO_L122P_YY	AC11
5	IO_L122N_YY	AE10
5	IO_L123P_YY	AC10
5	IO_L123N_YY	AA11
5	IO_L124P_Y	Y11
5	IO_L124N_Y	AD9
5	IO_L125P_YY	AB10
5	IO_L125N_YY	AF9
5	IO_L126P_YY	AD8
5	IO_VREF_L126N_YY	AA10
5	IO_L127P_YY	AE8
5	IO_L127N_YY	Y10
5	IO_L128P_Y	AC9
5	IO_VREF_L128N_Y	AF8 ²
5	IO_L129P_Y	AF7

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
NA	GND	D20
NA	GND	D12
NA	GND	C39
NA	GND	C37
NA	GND	C3
NA	GND	C20
NA	GND	C1
NA	GND	B39
NA	GND	B38
NA	GND	B2
NA	GND	B1
NA	GND	AW39
NA	GND	AW38
NA	GND	AW37
NA	GND	AW3
NA	GND	AW2
NA	GND	AW1
NA	GND	AV39
NA	GND	AV38
NA	GND	AV2
NA	GND	AV1
NA	GND	AU39
NA	GND	AU37
NA	GND	AU3
NA	GND	AU20
NA	GND	AU1
NA	GND	AT4
NA	GND	AT36
NA	GND	AT28
NA	GND	AT20
NA	GND	AT12
NA	GND	AR5
NA	GND	AR35
NA	GND	AR28
NA	GND	AR21
NA	GND	AR20

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
NA	GND	AR19
NA	GND	AR12
NA	GND	AH5
NA	GND	AH4
NA	GND	AH36
NA	GND	AH35
NA	GND	AA5
NA	GND	AA35
NA	GND	A39
NA	GND	A38
NA	GND	A37
NA	GND	A3
NA	GND	A2
NA	GND	A1

Notes:

1. V_{REF} or I/O option only in the XCV1000E, 1600E, 2000E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV1600E, 2000E; otherwise, I/O option only.
3. V_{REF} or I/O option only in the XCV2000E; otherwise, I/O option only.

Table 26: FG900 — XCV600E, XCV1000E, XCV1600E

Bank	Pin Description	Pin #
7	IO_L275N_YY	G3
7	IO_L275P_YY	E1
7	IO_L276N_YY	H6
7	IO_L276P_YY	E2
7	IO_L277N	E4
7	IO_VREF_L277P	K9
7	IO_L278N_YY	J8
7	IO_L278P_YY	F4
7	IO_L279N_Y	D1 ³
7	IO_L279P_Y	H7 ⁴
7	IO_L280N_YY	G6
7	IO_VREF_L280P_YY	C2 ¹
7	IO_L281N	D2
7	IO_L281P	F5
7	IO_L282N_YY	D3 ⁴
7	IO_L282P_YY	K10 ³
2	CCLK	F26
3	DONE	AJ28
NA	DXN	AJ3
NA	DXP	AH4
NA	M0	AF4
NA	M1	AC7
NA	M2	AK3
NA	PROGRAM	AG28
NA	TCK	B3
NA	TDI	H22
2	TDO	D26
NA	TMS	C1
NA	VCCINT	L11
NA	VCCINT	L12
NA	VCCINT	L19
NA	VCCINT	L20
NA	VCCINT	M11
NA	VCCINT	M12
NA	VCCINT	M19

Table 26: FG900 — XCV600E, XCV1000E, XCV1600E

Bank	Pin Description	Pin #
NA	VCCINT	M20
NA	VCCINT	N13
NA	VCCINT	N14
NA	VCCINT	N15
NA	VCCINT	N16
NA	VCCINT	N17
NA	VCCINT	N18
NA	VCCINT	P13
NA	VCCINT	P18
NA	VCCINT	R13
NA	VCCINT	R18
NA	VCCINT	T13
NA	VCCINT	T18
NA	VCCINT	U13
NA	VCCINT	U18
NA	VCCINT	V13
NA	VCCINT	V14
NA	VCCINT	V15
NA	VCCINT	V16
NA	VCCINT	V17
NA	VCCINT	V18
NA	VCCINT	W11
NA	VCCINT	W12
NA	VCCINT	W19
NA	VCCINT	W20
NA	VCCINT	Y11
NA	VCCINT	Y12
NA	VCCINT	Y19
NA	VCCINT	Y20
NA	VCCO_0	B6
NA	VCCO_0	M15
NA	VCCO_0	M14
NA	VCCO_0	L15
NA	VCCO_0	L14
NA	VCCO_0	H14
NA	VCCO_0	M13

FG900 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A $\checkmark$ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 27: FG900 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
GCLK LVDS					
3	0	C15	A15	NA	IO_DLL_ 34N
2	1	E15	E16	NA	IO_DLL_ 34P
1	5	AK16	AH16	NA	IO_DLL_ 177N
0	4	AJ16	AF16	NA	IO_DLL_ 177P
IO LVDS					
Total Pairs: 283, Asynchronous Output Pairs: 168					
0	0	F7	C4	4	-
1	0	G8	D5	2	-
2	0	H9	A3	2	VREF
3	0	J10	B4	2	-
4	0	D6	A4	$\checkmark$	-
5	0	B5	E7	$\checkmark$	VREF
6	0	F8	A5	1	-
7	0	N11	D7	1	-
8	0	E8	G9	$\checkmark$	-
9	0	J11	A6	$\checkmark$	VREF
10	0	B7	C7	2	-
11	0	H10	C8	2	-
12	0	F10	G10	$\checkmark$	-
13	0	H11	A8	$\checkmark$	VREF
14	0	C9	D9	NA	-
15	0	J12	B9	4	-
16	0	A9	E10	NA	VREF
17	0	B10	G11	NA	-

Table 27: FG900 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
18	0	C10	H12	4	-
19	0	F11	H13	2	-
20	0	D11	E11	2	-
21	0	G12	B11	2	-
22	0	C11	F12	$\checkmark$	-
23	0	D12	A10	$\checkmark$	VREF
24	0	A11	E12	1	-
25	0	B12	G13	1	-
26	0	K13	A12	$\checkmark$	-
27	0	B13	F13	$\checkmark$	VREF
28	0	E13	G14	2	-
29	0	B14	D14	2	-
30	0	J14	A14	$\checkmark$	-
31	0	J15	K14	$\checkmark$	VREF
32	0	H15	B15	NA	-
33	0	D15	F15	$\checkmark$	VREF
34	1	E16	A15	NA	IO_LVDS_DLL
35	1	F16	B16	4	VREF
36	1	H16	A16	4	-
37	1	K15	C16	$\checkmark$	VREF
38	1	G16	K16	$\checkmark$	-
39	1	E17	A17	2	-
40	1	C17	F17	2	-
41	1	A18	E18	$\checkmark$	VREF
42	1	A19	D18	$\checkmark$	-
43	1	G18	B19	1	-
44	1	H18	D19	1	-
45	1	F19	F18	$\checkmark$	VREF
46	1	K17	B20	$\checkmark$	-
47	1	A20	D20	2	-
48	1	C20	G19	2	-
49	1	E20	K18	2	-
50	1	D21	B21	4	-
51	1	A21	F20	$\checkmark$	-

Table 27: FG900 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
188	5	AA12	AJ12	√	VREF
189	5	AB12	AE11	√	-
190	5	AK12	Y13	2	-
191	5	AG11	AF11	2	-
192	5	AH11	AJ11	2	-
193	5	AE12	AG10	4	-
194	5	AD12	AK11	√	-
195	5	AJ10	AC12	√	VREF
196	5	AK10	AD11	4	-
197	5	AJ9	AE9	4	-
198	5	AH10	AF9	√	VREF
199	5	AH9	AK9	√	-
200	5	AF8	AB11	2	-
201	5	AC11	AG8	2	-
202	5	AK8	AF7	√	VREF
203	5	AG7	AK7	√	-
204	5	AJ7	AD10	1	-
205	5	AH6	AC10	1	-
206	5	AD9	AG6	√	VREF
207	5	AB10	AJ5	√	-
208	5	AD8	AK5	2	-
209	5	AC9	AJ4	2	VREF
210	5	AG5	AK4	2	-
211	5	AH5	AG3	4	-
212	6	AC6	AF3	√	-
213	6	AG2	AH2	NA	-
214	6	AE4	AB9	1	-
215	6	AH1	AE3	4	VREF
216	6	AD6	AB8	3	-
217	6	AA10	AG1	4	-
218	6	AD4	AA9	1	VREF
219	6	AD2	AD5	√	-
220	6	AF2	AD3	4	-
221	6	AA7	AA8	1	-

Table 27: FG900 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
222	6	Y9	AF1	√	VREF
223	6	AC4	AB6	√	-
224	6	W8	AE1	2	-
225	6	AB4	Y8	4	-
226	6	W9	AB3	4	VREF
227	6	W10	AA5	4	-
228	6	V10	AB1	4	-
229	6	AC1	Y7	4	VREF
230	6	AA3	V11	NA	-
231	6	U10	AA2	4	-
232	6	AA6	W7	1	-
233	6	Y4	Y6	4	-
234	6	V7	AA1	3	-
235	6	Y2	Y3	4	-
236	6	W5	Y5	1	VREF
237	6	W6	W4	√	-
238	6	W2	V6	4	-
239	6	V4	U9	1	-
240	6	T8	AB2	√	VREF
241	6	W1	U5	√	-
242	6	T9	Y1	2	-
243	6	U3	T7	4	-
244	6	V2	T5	4	VREF
245	6	T6	R9	4	-
246	6	U2	T4	4	VREF
247	7	R10	T1	NA	-
248	7	R6	R5	4	-
249	7	R4	R8	4	VREF
250	7	R3	R7	4	-
251	7	P6	P10	4	VREF
252	7	P2	P5	4	-
253	7	P4	P7	2	-
254	7	R2	N4	√	-
255	7	P1	N7	√	VREF