AMD Xilinx - XCV50E-8CS144C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	384
Number of Logic Elements/Cells	1728
Total RAM Bits	65536
Number of I/O	94
Number of Gates	71693
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-TFBGA, CSPBGA
Supplier Device Package	144-LCSBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv50e-8cs144c

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Dedicated Routing

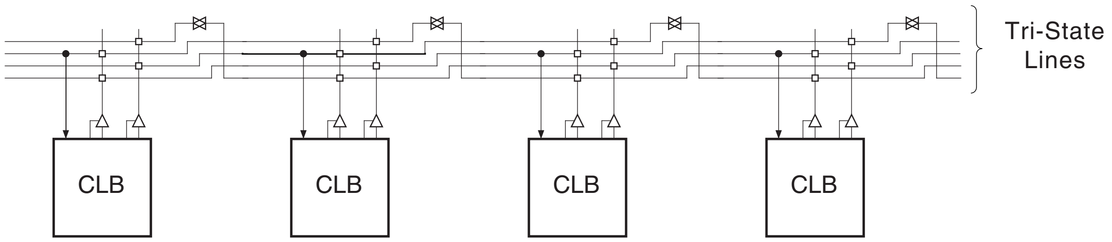
Some classes of signal require dedicated routing resources to maximize performance. In the Virtex-E architecture, dedicated routing resources are provided for two classes of signal.

- Horizontal routing resources are provided for on-chip 3-state buses. Four partitionable bus lines are provided per CLB row, permitting multiple buses within a row, as shown in Figure 8.
- Two dedicated nets per CLB propagate carry signals vertically to the adjacent CLB.Global Clock Distribution Network
- DLL Location

Clock Routing

Clock Routing resources distribute clocks and other signals with very high fanout throughout the device. Virtex-E devices include two tiers of clock routing resources referred to as global and local clock routing resources.

- The global routing resources are four dedicated global nets with dedicated input pins that are designed to distribute high-fanout clock signals with minimal skew. Each global clock net can drive all CLB, IOB, and block RAM clock pins. The global nets can be driven only by global buffers. There are four global buffers, one for each global net.
- The local clock routing resources consist of 24 backbone lines, 12 across the top of the chip and 12 across bottom. From these lines, up to 12 unique signals per column can be distributed via the 12 longlines in the column. These local resources are more flexible than the global resources since they are not restricted to routing only to clock pins.

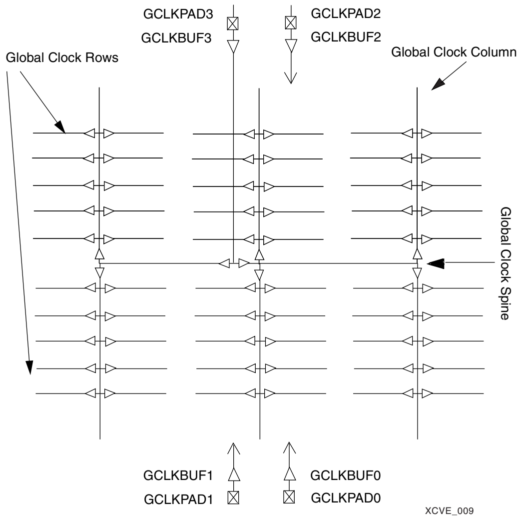


buft_c.eps

Figure 8: **BUFT Connections to Dedicated Horizontal Bus LInes**

Global Clock Distribution

Virtex-E provides high-speed, low-skew clock distribution through the global routing resources described above. A typical clock distribution net is shown in Figure 9.



XCVE_009

Figure 9: **Global Clock Distribution Network**

Four global buffers are provided, two at the top center of the device and two at the bottom center. These drive the four global nets that in turn drive any clock pin.

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is selected either from these pads or from signals in the general purpose routing.

Digital Delay-Locked Loops

There are eight DLLs (Delay-Locked Loops) per device, with four located at the top and four at the bottom, Figure 10. The DLLs can be used to eliminate skew between the clock input pad and the internal clock input pins throughout the device. Each DLL can drive two global clock networks.The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element. Additional delay is introduced such that clock edges arrive at internal flip-flops synchronized with clock edges arriving at the input.

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock, and can double the clock or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

3. At the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock. If BUSY is High (from a previous write), the data is not accepted. Acceptance instead occurs on the first clock after BUSY goes Low, and the data must be held until this has happened.
4. Repeat steps 2 and 3 until all the data has been sent.
5. De-assert $\overline{\text{CS}}$ and $\overline{\text{WRITE}}$.

Table 11: **SelectMAP Write Timing Characteristics**

	Description		Symbol		Units
CCLK	D_{0-7} Setup/Hold	1/2	T_{SMDCC}/T_{SMCCD}	5.0 / 1.7	ns, min
	$\overline{\text{CS}}$ Setup/Hold	3/4	T_{SMCSCC}/T_{SMCCCS}	7.0 / 1.7	ns, min
	$\overline{\text{WRITE}}$ Setup/Hold	5/6	T_{SMCCW}/T_{SMWCC}	7.0 / 1.7	ns, min
	BUSY Propagation Delay	7	T_{SMCKBY}	12.0	ns, max
	Maximum Frequency		F_{CC}	66	MHz, max
	Maximum Frequency with no handshake		F_{CCNH}	50	MHz, max

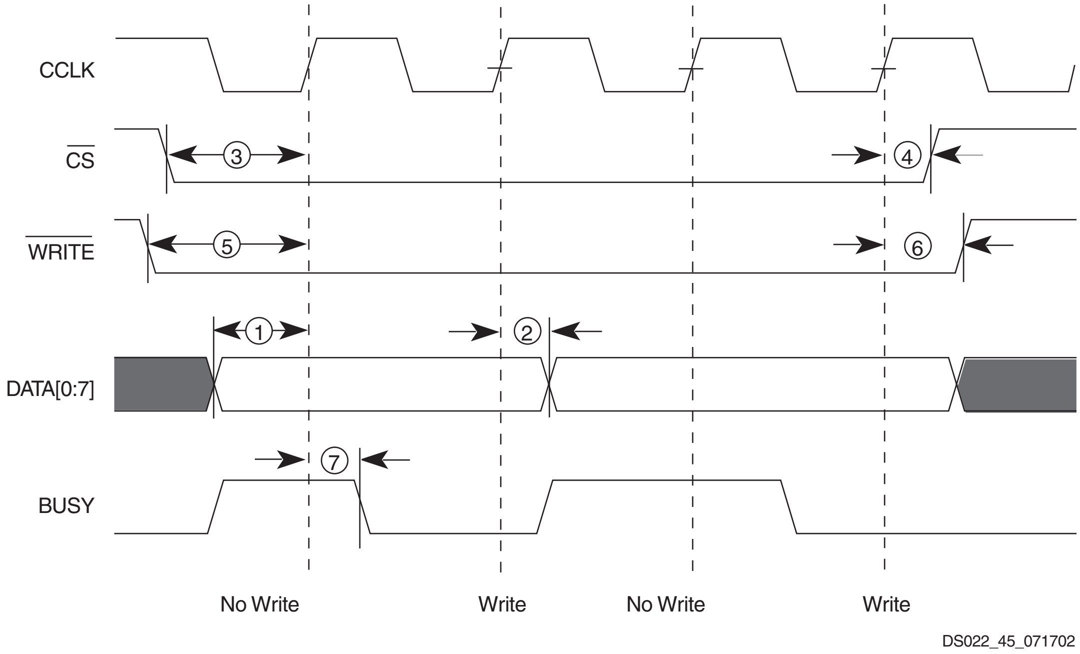


Figure 17: **Write Operations**

A flowchart for the write operation is shown in Figure 18. Note that if CCLK is slower than f_{CCNH}, the FPGA never asserts BUSY, In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.

Abort

During a given assertion of $\overline{\text{CS}}$, the user cannot switch from a write to a read, or vice-versa. This action causes the current packet command to be aborted. The device remains BUSY until the aborted operation has completed. Following an abort, data is assumed to be unaligned to word boundaries, and the FPGA requires a new synchronization word prior to accepting any new packets.

To initiate an abort during a write operation, de-assert $\overline{\text{WRITE}}$. At the rising edge of CCLK, an abort is initiated, as shown in Figure 19.

Fundamentals

Modern bus applications, pioneered by the largest and most influential companies in the digital electronics industry, are commonly introduced with a new I/O standard tailored specifically to the needs of that application. The bus I/O standards provide specifications to other vendors who create products designed to interface with these applications. Each standard often has its own specifications for current, voltage, I/O buffering, and termination techniques.

The ability to provide the flexibility and time-to-market advantages of programmable logic is increasingly dependent on the capability of the programmable logic device to support an ever increasing variety of I/O standards

The SelectI/O resources feature highly configurable input and output buffers which provide support for a wide variety of I/O standards. As shown in Table 18, each buffer type can support a variety of voltage requirements.

Table 18: **Virtex-E Supported I/O Standards**

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Board Termination Voltage (V_{TT})
LVTTL	3.3	3.3	N/A	N/A
LVCMOS2	2.5	2.5	N/A	N/A
LVCMOS18	1.8	1.8	N/A	N/A
SSTL3 I & II	3.3	N/A	1.50	1.50
SSTL2 I & II	2.5	N/A	1.25	1.25
GTL	N/A	N/A	0.80	1.20
GTL+	N/A	N/A	1.0	1.50
HSTL I	1.5	N/A	0.75	0.75
HSTL III & IV	1.5	N/A	0.90	1.50
CTT	3.3	N/A	1.50	1.50
AGP-2X	3.3	N/A	1.32	N/A
PCI33_3	3.3	3.3	N/A	N/A
PCI66_3	3.3	3.3	N/A	N/A
BLVDS & LVDS	2.5	N/A	N/A	N/A
LVPECL	3.3	N/A	N/A	N/A

Overview of Supported I/O Standards

This section provides a brief overview of the I/O standards supported by all Virtex-E devices.

While most I/O standards specify a range of allowed voltages, this document records typical voltage values only. Detailed information on each specification can be found on the Electronic Industry Alliance Jedec website at:

http://www.jedec.org

LVTTL — Low-Voltage TTL

The Low-Voltage TTL, or LVTTL standard is a general purpose EIA/JESDSA standard for 3.3V applications that uses an LVTTL input buffer and a Push-Pull output buffer. This standard requires a 3.3V output source voltage (V_{CCO}), but does not require the use of a reference voltage (V_{REF}) or a termination voltage (V_{TT}).

LVCMOS2 — Low-Voltage CMOS for 2.5 Volts

The Low-Voltage CMOS for 2.5 Volts or lower, or LVCMOS2 standard is an extension of the LVCMOS standard (JESD 8.-5) used for general purpose 2.5V applications. This standard requires a 2.5V output source voltage (V_{CCO}), but does not require the use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}).

LVCMOS18 — 1.8 V Low Voltage CMOS

This standard is an extension of the LVCMOS standard. It is used in general purpose 1.8 V applications. The use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}) is not required.

PCI — Peripheral Component Interface

The Peripheral Component Interface, or PCI standard specifies support for both 33 MHz and 66 MHz PCI bus applications. It uses a LVTTL input buffer and a Push-Pull output buffer. This standard does not require the use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}), however, it does require a 3.3V output source voltage (V_{CCO}).

GTL — Gunning Transceiver Logic Terminated

The Gunning Transceiver Logic, or GTL standard is a high-speed bus standard (JESD8.3) invented by Xerox. Xilinx has implemented the terminated variation for this standard. This standard requires a differential amplifier input buffer and a Open Drain output buffer.

GTL+ — Gunning Transceiver Logic Plus

The Gunning Transceiver Logic Plus, or GTL+ standard is a high-speed bus standard (JESD8.3) first used by the Pentium Pro processor.

HSTL — High-Speed Transceiver Logic

The High-Speed Transceiver Logic, or HSTL standard is a general purpose high-speed, 1.5V bus standard sponsored by IBM (EIA/JESD 8-6). This standard has four variations or classes. SelectI/O devices support Class I, III, and IV. This

The register elements can be packed in the IOB using the IOB property to TRUE on the register or by using the "map -pr [i|o|b]" where "i" is inputs only, "o" is outputs only and "b" is both inputs and outputs.

To improve design coding times VHDL and Verilog synthesis macro libraries have been developed to explicitly create these structures. The input library macros are listed below. The 3-state is configured to be 3-stated at GSR and when the PRE,CLR,S or R is asserted and shares it's clock enable with the output register. If this is not desirable then the library can be updated by the user for the desired functionality. The O and OB inputs to the macros are the external net connections.

Creating a LVDS Bidirectional Buffer

LVDS bidirectional buffers can be placed in a wide number of IOB locations. The exact locations are dependent on the package used. The Virtex-E package information lists the possible locations as IO_L#P for the P-side and IO_L#N for the N-side, where # is the pair number.

HDL Instantiation

Both bidirectional buffers are required to be instantiated in the design and placed on the correct IO_L#P and IO_L#N locations. The IOB must have the same net source the following pins, clock (C), set/reset (SR), 3-state (T), 3-state clock enable (TCE), output (O), output clock enable (OCE). In addition, the output (O) pins must be inverted with respect to each other, and if output registers are used, the INIT states must be opposite values (one HIGH and one LOW). If 3-state registers are used, they must be initialized to the same state. Failure to follow these rules leads to DRC errors in the software.

VHDL Instantiation

```
data0_p:   IOBUF_LVDS port map
(I=>data_out(0), T=>data_tri,
IO=>data_p(0), O=>data_int(0));

data0_inv: INV         port map
(I=>data_out(0),   O=>data_n_out(0));

data0_n   : IOBUF_LVDS port map
(I=>data_n_out(0), T=>data_tri,
IO=>data_n(0), O=>open);
```

Verilog Instantiation

```
IOBUF_LVDS data0_p(.I(data_out[0]),
.T(data_tri), .IO(data_p[0]),
.O(data_int[0]);

INV        data0_inv (.I(data_out[0],
.O(data_n_out[0]);

IOBUF_LVDS
data0_n(.I(data_n_out[0]),.T(data_tri),.
IO(data_n[0]).O());
```

Location Constraints

All LVDS buffers must be explicitly placed on a device. For the output buffers this can be done with the following constraint in the .ucf or .ncf file.

```
NET data_p<0> LOC = D28; # IO_L0P

NET data_n<0> LOC = B29; # IO_L0N
```

Synchronous vs. Asynchronous Bidirectional Buffers

If the output side of the bidirectional buffers are synchronous (registered in the IOB), then any IO_L#P|N pair can be used. If the output side of the bidirectional buffers are asynchronous (no output register), then they must use one of the pairs that is a part of the asynchronous LVDS IOB group. This applies for either the 3-state pin or the data out pin.

The LVDS pairs that can be used as asynchronous bidirectional buffers are listed in the Virtex-E pinout tables. Some pairs are marked as asynchronous capable for all devices in that package, and others are marked as available only for that device in the package. If the device size might change at some point in the product's lifetime, then only the common pairs for all packages should be used.

Adding Output and 3-State Registers

All LVDS buffers can have an output and input registers in the IOB. The output registers must be in both the P-side and N-side IOBs, the input register is only in the P-side. All the normal IOB register options are available (FD, FDE, FDC, FDCE, FDP, FDPE, FDR, FDRE, FDS, FDSE, LD, LDE, LDC, LDCE, LDP, LDPE). The register elements can be inferred or explicitly instantiated in the HDL code. Special care must be taken to insure that the D pins of the registers are inverted and that the INIT states of the registers are opposite. The 3-state (T), 3-state clock enable (CE), clock pin (C), output clock enable (CE), and set/reset (CLR/PRE or S/R) pins must connect to the same source. Failure to do this leads to a DRC error in the software.

The register elements can be packed in the IOB using the IOB property to TRUE on the register or by using the "map -pr [i|o|b]" where "i" is inputs only, "o" is outputs only and "b" is both inputs and outputs. To improve design coding times VHDL and Verilog synthesis macro libraries have been developed to explicitly create these structures. The bidirectional I/O library macros are listed in Table 44. The 3-state is configured to be 3-stated at GSR and when the PRE,CLR,S or R is asserted and shares its clock enable with the output and input register. If this is not desirable then the library can be updated be the user for the desired functionality. The I/O and IOB inputs to the macros are the external net connections.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply. This is the time required to reach the nominal power supply voltage of the device[1] from 0V. The fastest ramp rate is 0V to nominal voltage in 2 ms, and the slowest allowed ramp rate is 0V to nominal voltage in 50 ms. For more details on power supply requirements, see XAPP158 on www.xilinx.com.

Product (Commercial Grade)	Description(2)	Current Requirement(3)
XCV50E - XCV600E	Minimum required current supply	500 mA
XCV812E - XCV2000E	Minimum required current supply	1 A
XCV2600E - XCV3200E	Minimum required current supply	1.2 A
Virtex-E Family, Industrial Grade	Minimum required current supply	2 A

Notes:

1. Ramp rate used for this specification is from 0 - 1.8 V DC. Peak current occurs on or near the internal power-on reset threshold and lasts for less than 3 ms.
2. Devices are guaranteed to initialize properly with the minimum current available from the power supply as noted above.
3. Larger currents might result if ramp rates are forced to be faster.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTL(1)	– 0.5	0.8	2.0	3.6	0.4	2.4	24	– 24
LVCMOS2	– 0.5	0.7	1.7	2.7	0.4	1.9	12	– 12
LVCMOS18	– 0.5	35% V_{CCO}	65% V_{CCO}	1.95	0.4	V_{CCO} – 0.4	8	– 8
PCI, 3.3 V	– 0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
GTL	– 0.5	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	n/a	40	n/a
GTL+	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	n/a	36	n/a
HSTL I(3)	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	8	–8
HSTL III	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	24	–8
HSTL IV	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	48	–8
SSTL3 I	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.6	V_{REF} + 0.6	8	–8
SSTL3 II	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.8	V_{REF} + 0.8	16	–16
SSTL2 I	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.61	V_{REF} + 0.61	7.6	–7.6
SSTL2 II	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.80	V_{REF} + 0.80	15.2	–15.2

Table 4: **CS144 — XCV50E, XCV100E, XCV200E**

Bank	Pin Description	Pin #
1	VCCO	A13
1	VCCO	D7
2	VCCO	B12
3	VCCO	G11
3	VCCO	M13
4	VCCO	N13
5	VCCO	N1
5	VCCO	N7
6	VCCO	M2
7	VCCO	B2
7	VCCO	G2
NA	GND	A1
NA	GND	B9
NA	GND	B11
NA	GND	C7
NA	GND	D5
NA	GND	E4
NA	GND	E11
NA	GND	F1
NA	GND	G10
NA	GND	J1
NA	GND	J12
NA	GND	L3
NA	GND	L5
NA	GND	L7
NA	GND	L9
NA	GND	N12

Notes:
1. V_{REF} or I/O option only in the XCV200E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV100E, 200E; otherwise, I/O option only.

CS144 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 5: **CS144 Differential Pin Pair Summary XCV50E, XCV100E, XCV200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	K7	N8	NA	IO_DLL_L18P
1	5	M7	M6	NA	IO_DLL_L18N
2	1	A7	B7	NA	IO_DLL_L2P
3	0	A6	C6	NA	IO_DLL_L2N
IO LVDS Total Pairs: 30, Asynchronous Output Pairs: 18					
0	0	A4	B4	√	VREF
1	0	A5	B5	√	-
2	1	B7	C6	NA	IO_LVDS_DLL
3	1	D8	C8	√	-
4	1	D9	C9	√	VREF
5	1	D10	C10	√	CS, WRITE
6	2	C11	C12	√	DIN, D0
7	2	D13	E10	1	D1, VREF
8	2	E12	E13	√	D2
9	2	F10	F11	1	D3, VREF
10	3	F13	G13	NA	-
11	3	H12	H11	1	D4, VREF
12	3	H10	J13	√	D5
13	3	J11	J10	1	D6, VREF
14	3	K10	L13	√	INIT
15	4	L11	M11	√	-
16	4	N10	K9	√	VREF
17	4	N9	K8	√	-

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P210	GCK2	1
P209	IO_LVDS_DLL_L6P	1
P208	IO_VREF	1
P207	VCCO	1
P206	IO_L7N_Y	1
P205	IO_VREF_L7P_Y	1
P204	GND	NA
P203	IO_L8N_Y	1
P202	IO_L8P_Y	1
P201[1]	IO_VREF	1
P200	IO_L9N_YY	1
P199	IO_L9P_YY	1
P198	VCCINT	NA
P197	VCCO	1
P196	GND	NA
P195	IO_L10N_YY	1
P194	IO_VREF_L10P_YY	1
P193	IO_VREF	1
P192	IO_L11N_YY	1
P191	IO_VREF_L11P_YY	1
P190	GND	NA
P189	IO_L12N_YY	1
P188	IO_L12P_YY	1
P187	IO_VREF_L13N	1
P186	IO_L13P	1
P185	IO_WRITE_L14N_YY	1
P184	IO_CS_L14P_YY	1
P183	TDI	NA
P182	GND	NA
P181	TDO	2
P180	VCCO	1
P179	CCLK	2
P178	IO_DOUT_BUSY_L15P_YY	2
P177	IO_DIN_D0_L15N_YY	2
P176	VCCO	2
P175	IO_VREF	2
P174	IO_L16P_Y	2
P173	IO_L16N_Y	2
P172	GND	NA
P171	IO_VREF_L17P_Y	2
P170	IO_L17N_Y	2
P169	IO_VREF	2
P168	IO_VREF_L18P_Y	2
P167	IO_D1_L18N_Y	2
P166	GND	NA
P165	VCCO	2
P164	VCCINT	NA
P163	IO_D2_L19P_YY	2
P162	IO_L19N_YY	2
P161[1]	IO_VREF	2
P160	IO_L20P_Y	2
P159	IO_L20N_Y	2
P158	GND	NA
P157	IO_VREF_L21P_Y	2
P156	IO_D3_L21N_Y	2
P155	IO_L22P_Y	2
P154	IO_VREF_L22N_Y	2
P153	IO_L23P_YY	2
P152	IO_L23N_YY	2
P151	GND	NA
P150	VCCO	2
P149	IO	3
P148	VCCINT	NA
P147	IO_VREF	3
P146	VCCO	3
P145	IO_D4_L24P_Y	3
P144	IO_VREF_L24N_Y	3
P143	GND	NA
P142	IO_L25P_Y	3
P141	IO_L25N_Y	3
P140[1]	IO_VREF	3
P139	IO_L26P_YY	3

Table 10: **BG352 — XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
2	IO_D3_L30N _Y	M3
2	IO_L31P	M2
2	IO_L31N	M1
2	IO	N3[1]
2	IO_L32P_YY	N4
2	IO_L32N_YY	N2
3	IO	P1
3	IO	P3[1]
3	IO_L33P	R1
3	IO_L33N	R2
3	IO_D4_L34P _Y	R3
3	IO_VREF_3_L34N _Y	R4
3	IO_L35P_YY	T2
3	IO_L35N_YY	U2
3	IO	T3[1]
3	IO_L36P	T4
3	IO_L36N	V1
3	IO	V2[1]
3	IO_L37P_YY	U3
3	IO_D5_L37N_YY	U4
3	IO_D6_L38P _Y	V3
3	IO_VREF_3_L38N _Y	V4
3	IO_L39P _Y	Y1
3	IO_L39N _Y	Y2
3	IO	W3
3	IO	W4[1]
3	IO	AA1[1]
3	IO_L40P_Y	AA2
3	IO_VREF_3_L40N_Y	Y3
3	IO_L41P_YY	AC1
3	IO_L41N_YY	AB2
3	IO	AA3[1]
3	IO_L42P_YY	AA4
3	IO_VREF_3_L42N_YY	AC2[2]
3	IO	AB3
3	IO	AD1[1]
3	IO	AB4[1]
3	IO_D7_L43P_YY	AC3
3	IO_INIT_L43N_YY	AD2
4	IO_L44P_YY	AC5
4	IO_L44N_YY	AD4
4	IO	AE3[1]
4	IO	AD5[1]
4	IO	AC6
4	IO_VREF_4_L45P_YY	AE4[2]
4	IO_L45N_YY	AF3
4	IO	AF4[1]
4	IO_L46P_YY	AC7
4	IO_L46N_YY	AD6
4	IO_VREF_4_L47P_YY	AE5
4	IO_L47N_YY	AE6
4	IO	AD7[1]
4	IO	AE7[1]
4	IO_L48P	AF6
4	IO_L48N	AC9
4	IO	AD8
4	IO_VREF_4_L49P_YY	AE8
4	IO_L49N_YY	AF7
4	IO_L50P_YY	AD9
4	IO_L50N_YY	AE9
4	IO	AD10[1]
4	IO_L51P	AF9
4	IO_L51N	AC11
4	IO	AE10[1]
4	IO_L52P_Y	AD11
4	IO_L52N_Y	AE11

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
NA	GND	A29	
NA	GND	A32	
NA	GND	A33	
NA	GND	B1	
NA	GND	B6	
NA	GND	B9	
NA	GND	B15	
NA	GND	B23	
NA	GND	B27	
NA	GND	B31	
NA	GND	C2	
NA	GND	E1	
NA	GND	F32	
NA	GND	G2	
NA	GND	G33	
NA	GND	J32	
NA	GND	K1	
NA	GND	L2	
NA	GND	M33	
NA	GND	P1	
NA	GND	P33	
NA	GND	R32	
NA	GND	T1	
NA	GND	V33	
NA	GND	W2	
NA	GND	Y1	
NA	GND	Y33	
NA	GND	AB1	
NA	GND	AC32	
NA	GND	AD33	
NA	GND	AE2	
NA	GND	AG1	
NA	GND	AG32	
NA	GND	AH2	
NA	GND	AJ33	
NA	GND	AL32	
NA	GND	AM3	
NA	GND	AM7	
NA	GND	AM11	
NA	GND	AM19	
NA	GND	AM25	
NA	GND	AM28	
NA	GND	AM33	
NA	GND	AN1	
NA	GND	AN2	
NA	GND	AN5	
NA	GND	AN10	
NA	GND	AN14	
NA	GND	AN16	
NA	GND	AN20	
NA	GND	AN22	
NA	GND	AN27	
NA	GND	AN33	

Notes:

1. V_{REF} or I/O option only in the XCV2000E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV1600E & 2000E; otherwise, I/O option only.
3. V_{REF} or I/O option only in the XCV1000E, 1600E, & 2000E; otherwise, I/O option only.
4. V_{REF} or I/O option only in the XCV600E, 1000E, 1600E, & 2000E; otherwise, I/O option only.

Table 16: **FG256 Package — XCV50E, XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
4	IO_L43P_Y	P12
4	IO_VREF_L43N_Y	R13[2]
4	IO_L44P_YY	N12
4	IO_L44N_YY	T13
4	IO_VREF_L45P_YY	T12
4	IO_L45N_YY	P11
4	IO_L46P_Y	R12
4	IO_L46N_Y	N11
4	IO_VREF_L47P_YY	T11[1]
4	IO_L47N_YY	M11
4	IO_L48P_YY	R11
4	IO_L48N_YY	T10
4	IO_L49P_Y	R10
4	IO_L49N_Y	M10
4	IO_VREF_L50P_Y	P9
4	IO_L50N_Y	T9
4	IO_L51P_Y	N10
4	IO_L51N_Y	R9
4	IO_LVDS_DLL_L52P	N9
5	GCK1	R8
5	IO	N7
5	IO	T7
5	IO_LVDS_DLL_L52N	T8
5	IO_L53P_Y	R7
5	IO_VREF_L53N_Y	P8
5	IO_L54P_Y	P7
5	IO_L54N_Y	T6
5	IO_L55P_YY	M7
5	IO_L55N_YY	R6
5	IO_L56P_YY	P6
5	IO_VREF_L56N_YY	R5[1]
5	IO_L57P_Y	N6
5	IO_L57N_Y	T5
5	IO_L58P_YY	M6
5	IO_VREF_L58N_YY	T4
5	IO_L59P_YY	T3
5	IO_L59N_YY	P5
5	IO_VREF_L60P_Y	T2[2]
5	IO_L60N_Y	N5
6	IO_L61N_YY	M3
6	IO_L61P_YY	R1
6	IO_L62N	M4
6	IO_VREF_L62P	N2[2]
6	IO_L63N_YY	L5
6	IO_L63P_YY	P1
6	IO_VREF_L64N_Y	N1
6	IO_L64P_Y	L3
6	IO_L65N	M2
6	IO_L65P	L4
6	IO_VREF_L66N_Y	M1[1]
6	IO_L66P_Y	K4
6	IO_L67N_YY	L2
6	IO_L67P_YY	L1
6	IO_L68N	K3
6	IO_L68P	K1
6	IO_L69N_YY	K2
6	IO_L69P_YY	K5
6	IO_VREF_L70N_Y	J3
6	IO_L70P_Y	J1
6	IO_L71N	J4
6	IO_L71P	H1
6	IO	J2
7	IO	C2
7	IO_L72N_YY	G1
7	IO_L72P_YY	H4
7	IO_L73N	G5
7	IO_L73P	H2

FG456 Fine-Pitch Ball Grid Array Packages

XCV200E and XCV300E devices in FG456 fine-pitch Ball Grid Array packages have footprint compatibility. Pins labeled IO_VREF can be used as either in both devices provided in this package. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 18, see Table 19 for Differential Pair information.

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
0	GCK3	C11
0	IO	A2[1]
0	IO	A3
0	IO	A6[1]
0	IO	A10
0	IO	B5
0	IO	B9
0	IO	C5
0	IO	D8
0	IO	D10
0	IO	E11[1]
0	IO_L0N	D5
0	IO_L0P	B3
0	IO_VREF_L1N_YY	B4
0	IO_L1P_YY	E6
0	IO_L2N	A4
0	IO_L2P	E7
0	IO_VREF_L3N_YY	C6
0	IO_L3P_YY	D6
0	IO_L4N_Y	A5
0	IO_L4P_Y	B6
0	IO_L5N_Y	D7
0	IO_L5P_Y	C7
0	IO_VREF_L6N_YY	E8
0	IO_L6P_YY	B7
0	IO_L7N_YY	A7
0	IO_L7P_YY	E9
0	IO_L8N_Y	C8
0	IO_L8P_Y	B8
0	IO_L9N_Y	D9
0	IO_L9P_Y	A8
0	IO_L10N	C9
0	IO_L10P	E10
0	IO_VREF_L11N_YY	A9
0	IO_L11P_YY	C10
0	IO_L12N_Y	F11
0	IO_L12P_Y	B10
0	IO_LVDS_DLL_L13N	B11
1	GCK2	A11
1	IO	A12[1]
1	IO	A14
1	IO	B16[1]
1	IO	B19
1	IO	E13
1	IO	E15
1	IO	E16
1	IO	E17[1]
1	IO_LVDS_DLL_L13P	D11
1	IO_L14N_Y	C12
1	IO_L14P_Y	D12
1	IO_L15N_Y	B12
1	IO_L15P_Y	A13
1	IO_L16N_YY	E12
1	IO_VREF_L16P_YY	B13
1	IO_L17N_YY	C13
1	IO_L17P_YY	D13
1	IO_L18N_Y	B14
1	IO_L18P_Y	C14
1	IO_L19N_Y	F12
1	IO_L19P_Y	A15
1	IO_L20N_YY	B15
1	IO_L20P_YY	C15
1	IO_L21N_YY	A16
1	IO_VREF_L21P_YY	E14
1	IO_L22N_Y	D14
1	IO_L22P_Y	C16
1	IO_L23N_Y	D15

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
1	IO_L23P_Y	A17
1	IO_L24N_YY	B17
1	IO_VREF_L24P_YY	A18
1	IO_L25N_YY	D16
1	IO_L25P_YY	C17
1	IO_L26N_YY	B18
1	IO_VREF_L26P_YY	A19
1	IO_L27N_YY	D17
1	IO_L27P_YY	C18
1	IO_WRITE_L28N_YY	A20
1	IO_CS_L28P_YY	C19
2	IO	D18[1]
2	IO	E19[1]
2	IO	E20
2	IO	F20
2	IO	G21
2	IO	G22[1]
2	IO	J22
2	IO	L19[1]
2	IO_D3	K20
2	IO_DOUT_BUSY_L29P_YY	C21
2	IO_DIN_D0_L29N_YY	D20
2	IO_L30P_YY	C22
2	IO_L30N_YY	D21
2	IO_VREF_L31P_YY	D22
2	IO_L31N_YY	E21
2	IO_L32P_YY	E22
2	IO_L32N_YY	F18
2	IO_VREF_L33P_YY	F21
2	IO_L33N_YY	F19
2	IO_L34P_Y	F22
2	IO_L34N_Y	G19
2	IO_L35P_Y	G20
2	IO_L35N_Y	G18
2	IO_VREF_L36P_Y	H18
2	IO_D1_L36N_Y	H22
2	IO_D2_L37P_YY	H20
2	IO_L37N_YY	H19
2	IO_L38P_YY	H21
2	IO_L38N_YY	J19
2	IO_L39P_YY	J18
2	IO_L39N_YY	J20
2	IO_L40P_Y	K18
2	IO_L40N_Y	J21
2	IO_L41P	K22
2	IO_VREF_L41N	K21
2	IO_L42P_Y	K19
2	IO_L42N_Y	L22
2	IO_L43P_YY	L21
2	IO_L43N_YY	L18
2	IO_L44P_YY	L17
2	IO_L44N_YY	L20
3	IO	M21[1]
3	IO	P22
3	IO	R20[1]
3	IO	R22
3	IO	T19
3	IO	U18[1]
3	IO	V20
3	IO	V21
3	IO	Y22[1]
3	IO_L45P_YY	M18
3	IO_L45N_YY	M20
3	IO_L46P_Y	M19
3	IO_L46N_Y	M17
3	IO_D4_L47P_Y	N22
3	IO_VREF_L47N_Y	N21
3	IO_L48P_YY	N20
3	IO_L48N_YY	N18
3	IO_L49P_YY	N19
3	IO_L49N_YY	P21
3	IO_L50P_YY	P20

Table 20: **FG676 — XCV400E, XCV600E**

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
3	IO	Y26
3	IO	AB25
3	IO	AC25[1]
3	IO	AC26
3	IO_L69P_YY	P21
3	IO_L69N_YY	P23
3	IO_L70P_Y	P22
3	IO_VREF_L70N_Y	R25
3	IO_L71P_Y	P19
3	IO_L71N_Y	P20
3	IO_L72P_YY	R21
3	IO_L72N_YY	R22
3	IO_D4_L73P_YY	R24
3	IO_VREF_L73N_YY	R23
3	IO_L74P_Y	T24
3	IO_L74N_Y	R20
3	IO_L75P_Y	T22
3	IO_L75N_Y	U24
3	IO_L76P_Y	T23
3	IO_L76N_Y	U25
3	IO_L77P_Y	T21
3	IO_L77N_Y	U20
3	IO_L78P_YY	U22
3	IO_L78N_YY	V26
3	IO_L79P_YY	T20
3	IO_D5_L79N_YY	U23
3	IO_D6_L80P_YY	V24
3	IO_VREF_L80N_YY	U21
3	IO_L81P_YY	V23
3	IO_L81N_YY	W24
3	IO_L82P_Y	V22
3	IO_VREF_L82N_Y	W26[2]
3	IO_L83P_Y	Y25
3	IO_L83N_Y	V21
3	IO_L84P_YY	V20
3	IO_L84N_YY	AA26
3	IO_L85P_YY	Y24
3	IO_VREF_L85N_YY	W23
3	IO_L86P_Y	AA24
3	IO_L86N_Y	Y23
3	IO_L87P_Y	AB26
3	IO_L87N_Y	W21
3	IO_L88P_Y	Y22
3	IO_VREF_L88N_Y	W22
3	IO_L89P_Y	AA23
3	IO_L89N_Y	AB24
3	IO_L90P_YY	W20
3	IO_L90N_YY	AC24
3	IO_D7_L91P_YY	AB23
3	IO_INIT_L91N_YY	Y21
4	GCK0	AA14
4	IO	AC18
4	IO	AE15[1]
4	IO	AE20
4	IO	AE23
4	IO	AF14[1]
4	IO	AF16[1]
4	IO	AF18[1]
4	IO	AF21
4	IO	AF23[1]
4	IO_L92P_YY	AC22
4	IO_L92N_YY	AD26
4	IO_L93P_Y	AD23
4	IO_L93N_Y	AA20
4	IO_L94P_YY	Y19
4	IO_L94N_YY	AC21
4	IO_VREF_L95P_YY	AD22
4	IO_L95N_YY	AB20
4	IO_L96P	AE22
4	IO_L96N	Y18
4	IO_L97P	AF22
4	IO_L97N	AA19
4	IO_VREF_L98P_YY	AD21

FG680 Fine-Pitch Ball Grid Array Package

XCV600E, XCV1000E, XCV1600E, and XCV2000E devices in the FG680 fine-pitch Ball Grid Array package have footprint compatibility. Pins labeled IO_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 22, see Table 23 for Differential Pair information.

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
0	GCK3	A20
0	IO	D35
0	IO	B36
0	IO_L0N_Y	C35
0	IO_L0P_Y	A36
0	IO_VREF_L1N_Y	D34[1]
0	IO_L1P_Y	B35
0	IO_L2N_YY	C34
0	IO_L2P_YY	A35
0	IO_VREF_L3N_YY	D33
0	IO_L3P_YY	B34
0	IO_L4N	C33
0	IO_L4P	A34
0	IO_L5N_Y	D32
0	IO_L5P_Y	B33
0	IO_L6N_YY	C32
0	IO_L6P_YY	D31
0	IO_VREF_L7N_YY	A33
0	IO_L7P_YY	C31
0	IO_L8N_Y	B32
0	IO_L8P_Y	B31
0	IO_VREF_L9N_Y	A32[3]
0	IO_L9P_Y	D30
0	IO_L10N_YY	A31
0	IO_L10P_YY	C30
0	IO_VREF_L11N_YY	B30
0	IO_L11P_YY	D29
0	IO_L12N_Y	A30
0	IO_L12P_Y	C29
0	IO_L13N_Y	A29
0	IO_L13P_Y	B29
0	IO_VREF_L14N_YY	B28
0	IO_L14P_YY	A28
0	IO_L15N_YY	C28
0	IO_L15P_YY	B27
0	IO_L16N_Y	D27
0	IO_L16P_Y	A27
0	IO_L17N_Y	C27
0	IO_L17P_Y	B26
0	IO_L18N_YY	D26
0	IO_L18P_YY	C26
0	IO_VREF_L19N_YY	A26[1]
0	IO_L19P_YY	D25
0	IO_L20N_Y	B25
0	IO_L20P_Y	C25
0	IO_L21N_Y	A25
0	IO_L21P_Y	D24
0	IO_L22N_YY	A24
0	IO_L22P_YY	B23
0	IO_VREF_L23N_YY	C24
0	IO_L23P_YY	A23
0	IO_L24N_Y	B24
0	IO_L24P_Y	B22
0	IO_L25N_Y	E23
0	IO_L25P_Y	A22
0	IO_L26N_YY	D23
0	IO_L26P_YY	B21
0	IO_VREF_L27N_YY	C23
0	IO_L27P_YY	A21
0	IO_L28N_Y	E22
0	IO_L28P_Y	B20
0	IO_LVDS_DLL_L29N	C22
0	IO_VREF	D22[2]
1	GCK2	D21

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
2	IO	D29[5]
2	IO	G26[4]
2	IO	H24[4]
2	IO	H25[4]
2	IO	H28[5]
2	IO	J25[4]
2	IO	J27[5]
2	IO	K30[4]
2	IO	M24[4]
2	IO	M25[4]
2	IO	N20
2	IO	N23[4]
2	IO	P26[5]
2	IO	P27[5]
2	IO	P30[4]
2	IO	R30
2	IO_DOUT_BUSY_L70P_YY	J22
2	IO_DIN_D0_L70N_YY	E27
2	IO_L71P	C29[4]
2	IO_L71N	D28[3]
2	IO_L72P_Y	G25
2	IO_L72N_Y	E25
2	IO_VREF_L73P_YY	E28[1]
2	IO_L73N_YY	C30
2	IO_L74P_Y	K22[4]
2	IO_L74N_Y	F27[3]
2	IO_L75P_YY	D30
2	IO_L75N_YY	J23
2	IO_VREF_L76P_Y	L21
2	IO_L76N_Y	F28
2	IO_L77P_YY	G28
2	IO_L77N_YY	E30
2	IO_L78P_YY	G27
2	IO_L78N_YY	E29
2	IO_L79P	K23
2	IO_L79N	H26
2	IO_VREF_L80P_YY	F30
2	IO_L80N_YY	L22
2	IO_L81P_YY	H27
2	IO_L81N_YY	G29
2	IO_L82P	G30
2	IO_L82N	M21
2	IO_L83P_YY	J24
2	IO_L83N_YY	J26
2	IO_VREF_L84P_YY	H30
2	IO_L84N_YY	L23
2	IO_L85P_YY	K26[4]
2	IO_L85N_YY	J28[3]
2	IO_L86P_YY	J29
2	IO_L86N_YY	K24
2	IO_L87P_YY	K27[4]
2	IO_VREF_L87N_YY	J30
2	IO_D1_L88P	M22
2	IO_D2_L88N	K29
2	IO_L89P_YY	K28[3]
2	IO_L89N_YY	L25[4]
2	IO_L90P	N21
2	IO_L90N	K25
2	IO_L91P_YY	L24
2	IO_L91N_YY	L27
2	IO_L92P_Y	L29[4]
2	IO_L92N_Y	M23[4]
2	IO_L93P_YY	L26
2	IO_L93N_YY	L28
2	IO_VREF_L94P	L30[1]
2	IO_L94N	M27
2	IO_L95P_YY	M26
2	IO_L95N_YY	M29
2	IO_L96P_YY	N29
2	IO_L96N_YY	M30
2	IO_L97P	N25
2	IO_L97N	N27
2	IO_VREF_L98P_YY	N30
2	IO_D3_L98N_YY	P21

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
7	IO_L275N_YY	G3
7	IO_L275P_YY	E1
7	IO_L276N_YY	H6
7	IO_L276P_YY	E2
7	IO_L277N	E4
7	IO_VREF_L277P	K9
7	IO_L278N_YY	J8
7	IO_L278P_YY	F4
7	IO_L279N_Y	D1[3]
7	IO_L279P_Y	H7[4]
7	IO_L280N_YY	G6
7	IO_VREF_L280P_YY	C2[1]
7	IO_L281N	D2
7	IO_L281P	F5
7	IO_L282N_YY	D3[4]
7	IO_L282P_YY	K10[3]
2	CCLK	F26
3	DONE	AJ28
NA	DXN	AJ3
NA	DXP	AH4
NA	M0	AF4
NA	M1	AC7
NA	M2	AK3
NA	PROGRAM	AG28
NA	TCK	B3
NA	TDI	H22
2	TDO	D26
NA	TMS	C1
NA	VCCINT	L11
NA	VCCINT	L12
NA	VCCINT	L19
NA	VCCINT	L20
NA	VCCINT	M11
NA	VCCINT	M12
NA	VCCINT	M19

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
NA	VCCINT	M20
NA	VCCINT	N13
NA	VCCINT	N14
NA	VCCINT	N15
NA	VCCINT	N16
NA	VCCINT	N17
NA	VCCINT	N18
NA	VCCINT	P13
NA	VCCINT	P18
NA	VCCINT	R13
NA	VCCINT	R18
NA	VCCINT	T13
NA	VCCINT	T18
NA	VCCINT	U13
NA	VCCINT	U18
NA	VCCINT	V13
NA	VCCINT	V14
NA	VCCINT	V15
NA	VCCINT	V16
NA	VCCINT	V17
NA	VCCINT	V18
NA	VCCINT	W11
NA	VCCINT	W12
NA	VCCINT	W19
NA	VCCINT	W20
NA	VCCINT	Y11
NA	VCCINT	Y12
NA	VCCINT	Y19
NA	VCCINT	Y20
NA	VCCO_0	B6
NA	VCCO_0	M15
NA	VCCO_0	M14
NA	VCCO_0	L15
NA	VCCO_0	L14
NA	VCCO_0	H14
NA	VCCO_0	M13

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
0	IO_L40P_Y	A17
0	IO_VREF_L41N_Y	G17[1]
0	IO_L41P_Y	B17
0	IO_LVDS_DLL_L42N	C17
1	GCK2	D17
1	IO	A18
1	IO	B18[3]
1	IO	B24
1	IO	B25
1	IO	E22[3]
1	IO	E23[3]
1	IO	D18[3]
1	IO	D19
1	IO	D25[3]
1	IO	D26[3]
1	IO	D28[3]
1	IO	D29[3]
1	IO	G23[3]
1	IO	J23[3]
1	IO_LVDS_DLL_L42P	J18
1	IO_L43N_Y	G18
1	IO_VREF_L43P_Y	C18[1]
1	IO_L44N_Y	H18
1	IO_L44P_Y	F18
1	IO_L45N_YY	B19
1	IO_VREF_L45P_YY	A19
1	IO_L46N_YY	K19
1	IO_L46P_YY	C19
1	IO_L47N	F19[5]
1	IO_L47P	E19[4]
1	IO_L48N_Y	G19
1	IO_L48P_Y	J19
1	IO_L49N_Y	A20
1	IO_L49P_Y	G20
1	IO_L50N	B20[5]
1	IO_L50P	F20[4]
1	IO_L51N_YY	D20
1	IO_VREF_L51P_YY	E20
1	IO_L52N_YY	H20
1	IO_L52P_YY	A21
1	IO_L53N	E21[5]
1	IO_L53P	J20[4]
1	IO_L54N_Y	D21
1	IO_L54P_Y	K20
1	IO_L55N_Y	B21
1	IO_L55P_Y	H21
1	IO_L56N_YY	G21[5]
1	IO_L56P_YY	F21[4]
1	IO_L57N_YY	A22
1	IO_VREF_L57P_YY	B22
1	IO_L58N_YY	J21
1	IO_L58P_YY	C22
1	IO_L59N_Y	D22
1	IO_L59P_Y	G22
1	IO_L60N_Y	K21
1	IO_L60P_Y	A23
1	IO_L61N_Y	F22
1	IO_L61P_Y	B23
1	IO_L62N_Y	C23
1	IO_L62P_Y	H22
1	IO_L63N_YY	D23
1	IO_L63P_YY	K22
1	IO_L64N_YY	A24
1	IO_VREF_L64P_YY	J22
1	IO_L65N_Y	H23
1	IO_L65P_Y	D24
1	IO_L66N_Y	A25

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
4	IO_L212N_YY	AP18
4	IO_L213P_Y	AF18
4	IO_L213N_Y	AP17
4	IO_VREF_L214P_Y	AJ18[1]
4	IO_L214N_Y	AL18
4	IO_LVDS_DLL_L215P	AM18
5	GCK1	AL19
5	IO	AF17[3]
5	IO	AG12[3]
5	IO	AH12
5	IO	AJ10[3]
5	IO	AJ11[3]
5	IO	AK7[3]
5	IO	AK13[3]
5	IO	AL13[3]
5	IO	AM4[3]
5	IO	AN9
5	IO	AN10[3]
5	IO	AN16
5	IO	AN17[3]
5	IO_LVDS_DLL_L215N	AL17
5	IO_L216P_Y	AH17
5	IO_VREF_L216N_Y	AM17[1]
5	IO_L217P_Y	AJ17
5	IO_L217N_Y	AG17
5	IO_L218P_YY	AP16
5	IO_VREF_L218N_YY	AL16
5	IO_L219P_YY	AJ16
5	IO_L219N_YY	AM16
5	IO_L220P	AK16[5]
5	IO_L220N	AP15[4]
5	IO_L221P_Y	AL15
5	IO_L221N_Y	AH16
5	IO_L222P_Y	AN15
5	IO_L222N_Y	AF16
5	IO_L223P_Y	AP14[5]
5	IO_L223N_Y	AE16[4]
5	IO_L224P_YY	AK15
5	IO_VREF_L224N_YY	AJ15
5	IO_L225P_YY	AH15
5	IO_L225N_YY	AN14
5	IO_L226P	AK14[5]
5	IO_L226N	AG15[4]
5	IO_L227P_Y	AM13
5	IO_L227N_Y	AF15
5	IO_L228P_Y	AG14
5	IO_L228N_Y	AP13
5	IO_L229P_YY	AE14[5]
5	IO_L229N_YY	AE15[4]
5	IO_L230P_YY	AN13
5	IO_VREF_L230N_YY	AG13
5	IO_L231P_YY	AH14
5	IO_L231N_YY	AP12
5	IO_L232P_Y	AJ14
5	IO_L232N_Y	AL14
5	IO_L233P_Y	AF13
5	IO_L233N_Y	AN12
5	IO_L234P_Y	AF14
5	IO_L234N_Y	AP11
5	IO_L235P_Y	AN11
5	IO_L235N_Y	AH13
5	IO_L236P_YY	AM12
5	IO_L236N_YY	AL12
5	IO_L237P_YY	AJ13
5	IO_VREF_L237N_YY	AP10
5	IO_L238P_Y	AK12
5	IO_L238N_Y	AM10

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
NA	VCCINT	N22
NA	VCCINT	P13
NA	VCCINT	P22
NA	VCCINT	R13
NA	VCCINT	R22
NA	VCCINT	T13
NA	VCCINT	T22
NA	VCCINT	U10
NA	VCCINT	U25
NA	VCCINT	V10
NA	VCCINT	V25
NA	VCCINT	W13
NA	VCCINT	W22
NA	VCCINT	Y13
NA	VCCINT	Y22
NA	VCCINT	AA13
NA	VCCINT	AA22
NA	VCCINT	AB13
NA	VCCINT	AB14
NA	VCCINT	AB15
NA	VCCINT	AB16
NA	VCCINT	AB19
NA	VCCINT	AB20
NA	VCCINT	AB21
NA	VCCINT	AB22
NA	VCCINT	AC12
NA	VCCINT	AC23
NA	VCCINT	AD24
NA	VCCINT	AD11
NA	VCCINT	AE10
NA	VCCINT	AE17
NA	VCCINT	AE18
NA	VCCINT	AE25
NA	VCCO_0	M17
NA	VCCO_0	L17
NA	VCCO_0	L16
NA	VCCO_0	E10
NA	VCCO_0	C14
NA	VCCO_0	A6
NA	VCCO_0	M13
NA	VCCO_0	M14
NA	VCCO_0	M15
NA	VCCO_0	M16
NA	VCCO_0	L12
NA	VCCO_0	L13
NA	VCCO_0	L14
NA	VCCO_0	L15
NA	VCCO_1	M18
NA	VCCO_1	L18
NA	VCCO_1	L23
NA	VCCO_1	E25
NA	VCCO_1	C21
NA	VCCO_1	A29
NA	VCCO_1	M19
NA	VCCO_1	M20
NA	VCCO_1	M21
NA	VCCO_1	M22
NA	VCCO_1	L19
NA	VCCO_1	L20
NA	VCCO_1	L21
NA	VCCO_1	L22
NA	VCCO_2	U24
NA	VCCO_2	U23
NA	VCCO_2	N24
NA	VCCO_2	M24
NA	VCCO_2	K30
NA	VCCO_2	F34

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
71	1	A27	G24	3200 2000 1000	-
72	1	G25	B27	3200 1600	-
73	1	C27	E26	3200 2600 2000 1600 1000	VREF
74	1	B28	J24	3200 2600 2000 1600 1000	-
75	1	H25	K24	3200 2600	-
76	1	F26	D27	3200 1000	-
77	1	C28	G26	3200 1000	-
78	1	J25	E27	2000 1600	-
79	1	H26	A30	3200 2600 2000 1600 1000	VREF
80	1	B29	G27	3200 2600 2000 1600 1000	-
81	1	C29	F27	3200 2600 1000	-
82	1	F28	E28	3200 2000 1000	VREF
83	1	B30	L25	3200 2000 1000	-
84	1	E29	B31	3200 1600 1000	-
85	1	D30	A31	3200 2600 2000 1600 1000	CS
86	2	D32	J27	3200 2600 2000 1600 1000	DIN, D0
87	2	E31	F30	3200 2600 2000	-
88	2	G29	F32	2600 2000 1000	-
89	2	E32	G30	3200 2600 1600 1000	VREF
90	2	M25	G31	2600 1600	-
91	2	L26	D33	3200 2600 1600 1000	-
92	2	D34	H29	2600 2000 1000	VREF
93	2	J28	E33	3200 2600 2000 1600	-
94	2	H28	H30	3200 2600 2000 1600 1000	-
95	2	H32	K28	3200 2600 1600 1000	-
96	2	L27	F33	3200 2600 2000	-
97	2	M26	E34	2600 2000 1000	-
98	2	H31	G32	3200 2600 2000 1600 1000	VREF
99	2	N25	J31	2000 1600	-
100	2	J30	G33	3200 2600 2000 1600 1000	-
101	2	H34	J29	2600 1000	VREF
102	2	M27	H33	3200 2600 1600	-
103	2	K29	J34	3200 2600 1600 1000	-
104	2	L29	J33	3200 2600 2000 1600 1000	VREF
105	2	M28	K34	3200 2600 2000 1600 1000	-
106	2	N27	L34	3200 1600 1000	-
107	2	K33	P26	2000 1600 1000	D1
108	2	R25	M34	3200 2600 2000	-
109	2	L31	L33	2000 1000	-
110	2	P27	M33	3200 2600 1600 1000	-