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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	3456
Number of Logic Elements/Cells	15552
Total RAM Bits	294912
Number of I/O	316
Number of Gates	985882
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	432-LBGA Exposed Pad, Metal
Supplier Device Package	432-MBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv600e-6bg432c

Architectural Description

Virtex-E Array

The Virtex-E user-programmable gate array, shown in **Figure 1**, comprises two major configurable elements: configurable logic blocks (CLBs) and input/output blocks (IOBs).

- CLBs provide the functional elements for constructing logic
- IOBs provide the interface between the package pins and the CLBs

CLBs interconnect through a general routing matrix (GRM). The GRM comprises an array of routing switches located at the intersections of horizontal and vertical routing channels. Each CLB nests into a VersaBlock™ that also provides local routing resources to connect the CLB to the GRM.

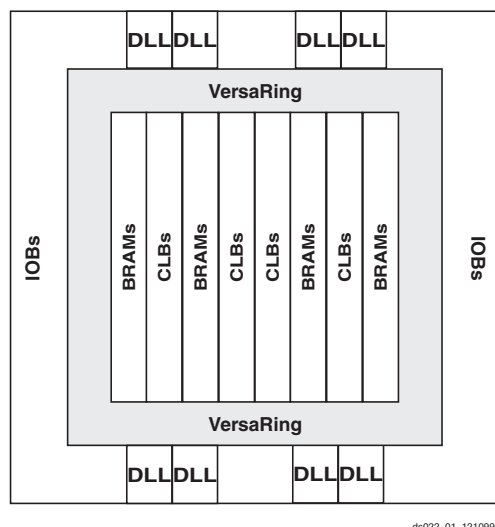


Figure 1: Virtex-E Architecture Overview

The VersaRing™ I/O interface provides additional routing resources around the periphery of the device. This routing improves I/O routability and facilitates pin locking.

The Virtex-E architecture also includes the following circuits that connect to the GRM.

- Dedicated block memories of 4096 bits each
- Clock DLLs for clock-distribution delay compensation and clock domain control
- 3-State buffers (BUFTs) associated with each CLB that drive dedicated segmentable horizontal routing resources

Values stored in static memory cells control the configurable logic elements and interconnect resources. These values load into the memory cells on power-up, and can reload if necessary to change the function of the device.

Input/Output Block

The Virtex-E IOB, **Figure 2**, features SelectI/O+ inputs and outputs that support a wide variety of I/O signalling standards, see **Table 1**.

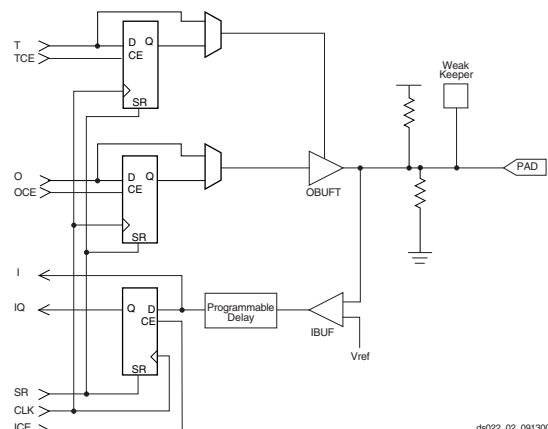


Figure 2: Virtex-E Input/Output Block (IOB)

The three IOB storage elements function either as edge-triggered D-type flip-flops or as level-sensitive latches. Each IOB has a clock signal (CLK) shared by the three flip-flops and independent clock enable signals for each flip-flop.

Application Examples

Creating a design with the SelectI/O features requires the instantiation of the desired library symbol within the design code. At the board level, designers need to know the termination techniques required for each I/O standard.

This section describes some common application examples illustrating the termination techniques recommended by each of the standards supported by the SelectI/O features.

Termination Examples

Circuit examples involving typical termination techniques for each of the SelectI/O standards follow. For a full range of accepted values for the DC voltage specifications for each standard, refer to the table associated with each figure.

The resistors used in each termination technique example and the transmission lines depicted represent board level components and are not meant to represent components on the device.

GTL

A sample circuit illustrating a valid termination technique for GTL is shown in Figure 44.

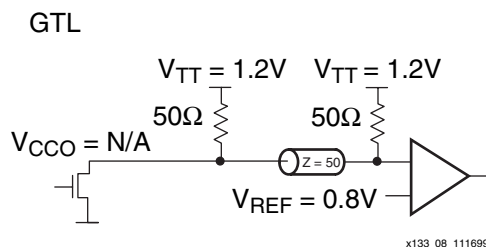


Figure 44: Terminated GTL

Table 23 lists DC voltage specifications.

Table 23: GTL Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	-	N/A	-
$V_{REF} = N \times V_{TT}^1$	0.74	0.8	0.86
V_{TT}	1.14	1.2	1.26
$V_{IH} = V_{REF} + 0.05$	0.79	0.85	-
$V_{IL} = V_{REF} - 0.05$	-	0.75	0.81
V_{OH}	-	-	-
V_{OL}	-	0.2	0.4
I_{OH} at V_{OH} (mA)	-	-	-
I_{OL} at V_{OL} (mA) at 0.4V	32	-	-
I_{OL} at V_{OL} (mA) at 0.2V	-	-	40

Notes:

1. N must be greater than or equal to 0.653 and less than or equal to 0.68.

GTL+

A sample circuit illustrating a valid termination technique for GTL+ appears in Figure 45. DC voltage specifications appear in Table 24.

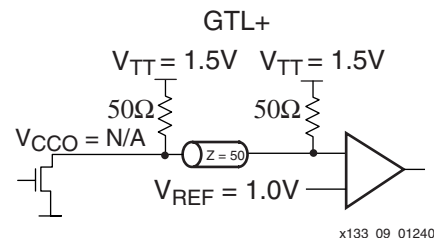


Figure 45: Terminated GTL+

Table 24: GTL+ Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	-	-	-
$V_{REF} = N \times V_{TT}^1$	0.88	1.0	1.12
V_{TT}	1.35	1.5	1.65
$V_{IH} = V_{REF} + 0.1$	0.98	1.1	-
$V_{IL} = V_{REF} - 0.1$	-	0.9	1.02
V_{OH}	-	-	-
V_{OL}	0.3	0.45	0.6
I_{OH} at V_{OH} (mA)	-	-	-
I_{OL} at V_{OL} (mA) at 0.6V	36	-	-
I_{OL} at V_{OL} (mA) at 0.3V	-	-	48

Notes:

1. N must be greater than or equal to 0.653 and less than or equal to 0.68.

Table 44: Bidirectional I/O Library Macros

Name	Inputs	Bidirectional	Outputs
IOBUFDS_FD_LVDS	D, T, C	IO, IOB	Q
IOBUFDS_FDE_LVDS	D, T, CE, C	IO, IOB	Q
IOBUFDS_FDC_LVDS	D, T, C, CLR	IO, IOB	Q
IOBUFDS_FDCE_LVDS	D, T, CE, C, CLR	IO, IOB	Q
IOBUFDS_FDP_LVDS	D, T, C, PRE	IO, IOB	Q
IOBUFDS_FDPE_LVDS	D, T, CE, C, PRE	IO, IOB	Q
IOBUFDS_FDR_LVDS	D, T, C, R	IO, IOB	Q
IOBUFDS_FDRE_LVDS	D, T, CE, C, R	IO, IOB	Q
IOBUFDS_FDS_LVDS	D, T, C, S	IO, IOB	Q
IOBUFDS_FDSE_LVDS	D, T, CE, C, S	IO, IOB	Q
IOBUFDS_LD_LVDS	D, T, G	IO, IOB	Q
IOBUFDS_LDE_LVDS	D, T, GE, G	IO, IOB	Q
IOBUFDS_LDC_LVDS	D, T, G, CLR	IO, IOB	Q
IOBUFDS_LDCE_LVDS	D, T, GE, G, CLR	IO, IOB	Q
IOBUFDS_LDP_LVDS	D, T, G, PRE	IO, IOB	Q
IOBUFDS_LDPE_LVDS	D, T, GE, G, PRE	IO, IOB	Q

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/7/99	1.0	Initial Xilinx release.
1/10/00	1.1	Re-released with spd.txt v. 1.18, FG860/900/1156 package information, and additional DLL, Select RAM and SelectI/O information.
1/28/00	1.2	Added Delay Measurement Methodology table, updated SelectI/O section, Figures 30, 54, & 55, text explaining Table 5, T_{BYP} values, buffered Hex Line info, p. 8, I/O Timing Measurement notes, notes for Tables 15, 16, and corrected F1156 pinout table footnote references.
2/29/00	1.3	Updated pinout tables, V_{CC} page 20, and corrected Figure 20.
5/23/00	1.4	Correction to table on p. 22.
7/10/00	1.5	- Numerous minor edits. - Data sheet upgraded to Preliminary. - Preview -8 numbers added to Virtex-E Electrical Characteristics tables.
8/1/00	1.6	- Reformatted entire document to follow new style guidelines. - Changed speed grade values in tables on pages 35-37.

Virtex-E Electrical Characteristics

Definition of Terms

Electrical and switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance: These speed files are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These speed files are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production: These speed files are released once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. Contact the factory for design considerations requiring more detailed information.

Table 1 correlates the current status of each Virtex-E device with a corresponding speed file designation.

Table 1: Virtex-E Device Speed Grade Designations

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XCV50E			-8, -7, -6
XCV100E			-8, -7, -6
XCV200E			-8, -7, -6
XCV300E			-8, -7, -6
XCV400E			-8, -7, -6
XCV600E			-8, -7, -6
XCV1000E			-8, -7, -6
XCV1600E			-8, -7, -6
XCV2000E			-8, -7, -6
XCV2600E			-8, -7, -6
XCV3200E			-8, -7, -6

All specifications are subject to change without notice.

Table 2: IOB Input Switching Characteristics (Continued)

			Speed Grade ⁽¹⁾				Units
Description ⁽²⁾	Symbol	Device	Min	-8	-7	-6	
Sequential Delays							
Clock CLK							
Minimum Pulse Width, High	T _{CH}	All	0.56	1.2	1.3	1.4	ns, min
Minimum Pulse Width, Low	T _{CL}		0.56	1.2	1.3	1.4	ns, min
Clock CLK to output IQ	T _{IOCKIQ}		0.18	0.4	0.7	0.7	ns, max
Setup and Hold Times with respect to Clock at IOB Input Register							
Pad, no delay	T _{IOICKP} / T _{IOICKP}	All	0.69 / 0	1.3 / 0	1.4 / 0	1.5 / 0	ns, min
Pad, with delay	T _{IOICKD} / T _{IOICKPD}	XCV50E	1.25 / 0	2.8 / 0	2.9 / 0	2.9 / 0	ns, min
		XCV100E	1.25 / 0	2.8 / 0	2.9 / 0	2.9 / 0	ns, min
		XCV200E	1.33 / 0	3.0 / 0	3.1 / 0	3.1 / 0	ns, min
		XCV300E	1.33 / 0	3.0 / 0	3.1 / 0	3.1 / 0	ns, min
		XCV400E	1.37 / 0	3.1 / 0	3.2 / 0	3.2 / 0	ns, min
		XCV600E	1.49 / 0	3.4 / 0	3.5 / 0	3.5 / 0	ns, min
		XCV1000E	1.49 / 0	3.4 / 0	3.5 / 0	3.5 / 0	ns, min
		XCV1600E	1.53 / 0	3.5 / 0	3.6 / 0	3.6 / 0	ns, min
		XCV2000E	1.53 / 0	3.5 / 0	3.6 / 0	3.6 / 0	ns, min
		XCV2600E	1.53 / 0	3.5 / 0	3.6 / 0	3.6 / 0	ns, min
XCV3200E	1.53 / 0	3.5 / 0	3.6 / 0	3.6 / 0	ns, min		
ICE input	T _{IOICECK} / T _{IOCKICE}	All	0.28 / 0.0	0.55 / 0.01	0.7 / 0.01	0.7 / 0.01	ns, min
SR input (IFF, synchronous)	T _{IOSRCKI}	All	0.38	0.8	0.9	1.0	ns, min
Set/Reset Delays							
SR input to IQ (asynchronous)	T _{IOSRIQ}	All	0.54	1.1	1.2	1.4	ns, max
GSR to output IQ	T _{GSRQ}	All	3.88	7.6	8.5	9.7	ns, max

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. Input timing t_i for LVTTTL is measured at 1.4 V. For other I/O standards, see Table 4.

Clock Distribution Switching Characteristics

		Speed Grade				Units
Description	Symbol	Min	-8	-7	-6	
GCLK IOB and Buffer						
Global Clock PAD to output.	T _{GPIO}	0.38	0.7	0.7	0.7	ns, max
Global Clock Buffer I input to O output	T _{GIO}	0.11	0.20	0.45	0.50	ns, max

I/O Standard Global Clock Input Adjustments

Description	Symbol ⁽¹⁾	Standard	Speed Grade				Units
			Min	-8	-7	-6	
Data Input Delay Adjustments							
Standard-specific global clock input delay adjustments	T _{GPLVTTL}	LVTTL	0.0	0.0	0.0	0.0	ns, max
	T _{GPLVCMOS2}	LVC MOS2	−0.02	0.0	0.0	0.0	ns, max
	T _{GPLVCMOS18}	LVC MOS18	0.12	0.20	0.20	0.20	ns, max
	T _{GLVDS}	LVDS	0.23	0.38	0.38	0.38	ns, max
	T _{GLVPECL}	LVPECL	0.23	0.38	0.38	0.38	ns, max
	T _{GP PCI33_3}	PCI, 33 MHz, 3.3 V	−0.05	0.08	0.08	0.08	ns, max
	T _{GP PCI66_3}	PCI, 66 MHz, 3.3 V	−0.05	−0.11	−0.11	−0.11	ns, max
	T _{GPGTL}	GTL	0.20	0.37	0.37	0.37	ns, max
	T _{GPGTLP}	GTL+	0.20	0.37	0.37	0.37	ns, max
	T _{GPHSTL}	HSTL	0.18	0.27	0.27	0.27	ns, max
	T _{GPSSTL2}	SSTL2	0.21	0.27	0.27	0.27	ns, max
	T _{GPSSTL3}	SSTL3	0.18	0.27	0.27	0.27	ns, max
	T _{GPCTT}	CTT	0.22	0.33	0.33	0.33	ns, max
	T _{GPAGP}	AGP	0.21	0.27	0.27	0.27	ns, max

Notes:

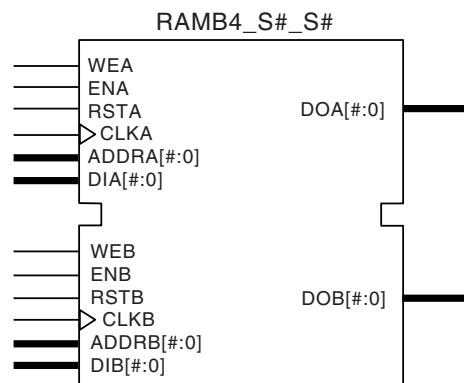
1. Input timing for GPLVTTL is measured at 1.4 V. For other I/O standards, see [Table 4](#).

CLB Distributed RAM Switching Characteristics

		Speed Grade ⁽¹⁾				Units
Description	Symbol	Min	-8	-7	-6	
Sequential Delays						
Clock CLK to X/Y outputs (WE active) 16 x 1 mode	T _{SHCKO16}	0.67	1.38	1.5	1.7	ns, max
Clock CLK to X/Y outputs (WE active) 32 x 1 mode	T _{SHCKO32}	0.84	1.66	1.9	2.1	ns, max
Shift-Register Mode						
Clock CLK to X/Y outputs	T _{REG}	1.25	2.39	2.9	3.2	ns, max
Setup and Hold Times before/after Clock CLK						
F/G address inputs	T _{AS} /T _{AH}	0.19 / 0	0.38 / 0	0.42 / 0	0.47 / 0	ns, min
BX/BY data inputs (DIN)	T _{DS} /T _{DH}	0.44 / 0	0.87 / 0	0.97 / 0	1.09 / 0	ns, min
SR input (WE)	T _{WS} /T _{WH}	0.29 / 0	0.57 / 0	0.7 / 0	0.8 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T _{WPH}	0.96	1.9	2.1	2.4	ns, min
Minimum Pulse Width, Low	T _{WPL}	0.96	1.9	2.1	2.4	ns, min
Minimum clock period to meet address write cycle time	T _{WC}	1.92	3.8	4.2	4.8	ns, min
Shift-Register Mode						
Minimum Pulse Width, High	T _{SRPH}	1.0	1.9	2.1	2.4	ns, min
Minimum Pulse Width, Low	T _{SRPL}	1.0	1.9	2.1	2.4	ns, min

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.



ds022_06_121699

Figure 3: Dual-Port Block SelectRAM

Table 6: PQ240 — XCV50E, XCV100E, XCV200E, XCV300E, XCV400E

Pin #	Pin Description	Bank
P74	IO_L43P_YY	5
P73 ¹	IO_VREF_L43N_YY	5
P72	IO	5
P71	IO_L44P_YY	5
P70	IO_VREF_L44N_YY	5
P68	IO_L45P_YY	5
P67	IO_L45N_YY	5
P66 ²	IO_VREF_L46P_Y	5
P65	IO_L46N_Y	5
P64	IO_L47P_YY	5
P63	IO_L47N_YY	5
P57	IO_L48N_YY	6
P56	IO_L48P_YY	6
P54 ²	IO_VREF	6
P53	IO_L49N_Y	6
P52	IO_L49P_Y	6
P50	IO_VREF_L50N_Y	6
P49	IO_L50P_Y	6
P48	IO	6
P47 ¹	IO_VREF_L51N_Y	6
P46	IO_L51P_Y	6
P42	IO_L52N_YY	6
P41	IO_L52P_YY	6
P40	IO	6
P39	IO_L53N_Y	6
P38	IO_L53P_Y	6
P36	IO_VREF_L54N_Y	6
P35	IO_L54P_Y	6
P34	IO_L55N_Y	6
P33 ³	IO_VREF_L55P_Y	6
P31	IO	6
P28	IO_L56N_YY	7
P27	IO_L56P_YY	7

Table 6: PQ240 — XCV50E, XCV100E, XCV200E, XCV300E, XCV400E

Pin #	Pin Description	Bank
P26 ³	IO_VREF	7
P24	IO_L57N_Y	7
P23	IO_VREF_L57P_Y	7
P21	IO_L58N_Y	7
P20	IO_L58P_Y	7
P19	IO	7
P18	IO_L59N_YY	7
P17	IO_L59P_YY	7
P13	IO_L60N_Y	7
P12 ¹	IO_VREF_L60P_Y	7
P11	IO	7
P10	IO_L61N_Y	7
P9	IO_VREF_L61P_Y	7
P7	IO_L62N_Y	7
P6	IO_L62P_Y	7
P5 ²	IO_VREF_L63N_Y	7
P4	IO_L63P_Y	7
P3	IO	7
P179	CCLK	2
P120	DONE	3
P60	M0	NA
P58	M1	NA
P62	M2	NA
P122	PROGRAM	NA
P183	TDI	NA
P239	TCK	NA
P181	TDO	2
P2	TMS	NA
P225	VCCINT	NA
P214	VCCINT	NA
P198	VCCINT	NA
P164	VCCINT	NA
P148	VCCINT	NA

Table 6: PQ240 — XCV50E, XCV100E, XCV200E, XCV300E, XCV400E

Pin #	Pin Description	Bank
P137	VCCINT	NA
P104	VCCINT	NA
P88	VCCINT	NA
P77	VCCINT	NA
P43	VCCINT	NA
P32	VCCINT	NA
P16	VCCINT	NA
P240	VCCO	7
P232	VCCO	0
P226	VCCO	0
P212	VCCO	0
P207	VCCO	1
P197	VCCO	1
P180	VCCO	1
P176	VCCO	2
P165	VCCO	2
P150	VCCO	2
P146	VCCO	3
P136	VCCO	3
P121	VCCO	3
P116	VCCO	4
P105	VCCO	4
P90	VCCO	4
P85	VCCO	5
P76	VCCO	5
P61	VCCO	5
P55	VCCO	6
P44	VCCO	6
P30	VCCO	6
P25	VCCO	7
P15	VCCO	7
P233	GND	NA
P227	GND	NA

Table 6: PQ240 — XCV50E, XCV100E, XCV200E, XCV300E, XCV400E

Pin #	Pin Description	Bank
P219	GND	NA
P211	GND	NA
P204	GND	NA
P196	GND	NA
P190	GND	NA
P182	GND	NA
P172	GND	NA
P166	GND	NA
P158	GND	NA
P151	GND	NA
P143	GND	NA
P135	GND	NA
P129	GND	NA
P119	GND	NA
P112	GND	NA
P106	GND	NA
P98	GND	NA
P91	GND	NA
P83	GND	NA
P75	GND	NA
P69	GND	NA
P59	GND	NA
P51	GND	NA
P45	GND	NA
P37	GND	NA
P29	GND	NA
P22	GND	NA
P14	GND	NA
P8	GND	NA
P1	GND	NA

Notes:

1. V_{REF} or I/O option only in the XCV100E, 200E, 300E, 400E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV200E, 300E, 400E; otherwise, I/O option only.
3. V_{REF} or I/O option only in the XCV400E; otherwise, I/O option only.

Table 14: BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin#	See Note
4	IO_L104N_YY	AJ12	
4	IO_L105P_Y	AN11	
4	IO_L105N_Y	AK12	
4	IO_L106P_YY	AL12	
4	IO_L106N_YY	AM12	
4	IO_VREF_L107P_YY	AK13	3
4	IO_L107N_YY	AL13	
4	IO_L108P_Y	AM13	
4	IO_L108N_Y	AN13	
4	IO_L109P_YY	AJ14	
4	IO_L109N_YY	AK14	
4	IO_VREF_L110P_YY	AM14	
4	IO_L110N_YY	AN15	
4	IO_L111P_Y	AJ15	
4	IO_L111N_Y	AK15	
4	IO_L112P_Y	AL15	
4	IO_L112N_Y	AM16	
4	IO_VREF_L113P_Y	AL16	
4	IO_L113N_Y	AJ16	
4	IO_L114P_Y	AK16	
4	IO_VREF_L114N_Y	AN17	2
4	IO_LVDS_DLL_L115P	AM17	
5	GCK1	AJ17	
5	IO	AL25	
5	IO	AL28	
5	IO	AL30	
5	IO	AN28	
5	IO_LVDS_DLL_L115N	AM18	
5	IO_VREF	AL18	2
5	IO_L116P_Y	AK18	
5	IO_VREF_L116N_Y	AJ18	
5	IO_L117P_Y	AN19	
5	IO_L117N_Y	AL19	
5	IO_L118P_Y	AK19	

Table 14: BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin#	See Note
5	IO_L118N_Y	AM20	
5	IO_L119P_YY	AJ19	
5	IO_VREF_L119N_YY	AL20	
5	IO_L120P_YY	AN21	
5	IO_L120N_YY	AL21	
5	IO_L121P_Y	AJ20	
5	IO_L121N_Y	AM22	
5	IO_L122P_YY	AK21	
5	IO_VREF_L122N_YY	AN23	3
5	IO_L123P_YY	AJ21	
5	IO_L123N_YY	AM23	
5	IO_L124P_Y	AK22	
5	IO_L124N_Y	AM24	
5	IO_L125P_YY	AL23	
5	IO_L125N_YY	AJ22	
5	IO_L126P_YY	AK23	
5	IO_VREF_L126N_YY	AL24	
5	IO_L127P_Y	AN26	
5	IO_L127N_Y	AJ23	
5	IO_L128P_Y	AK24	
5	IO_VREF_L128N_Y	AM26	4
5	IO_L129P_Y	AM27	
5	IO_L129N_Y	AJ24	
5	IO_L130P_Y	AL26	
5	IO_VREF_L130N_Y	AK25	1
5	IO_L131P_YY	AN29	
5	IO_VREF_L131N_YY	AJ25	
5	IO_L132P_YY	AK26	
5	IO_L132N_YY	AM29	
5	IO_L133P_Y	AM30	
5	IO_L133N_Y	AJ26	
5	IO_L134P_YY	AK27	
5	IO_VREF_L134N_YY	AL29	
5	IO_L135P_YY	AN31	
5	IO_L135N_YY	AJ27	

Table 15: BG560 Differential Pin Pair Summary
XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
109	4	AJ14	AK14	√	-
110	4	AM14	AN15	√	VREF
111	4	AJ15	AK15	1	-
112	4	AL15	AM16	7	-
113	4	AL16	AJ16	7	VREF
114	4	AK16	AN17	2	VREF
115	5	AM17	AM18	NA	IO_LVDS_DLL
116	5	AK18	AJ18	7	VREF
117	5	AN19	AL19	7	-
118	5	AK19	AM20	9	-
119	5	AJ19	AL20	√	VREF
120	5	AN21	AL21	√	-
121	5	AJ20	AM22	3	-
122	5	AK21	AN23	√	VREF
123	5	AJ21	AM23	√	-
124	5	AK22	AM24	8	-
125	5	AL23	AJ22	√	-
126	5	AK23	AL24	√	VREF
127	5	AN26	AJ23	13	-
128	5	AK24	AM26	7	VREF
129	5	AM27	AJ24	7	-
130	5	AL26	AK25	5	VREF
131	5	AN29	AJ25	√	VREF
132	5	AK26	AM29	√	-
133	5	AM30	AJ26	11	-
134	5	AK27	AL29	√	VREF
135	5	AN31	AJ27	√	-
136	5	AM31	AK28	12	VREF
137	6	AJ30	AH29	√	-
138	6	AH30	AK31	17	VREF
139	6	AJ31	AG29	14	-

Table 15: BG560 Differential Pin Pair Summary
XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
140	6	AG30	AK32	15	VREF
141	6	AF29	AH31	16	-
142	6	AF30	AH32	15	-
143	6	AH33	AE29	√	VREF
144	6	AE30	AG33	17	VREF
145	6	AF32	AD29	14	-
146	6	AD30	AE31	18	VREF
147	6	AC29	AE32	19	-
148	6	AC30	AD31	√	VREF
149	6	AC31	AB29	√	-
150	6	AB30	AC33	17	-
151	6	AA29	AB31	14	-
152	6	AA31	AA30	15	VREF
153	6	Y29	AA32	16	-
154	6	Y30	AA33	15	-
155	6	W29	Y32	√	VREF
156	6	W31	W30	17	-
157	6	V30	W33	14	-
158	6	V31	V29	18	VREF
159	6	U33	V32	19	VREF
160	7	U32	U31	√	-
161	7	T30	T32	19	VREF
162	7	T31	T29	18	VREF
163	7	R31	R33	14	-
164	7	R29	R30	17	-
165	7	P31	P32	√	VREF
166	7	P29	P30	15	-
167	7	N31	M32	16	-
168	7	L33	N30	15	VREF
169	7	L32	M31	14	-
170	7	L31	M30	17	-

Table 16: FG256 Package — XCV50E, XCV100E, XCV200E, XCV300E

Bank	Pin Description	Pin #
NA	GND	K11
NA	GND	K10
NA	GND	K9
NA	GND	K8
NA	GND	K7
NA	GND	K6
NA	GND	J10
NA	GND	J9
NA	GND	J8
NA	GND	J7
NA	GND	H10
NA	GND	H9
NA	GND	H8
NA	GND	H7
NA	GND	G11
NA	GND	G10
NA	GND	G9
NA	GND	G8
NA	GND	G7
NA	GND	G6
NA	GND	F11
NA	GND	F10
NA	GND	F7
NA	GND	F6
NA	GND	B15
NA	GND	B2
NA	GND	A16
NA	GND	A1

Notes:

1. V_{REF} or I/O option only in the XCV100E, 200E, 300E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV200E, 300E; otherwise, I/O option only.

FG256 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A $\checkmark$ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 17: FG256 Differential Pin Pair Summary XCV50E, XCV100E, XCV200E, XCV300E

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	N8	N9	NA	IO_DLL_L52P
1	5	R8	T8	NA	IO_DLL_L52N
2	1	C9	A8	NA	IO_DLL_L8P
3	0	B8	A7	NA	IO_DLL_L8N
IO LVDS					
Total Pairs: 83, Asynchronous Outputs: 35					
0	0	A3	C5	7	VREF
1	0	E6	D5	$\checkmark$	-
2	0	A4	B4	$\checkmark$	VREF
3	0	B5	D6	2	-
4	0	A5	C6	$\checkmark$	VREF
5	0	C7	B6	$\checkmark$	-
6	0	C8	D7	1	-
7	0	A6	B7	1	VREF
8	1	A8	A7	NA	IO_LVDS_DLL
9	1	A9	D9	2	-
10	1	B9	E10	1	VREF
11	1	D10	A10	1	-
12	1	A11	C10	$\checkmark$	-
13	1	E11	B11	$\checkmark$	VREF
14	1	D11	A12	2	-
15	1	C11	A13	$\checkmark$	VREF
16	1	D12	B12	$\checkmark$	-
17	1	C12	A14	7	VREF
18	1	B13	C13	$\checkmark$	CS

Table 18: FG456 — XCV200E and XCV300E

Bank	Pin Description	Pin #
NA	GND	M14
NA	GND	M13
NA	GND	M12
NA	GND	M11
NA	GND	M10
NA	GND	M9
NA	GND	L14
NA	GND	L13
NA	GND	L12
NA	GND	L11
NA	GND	L10
NA	GND	L9
NA	GND	K14
NA	GND	K13
NA	GND	K12
NA	GND	K11
NA	GND	K10
NA	GND	K9
NA	GND	J14
NA	GND	J13
NA	GND	J12
NA	GND	J11
NA	GND	J10
NA	GND	J9
NA	GND	C20
NA	GND	C3
NA	GND	B21
NA	GND	B2
NA	GND	A22
NA	GND	A1

Note 1: NC in the XCV200E device.

FG456 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 19: FG456 Differential Pin Pair Summary
XCV200E, XCV300E

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	W12	U12	NA	IO_DLL_L75P
1	5	Y11	AA11	NA	IO_DLL_L75N
2	1	A11	D11	NA	IO_DLL_L13P
3	0	C11	B11	NA	IO_DLL_L13N
IO LVDS					
Total Pairs: 119, Asynchronous Output Pairs: 69					
0	0	B3	D5	NA	-
1	0	E6	B4	√	VREF
2	0	E7	A4	NA	-
3	0	D6	C6	√	VREF
4	0	B6	A5	1	-
5	0	C7	D7	1	-
6	0	B7	E8	√	VREF
7	0	E9	A7	√	-
8	0	B8	C8	1	-
9	0	A8	D9	1	-
10	0	E10	C9	NA	-
11	0	C10	A9	√	VREF
12	0	B10	F11	2	-
13	1	D11	B11	NA	IO_LVDS_DLL
14	1	D12	C12	2	-
15	1	A13	B12	2	-
16	1	B13	E12	√	VREF
17	1	D13	C13	√	-

Table 21: FG676 Differential Pin Pair Summary
XCV400E, XCV600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
52	2	G24	H22	√	-
53	2	J21	G25	2	-
54	2	G26	J22	1	VREF
55	2	H24	J23	√	-
56	2	J24	K20	√	VREF
57	2	K22	K21	√	D2
58	2	H25	K23	√	-
59	2	L20	J26	2	-
60	2	K25	L22	1	-
61	2	L21	L23	1	-
62	2	M20	L24	1	-
63	2	M23	M22	√	D3
64	2	L26	M21	√	-
65	2	N19	M24	2	-
66	2	M26	N20	1	VREF
67	2	N24	N21	√	-
68	2	N23	N22	√	-
69	3	P21	P23	√	-
70	3	P22	R25	1	VREF
71	3	P19	P20	2	-
72	3	R21	R22	√	-
73	3	R24	R23	√	VREF
74	3	T24	R20	1	-
75	3	T22	U24	1	-
76	3	T23	U25	1	-
77	3	T21	U20	2	-
78	3	U22	V26	√	-
79	3	T20	U23	√	D5
80	3	V24	U21	√	VREF
81	3	V23	W24	√	-
82	3	V22	W26	1	VREF
83	3	Y25	V21	2	-
84	3	V20	AA26	√	-
85	3	Y24	W23	√	VREF

Table 21: FG676 Differential Pin Pair Summary
XCV400E, XCV600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
86	3	AA24	Y23	1	-
87	3	AB26	W21	2	-
88	3	Y22	W22	1	VREF
89	3	AA23	AB24	2	-
90	3	W20	AC24	√	-
91	3	AB23	Y21	√	INIT
92	4	AC22	AD26	√	-
93	4	AD23	AA20	1	-
94	4	Y19	AC21	√	-
95	4	AD22	AB20	√	VREF
96	4	AE22	Y18	NA	-
97	4	AF22	AA19	NA	-
98	4	AD21	AB19	√	VREF
99	4	AC20	AA18	√	-
100	4	AC19	AD20	1	-
101	4	AF20	AB18	1	VREF
102	4	AD19	Y17	NA	-
103	4	AE19	AD18	NA	VREF
104	4	AF19	AA17	√	-
105	4	AC17	AB17	1	-
106	4	Y16	AE17	√	-
107	4	AF17	AA16	√	-
108	4	AD17	AB16	NA	-
109	4	AC16	AD16	√	-
110	4	AC15	Y15	√	VREF
111	4	AD15	AA15	√	-
112	4	W14	AB15	1	-
113	4	AF15	Y14	1	VREF
114	4	AD14	AB14	NA	-
115	5	AC14	AF13	NA	IO_LVDS_DLL
116	5	AA13	AF12	1	VREF
117	5	AC13	W13	1	-
118	5	AA12	AD12	√	-
119	5	AC12	AB12	√	VREF

Table 21: FG676 Differential Pin Pair Summary
XCV400E, XCV600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
120	5	AD11	Y12	√	-
121	5	AB11	AD10	NA	-
122	5	AC11	AE10	√	-
123	5	AC10	AA11	√	-
124	5	Y11	AD9	1	-
125	5	AB10	AF9	√	-
126	5	AD8	AA10	√	VREF
127	5	AE8	Y10	√	-
128	5	AC9	AF8	1	VREF
129	5	AF7	AB9	1	-
130	5	AA9	AF6	√	-
131	5	AC8	AC7	√	VREF
132	5	AD6	Y9	√	-
133	5	AE5	AA8	√	-
134	5	AC6	AB8	√	VREF
135	5	AD5	AA7	√	-
136	5	AF4	AC5	2	-
137	6	AC3	AA5	√	-
138	6	AB4	AC2	√	-
139	6	AA4	W6	2	-
140	6	Y5	AB3	1	VREF
141	6	V7	AB2	1	-
142	6	Y4	AB1	√	-
143	6	W5	V5	√	VREF
144	6	V6	AA1	√	-
145	6	Y3	W4	2	-
146	6	U7	Y1	1	VREF
147	6	V4	W1	√	-
148	6	U6	W2	√	VREF
149	6	T5	V3	√	-
150	6	U4	U5	√	-
151	6	U3	T7	2	-
152	6	T6	U2	1	-
153	6	T4	U1	1	-

Table 21: FG676 Differential Pin Pair Summary
XCV400E, XCV600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
154	6	T3	R7	1	-
155	6	R6	R4	√	VREF
156	6	R5	R3	√	-
157	6	P7	P8	2	-
158	6	P6	R1	1	VREF
159	6	P4	P5	√	-
160	7	N8	N5	√	-
161	7	N3	N6	√	-
162	7	M2	N4	1	VREF
163	7	M7	N7	2	-
164	7	M3	M6	√	-
165	7	M5	M4	√	VREF
166	7	L7	L3	1	-
167	7	K2	L6	1	-
168	7	K1	L4	1	-
169	7	L5	K3	2	-
170	7	J3	K5	√	-
171	7	J4	K4	√	-
172	7	K6	H3	√	VREF
173	7	G3	K7	√	-
174	7	H1	J5	1	VREF
175	7	J6	G2	2	-
176	7	F1	J7	√	-
177	7	G4	H4	√	VREF
178	7	H5	F3	1	-
179	7	H6	E2	2	-
180	7	F4	G5	1	VREF
181	7	G6	H7	2	-
182	7	E4	E3	√	-

Notes:

1. AO in the XCV600E.
2. AO in the XCV400E.

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
6	IO_VREF_L245N_Y	AB40 ¹
6	IO_L245P_Y	AC39
7	IO	F38
7	IO	H40
7	IO	H41
7	IO	J42
7	IO	K39
7	IO	L42
7	IO	N40
7	IO	T40
7	IO	U40
7	IO	V38
7	IO	W42
7	IO	Y42
7	IO	AA42
7	IO_L246N_YY	AA41
7	IO_L246P_YY	AB39
7	IO_L247N_Y	Y41
7	IO_VREF_L247P_Y	AA39 ¹
7	IO_L248N_YY	Y40
7	IO_L248P_YY	Y39
7	IO_L249N_YY	Y38
7	IO_VREF_L249P_YY	W41
7	IO_L250N_Y	W40
7	IO_L250P_Y	W39
7	IO_L251N_Y	W38
7	IO_L251P_Y	V41
7	IO_L252N_YY	V39
7	IO_L252P_YY	V40
7	IO_L253N_YY	V42
7	IO_VREF_L253P_YY	U39
7	IO_L254N_Y	U41
7	IO_L254P_Y	U38
7	IO_L255N_Y	U42
7	IO_L255P_Y	T39
7	IO_L256N_YY	T41

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
7	IO_L256P_YY	T38
7	IO_L257N_Y	R39
7	IO_VREF_L257P_Y	T42
7	IO_L258N_Y	R42
7	IO_L258P_Y	R38
7	IO_L259N	R40
7	IO_L259P	P39
7	IO_L260N_Y	R41
7	IO_L260P_Y	P38
7	IO_L261N_Y	P42
7	IO_L261P_Y	N39
7	IO_L262N_Y	P40
7	IO_L262P_Y	M39
7	IO_L263N_YY	P41
7	IO_L263P_YY	M38
7	IO_L264N_YY	N42
7	IO_VREF_L264P_YY	L39
7	IO_L265N_Y	L38
7	IO_L265P_Y	N41
7	IO_L266N_YY	K40
7	IO_L266P_YY	M42
7	IO_L267N_YY	M40
7	IO_VREF_L267P_YY	K38
7	IO_L268N_Y	M41
7	IO_L268P_Y	J40
7	IO_L269N_Y	J39
7	IO_VREF_L269P_Y	L40
7	IO_L270N_YY	J38
7	IO_L270P_YY	L41
7	IO_L271N_YY	K42
7	IO_VREF_L271P_YY	H39
7	IO_L272N_Y	K41
7	IO_L272P_Y	H38
7	IO_L273N_Y	J41
7	IO_L273P_Y	G40
7	IO_L274N_YY	H42
7	IO_L274P_YY	G39

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
NA	VCCO_1	F15
NA	VCCO_1	F19
NA	VCCO_1	F20
NA	VCCO_1	F7
NA	VCCO_1	F8
NA	VCCO_2	G6
NA	VCCO_2	H6
NA	VCCO_2	L6
NA	VCCO_2	M6
NA	VCCO_2	P6
NA	VCCO_2	R6
NA	VCCO_2	W6
NA	VCCO_2	Y6
NA	VCCO_3	AC6
NA	VCCO_3	AD6
NA	VCCO_3	AH6
NA	VCCO_3	AJ6
NA	VCCO_3	AL6
NA	VCCO_3	AM6
NA	VCCO_3	AR6
NA	VCCO_3	AT6
NA	VCCO_4	AU11
NA	VCCO_4	AU12
NA	VCCO_4	AU14
NA	VCCO_4	AU15
NA	VCCO_4	AU19
NA	VCCO_4	AU20
NA	VCCO_4	AU7
NA	VCCO_4	AU8
NA	VCCO_5	AU23
NA	VCCO_5	AU24
NA	VCCO_5	AU28
NA	VCCO_5	AU29
NA	VCCO_5	AU31
NA	VCCO_5	AU32
NA	VCCO_5	AU35
NA	VCCO_5	AU36

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
NA	VCCO_6	AC37
NA	VCCO_6	AD37
NA	VCCO_6	AH37
NA	VCCO_6	AJ37
NA	VCCO_6	AL37
NA	VCCO_6	AM37
NA	VCCO_6	AR37
NA	VCCO_6	AT37
NA	VCCO_7	G37
NA	VCCO_7	H37
NA	VCCO_7	L37
NA	VCCO_7	M37
NA	VCCO_7	P37
NA	VCCO_7	R37
NA	VCCO_7	W37
NA	VCCO_7	Y37
NA	GND	N6
NA	GND	N5
NA	GND	N38
NA	GND	N37
NA	GND	F6
NA	GND	F37
NA	GND	F30
NA	GND	F22
NA	GND	F21
NA	GND	F13
NA	GND	E5
NA	GND	E38
NA	GND	E30
NA	GND	E22
NA	GND	E21
NA	GND	E13
NA	GND	D42
NA	GND	D4
NA	GND	D39
NA	GND	D1

Table 26: FG900 — XCV600E, XCV1000E, XCV1600E

Bank	Pin Description	Pin #
2	IO_L99P_YY	N26
2	IO_L99N_YY	P28
2	IO_L100P	P29
2	IO_L100N	N24
2	IO_L101P_YY	P22
2	IO_L101N_YY	R26
2	IO_VREF_L102P_YY	P25
2	IO_L102N_YY	R29
2	IO_L103P_YY	R21 ⁴
2	IO_L103N_YY	R28 ³
2	IO_VREF_L104P_YY	R25 ²
2	IO_L104N_YY	T30
2	IO_L105P_YY	P24 ⁴
2	IO_L105N_YY	R27 ³
2	IO_L106P	R24
3	IO	T22 ⁴
3	IO	T24 ⁴
3	IO	T26 ⁴
3	IO	T29 ⁴
3	IO	U26 ⁵
3	IO	V23 ⁴
3	IO	V25 ⁴
3	IO	V30 ⁵
3	IO	Y21 ⁴
3	IO	AA26 ⁴
3	IO	AA23 ⁴
3	IO	AB27 ⁴
3	IO	AB29 ⁴
3	IO	AC28 ⁵
3	IO	AD26 ⁴
3	IO	AD29 ⁵
3	IO	AE27 ⁵
3	IO_L106N	U29
3	IO_L107P_YY	R22
3	IO_VREF_L107N_YY	T27 ²
3	IO_L108P_YY	R23

Table 26: FG900 — XCV600E, XCV1000E, XCV1600E

Bank	Pin Description	Pin #
3	IO_L108N_YY	T28
3	IO_L109P_YY	T21
3	IO_VREF_L109N_YY	T25
3	IO_L110P_YY	U28
3	IO_L110N_YY	U30
3	IO_L111P	T23
3	IO_L111N	U27
3	IO_L112P_YY	U25
3	IO_L112N_YY	V27
3	IO_D4_L113P_YY	U24
3	IO_VREF_L113N_YY	V29
3	IO_L114P	W30
3	IO_L114N	U22
3	IO_L115P_YY	U21
3	IO_L115N_YY	W29
3	IO_L116P_YY	V26
3	IO_L116N_YY	W27
3	IO_L117P	W26
3	IO_VREF_L117N	Y29 ¹
3	IO_L118P_YY	W25
3	IO_L118N_YY	Y30
3	IO_L119P_Y	V24 ⁴
3	IO_L119N_Y	Y28 ⁴
3	IO_L120P_YY	AA30
3	IO_L120N_YY	W24
3	IO_L121P	AA29
3	IO_L121N	V20
3	IO_L122P	Y27 ⁴
3	IO_L122N	W23 ⁴
3	IO_L123P_YY	Y26
3	IO_D5_L123N_YY	AB30
3	IO_D6_L124P_YY	V21
3	IO_VREF_L124N_YY	AA28
3	IO_L125P_YY	Y25
3	IO_L125N_YY	AA27
3	IO_L126P_YY	W22
3	IO_L126N_YY	Y23

Table 27: FG900 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
120	3	AA30	W24	4	-
121	3	AA29	V20	1	-
122	3	Y27	W23	NA	-
123	3	Y26	AB30	√	D5
124	3	V21	AA28	√	VREF
125	3	Y25	AA27	4	-
126	3	W22	Y23	4	-
127	3	Y24	AB28	4	VREF
128	3	AC30	AA25	√	-
129	3	W21	AA24	2	-
130	3	AB26	AD30	√	-
131	3	Y22	AC27	√	VREF
132	3	AD28	AB25	2	-
133	3	AC26	AE30	4	-
134	3	AD27	AF30	√	-
135	3	AF29	AB24	1	VREF
136	3	AB23	AE28	4	-
137	3	AG30	AC25	3	-
138	3	AE26	AG29	4	VREF
139	3	AH30	AC24	1	-
140	3	AF28	AD25	NA	-
141	3	AH29	AA22	√	INIT
142	4	AF27	AK28	√	-
143	4	AG26	AH27	4	-
144	4	AD23	AJ27	2	-
145	4	AB21	AF25	2	VREF
146	4	AC22	AH26	2	-
147	4	AA21	AG25	√	-
148	4	AJ26	AD22	√	VREF
149	4	AA20	AH25	1	-
150	4	AC21	AF24	1	-
151	4	AG24	AK26	√	-
152	4	AJ24	AF23	√	VREF
153	4	AE23	AB20	2	-

Table 27: FG900 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
154	4	AC20	AG23	2	-
155	4	AF22	AE22	√	-
156	4	AJ22	AG22	√	VREF
157	4	AK24	AD20	NA	-
158	4	AA19	AF21	4	-
159	4	AH22	AA18	NA	VREF
160	4	AG21	AK23	NA	-
161	4	AH21	AD19	4	-
162	4	AE20	AJ21	2	-
163	4	AG20	AF20	2	-
164	4	AC18	AF19	2	-
165	4	AJ20	AE19	√	-
166	4	AK22	AH20	√	VREF
167	4	AG19	AB17	1	-
168	4	AJ19	AD17	1	-
169	4	AA16	AA17	√	-
170	4	AK21	AB16	√	VREF
171	4	AG18	AK20	2	-
172	4	AK19	AD16	2	-
173	4	AE16	AE17	√	-
174	4	AG17	AJ17	√	VREF
175	4	AD15	AH17	NA	-
176	4	AG16	AK17	4	VREF
177	5	AF16	AH16	NA	IO_LVDS_DLL
178	5	AC15	AG15	4	VREF
179	5	AB15	AF15	√	-
180	5	AA15	AF14	√	VREF
181	5	AH15	AK15	√	-
182	5	AB14	AF13	2	-
183	5	AH14	AJ14	2	-
184	5	AE14	AG13	√	VREF
185	5	AK13	AD13	√	-
186	5	AE13	AF12	1	-
187	5	AC13	AA13	1	-

Table 27: FG900 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
188	5	AA12	AJ12	√	VREF
189	5	AB12	AE11	√	-
190	5	AK12	Y13	2	-
191	5	AG11	AF11	2	-
192	5	AH11	AJ11	2	-
193	5	AE12	AG10	4	-
194	5	AD12	AK11	√	-
195	5	AJ10	AC12	√	VREF
196	5	AK10	AD11	4	-
197	5	AJ9	AE9	4	-
198	5	AH10	AF9	√	VREF
199	5	AH9	AK9	√	-
200	5	AF8	AB11	2	-
201	5	AC11	AG8	2	-
202	5	AK8	AF7	√	VREF
203	5	AG7	AK7	√	-
204	5	AJ7	AD10	1	-
205	5	AH6	AC10	1	-
206	5	AD9	AG6	√	VREF
207	5	AB10	AJ5	√	-
208	5	AD8	AK5	2	-
209	5	AC9	AJ4	2	VREF
210	5	AG5	AK4	2	-
211	5	AH5	AG3	4	-
212	6	AC6	AF3	√	-
213	6	AG2	AH2	NA	-
214	6	AE4	AB9	1	-
215	6	AH1	AE3	4	VREF
216	6	AD6	AB8	3	-
217	6	AA10	AG1	4	-
218	6	AD4	AA9	1	VREF
219	6	AD2	AD5	√	-
220	6	AF2	AD3	4	-
221	6	AA7	AA8	1	-

Table 27: FG900 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
222	6	Y9	AF1	√	VREF
223	6	AC4	AB6	√	-
224	6	W8	AE1	2	-
225	6	AB4	Y8	4	-
226	6	W9	AB3	4	VREF
227	6	W10	AA5	4	-
228	6	V10	AB1	4	-
229	6	AC1	Y7	4	VREF
230	6	AA3	V11	NA	-
231	6	U10	AA2	4	-
232	6	AA6	W7	1	-
233	6	Y4	Y6	4	-
234	6	V7	AA1	3	-
235	6	Y2	Y3	4	-
236	6	W5	Y5	1	VREF
237	6	W6	W4	√	-
238	6	W2	V6	4	-
239	6	V4	U9	1	-
240	6	T8	AB2	√	VREF
241	6	W1	U5	√	-
242	6	T9	Y1	2	-
243	6	U3	T7	4	-
244	6	V2	T5	4	VREF
245	6	T6	R9	4	-
246	6	U2	T4	4	VREF
247	7	R10	T1	NA	-
248	7	R6	R5	4	-
249	7	R4	R8	4	VREF
250	7	R3	R7	4	-
251	7	P6	P10	4	VREF
252	7	P2	P5	4	-
253	7	P4	P7	2	-
254	7	R2	N4	√	-
255	7	P1	N7	√	VREF