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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3456
Number of Logic Elements/Cells	15552
Total RAM Bits	294912
Number of I/O	404
Number of Gates	985882
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	560-LBGA Exposed Pad, Metal
Supplier Device Package	560-MBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv600e-6bg560c

Configuration through the TAP uses the CFG_IN instruction. This instruction allows data input on TDI to be converted into data packets for the internal configuration bus.

The following steps are required to configure the FPGA through the Boundary Scan port (when using TCK as a start-up clock).

1. Load the CFG_IN instruction into the Boundary Scan instruction register (IR).
2. Enter the Shift-DR (SDR) state.
3. Shift a configuration bitstream into TDI.
4. Return to Run-Test-Idle (RTI).
5. Load the JSTART instruction into IR.
6. Enter the SDR state.
7. Clock TCK through the startup sequence.
8. Return to RTI.

Configuration and readback via the TAP is always available. The Boundary Scan mode is selected by a <101> or <001> on the mode pins (M2, M1, M0). For details on TAP characteristics, refer to XAPP139.

Configuration Sequence

The configuration of Virtex-E devices is a three-phase process. First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user, as described below. The configuration process can also be initiated by asserting $\overline{\text{PROGRAM}}$. The end of the memory-clearing phase is signalled by $\overline{\text{INIT}}$ going High, and the completion of the entire process is signalled by DONE going High.

The power-up timing of configuration signals is shown in Figure 20.

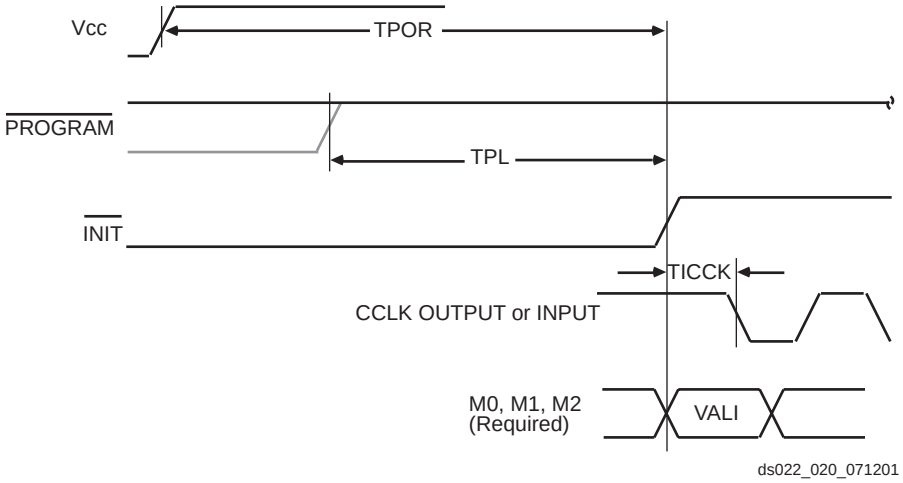

Figure 20: Power-Up Timing Configuration Signals

The corresponding timing characteristics are listed in Table 12.

Table 12: Power-up Timing Characteristics

Description	Symbol	Value	Units
Power-on Reset[1]	T_{POR}	2.0	ms, max
Program Latency	T_{PL}	100.0	µs, max
CCLK (output) Delay	T_{ICCK}	0.5	µs, min
		4.0	µs, max
Program Pulse Width	$T_{PROGRAM}$	300	ns, min

Notes:
1. T_{POR} delay is the initialization time required after V_{CCINT} and V_{CCO} in Bank 2 reach the recommended operating voltage.

Delaying Configuration

$\overline{\text{INIT}}$ can be held Low using an open-drain driver. An open-drain is required since $\overline{\text{INIT}}$ is a bidirectional open-drain pin that is held Low by the FPGA while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

Start-Up Sequence

The default Start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary.

One CCLK cycle later, the Global Set/Reset (GSR) and Global Write Enable (GWE) signals are released. This permits

Input termination techniques include the following.

- None
- Parallel (Shunt)

These termination techniques can be applied in any combination. A generic example of each combination of termination methods appears in Figure 43.

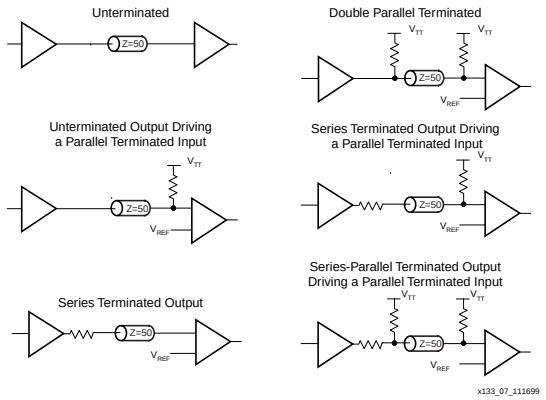

Figure 43: Overview of Standard Input and Output Termination Methods

Simultaneous Switching Guidelines

Ground bounce can occur with high-speed digital ICs when multiple outputs change states simultaneously, causing undesired transient behavior on an output, or in the internal logic. This problem is also referred to as the Simultaneous Switching Output (SSO) problem.

Ground bounce is primarily due to current changes in the combined inductance of ground pins, bond wires, and ground metallization. The IC internal ground level deviates from the external system ground level for a short duration (a few nanoseconds) after multiple outputs change state simultaneously.

Ground bounce affects stable Low outputs and all inputs because they interpret the incoming signal by comparing it to the internal ground. If the ground bounce amplitude exceeds the actual instantaneous noise margin, then a non-changing input can be interpreted as a short pulse with a polarity opposite to the ground bounce.

Table 21 provides guidelines for the maximum number of simultaneously switching outputs allowed per output power/ground pair to avoid the effects of ground bounce. See Table 22 for the number of effective output power/ground pairs for each Virtex-E device and package combination.

Table 21: Guidelines for Max Number of Simultaneously Switching Outputs per Power/Ground Pair

Standard	Package		
	BGA, CS, FGA	HQ	PQ, TQ
LVTTL Slow Slew Rate, 2 mA drive	68	49	36
LVTTL Slow Slew Rate, 4 mA drive	41	31	20
LVTTL Slow Slew Rate, 6 mA drive	29	22	15
LVTTL Slow Slew Rate, 8 mA drive	22	17	12
LVTTL Slow Slew Rate, 12 mA drive	17	12	9
LVTTL Slow Slew Rate, 16 mA drive	14	10	7
LVTTL Slow Slew Rate, 24 mA drive	9	7	5
LVTTL Fast Slew Rate, 2 mA drive	40	29	21
LVTTL Fast Slew Rate, 4 mA drive	24	18	12
LVTTL Fast Slew Rate, 6 mA drive	17	13	9
LVTTL Fast Slew Rate, 8 mA drive	13	10	7
LVTTL Fast Slew Rate, 12 mA drive	10	7	5
LVTTL Fast Slew Rate, 16 mA drive	8	6	4
LVTTL Fast Slew Rate, 24 mA drive	5	4	3
LVCMOS	10	7	5
PCI	8	6	4
GTL	4	4	4
GTL+	4	4	4

Table 42: Input Library Macros

Name	Inputs	Outputs
IBUFDS_FD_LVDS	I, IB, C	Q
IBUFDS_FDE_LVDS	I, IB, CE, C	Q
IBUFDS_FDC_LVDS	I, IB, C, CLR	Q
IBUFDS_FDCE_LVDS	I, IB, CE, C, CLR	Q
IBUFDS_FDP_LVDS	I, IB, C, PRE	Q
IBUFDS_FDPE_LVDS	I, IB, CE, C, PRE	Q
IBUFDS_FDR_LVDS	I, IB, C, R	Q
IBUFDS_FDRE_LVDS	I, IB, CE, C, R	Q
IBUFDS_FDS_LVDS	I, IB, C, S	Q
IBUFDS_FDSE_LVDS	I, IB, CE, C, S	Q
IBUFDS_LD_LVDS	I, IB, G	Q
IBUFDS_LDE_LVDS	I, IB, GE, G	Q
IBUFDS_LDC_LVDS	I, IB, G, CLR	Q
IBUFDS_LDCE_LVDS	I, IB, GE, G, CLR	Q
IBUFDS_LDP_LVDS	I, IB, G, PRE	Q
IBUFDS_LDPE_LVDS	I, IB, GE, G, PRE	Q

Creating LVDS Output Buffers

LVDS output buffers can be placed in a wide number of IOB locations. The exact locations are dependent on the package used. The Virtex-E package information lists the possible locations as IO_L#P for the P-side and IO_L#N for the N-side, where # is the pair number.

HDL Instantiation

Both output buffers are required to be instantiated in the design and placed on the correct IO_L#P and IO_L#N locations. The IOB must have the same net source the following pins, clock (C), set/reset (SR), output (O), output clock enable (OCE). In addition, the output (O) pins must be inverted with respect to each other, and if output registers are used, the INIT states must be opposite values (one HIGH and one LOW). Failure to follow these rules leads to DRC errors in software.

VHDL Instantiation

```
data0_p  : OBUF_LVDS port map
(I=>data_int(0),   O=>data_p(0));

data0_inv: INV       port map
(I=>data_int(0),   O=>data_n_int(0));

data0_n  : OBUF_LVDS port map
(I=>data_n_int(0), O=>data_n(0));
```

Verilog Instantiation

```
OBUF_LVDS data0_p   (.I(data_int[0]),
.O(data_p[0]));

INV       data0_inv (.I(data_int[0],
.O(data_n_int[0]);

OBUF_LVDS data0_n   (.I(data_n_int[0]),
.O(data_n[0]));
```

Location Constraints

All LVDS buffers must be explicitly placed on a device. For the output buffers this can be done with the following constraint in the .ucf or .ncf file.

```
NET data_p<0> LOC = D28; # IO_L0P

NET data_n<0> LOC = B29; # IO_L0N
```

Synchronous vs. Asynchronous Outputs

If the outputs are synchronous (registered in the IOB) then any IO_L#P|N pair can be used. If the outputs are asynchronous (no output register), then they must use one of the pairs that are part of the same IOB group at the end of a ROW or COLUMN in the device.

The LVDS pairs that can be used as asynchronous outputs are listed in the Virtex-E pinout tables. Some pairs are marked as asynchronous-capable for all devices in that package, and others are marked as available only for that device in the package. If the device size might change at some point in the product lifetime, then only the common pairs for all packages should be used.

Adding an Output Register

All LVDS buffers can have an output register in the IOB. The output registers must be in both the P-side and N-side IOBs. All the normal IOB register options are available (FD, FDE, FDC, FDCE, FDP, FDPE, FDR, FDRE, FDS, FDSE, LD, LDE, LDC, LDCE, LDP, LDPE). The register elements can be inferred or explicitly instantiated in the HDL code.

Special care must be taken to insure that the D pins of the registers are inverted and that the INIT states of the registers are opposite. The clock pin (C), clock enable (CE) and set/reset (CLR/PRE or S/R) pins must connect to the same source. Failure to do this leads to a DRC error in the software.

The register elements can be packed in the IOB using the IOB property to TRUE on the register or by using the “map -pr [i|o|b]” where “i” is inputs only, “o” is outputs only and “b” is both inputs and outputs.

To improve design coding times VHDL and Verilog synthesis macro libraries have been developed to explicitly create these structures. The output library macros are listed in Table 43. The O and OB inputs to the macros are the external net connections.

Virtex-E Electrical Characteristics

Definition of Terms

Electrical and switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance : These speed files are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary : These speed files are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production : These speed files are released once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. Contact the factory for design considerations requiring more detailed information.

Table 1 correlates the current status of each Virtex-E device with a corresponding speed file designation.

Table 1: Virtex-E Device Speed Grade Designations

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XCV50E			–8, –7, –6
XCV100E			–8, –7, –6
XCV200E			–8, –7, –6
XCV300E			–8, –7, –6
XCV400E			–8, –7, –6
XCV600E			–8, –7, –6
XCV1000E			–8, –7, –6
XCV1600E			–8, –7, –6
XCV2000E			–8, –7, –6
XCV2600E			–8, –7, –6
XCV3200E			–8, –7, –6

All specifications are subject to change without notice.

Table 15: BG560 Differential Pin Pair Summary
XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
47	2	F4	C1	14	-
48	2	G5	E3	15	VREF
49	2	D2	G4	16	-
50	2	H5	E2	15	-
51	2	H4	G3	—	VREF
52	2	J5	F1	17	VREF
53	2	J4	H3	14	-
54	2	K5	H2	18	VREF
55	2	J3	K4	19	-
56	2	L5	K3	—	D1
57	2	L4	K2	—	D2
58	2	M5	L3	17	-
59	2	L1	M4	14	-
60	2	N5	M2	15	VREF
61	2	N4	N3	16	-
62	2	N2	P5	15	-
63	2	P4	P3	—	D3
64	2	P2	R5	17	-
65	2	R4	R3	14	-
66	2	R1	T4	18	VREF
67	2	T5	T3	19	VREF
68	2	T2	U3	—	-
69	3	U1	U2	19	VREF
70	3	V2	V4	18	VREF
71	3	V5	V3	14	-
72	3	W1	W3	17	-
73	3	W4	W5	—	VREF
74	3	Y3	Y4	15	-
75	3	AA1	Y5	16	-
76	3	AA3	AA4	15	VREF
77	3	AB3	AA5	14	-

Table 15: BG560 Differential Pin Pair Summary
XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
78	3	AC1	AB4	17	-
79	3	AC3	AB5	—	D5
80	3	AC4	AD3	—	VREF
81	3	AE1	AC5	4	-
82	3	AD4	AF1	18	VREF
83	3	AF2	AD5	14	-
84	3	AG2	AE4	20	VREF
85	3	AH1	AE5	—	VREF
86	3	AF4	AJ1	15	-
87	3	AJ2	AF5	14	-
88	3	AG4	AK2	15	VREF
89	3	AJ3	AG5	14	-
90	3	AL1	AH4	14	VREF
91	3	AJ4	AH5	—	INIT
92	4	AL4	AJ6	—	-
93	4	AK5	AN3	8	VREF
94	4	AL5	AJ7	—	-
95	4	AM4	AM5	—	VREF
96	4	AK7	AL6	3	-
97	4	AM6	AN6	—	-
98	4	AL7	AJ9	—	VREF
99	4	AN7	AL8	9	VREF
100	4	AM8	AJ10	7	-
101	4	AL9	AM9	7	VREF
102	4	AK10	AN9	2	-
103	4	AL10	AM10	—	VREF
104	4	AL11	AJ12	—	-
105	4	AN11	AK12	8	-
106	4	AL12	AM12	—	-
107	4	AK13	AL13	—	VREF
108	4	AM13	AN13	3	-

Table 15: BG560 Differential Pin Pair Summary
XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
109	4	AJ14	AK14	—	-
110	4	AM14	AN15	—	VREF
111	4	AJ15	AK15	1	-
112	4	AL15	AM16	7	-
113	4	AL16	AJ16	7	VREF
114	4	AK16	AN17	2	VREF
115	5	AM17	AM18	NA	IO_LVDS_DLL
116	5	AK18	AJ18	7	VREF
117	5	AN19	AL19	7	-
118	5	AK19	AM20	9	-
119	5	AJ19	AL20	—	VREF
120	5	AN21	AL21	—	-
121	5	AJ20	AM22	3	-
122	5	AK21	AN23	—	VREF
123	5	AJ21	AM23	—	-
124	5	AK22	AM24	8	-
125	5	AL23	AJ22	—	-
126	5	AK23	AL24	—	VREF
127	5	AN26	AJ23	13	-
128	5	AK24	AM26	7	VREF
129	5	AM27	AJ24		-
130	5	AL26	AK25	5	VREF
131	5	AN29	AJ25	—	VREF
132	5	AK26	AM29	—	-
133	5	AM30	AJ26	11	-
134	5	AK27	AL29	—	VREF
135	5	AN31	AJ27	—	-
136	5	AM31	AK28	12	VREF
137	6	AJ30	AH29	—	-
138	6	AH30	AK31	17	VREF
139	6	AJ31	AG29	14	-

Table 15: BG560 Differential Pin Pair Summary
XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
140	6	AG30	AK32	15	VREF
141	6	AF29	AH31	16	-
142	6	AF30	AH32	15	-
143	6	AH33	AE29	—	VREF
144	6	AE30	AG33	17	VREF
145	6	AF32	AD29	14	-
146	6	AD30	AE31	18	VREF
147	6	AC29	AE32	19	-
148	6	AC30	AD31	—	VREF
149	6	AC31	AB29	—	-
150	6	AB30	AC33	17	-
151	6	AA29	AB31	14	-
152	6	AA31	AA30	15	VREF
153	6	Y29	AA32	16	-
154	6	Y30	AA33	15	-
155	6	W29	Y32	—	VREF
156	6	W31	W30	17	-
157	6	V30	W33	14	-
158	6	V31	V29	18	VREF
159	6	U33	V32	19	VREF
160	7	U32	U31	—	-
161	7	T30	T32	19	VREF
162	7	T31	T29	18	VREF
163	7	R31	R33	14	-
164	7	R29	R30	17	-
165	7	P31	P32	—	VREF
166	7	P29	P30	15	-
167	7	N31	M32	16	-
168	7	L33	N30	15	VREF
169	7	L32	M31	14	-
170	7	L31	M30	17	-

Table 16: FG256 Package — XCV50E, XCV100E, XCV200E, XCV300E

Bank	Pin Description	Pin #
7	IO_L74N_Y	G4
7	IO_VREF_L74P_Y	H3
7	IO_L75N_YY	G2
7	IO_L75P_YY	F5
7	IO_L76N	F4
7	IO_L76P	F1
7	IO_L77N_YY	G3
7	IO_L77P_YY	F2
7	IO_L78N_Y	E1
7	IO_VREF_L78P_Y	D1[1]
7	IO_L79N	E4
7	IO_L79P	E2
7	IO_L80N_Y	F3
7	IO_VREF_L80P_Y	C1
7	IO_L81N_YY	D2
7	IO_L81P_YY	E3
7	IO_VREF_L82N	B1[2]
7	IO_L82P	A2
2	CCLK	D15
3	DONE	R14
NA	DXN	R4
NA	DXP	P4
NA	M0	N3
NA	M1	P2
NA	M2	R3
NA	PROGRAM	P15
NA	TCK	C4
NA	TDI	A15
2	TDO	B14
NA	TMS	D3
NA	VCCINT	C3
NA	VCCINT	C14
NA	VCCINT	D4

Table 16: FG256 Package — XCV50E, XCV100E, XCV200E, XCV300E

Bank	Pin Description	Pin #
NA	VCCINT	D13
NA	VCCINT	E5
NA	VCCINT	E12
NA	VCCINT	M5
NA	VCCINT	M12
NA	VCCINT	N4
NA	VCCINT	N13
NA	VCCINT	P3
NA	VCCINT	P14
0	VCCO	F8
0	VCCO	E8
1	VCCO	F9
1	VCCO	E9
2	VCCO	H12
2	VCCO	H11
3	VCCO	J12
3	VCCO	J11
4	VCCO	M9
4	VCCO	L9
5	VCCO	M8
5	VCCO	L8
6	VCCO	J6
6	VCCO	J5
7	VCCO	H6
7	VCCO	H5
NA	GND	T16
NA	GND	T1
NA	GND	R15
NA	GND	R2
NA	GND	L11
NA	GND	L10
NA	GND	L7
NA	GND	L6

FG456 Fine-Pitch Ball Grid Array Packages

XCV200E and XCV300E devices in FG456 fine-pitch Ball Grid Array packages have footprint compatibility. Pins labeled I0_VREF can be used as either in both devices provided in this package. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 18, see Table 19 for Differential Pair information.

Table 18: FG456 — XCV200E and XCV300E

Bank	Pin Description	Pin #
0	GCK3	C11
0	IO	A2[1]
0	IO	A3
0	IO	A6[1]
0	IO	A10
0	IO	B5
0	IO	B9
0	IO	C5
0	IO	D8
0	IO	D10
0	IO	E11[1]
0	IO_L0N	D5
0	IO_L0P	B3
0	IO_VREF_L1N_YY	B4
0	IO_L1P_YY	E6
0	IO_L2N	A4
0	IO_L2P	E7
0	IO_VREF_L3N_YY	C6
0	IO_L3P_YY	D6
0	IO_L4N_Y	A5
0	IO_L4P_Y	B6
0	IO_L5N_Y	D7
0	IO_L5P_Y	C7
0	IO_VREF_L6N_YY	E8
0	IO_L6P_YY	B7
0	IO_L7N_YY	A7
0	IO_L7P_YY	E9
0	IO_L8N_Y	C8
0	IO_L8P_Y	B8
0	IO_L9N_Y	D9
0	IO_L9P_Y	A8
0	IO_L10N	C9
0	IO_L10P	E10
0	IO_VREF_L11N_YY	A9
0	IO_L11P_YY	C10
0	IO_L12N_Y	F11
0	IO_L12P_Y	B10
0	IO_LVDS_DLL_L13N	B11
1	GCK2	A11
1	IO	A12[1]
1	IO	A14
1	IO	B16[1]
1	IO	B19
1	IO	E13
1	IO	E15
1	IO	E16
1	IO	E17[1]
1	IO_LVDS_DLL_L13P	D11
1	IO_L14N_Y	C12
1	IO_L14P_Y	D12
1	IO_L15N_Y	B12
1	IO_L15P_Y	A13
1	IO_L16N_YY	E12
1	IO_VREF_L16P_YY	B13
1	IO_L17N_YY	C13
1	IO_L17P_YY	D13
1	IO_L18N_Y	B14
1	IO_L18P_Y	C14
1	IO_L19N_Y	F12
1	IO_L19P_Y	A15
1	IO_L20N_YY	B15
1	IO_L20P_YY	C15
1	IO_L21N_YY	A16
1	IO_VREF_L21P_YY	E14
1	IO_L22N_Y	D14
1	IO_L22P_Y	C16
1	IO_L23N_Y	D15

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
3	IO	Y26
3	IO	AB25
3	IO	AC25[1]
3	IO	AC26
3	IO_L69P_YY	P21
3	IO_L69N_YY	P23
3	IO_L70P_Y	P22
3	IO_VREF_L70N_Y	R25
3	IO_L71P_Y	P19
3	IO_L71N_Y	P20
3	IO_L72P_YY	R21
3	IO_L72N_YY	R22
3	IO_D4_L73P_YY	R24
3	IO_VREF_L73N_YY	R23
3	IO_L74P_Y	T24
3	IO_L74N_Y	R20
3	IO_L75P_Y	T22
3	IO_L75N_Y	U24
3	IO_L76P_Y	T23
3	IO_L76N_Y	U25
3	IO_L77P_Y	T21
3	IO_L77N_Y	U20
3	IO_L78P_YY	U22
3	IO_L78N_YY	V26
3	IO_L79P_YY	T20
3	IO_D5_L79N_YY	U23
3	IO_D6_L80P_YY	V24
3	IO_VREF_L80N_YY	U21
3	IO_L81P_YY	V23
3	IO_L81N_YY	W24
3	IO_L82P_Y	V22
3	IO_VREF_L82N_Y	W26[2]
3	IO_L83P_Y	Y25
3	IO_L83N_Y	V21
3	IO_L84P_YY	V20
3	IO_L84N_YY	AA26
3	IO_L85P_YY	Y24

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
3	IO_VREF_L85N_YY	W23
3	IO_L86P_Y	AA24
3	IO_L86N_Y	Y23
3	IO_L87P_Y	AB26
3	IO_L87N_Y	W21
3	IO_L88P_Y	Y22
3	IO_VREF_L88N_Y	W22
3	IO_L89P_Y	AA23
3	IO_L89N_Y	AB24
3	IO_L90P_YY	W20
3	IO_L90N_YY	AC24
3	IO_D7_L91P_YY	AB23
3	IO_INIT_L91N_YY	Y21
4	GCK0	AA14
4	IO	AC18
4	IO	AE15[1]
4	IO	AE20
4	IO	AE23
4	IO	AF14[1]
4	IO	AF16[1]
4	IO	AF18[1]
4	IO	AF21
4	IO	AF23[1]
4	IO_L92P_YY	AC22
4	IO_L92N_YY	AD26
4	IO_L93P_Y	AD23
4	IO_L93N_Y	AA20
4	IO_L94P_YY	Y19
4	IO_L94N_YY	AC21
4	IO_VREF_L95P_YY	AD22
4	IO_L95N_YY	AB20
4	IO_L96P	AE22
4	IO_L96N	Y18
4	IO_L97P	AF22
4	IO_L97N	AA19
4	IO_VREF_L98P_YY	AD21

FG676 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A — in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 21: FG676 Differential Pin Pair Summary
XCV400E, XCV600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
3	0	E13	B13	NA	IO_DLL_L21N
2	1	C13	F14	NA	IO_DLL_L21P
1	5	AB13	AF13	NA	IO_DLL_L115N
0	4	AA14	AC14	NA	IO_DLL_L115P
IOLVDS Total Pairs: 183, Asynchronous Output Pairs: 97					
0	0	F7	C4	1	-
1	0	C5	G8	—	-
2	0	E7	D6	—	VREF
3	0	F8	A4	NA	-
4	0	D7	B5	NA	-
5	0	G9	E8	—	VREF
6	0	F9	A5	—	-
7	0	C7	D8	1	-
8	0	E9	B7	1	VREF
9	0	D9	A7	NA	-
10	0	G10	B8	NA	VREF
11	0	F10	C9	—	-
12	0	E10	A8	1	-
13	0	D10	G11	—	-
14	0	F11	B10	—	-
15	0	E11	C10	NA	-
16	0	D11	G12	—	-
17	0	F12	C11	—	VREF

Table 21: FG676 Differential Pin Pair Summary
XCV400E, XCV600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
18	0	E12	A11	—	-
19	0	C12	D12	1	-
20	0	H13	A12	1	VREF
21	1	F14	B13	NA	IO_LVDS_DLL
22	1	F13	E14	NA	-
23	1	A14	D14	1	VREF
24	1	H14	C14	1	-
25	1	C15	G14	—	-
26	1	D15	E15	—	VREF
27	1	F15	C16	—	-
28	1	D16	G15	-	-
29	1	A17	E16	—	-
30	1	E17	C17	—	-
31	1	D17	F16	1	-
32	1	C18	F17	—	-
33	1	G16	A18	—	VREF
34	1	G17	C19	—	-
35	1	B19	D18	1	VREF
36	1	E18	D19	1	-
37	1	B20	F18	—	-
38	1	C20	G19	—	VREF
39	1	E19	G18	—	-
40	1	D20	A21	—	-
41	1	C21	F19	—	VREF
42	1	E20	B22	—	-
43	1	D21	A23	2	-
44	1	E21	C22	—	CS
45	2	E23	F22	—	DIN, D0
46	2	E24	F20	—	-
47	2	G21	G22	2	-
48	2	F24	H20	1	VREF
49	2	E25	H21	1	-
50	2	F23	G23	—	-
51	2	H23	J20	—	VREF

FG680 Fine-Pitch Ball Grid Array Package

XCV600E, XCV1000E, XCV1600E, and XCV2000E devices in the FG680 fine-pitch Ball Grid Array package have footprint compatibility. Pins labeled I0_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 22, see Table 23 for Differential Pair information.

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
0	GCK3	A20
0	IO	D35
0	IO	B36
0	IO_L0N_Y	C35
0	IO_L0P_Y	A36
0	IO_VREF_L1N_Y	D34[1]
0	IO_L1P_Y	B35
0	IO_L2N_YY	C34
0	IO_L2P_YY	A35
0	IO_VREF_L3N_YY	D33
0	IO_L3P_YY	B34
0	IO_L4N	C33
0	IO_L4P	A34
0	IO_L5N_Y	D32
0	IO_L5P_Y	B33
0	IO_L6N_YY	C32
0	IO_L6P_YY	D31
0	IO_VREF_L7N_YY	A33
0	IO_L7P_YY	C31
0	IO_L8N_Y	B32
0	IO_L8P_Y	B31
0	IO_VREF_L9N_Y	A32[3]
0	IO_L9P_Y	D30
0	IO_L10N_YY	A31
0	IO_L10P_YY	C30
0	IO_VREF_L11N_YY	B30
0	IO_L11P_YY	D29
0	IO_L12N_Y	A30
0	IO_L12P_Y	C29

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
0	IO_L13N_Y	A29
0	IO_L13P_Y	B29
0	IO_VREF_L14N_YY	B28
0	IO_L14P_YY	A28
0	IO_L15N_YY	C28
0	IO_L15P_YY	B27
0	IO_L16N_Y	D27
0	IO_L16P_Y	A27
0	IO_L17N_Y	C27
0	IO_L17P_Y	B26
0	IO_L18N_YY	D26
0	IO_L18P_YY	C26
0	IO_VREF_L19N_YY	A26[1]
0	IO_L19P_YY	D25
0	IO_L20N_Y	B25
0	IO_L20P_Y	C25
0	IO_L21N_Y	A25
0	IO_L21P_Y	D24
0	IO_L22N_YY	A24
0	IO_L22P_YY	B23
0	IO_VREF_L23N_YY	C24
0	IO_L23P_YY	A23
0	IO_L24N_Y	B24
0	IO_L24P_Y	B22
0	IO_L25N_Y	E23
0	IO_L25P_Y	A22
0	IO_L26N_YY	D23
0	IO_L26P_YY	B21
0	IO_VREF_L27N_YY	C23
0	IO_L27P_YY	A21
0	IO_L28N_Y	E22
0	IO_L28P_Y	B20
0	IO_LVDS_DLL_L29N	C22
0	IO_VREF	D22[2]
1	GCK2	D21

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
0	IO_VREF_L27N_YY	D27
0	IO_L27P_YY	B25
0	IO_L28N_Y	A25
0	IO_L28P_Y	D26
0	IO_L29N_Y	A24
0	IO_L29P_Y	E25
0	IO_L30N_YY	D25
0	IO_L30P_YY	B24
0	IO_VREF_L31N_YY	E24
0	IO_L31P_YY	A23
0	IO_L32N_Y	C23
0	IO_L32P_Y	E23
0	IO_VREF_L33N_Y	B23[1]
0	IO_L33P_Y	D23
0	IO_LVDS_DLL_L34N	A22
1	GCK2	B22
1	IO	A14
1	IO	A20
1	IO	B11
1	IO	B13
1	IO	C8
1	IO	C18
1	IO	C21
1	IO	D7
1	IO	D10
1	IO	D15
1	IO	D17
1	IO	E20
1	IO_LVDS_DLL_L34P	D22
1	IO_L35N_Y	D21
1	IO_VREF_L35P_Y	B21[1]
1	IO_L36N_Y	D20
1	IO_L36P_Y	A21
1	IO_L37N_YY	C20
1	IO_VREF_L37P_YY	D19
1	IO_L38N_YY	B20

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
1	IO_L38P_YY	E19
1	IO_L39N_Y	D18
1	IO_L39P_Y	A19
1	IO_L40N_Y	E18
1	IO_L40P_Y	C19
1	IO_L41N_YY	B19
1	IO_VREF_L41P_YY	E17
1	IO_L42N_YY	A18
1	IO_L42P_YY	D16
1	IO_L43N_Y	E16
1	IO_L43P_Y	B18
1	IO_L44N_Y	F16
1	IO_L44P_Y	A17
1	IO_L45N_YY	C17
1	IO_VREF_L45P_YY	E15
1	IO_L46N_YY	B17
1	IO_L46P_YY	D14
1	IO_L47N_Y	A16
1	IO_L47P_Y	E14
1	IO_L48N_Y	C16
1	IO_L48P_Y	D13
1	IO_L49N_Y	B16
1	IO_L49P_Y	D12
1	IO_L50N_Y	A15
1	IO_L50P_Y	E12
1	IO_L51N_YY	C15
1	IO_L51P_YY	C11
1	IO_L52N_YY	B15
1	IO_VREF_L52P_YY	D11
1	IO_L53N_Y	E11
1	IO_L53P_Y	C14
1	IO_L54N_Y	C10
1	IO_L54P_Y	B14
1	IO_L55N_YY	A13
1	IO_VREF_L55P_YY	E10
1	IO_L56N_YY	C13
1	IO_L56P_YY	C9

Table 25: FG860 Differential Pin Pair Summary
XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
256	7	T38	T41	—	-
257	7	T42	R39	1	VREF
258	7	R38	R42	2	-
259	7	P39	R40	4	-
260	7	P38	R41	2	-
261	7	N39	P42	1	-
262	7	M39	P40	3	-
263	7	M38	P41	—	-
264	7	L39	N42	—	VREF
265	7	N41	L38	2	-
266	7	M42	K40	—	-
267	7	K38	M40	—	VREF
268	7	J40	M41	2	-
269	7	L40	J39	5	VREF
270	7	L41	J38	—	-
271	7	H39	K42	—	VREF
272	7	H38	K41	1	-
273	7	G40	J41	2	-
274	7	G39	H42	—	-
275	7	G42	G38	1	VREF
276	7	F40	G41	2	-
277	7	F41	F42	4	-
278	7	E42	F39	2	VREF
279	7	E41	E40	1	-
280	7	D41	E39	3	-

Notes:
1. AO in the XCV1000E, 2000E.
2. AO in the XCV1000E, 1600E.
3. AO in the XCV2000E.
4. AO in the XCV1600E.
5. AO in the XCV1000E.

FG900 Fine-Pitch Ball Grid Array Package

XCV600E, XCV1000E, and XCV1600E devices in the FG900 fine-pitch Ball Grid Array package have footprint compatibility. Pins labeled I0_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 26, see Table 27 for Differential Pair information.

Table 26: FG900 — XCV600E, XCV1000E, XCV1600E

Bank	Pin Description	Pin #
0	GCK3	C15
0	IO	A7[4]
0	IO	A13[4]
0	IO	C5[4]
0	IO	C6[4]
0	IO	C14[4]
0	IO	D8[5]
0	IO	D10
0	IO	D13[4]
0	IO	E6
0	IO	E9[5]
0	IO	E14[5]
0	IO	F9[4]
0	IO	F14[5]
0	IO	G15
0	IO	K11[5]
0	IO	K12
0	IO	L13[4]
0	IO_L0N_YY	C4[4]
0	IO_L0P_YY	F7[3]
0	IO_L1N_Y	D5
0	IO_L1P_Y	G8
0	IO_VREF_L2N_Y	A3[1]
0	IO_L2P_Y	H9
0	IO_L3N_Y	B4[4]
0	IO_L3P_Y	J10[4]
0	IO_L4N_YY	A4
0	IO_L4P_YY	D6
0	IO_VREF_L5N_YY	E7
0	IO_L5P_YY	B5

Table 26: FG900 — XCV600E, XCV1000E, XCV1600E

Bank	Pin Description	Pin #
6	IO	AC5[4]
6	IO	AD1[4]
6	IO	AE5[5]
6	IO_L212N_YY	AF3
6	IO_L212P_YY	AC6
6	IO_L213N	AH2[4]
6	IO_L213P	AG2[3]
6	IO_L214N	AB9
6	IO_L214P	AE4
6	IO_VREF_L215N_YY	AE3[1]
6	IO_L215P_YY	AH1
6	IO_L216N_Y	AB8[4]
6	IO_L216P_Y	AD6[3]
6	IO_L217N_YY	AG1
6	IO_L217P_YY	AA10
6	IO_VREF_L218N	AA9
6	IO_L218P	AD4
6	IO_L219N_YY	AD5
6	IO_L219P_YY	AD2
6	IO_L220N_YY	AD3
6	IO_L220P_YY	AF2
6	IO_L221N	AA8
6	IO_L221P	AA7
6	IO_VREF_L222N_YY	AF1
6	IO_L222P_YY	Y9
6	IO_L223N_YY	AB6
6	IO_L223P_YY	AC4
6	IO_L224N	AE1
6	IO_L224P	W8
6	IO_L225N_YY	Y8
6	IO_L225P_YY	AB4
6	IO_VREF_L226N_YY	AB3
6	IO_L226P_YY	W9
6	IO_L227N_YY	AA5[4]
6	IO_L227P_YY	W10[3]
6	IO_L228N_YY	AB1
6	IO_L228P_YY	V10

Table 26: FG900 — XCV600E, XCV1000E, XCV1600E

Bank	Pin Description	Pin #
6	IO_L229N_YY	Y7[4]
6	IO_VREF_L229P_YY	AC1
6	IO_L230N	V11
6	IO_L230P	AA3
6	IO_L231N_YY	AA2[3]
6	IO_L231P_YY	U10[4]
6	IO_L232N	W7
6	IO_L232P	AA6
6	IO_L233N_YY	Y6
6	IO_L233P_YY	Y4
6	IO_L234N_Y	AA1[4]
6	IO_L234P_Y	V7[4]
6	IO_L235N_YY	Y3
6	IO_L235P_YY	Y2
6	IO_VREF_L236N	Y5[1]
6	IO_L236P	W5
6	IO_L237N_YY	W4
6	IO_L237P_YY	W6
6	IO_L238N_YY	V6
6	IO_L238P_YY	W2
6	IO_L239N	U9
6	IO_L239P	V4
6	IO_VREF_L240N_YY	AB2
6	IO_L240P_YY	T8
6	IO_L241N_YY	U5
6	IO_L241P_YY	W1
6	IO_L242N	Y1
6	IO_L242P	T9
6	IO_L243N_YY	T7
6	IO_L243P_YY	U3
6	IO_VREF_L244N_YY	T5
6	IO_L244P_YY	V2
6	IO_L245N_YY	R9[4]
6	IO_L245P_YY	T6[3]
6	IO_VREF_L246N_YY	T4[2]
6	IO_L246P_YY	U2
6	IO_L247N	T1

Table 26: FG900 — XCV600E, XCV1000E, XCV1600E

Bank	Pin Description	Pin #
NA	GND	AG27
NA	GND	D27
NA	GND	AF26
NA	GND	E26
NA	GND	F25
NA	GND	AE25
NA	GND	G24
NA	GND	AJ23
NA	GND	AD24
NA	GND	H23
NA	GND	B23
NA	GND	AC23
NA	GND	AB22
NA	GND	V22
NA	GND	N22
NA	GND	AH18
NA	GND	AB18
NA	GND	J18
NA	GND	C18
NA	GND	U17
NA	GND	T17
NA	GND	R17
NA	GND	P17
NA	GND	U16
NA	GND	T16
NA	GND	R16
NA	GND	P16
NA	GND	U15
NA	GND	T15
NA	GND	R15
NA	GND	P15
NA	GND	U14
NA	GND	T14
NA	GND	R14
NA	GND	P14
NA	GND	AH13
NA	GND	AB13

Table 26: FG900 — XCV600E, XCV1000E, XCV1600E

Bank	Pin Description	Pin #
NA	GND	J13
NA	GND	C13
NA	GND	V9
NA	GND	N9
NA	GND	J9
NA	GND	AJ8
NA	GND	AC8
NA	GND	H8
NA	GND	AD7
NA	GND	B8
NA	GND	AE6
NA	GND	G7
NA	GND	F6
NA	GND	AF5
NA	GND	E5
NA	GND	AG4
NA	GND	D4
NA	GND	V3
NA	GND	N3
NA	GND	C3
NA	GND	AK2
NA	GND	AH3
NA	GND	AC2
NA	GND	H2
NA	GND	B2
NA	GND	A2
NA	GND	AK1
NA	GND	AJ2
NA	GND	AJ1
NA	GND	A1
NA	GND	B1

Notes:
1. V_{REF} or I/O option only in the XCV1000E and XCV1600E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV1600E; otherwise, I/O option only.
3. I/O option only in the XCV600E.
4. No Connect in the XCV600E.
5. No Connect in the XCV600E, 1000E.

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
0	IO_L40P_Y	A17
0	IO_VREF_L41N_Y	G17[1]
0	IO_L41P_Y	B17
0	IO_LVDS_DLL_L42N	C17
1	GCK2	D17
1	IO	A18
1	IO	B18[3]
1	IO	B24
1	IO	B25
1	IO	E22[3]
1	IO	E23[3]
1	IO	D18[3]
1	IO	D19
1	IO	D25[3]
1	IO	D26[3]
1	IO	D28[3]
1	IO	D29[3]
1	IO	G23[3]
1	IO	J23[3]
1	IO_LVDS_DLL_L42P	J18
1	IO_L43N_Y	G18
1	IO_VREF_L43P_Y	C18[1]
1	IO_L44N_Y	H18
1	IO_L44P_Y	F18
1	IO_L45N_YY	B19
1	IO_VREF_L45P_YY	A19
1	IO_L46N_YY	K19
1	IO_L46P_YY	C19
1	IO_L47N	F19[5]
1	IO_L47P	E19[4]
1	IO_L48N_Y	G19
1	IO_L48P_Y	J19
1	IO_L49N_Y	A20

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
1	IO_L49P_Y	G20
1	IO_L50N	B20[5]
1	IO_L50P	F20[4]
1	IO_L51N_YY	D20
1	IO_VREF_L51P_YY	E20
1	IO_L52N_YY	H20
1	IO_L52P_YY	A21
1	IO_L53N	E21[5]
1	IO_L53P	J20[4]
1	IO_L54N_Y	D21
1	IO_L54P_Y	K20
1	IO_L55N_Y	B21
1	IO_L55P_Y	H21
1	IO_L56N_YY	G21[5]
1	IO_L56P_YY	F21[4]
1	IO_L57N_YY	A22
1	IO_VREF_L57P_YY	B22
1	IO_L58N_YY	J21
1	IO_L58P_YY	C22
1	IO_L59N_Y	D22
1	IO_L59P_Y	G22
1	IO_L60N_Y	K21
1	IO_L60P_Y	A23
1	IO_L61N_Y	F22
1	IO_L61P_Y	B23
1	IO_L62N_Y	C23
1	IO_L62P_Y	H22
1	IO_L63N_YY	D23
1	IO_L63P_YY	K22
1	IO_L64N_YY	A24
1	IO_VREF_L64P_YY	J22
1	IO_L65N_Y	H23
1	IO_L65P_Y	D24
1	IO_L66N_Y	A25