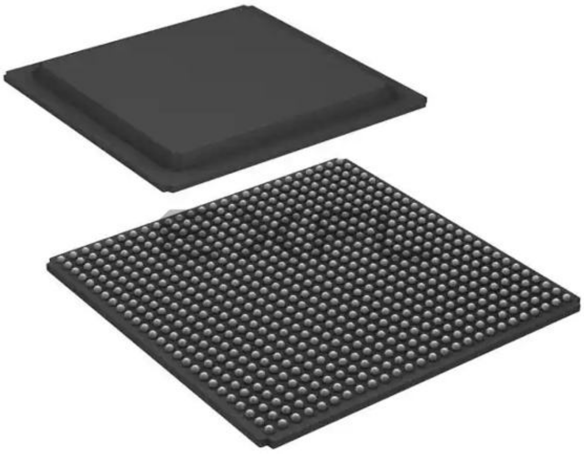

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	3456
Number of Logic Elements/Cells	15552
Total RAM Bits	294912
Number of I/O	444
Number of Gates	985882
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv600e-6fg676c

Table 1: **Supported I/O Standards**

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Board Termination Voltage (V_{TT})
LVTTL	3.3	3.3	N/A	N/A
LVCMOS2	2.5	2.5	N/A	N/A
LVCMOS18	1.8	1.8	N/A	N/A
SSTL3 I & II	3.3	N/A	1.50	1.50
SSTL2 I & II	2.5	N/A	1.25	1.25
GTL	N/A	N/A	0.80	1.20
GTL+	N/A	N/A	1.0	1.50
HSTL I	1.5	N/A	0.75	0.75
HSTL III & IV	1.5	N/A	0.90	1.50
CTT	3.3	N/A	1.50	1.50
AGP-2X	3.3	N/A	1.32	N/A
PCI33_3	3.3	3.3	N/A	N/A
PCI66_3	3.3	3.3	N/A	N/A
BLVDS & LVDS	2.5	N/A	N/A	N/A
LVPECL	3.3	N/A	N/A	N/A

In addition to the CLK and CE control signals, the three flip-flops share a Set/Reset (SR). For each flip-flop, this signal can be independently configured as a synchronous Set, a synchronous Reset, an asynchronous Preset, or an asynchronous Clear.

The output buffer and all of the IOB control signals have independent polarity controls.

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. After configuration, clamping diodes are connected to V_{CCO} with the exception of LVCMOS18, LVCMOS25, GTL, GTL+, LVDS, and LVPECL.

Optional pull-up, pull-down and weak-keeper circuits are attached to each pad. Prior to configuration all outputs not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive, but I/Os can optionally be pulled up.

The activation of pull-up resistors prior to configuration is controlled on a global basis by the configuration mode pins. If the pull-up resistors are not activated, all the pins are in a high-impedance state. Consequently, external pull-up or pull-down resistors must be provided on pins required to be at a well-defined logic level prior to configuration.

All Virtex-E IOBs support IEEE 1149.1-compatible Boundary Scan testing.

Input Path

The Virtex-E IOB input path routes the input signal directly to internal logic and/ or through an optional input flip-flop.

An optional delay element at the D-input of this flip-flop eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the FPGA, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signalling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF}. The need to supply V_{REF} imposes constraints on which standards can be used in close proximity to each other. See **I/O Banking**.

There are optional pull-up and pull-down resistors at each user I/O input for use after configuration. Their value is in the range 50 – 100 kΩ.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output signal can be routed to the buffer directly from the internal logic or through an optional IOB output flip-flop.

The 3-state control of the output can also be routed directly from the internal logic or through a flip-flip that provides synchronous enable and disable.

Each output driver can be individually programmed for a wide range of low-voltage signalling standards. Each output buffer can source up to 24 mA and sink up to 48 mA. Drive strength and slew rate controls minimize bus transients.

In most signalling standards, the output High voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in close proximity to each other. See **I/O Banking**.

An optional weak-keeper circuit is connected to each output. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low to match the input signal. If the pin is connected to a multiple-source signal, the weak keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way eliminates bus chatter.

Since the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate V_{REF} voltage must be provided if the signalling standard requires one. The provision of this voltage must comply with the I/O banking rules.

I/O Banking

Some of the I/O standards described above require V_{CCO} and/or V_{REF} voltages. These voltages are externally supplied and connected to device pins that serve groups of IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

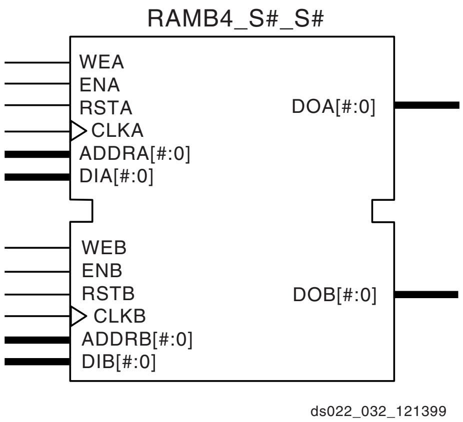

Figure 31: **Dual-Port Block SelectRAM+ Memory**

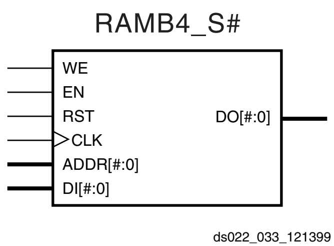

Figure 32: **Single-Port Block SelectRAM+ Memory**

Table 14: **Available Library Primitives**

Primitive	Port A Width	Port B Width
RAMB4_S1	1	N/A
RAMB4_S1_S1		1
RAMB4_S1_S2		2
RAMB4_S1_S4		4
RAMB4_S1_S8		8
RAMB4_S1_S16		16
RAMB4_S2	2	N/A
RAMB4_S2_S2		2
RAMB4_S2_S4		4
RAMB4_S2_S8		8
RAMB4_S2_S16		16
RAMB4_S4	4	N/A
RAMB4_S4_S4		4
RAMB4_S4_S8		8
RAMB4_S4_S16		16
RAMB4_S8	8	N/A
RAMB4_S8_S8		8
RAMB4_S8_S16		16
RAMB4_S16	16	N/A
RAMB4_S16_S16		16

Port Signals

Each block SelectRAM+ port operates independently of the others while accessing the same set of 4096 memory cells.

Table 15 describes the depth and width aspect ratios for the block SelectRAM+ memory.

Table 15: **Block SelectRAM+ Port Aspect Ratios**

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

Clock—CLK[A|B]

Each port is fully synchronous with independent clock pins. All port input pins have setup time referenced to the port CLK pin. The data output bus has a clock-to-out time referenced to the CLK pin.

Enable—EN[A|B]

The enable pin affects the read, write and reset functionality of the port. Ports with an inactive enable pin keep the output pins in the previous state and do not write data to the memory cells.

Write Enable—WE[A|B]

Activating the write enable pin allows the port to write to the memory cells. When active, the contents of the data input bus are written to the RAM at the address pointed to by the address bus, and the new data also reflects on the data out bus. When inactive, a read operation occurs and the contents of the memory cells referenced by the address bus reflect on the data out bus.

Reset—RST[A|B]

The reset pin forces the data output bus latches to zero synchronously. This does not affect the memory cells of the RAM and does not disturb a write operation on the other port.

Address Bus—ADDR[A|B]<#:0>

The address bus selects the memory cells for read or write. The width of the port determines the required width of this bus as shown in Table 15.

Data In Bus—DI[A|B]<#:0>

The data in bus provides the new data value to be written into the RAM. This bus and the port have the same width, as shown in Table 15.

Table 43: **Output Library Macros**

Name	Inputs	Outputs
OBUFDS_FD_LVDS	D, C	O, OB
OBUFDS_FDE_LVDS	DD, CE, C	O, OB
OBUFDS_FDC_LVDS	D, C, CLR	O, OB
OBUFDS_FDCE_LVDS	D, CE, C, CLR	O, OB
OBUFDS_FDP_LVDS	D, C, PRE	O, OB
OBUFDS_FDPE_LVDS	D, CE, C, PRE	O, OB
OBUFDS_FDR_LVDS	D, C, R	O, OB
OBUFDS_FDRE_LVDS	D, CE, C, R	O, OB
OBUFDS_FDS_LVDS	D, C, S	O, OB
OBUFDS_FDSE_LVDS	D, CE, C, S	O, OB
OBUFDS_LD_LVDS	D, G	O, OB
OBUFDS_LDE_LVDS	D, GE, G	O, OB
OBUFDS_LDC_LVDS	D, G, CLR	O, OB
OBUFDS_LDCE_LVDS	D, GE, G, CLR	O, OB
OBUFDS_LDP_LVDS	D, G, PRE	O, OB
OBUFDS_LDPE_LVDS	D, GE, G, PRE	O, OB

Creating LVDS Output 3-State Buffers

LVDS output 3-state buffers can be placed in a wide number of IOB locations. The exact locations are dependent on the package used. The Virtex-E package information lists the possible locations as IO_L#P for the P-side and IO_L#N for the N-side, where # is the pair number.

HDL Instantiation

Both output 3-state buffers are required to be instantiated in the design and placed on the correct IO_L#P and IO_L#N locations. The IOB must have the same net source the following pins, clock (C), set/reset (SR), 3-state (T), 3-state clock enable (TCE), output (O), output clock enable (OCE). In addition, the output (O) pins must be inverted with respect to each other, and if output registers are used, the INIT states must be opposite values (one High and one Low). If 3-state registers are used, they must be initialized to the same state. Failure to follow these rules leads to DRC errors in the software.

VHDL Instantiation

```
data0_p:   OBUFT_LVDS port map
(I=>data_int(0), T=>data_tri,
O=>data_p(0));

data0_inv: INV port map
(I=>data_int(0), O=>data_n_int(0));

data0_n:    OBUFT_LVDS port map
(I=>data_n_int(0), T=>data_tri,
O=>data_n(0));
```

Verilog Instantiation

```
OBUFT_LVDS data0_p   (.I(data_int[0]),
.T(data_tri), .O(data_p[0]));

INV        data0_inv (.I(data_int[0],
.O(data_n_int[0]);

OBUFT_LVDS data0_n   (.I(data_n_int[0]),
.T(data_tri), .O(data_n[0]));
```

Location Constraints

All LVDS buffers must be explicitly placed on a device. For the output buffers this can be done with the following constraint in the .ucf or .ncf file.

```
NET data_p<0> LOC = D28; # IO_L0P

NET data_n<0> LOC = B29; # IO_L0N
```

Synchronous vs. Asynchronous 3-State Outputs

If the outputs are synchronous (registered in the IOB), then any IO_L#P|N pair can be used. If the outputs are asynchronous (no output register), then they must use one of the pairs that are part of the same IOB group at the end of a ROW or COLUMN in the device. This applies for either the 3-state pin or the data out pin.

LVDS pairs that can be used as asynchronous outputs are listed in the Virtex-E pinout tables. Some pairs are marked as "asynchronous capable" for all devices in that package, and others are marked as available only for that device in the package. If the device size might be changed at some point in the product lifetime, then only the common pairs for all packages should be used.

Adding Output and 3-State Registers

All LVDS buffers can have an output register in the IOB. The output registers must be in both the P-side and N-side IOBs. All the normal IOB register options are available (FD, FDE, FDC, FDCE, FDP, FDPE, FDR, FDRE, FDS, FDSE, LD, LDE, LDC, LDCE, LDP, LDPE). The register elements can be inferred or explicitly instantiated in the HDL code.

Special care must be taken to insure that the D pins of the registers are inverted and that the INIT states of the registers are opposite. The 3-state (T), 3-state clock enable (CE), clock pin (C), output clock enable (CE) and set/reset (CLR/PRE or S/R) pins must connect to the same source. Failure to do this leads to a DRC error in the software.

Virtex-E Data Sheet

The Virtex-E Data Sheet contains the following modules:

- DS022-1, Virtex-E 1.8V FPGAs:
  Introduction and Ordering Information (Module 1)
- DS022-2, Virtex-E 1.8V FPGAs:
  Functional Description (Module 2)
- DS022-3, Virtex-E 1.8V FPGAs:
  DC and Switching Characteristics (Module 3)
- DS022-4, Virtex-E 1.8V FPGAs:
  Pinout Tables (Module 4)

DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Device	Min	Max	Units
V_{DRINT}	Data Retention V_{CCINT} Voltage (below which configuration data might be lost)		All	1.5		V
V_{DRIO}	Data Retention V_{CCO} Voltage (below which configuration data might be lost)		All	1.2		V
I_{CCINTQ}	Quiescent V_{CCINT} supply current (Note 1)		XCV50E		200	mA
			XCV100E		200	mA
			XCV200E		300	mA
			XCV300E		300	mA
			XCV400E		300	mA
			XCV600E		400	mA
			XCV1000E		500	mA
			XCV1600E		500	mA
			XCV2000E		500	mA
			XCV2600E		500	mA
			XCV3200E		500	mA
I_{CCOQ}	Quiescent V_{CCO} supply current (Note 1)		XCV50E		2	mA
			XCV100E		2	mA
			XCV200E		2	mA
			XCV300E		2	mA
			XCV400E		2	mA
			XCV600E		2	mA
			XCV1000E		2	mA
			XCV1600E		2	mA
			XCV2000E		2	mA
			XCV2600E		2	mA
			XCV3200E		2	mA
I_L	Input or output leakage current		All	–10	+10	µA
C_{IN}	Input capacitance (sample tested)	BGA, PQ, HQ, packages	All		8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0 V, V_{CCO} = 3.3 V (sample tested)		All	Note 2	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 3.6 V (sample tested)			Note 2	0.25	mA

Notes:
1. With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating.
2. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
0	IO_L11P_YY	B24	
0	IO_L12N_Y	E22	
0	IO_L12P_Y	C23	
0	IO_L13N_YY	A23	
0	IO_L13P_YY	D22	
0	IO_VREF_L14N_YY	E21	3
0	IO_L14P_YY	B22	
0	IO_L15N_Y	D21	
0	IO_L15P_Y	C21	
0	IO_L16N_YY	B21	
0	IO_L16P_YY	E20	
0	IO_VREF_L17N_YY	D20	
0	IO_L17P_YY	C20	
0	IO_L18N_Y	B20	
0	IO_L18P_Y	E19	
0	IO_L19N_Y	D19	
0	IO_L19P_Y	C19	
0	IO_VREF_L20N_Y	A19	
0	IO_L20P_Y	D18	
0	IO_LVDS_DLL_L21N	C18	
0	IO_VREF	E18	2
1	GCK2	D17	
1	IO	A3	
1	IO	D9	
1	IO	E8	
1	IO	E11	
1	IO_LVDS_DLL_L21P	E17	
1	IO_VREF_L22N_Y	C17	2
1	IO_L22P_Y	B17	
1	IO_L23N_Y	B16	
1	IO_VREF_L23P_Y	D16	
1	IO_L24N_Y	E16	
1	IO_L24P_Y	C16	
1	IO_L25N_Y	A15	

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
1	IO_L25P_Y	C15	
1	IO_L26N_YY	D15	
1	IO_VREF_L26P_YY	E15	
1	IO_L27N_YY	C14	
1	IO_L27P_YY	D14	
1	IO_L28N_Y	A13	
1	IO_L28P_Y	E14	
1	IO_L29N_YY	C13	
1	IO_VREF_L29P_YY	D13	3
1	IO_L30N_YY	C12	
1	IO_L30P_YY	E13	
1	IO_L31N_Y	A11	
1	IO_L31P_Y	D12	
1	IO_L32N_YY	B11	
1	IO_L32P_YY	C11	
1	IO_L33N_YY	B10	
1	IO_VREF_L33P_YY	D11	
1	IO_L34N_Y	C10	
1	IO_L34P_Y	A9	
1	IO_L35N_Y	C9	
1	IO_VREF_L35P_Y	D10	4
1	IO_L36N_Y	A8	
1	IO_L36P_Y	B8	
1	IO_L37N_Y	E10	
1	IO_VREF_L37P_Y	C8	1
1	IO_L38N_YY	B7	
1	IO_VREF_L38P_YY	A6	
1	IO_L39N_YY	C7	
1	IO_L39P_YY	D8	
1	IO_L40N_Y	A5	
1	IO_L40P_Y	B5	
1	IO_L41N_YY	C6	
1	IO_VREF_L41P_YY	D7	
1	IO_L42N_YY	A4	
1	IO_L42P_YY	B4	

Table 15: **BG560 Differential Pin Pair Summary XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
171	7	J33	M29	√	-
172	7	K31	L30	√	VREF
173	7	H33	L29	4	-
174	7	H32	J31	18	VREF
175	7	H31	K29	14	-
176	7	G32	J30	20	VREF
177	7	G31	J29	√	VREF
178	7	E32	E33	15	-
179	7	F31	H29	14	-
180	7	E31	D32	15	VREF
181	7	C33	G29	14	-
182	7	D31	F30	14	VREF

Notes:
1. AO in the XCV1600E.
2. AO in the XCV2000E.
3. AO in the XCV1600E, 2000E.
4. AO in the XCV1000E, 1600E.
5. AO in the XCV1000E, 2000E.
6. AO in the XCV1000E.
7. AO in the XCV1000E, 1600E, 2000E.
8. AO in the XCV600E, 1600E.
9. AO in the XCV400E, 600E, 1600E.
10. AO in the XCV400E, 600E, 1000E, 2000E.
11. AO in the XCV400E, 600E, 1000E.
12. AO in the XCV400E, 1000E, 2000E.
13. AO in the XCV400E, 600E, 1000E, 1600E.
14. AO in the XCV400E, 1000E, 1600E.
15. AO in the XCV600E, 1000E, 2000E.
16. AO in the XCV600E, 2000E.
17. AO in the XCV400E, 600E, 1600E, 2000E.
18. AO in the XCV600E, 1000E, 1600E, 2000E.
19. AO in the XCV400E, 600E, 2000E.
20. AO in the XCV400E, 1000E.

FG256 Fine-Pitch Ball Grid Array Packages

XCV50E, XCV100E, XCV200E, and XCV300E devices in FG256 fine-pitch Ball Grid Array packages have footprint compatibility. Pins labeled I0_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 16, see Table 17 for Differential Pair information.

Table 16: **FG256 Package — XCV50E, XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
0	GCK3	B8
0	IO	B3
0	IO	E7
0	IO	D8
0	IO_L0N_Y	C5
0	IO_VREF_L0P_Y	A3[2]
0	IO_L1N_YY	D5
0	IO_L1P_YY	E6
0	IO_VREF_L2N_YY	B4
0	IO_L2P_YY	A4
0	IO_L3N_Y	D6
0	IO_L3P_Y	B5
0	IO_VREF_L4N_YY	C6[1]
0	IO_L4P_YY	A5
0	IO_L5N_YY	B6
0	IO_L5P_YY	C7
0	IO_L6N_Y	D7
0	IO_L6P_Y	C8
0	IO_VREF_L7N_Y	B7
0	IO_L7P_Y	A6
0	IO_LVDS_DLL_L8N	A7
1	GCK2	C9
1	IO	B10
1	IO_LVDS_DLL_L8P	A8
1	IO_L9N_Y	D9
1	IO_L9P_Y	A9
1	IO_L10N_Y	E10
1	IO_VREF_L10P_Y	B9

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
3	IO_L50N_YY	P19
3	IO_L51P_YY	P18
3	IO_D5_L51N_YY	R21
3	IO_D6_L52P_Y	T22
3	IO_VREF_L52N_Y	R19
3	IO_L53P_Y	U22
3	IO_L53N_Y	R18
3	IO_L54P_YY	T21
3	IO_L54N_YY	V22
3	IO_L55P_YY	T20
3	IO_VREF_L55N_YY	U21
3	IO_L56P_YY	W22
3	IO_L56N_YY	T18
3	IO_L57P_YY	U19
3	IO_VREF_L57N_YY	U20
3	IO_L58P_YY	W21
3	IO_L58N_YY	AA22
3	IO_D7_L59P_YY	Y21
3	IO_INIT_L59N_YY	V19
3	IO	M22
4	GCK0	W12
4	IO	W14
4	IO	Y13
4	IO	Y17
4	IO	AA16[1]
4	IO	AA19
4	IO	AB12[1]
4	IO	AB17
4	IO	AB21[1]
4	IO_L60P_YY	W18
4	IO_L60N_YY	AA20
4	IO_L61P	Y18
4	IO_L61N	V17
4	IO_VREF_L62P_YY	AB20
4	IO_L62N_YY	W17
4	IO_L63P	AA18

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
4	IO_L63N	V16
4	IO_VREF_L64P_YY	AB19
4	IO_L64N_YY	AB18
4	IO_L65P_Y	W16
4	IO_L65N_Y	AA17
4	IO_L66P_Y	Y16
4	IO_L66N_Y	V15
4	IO_VREF_L67P_YY	AB16
4	IO_L67N_YY	Y15
4	IO_L68P_YY	AA15
4	IO_L68N_YY	AB15
4	IO_L69P_Y	W15
4	IO_L69N_Y	Y14
4	IO_L70P_Y	V14
4	IO_L70N_Y	AA14
4	IO_L71P	AB14
4	IO_L71N	V13
4	IO_VREF_L72P_YY	AA13
4	IO_L72N_YY	AB13
4	IO_L73P_Y	W13
4	IO_L73N_Y	AA12
4	IO_L74P_Y	Y12
4	IO_L74N_Y	V12
4	IO_LVDS_DLL_L75P	U12
5	IO	U11[1]
5	IO	V8
5	IO	W5
5	IO	AA3[1]
5	IO	AA9
5	IO	AA10
5	IO	AB4
5	IO	AB7[1]
5	IO	AB8
5	GCK1	Y11
5	IO_LVDS_DLL_L75N	AA11
5	IO_L76P_Y	AB11

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
7	IO	J1
7	IO	J4
7	IO	L2[1]
7	IO_L104N_YY	L3
7	IO_L104P_YY	L4
7	IO_L105N_YY	L5
7	IO_L105P_YY	L1
7	IO_L106N_Y	L6
7	IO_L106P_Y	K2
7	IO_L107N_Y	K4
7	IO_VREF_L107P_Y	K3
7	IO_L108N_YY	K1
7	IO_L108P_YY	K5
7	IO_L109N_YY	J3
7	IO_L109P_YY	J2
7	IO_L110N_YY	J5
7	IO_L110P_YY	H1
7	IO_L111N_YY	H2
7	IO_L111P_YY	H3
7	IO_L112N_Y	G1
7	IO_VREF_L112P_Y	H4
7	IO_L113N_Y	F1
7	IO_L113P_Y	F2
7	IO_L114N_YY	H5
7	IO_L114P_YY	G3
7	IO_L115N_YY	E1
7	IO_VREF_L115P_YY	E2
7	IO_L116N_YY	F3
7	IO_L116P_YY	G5
7	IO_L117N_YY	E3
7	IO_VREF_L117P_YY	D2
7	IO_L118N_YY	F5
7	IO_L118P_YY	C1
2	CCLK	B22
3	DONE	Y19
NA	DXN	Y5

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
NA	DXP	V6
NA	M0	AB2
NA	M1	U5
NA	M2	Y4
NA	PROGRAM	W20
NA	TCK	C4
NA	TDI	B20
2	TDO	A21
NA	TMS	D3
NA	NC	W19
NA	NC	W4
NA	NC	D19
NA	NC	D4
NA	VCCINT	E5
NA	VCCINT	E18
NA	VCCINT	F6
NA	VCCINT	F17
NA	VCCINT	G7
NA	VCCINT	G8
NA	VCCINT	G9
NA	VCCINT	G14
NA	VCCINT	G15
NA	VCCINT	H7
NA	VCCINT	G16
NA	VCCINT	H16
NA	VCCINT	J7
NA	VCCINT	J16
NA	VCCINT	P7
NA	VCCINT	P16
NA	VCCINT	R7
NA	VCCINT	R16
NA	VCCINT	T7
NA	VCCINT	T8
NA	VCCINT	T9
NA	VCCINT	T14

Table 19: **FG456 Differential Pin Pair Summary XCV200E, XCV300E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
88	5	V7	AB3	√	-
89	6	Y2	W3	√	-
90	6	V3	V4	√	-
91	6	U4	Y1	√	VREF
92	6	W1	V2	√	-
93	6	U2	T3	√	VREF
94	6	V1	T5	2	-
95	6	U1	R5	1	-
96	6	T1	R4	2	VREF
97	6	P3	R2	√	-
98	6	R1	P5	√	-
99	6	N5	P2	√	-
100	6	N4	P1	2	-
101	6	N2	N3	1	VREF
102	6	M4	N1	2	-
103	6	M6	M3	√	-
104	7	L4	L3	√	-
105	7	L1	L5	√	-
106	7	K2	L6	2	-
107	7	K3	K4	2	VREF
108	7	K5	K1	√	-
109	7	J2	J3	√	-
110	7	H1	J5	√	-
111	7	H3	H2	√	-
112	7	H4	G1	2	VREF
113	7	F2	F1	2	-
114	7	G3	H5	√	-
115	7	E2	E1	√	VREF
116	7	G5	F3	√	-
117	7	D2	E3	√	VREF
118	7	C1	F5	√	-

Notes:
1. AO in the XCV200E.
2. AO in the XCV300E.

FG676 Fine-Pitch Ball Grid Array Package

XCV400E and XCV600E devices in the FG676 fine-pitch Ball Grid Array package have footprint compatibility. Pins labeled I0_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 20, see Table 21 for Differential Pair information.

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
0	GCK3	E13
0	IO	A6
0	IO	A9[1]
0	IO	A10[1]
0	IO	B3
0	IO	B4[1]
0	IO	B12[1]
0	IO	C6
0	IO	C8
0	IO	D5
0	IO	D13[1]
0	IO	G13
0	IO_L0N_Y	C4
0	IO_L0P_Y	F7
0	IO_L1N_YY	G8
0	IO_L1P_YY	C5
0	IO_VREF_L2N_YY	D6
0	IO_L2P_YY	E7
0	IO_L3N	A4
0	IO_L3P	F8
0	IO_L4N	B5
0	IO_L4P	D7
0	IO_VREF_L5N_YY	E8
0	IO_L5P_YY	G9
0	IO_L6N_YY	A5
0	IO_L6P_YY	F9
0	IO_L7N_Y	D8
0	IO_L7P_Y	C7
0	IO_VREF_L8N_Y	B7[2]
0	IO_L8P_Y	E9

Table 21: **FG676 Differential Pin Pair Summary XCV400E, XCV600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
120	5	AD11	Y12	√	-
121	5	AB11	AD10	NA	-
122	5	AC11	AE10	√	-
123	5	AC10	AA11	√	-
124	5	Y11	AD9	1	-
125	5	AB10	AF9	√	-
126	5	AD8	AA10	√	VREF
127	5	AE8	Y10	√	-
128	5	AC9	AF8	1	VREF
129	5	AF7	AB9	1	-
130	5	AA9	AF6	√	-
131	5	AC8	AC7	√	VREF
132	5	AD6	Y9	√	-
133	5	AE5	AA8	√	-
134	5	AC6	AB8	√	VREF
135	5	AD5	AA7	√	-
136	5	AF4	AC5	2	-
137	6	AC3	AA5	√	-
138	6	AB4	AC2	√	-
139	6	AA4	W6	2	-
140	6	Y5	AB3	1	VREF
141	6	V7	AB2	1	-
142	6	Y4	AB1	√	-
143	6	W5	V5	√	VREF
144	6	V6	AA1	√	-
145	6	Y3	W4	2	-
146	6	U7	Y1	1	VREF
147	6	V4	W1	√	-
148	6	U6	W2	√	VREF
149	6	T5	V3	√	-
150	6	U4	U5	√	-
151	6	U3	T7	2	-
152	6	T6	U2	1	-
153	6	T4	U1	1	-

Table 21: **FG676 Differential Pin Pair Summary XCV400E, XCV600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
154	6	T3	R7	1	-
155	6	R6	R4	√	VREF
156	6	R5	R3	√	-
157	6	P7	P8	2	-
158	6	P6	R1	1	VREF
159	6	P4	P5	√	-
160	7	N8	N5	√	-
161	7	N3	N6	√	-
162	7	M2	N4	1	VREF
163	7	M7	N7	2	-
164	7	M3	M6	√	-
165	7	M5	M4	√	VREF
166	7	L7	L3	1	-
167	7	K2	L6	1	-
168	7	K1	L4	1	-
169	7	L5	K3	2	-
170	7	J3	K5	√	-
171	7	J4	K4	√	-
172	7	K6	H3	√	VREF
173	7	G3	K7	√	-
174	7	H1	J5	1	VREF
175	7	J6	G2	2	-
176	7	F1	J7	√	-
177	7	G4	H4	√	VREF
178	7	H5	F3	1	-
179	7	H6	E2	2	-
180	7	F4	G5	1	VREF
181	7	G6	H7	2	-
182	7	E4	E3	√	-

Notes:
1. AO in the XCV600E.
2. AO in the XCV400E.

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
7	IO_L234N_YY	K38
7	IO_L234P_YY	L37
7	IO_L235N_YY	J39
7	IO_VREF_L235P_YY	L36
7	IO_L236N	J38
7	IO_L236P	K37
7	IO_L237N	H39
7	IO_VREF_L237P	K36[3]
7	IO_L238N_YY	H38
7	IO_L238P_YY	J37
7	IO_L239N_YY	G39
7	IO_VREF_L239P_YY	G38
7	IO_L240N_Y	J36
7	IO_L240P_Y	F39
7	IO_L241N	H37
7	IO_L241P	F38
7	IO_L242N_YY	H36
7	IO_L242P_YY	E39
7	IO_L243N_Y	G37
7	IO_VREF_L243P_Y	E38
7	IO_L244N	G36
7	IO_L244P	D39
7	IO_L245N	D38
7	IO_VREF_L245P	F36[1]
7	IO_L246N_Y	D37
7	IO_L246P_Y	E37
2	CCLK	E4
3	DONE	AU5
NA	DXN	AV37
NA	DXP	AU35
NA	M0	AT37
NA	M1	AU38
NA	M2	AT35
NA	PROGRAM	AT5
NA	TCK	C36

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
NA	TDI	B3
2	TDO	C4
NA	TMS	E36
NA	VCCINT	E8
NA	VCCINT	E9
NA	VCCINT	E15
NA	VCCINT	E16
NA	VCCINT	E24
NA	VCCINT	E25
NA	VCCINT	E31
NA	VCCINT	E32
NA	VCCINT	H5
NA	VCCINT	H35
NA	VCCINT	J5
NA	VCCINT	J35
NA	VCCINT	R5
NA	VCCINT	R35
NA	VCCINT	T5
NA	VCCINT	T35
NA	VCCINT	AD5
NA	VCCINT	AD35
NA	VCCINT	AE5
NA	VCCINT	AE35
NA	VCCINT	AL5
NA	VCCINT	AL35
NA	VCCINT	AM5
NA	VCCINT	AM35
NA	VCCINT	AR8
NA	VCCINT	AR9
NA	VCCINT	AR15
NA	VCCINT	AR16
NA	VCCINT	AR24
NA	VCCINT	AR25
NA	VCCINT	AR31
NA	VCCINT	AR32

FG680 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 23: **FG680 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
GCLK LVDS					
3	0	A20	C22	NA	IO_DLL_L29N
2	1	D21	A19	NA	IO_DLL_L29P
1	5	AU22	AT22	NA	IO_DLL_L155N
0	4	AW19	AT21	NA	IO_DLL_L155P
IO LVDS Total Pairs: 247, Asynchronous Output Pairs: 111					
0	0	A36	C35	5	-
1	0	B35	D34	5	VREF
2	0	A35	C34	√	-
3	0	B34	D33	√	VREF
4	0	A34	C33	3	-
5	0	B33	D32	3	-
6	0	D31	C32	√	-
7	0	C31	A33	√	VREF
8	0	B31	B32	5	-
9	0	D30	A32	5	VREF
10	0	C30	A31	√	-
11	0	D29	B30	√	VREF
12	0	C29	A30	2	-
13	0	B29	A29	2	-
14	0	A28	B28	√	VREF
15	0	B27	C28	√	-
16	0	A27	D27	5	-
17	0	B26	C27	5	-

Table 23: **FG680 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
18	0	C26	D26	√	-
19	0	D25	A26	√	VREF
20	0	C25	B25	3	-
21	0	D24	A25	3	-
22	0	B23	A24	√	-
23	0	A23	C24	√	VREF
24	0	B22	B24	5	-
25	0	A22	E23	5	-
26	0	B21	D23	√	-
27	0	A21	C23	√	VREF
28	0	B20	E22	2	-
29	1	A19	C22	NA	IO_LVDS_DLL
30	1	B19	C21	2	VREF
31	1	A18	C19	2	-
32	1	B18	D19	√	VREF
33	1	A17	C18	√	-
34	1	B17	D18	5	-
35	1	A16	E18	5	-
36	1	D17	C17	√	VREF
37	1	E17	B16	√	-
38	1	C16	A15	3	-
39	1	D16	B15	3	-
40	1	B14	A14	√	VREF
41	1	A13	C15	√	-
42	1	B13	D15	5	-
43	1	A12	C14	5	-
44	1	C13	D14	√	-
45	1	D13	B12	√	VREF
46	1	C12	A11	2	-
47	1	C11	B11	2	-
48	1	D11	A10	√	VREF
49	1	C10	B10	√	-
50	1	D10	A9	5	VREF
51	1	C9	B9	5	-

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
0	IO_VREF_L27N_YY	D27
0	IO_L27P_YY	B25
0	IO_L28N_Y	A25
0	IO_L28P_Y	D26
0	IO_L29N_Y	A24
0	IO_L29P_Y	E25
0	IO_L30N_YY	D25
0	IO_L30P_YY	B24
0	IO_VREF_L31N_YY	E24
0	IO_L31P_YY	A23
0	IO_L32N_Y	C23
0	IO_L32P_Y	E23
0	IO_VREF_L33N_Y	B23[1]
0	IO_L33P_Y	D23
0	IO_LVDS_DLL_L34N	A22
1	GCK2	B22
1	IO	A14
1	IO	A20
1	IO	B11
1	IO	B13
1	IO	C8
1	IO	C18
1	IO	C21
1	IO	D7
1	IO	D10
1	IO	D15
1	IO	D17
1	IO	E20
1	IO_LVDS_DLL_L34P	D22
1	IO_L35N_Y	D21
1	IO_VREF_L35P_Y	B21[1]
1	IO_L36N_Y	D20
1	IO_L36P_Y	A21
1	IO_L37N_YY	C20
1	IO_VREF_L37P_YY	D19
1	IO_L38N_YY	B20

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
1	IO_L38P_YY	E19
1	IO_L39N_Y	D18
1	IO_L39P_Y	A19
1	IO_L40N_Y	E18
1	IO_L40P_Y	C19
1	IO_L41N_YY	B19
1	IO_VREF_L41P_YY	E17
1	IO_L42N_YY	A18
1	IO_L42P_YY	D16
1	IO_L43N_Y	E16
1	IO_L43P_Y	B18
1	IO_L44N_Y	F16
1	IO_L44P_Y	A17
1	IO_L45N_YY	C17
1	IO_VREF_L45P_YY	E15
1	IO_L46N_YY	B17
1	IO_L46P_YY	D14
1	IO_L47N_Y	A16
1	IO_L47P_Y	E14
1	IO_L48N_Y	C16
1	IO_L48P_Y	D13
1	IO_L49N_Y	B16
1	IO_L49P_Y	D12
1	IO_L50N_Y	A15
1	IO_L50P_Y	E12
1	IO_L51N_YY	C15
1	IO_L51P_YY	C11
1	IO_L52N_YY	B15
1	IO_VREF_L52P_YY	D11
1	IO_L53N_Y	E11
1	IO_L53P_Y	C14
1	IO_L54N_Y	C10
1	IO_L54P_Y	B14
1	IO_L55N_YY	A13
1	IO_VREF_L55P_YY	E10
1	IO_L56N_YY	C13
1	IO_L56P_YY	C9

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
0	IO_L6N_Y	A5
0	IO_L6P_Y	F8
0	IO_L7N_Y	D7
0	IO_L7P_Y	N11
0	IO_L8N_YY	G9
0	IO_L8P_YY	E8
0	IO_VREF_L9N_YY	A6
0	IO_L9P_YY	J11
0	IO_L10N_Y	C7
0	IO_L10P_Y	B7
0	IO_L11N_Y	C8
0	IO_L11P_Y	H10
0	IO_L12N_YY	G10
0	IO_L12P_YY	F10
0	IO_VREF_L13N_YY	A8
0	IO_L13P_YY	H11
0	IO_L14N	D9[4]
0	IO_L14P	C9[3]
0	IO_L15N_YY	B9
0	IO_L15P_YY	J12
0	IO_L16N	E10[4]
0	IO_VREF_L16P	A9
0	IO_L17N	G11
0	IO_L17P	B10
0	IO_L18N_YY	H12[4]
0	IO_L18P_YY	C10[4]
0	IO_L19N_Y	H13
0	IO_L19P_Y	F11
0	IO_L20N_Y	E11
0	IO_L20P_Y	D11
0	IO_L21N_Y	B11[4]
0	IO_L21P_Y	G12[4]
0	IO_L22N_YY	F12
0	IO_L22P_YY	C11
0	IO_VREF_L23N_YY	A10[1]
0	IO_L23P_YY	D12
0	IO_L24N_Y	E12
0	IO_L24P_Y	A11
0	IO_L25N_Y	G13
0	IO_L25P_Y	B12
0	IO_L26N_YY	A12
0	IO_L26P_YY	K13
0	IO_VREF_L27N_YY	F13
0	IO_L27P_YY	B13
0	IO_L28N_Y	G14
0	IO_L28P_Y	E13
0	IO_L29N_Y	D14
0	IO_L29P_Y	B14
0	IO_L30N_YY	A14
0	IO_L30P_YY	J14
0	IO_VREF_L31N_YY	K14
0	IO_L31P_YY	J15
0	IO_L32N	B15[4]
0	IO_L32P	H15[3]
0	IO_VREF_L33N_YY	F15[2,3]
0	IO_L33P_YY	D15[4]
0	IO_LVDS_DLL_L34N	A15
1	GCK2	E15
1	IO	A25[4]
1	IO	B17[4]
1	IO	B18[4]
1	IO	C23[4]
1	IO	D16[4]
1	IO	D17[5]
1	IO	D23[4]
1	IO	E19[4]
1	IO	E24[5]
1	IO	F22[4]
1	IO	G17[5]
1	IO	G20[4]
1	IO	J16[4]
1	IO	J17[4]
1	IO	J19[5]

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
2	IO_L99P_YY	N26
2	IO_L99N_YY	P28
2	IO_L100P	P29
2	IO_L100N	N24
2	IO_L101P_YY	P22
2	IO_L101N_YY	R26
2	IO_VREF_L102P_YY	P25
2	IO_L102N_YY	R29
2	IO_L103P_YY	R21[4]
2	IO_L103N_YY	R28[3]
2	IO_VREF_L104P_YY	R25[2]
2	IO_L104N_YY	T30
2	IO_L105P_YY	P24[4]
2	IO_L105N_YY	R27[3]
2	IO_L106P	R24
3	IO	T22[4]
3	IO	T24[4]
3	IO	T26[4]
3	IO	T29[4]
3	IO	U26[5]
3	IO	V23[4]
3	IO	V25[4]
3	IO	V30[5]
3	IO	Y21[4]
3	IO	AA26[4]
3	IO	AA23[4]
3	IO	AB27[4]
3	IO	AB29[4]
3	IO	AC28[5]
3	IO	AD26[4]
3	IO	AD29[5]
3	IO	AE27[5]
3	IO_L106N	U29
3	IO_L107P_YY	R22
3	IO_VREF_L107N_YY	T27[2]
3	IO_L108P_YY	R23
3	IO_L108N_YY	T28
3	IO_L109P_YY	T21
3	IO_VREF_L109N_YY	T25
3	IO_L110P_YY	U28
3	IO_L110N_YY	U30
3	IO_L111P	T23
3	IO_L111N	U27
3	IO_L112P_YY	U25
3	IO_L112N_YY	V27
3	IO_D4_L113P_YY	U24
3	IO_VREF_L113N_YY	V29
3	IO_L114P	W30
3	IO_L114N	U22
3	IO_L115P_YY	U21
3	IO_L115N_YY	W29
3	IO_L116P_YY	V26
3	IO_L116N_YY	W27
3	IO_L117P	W26
3	IO_VREF_L117N	Y29[1]
3	IO_L118P_YY	W25
3	IO_L118N_YY	Y30
3	IO_L119P_Y	V24[4]
3	IO_L119N_Y	Y28[4]
3	IO_L120P_YY	AA30
3	IO_L120N_YY	W24
3	IO_L121P	AA29
3	IO_L121N	V20
3	IO_L122P	Y27[4]
3	IO_L122N	W23[4]
3	IO_L123P_YY	Y26
3	IO_D5_L123N_YY	AB30
3	IO_D6_L124P_YY	V21
3	IO_VREF_L124N_YY	AA28
3	IO_L125P_YY	Y25
3	IO_L125N_YY	AA27
3	IO_L126P_YY	W22
3	IO_L126N_YY	Y23

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
7	IO_L275N_YY	G3
7	IO_L275P_YY	E1
7	IO_L276N_YY	H6
7	IO_L276P_YY	E2
7	IO_L277N	E4
7	IO_VREF_L277P	K9
7	IO_L278N_YY	J8
7	IO_L278P_YY	F4
7	IO_L279N_Y	D1[3]
7	IO_L279P_Y	H7[4]
7	IO_L280N_YY	G6
7	IO_VREF_L280P_YY	C2[1]
7	IO_L281N	D2
7	IO_L281P	F5
7	IO_L282N_YY	D3[4]
7	IO_L282P_YY	K10[3]
2	CCLK	F26
3	DONE	AJ28
NA	DXN	AJ3
NA	DXP	AH4
NA	M0	AF4
NA	M1	AC7
NA	M2	AK3
NA	PROGRAM	AG28
NA	TCK	B3
NA	TDI	H22
2	TDO	D26
NA	TMS	C1
NA	VCCINT	L11
NA	VCCINT	L12
NA	VCCINT	L19
NA	VCCINT	L20
NA	VCCINT	M11
NA	VCCINT	M12
NA	VCCINT	M19

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
NA	VCCINT	M20
NA	VCCINT	N13
NA	VCCINT	N14
NA	VCCINT	N15
NA	VCCINT	N16
NA	VCCINT	N17
NA	VCCINT	N18
NA	VCCINT	P13
NA	VCCINT	P18
NA	VCCINT	R13
NA	VCCINT	R18
NA	VCCINT	T13
NA	VCCINT	T18
NA	VCCINT	U13
NA	VCCINT	U18
NA	VCCINT	V13
NA	VCCINT	V14
NA	VCCINT	V15
NA	VCCINT	V16
NA	VCCINT	V17
NA	VCCINT	V18
NA	VCCINT	W11
NA	VCCINT	W12
NA	VCCINT	W19
NA	VCCINT	W20
NA	VCCINT	Y11
NA	VCCINT	Y12
NA	VCCINT	Y19
NA	VCCINT	Y20
NA	VCCO_0	B6
NA	VCCO_0	M15
NA	VCCO_0	M14
NA	VCCO_0	L15
NA	VCCO_0	L14
NA	VCCO_0	H14
NA	VCCO_0	M13

FG900 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 27: **FG900 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
GCLK LVDS					
3	0	C15	A15	NA	IO_DLL_ 34N
2	1	E15	E16	NA	IO_DLL_ 34P
1	5	AK16	AH16	NA	IO_DLL_ 177N
0	4	AJ16	AF16	NA	IO_DLL_ 177P
IO LVDS Total Pairs: 283, Asynchronous Output Pairs: 168					
0	0	F7	C4	4	-
1	0	G8	D5	2	-
2	0	H9	A3	2	VREF
3	0	J10	B4	2	-
4	0	D6	A4	√	-
5	0	B5	E7	√	VREF
6	0	F8	A5	1	-
7	0	N11	D7	1	-
8	0	E8	G9	√	-
9	0	J11	A6	√	VREF
10	0	B7	C7	2	-
11	0	H10	C8	2	-
12	0	F10	G10	√	-
13	0	H11	A8	√	VREF
14	0	C9	D9	NA	-
15	0	J12	B9	4	-
16	0	A9	E10	NA	VREF
17	0	B10	G11	NA	-
18	0	C10	H12	4	-
19	0	F11	H13	2	-
20	0	D11	E11	2	-
21	0	G12	B11	2	-
22	0	C11	F12	√	-
23	0	D12	A10	√	VREF
24	0	A11	E12	1	-
25	0	B12	G13	1	-
26	0	K13	A12	√	-
27	0	B13	F13	√	VREF
28	0	E13	G14	2	-
29	0	B14	D14	2	-
30	0	J14	A14	√	-
31	0	J15	K14	√	VREF
32	0	H15	B15	NA	-
33	0	D15	F15	√	VREF
34	1	E16	A15	NA	IO_ LVDS_DLL
35	1	F16	B16	4	VREF
36	1	H16	A16	4	-
37	1	K15	C16	√	VREF
38	1	G16	K16	√	-
39	1	E17	A17	2	-
40	1	C17	F17	2	-
41	1	A18	E18	√	VREF
42	1	A19	D18	√	-
43	1	G18	B19	1	-
44	1	H18	D19	1	-
45	1	F19	F18	√	VREF
46	1	K17	B20	√	-
47	1	A20	D20	2	-
48	1	C20	G19	2	-
49	1	E20	K18	2	-
50	1	D21	B21	4	-
51	1	A21	F20	√	-

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
6	IO_VREF_L299N_YY	W5
6	IO_L299P_YY	V1
6	IO_L300N_YY	V7
6	IO_L300P_YY	U2
6	IO_VREF_L301N_Y	V6[1]
6	IO_L301P_Y	U1
7	IO	F5
7	IO	G6[3]
7	IO	H1
7	IO	H7[3]
7	IO	K2[3]
7	IO	K4[3]
7	IO	L6[3]
7	IO	M5[3]
7	IO	M10[3]
7	IO	N5[3]
7	IO	N10
7	IO	R7[4]
7	IO	T2
7	IO	T7[3]
7	IO	U8
7	IO	V4[3]
7	IO_L302N_YY	U9
7	IO_L302P_YY	U4
7	IO_L303N_Y	U7
7	IO_VREF_L303P_Y	U5[1]
7	IO_L304N_YY	U3
7	IO_L304P_YY	U6
7	IO_L305N_YY	T3
7	IO_VREF_L305P_YY	T6
7	IO_L306N_Y	T9
7	IO_L306P_Y	T4
7	IO_L307N_Y	T5[5]

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
7	IO_L307P_Y	R1[4]
7	IO_L308N_Y	R6
7	IO_L308P_Y	T10
7	IO_L309N_YY	R2
7	IO_L309P_YY	R5
7	IO_L310N_YY	P1
7	IO_VREF_L310P_YY	P5
7	IO_L311N_Y	R8
7	IO_L311P_Y	P2
7	IO_L312N_Y	R9[5]
7	IO_L312P_Y	N1[4]
7	IO_L313N_Y	P4
7	IO_L313P_Y	R10
7	IO_L314N_YY	P8
7	IO_L314P_YY	N2
7	IO_L315N_YY	P6[5]
7	IO_L315P_YY	P7[4]
7	IO_L316N_Y	M1
7	IO_VREF_L316P_Y	N4
7	IO_L317N_Y	N6
7	IO_L317P_Y	N3
7	IO_L318N	P9
7	IO_L318P	M2
7	IO_L319N_Y	N7
7	IO_L319P_Y	M3
7	IO_L320N_Y	P10
7	IO_L320P_Y	M4
7	IO_L321N_Y	L1
7	IO_L321P_Y	N8
7	IO_L322N_YY	L2
7	IO_L322P_YY	N9
7	IO_L323N_YY	M7
7	IO_VREF_L323P_YY	K1
7	IO_L324N_Y	M8