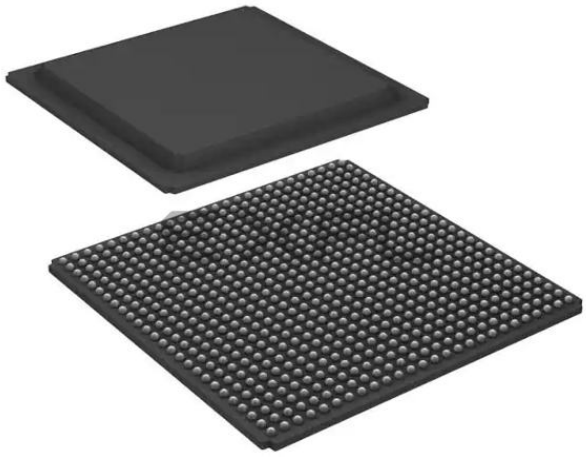

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3456
Number of Logic Elements/Cells	15552
Total RAM Bits	294912
Number of I/O	444
Number of Gates	985882
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv600e-7fg676c

resources. The abundance of routing resources permits the Virtex-E family to accommodate even the largest and most complex designs.

Virtex-E FPGAs are SRAM-based, and are customized by loading configuration data into internal memory cells. Configuration data can be read from an external SPROM (master serial mode), or can be written into the FPGA (SelectMAP™, slave serial, and JTAG modes).

The standard Xilinx Foundation Series™ and Alliance Series™ Development systems deliver complete design support for Virtex-E, covering every aspect from behavioral and schematic entry, through simulation, automatic design translation and implementation, to the creation and downloading of a configuration bit stream.

Higher Performance

Virtex-E devices provide better performance than previous generations of FPGAs. Designs can achieve synchronous system clock rates up to 240 MHz including I/O or 622 Mb/s using Source Synchronous data transmission architectures. Virtex-E I/Os comply fully with 3.3 V PCI specifications, and interfaces can be implemented that operate at 33 MHz or 66 MHz.

While performance is design-dependent, many designs operate internally at speeds in excess of 133 MHz and can achieve over 311 MHz. Table 2 shows performance data for representative circuits, using worst-case timing parameters.

Table 2: **Performance for Common Circuit Functions**

Function	Bits	Virtex-E (-7)
Register-to-Register		
Adder	16 64	4.3 ns 6.3 ns
Pipelined Multiplier	8 x 8 16 x 16	4.4 ns 5.1 ns
Address Decoder	16 64	3.8 ns 5.5 ns
16:1 Multiplexer		4.6 ns
Parity Tree	9 18 36	3.5 ns 4.3 ns 5.9 ns
Chip-to-Chip		
HSTL Class IV		
LVTTL,16mA, fast slew		
LVDS		
LVPECL		

Virtex-E Device/Package Combinations and Maximum I/O

Table 3: **Virtex-E Family Maximum User I/O by Device/Package (Excluding Dedicated Clock Pins)**

	XCV 50E	XCV 100E	XCV 200E	XCV 300E	XCV 400E	XCV 600E	XCV 1000E	XCV 1600E	XCV 2000E	XCV 2600E	XCV 3200E
CS144	94	94	94								
PQ240	158	158	158	158	158						
HQ240						158	158				
BG352		196	260	260							
BG432				316	316	316					
BG560					404	404	404	404	404		
FG256	176	176	176	176							
FG456			284	312							
FG676					404	444					
FG680						512	512	512	512		
FG860							660	660	660		
FG900						512	660	700			
FG1156							660	724	804	804	804

DLL Properties

Properties provide access to some of the Virtex-E series DLL features, (for example, clock division and duty cycle correction).

Duty Cycle Correction Property

The 1x clock outputs, CLK0, CLK90, CLK180, and CLK270, use the duty-cycle corrected default, exhibiting a 50/50 duty cycle. The DUTY_CYCLE_CORRECTION property (by default TRUE) controls this feature. To deactivate the DLL duty-cycle correction for the 1x clock outputs, attach the DUTY_CYCLE_CORRECTION=FALSE property to the DLL symbol.

Clock Divide Property

The CLKDV_DIVIDE property specifies how the signal on the CLKDV pin is frequency divided with respect to the CLK0 pin. The values allowed for this property are 1.5, 2, 2.5, 3, 4, 5, 8, or 16; the default value is 2.

Startup Delay Property

This property, STARTUP_WAIT, takes on a value of TRUE or FALSE (the default value). When TRUE the device configuration DONE signal waits until the DLL locks before going to High.

Virtex-E DLL Location Constraints

As shown in Figure 26, there are four additional DLLs in the Virtex-E devices, for a total of eight per Virtex-E device. These DLLs are located in silicon, at the top and bottom of the two innermost block SelectRAM columns. The location constraint LOC, attached to the DLL symbol with the identifier DLL0S, DLL0P, DLL1S, DLL1P, DLL2S, DLL2P, DLL3S, or DLL3P, controls the DLL location.

The LOC property uses the following form:

LOC = DLL0P

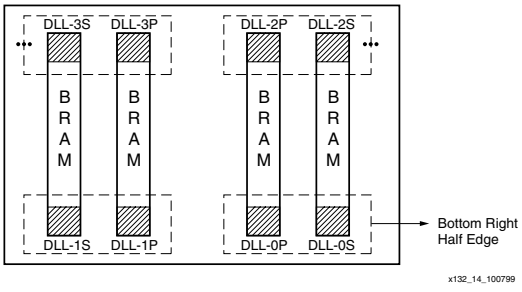

Figure 26: **Virtex Series DLLs**

Design Factors

Use the following design considerations to avoid pitfalls and improve success designing with Xilinx devices.

Input Clock

The output clock signal of a DLL, essentially a delayed version of the input clock signal, reflects any instability on the input clock in the output waveform. For this reason the quality of the DLL input clock relates directly to the quality of the output clock waveforms generated by the DLL. The DLL input clock requirements are specified in the data sheet.

In most systems a crystal oscillator generates the system clock. The DLL can be used with any commercially available quartz crystal oscillator. For example, most crystal oscillators produce an output waveform with a frequency tolerance of 100 PPM, meaning 0.01 percent change in the clock period. The DLL operates reliably on an input waveform with a frequency drift of up to 1 ns — orders of magnitude in excess of that needed to support any crystal oscillator in the industry. However, the cycle-to-cycle jitter must be kept to less than 300 ps in the low frequencies and 150 ps for the high frequencies.

Input Clock Changes

Changing the period of the input clock beyond the maximum drift amount requires a manual reset of the CLKDLL. Failure to reset the DLL produces an unreliable lock signal and output clock.

It is possible to stop the input clock with little impact to the DLL. Stopping the clock should be limited to less than 100 µs to keep device cooling to a minimum. The clock should be stopped during a Low phase, and when restored the full High period should be seen. During this time, LOCKED stays High and remains High when the clock is restored.

When the clock is stopped, one to four more clocks are still observed as the delay line is flushed. When the clock is restarted, the output clocks are not observed for one to four clocks as the delay line is filled. The most common case is two or three clocks.

In a similar manner, a phase shift of the input clock is also possible. The phase shift propagates to the output one to four clocks after the original shift, with no disruption to the CLKDLL control.

Output Clocks

As mentioned earlier in the DLL pin descriptions, some restrictions apply regarding the connectivity of the output pins. The DLL clock outputs can drive an OBUF, a global clock buffer BUFG, or they can route directly to destination clock pins. The only BUFGs that the DLL clock outputs can drive are the two on the same edge of the device (top or bottom). In addition, the CLK2X output of the secondary DLL can connect directly to the CLKIN of the primary DLL in the same quadrant.

Do not use the DLL output clock signals until after activation of the LOCKED signal. Prior to the activation of the LOCKED signal, the DLL output clocks are not valid and can exhibit glitches, spikes, or other spurious movement.

standard requires a Differential Amplifier input buffer and a Push-Pull output buffer.

SSTL3 — Stub Series Terminated Logic for 3.3V

The Stub Series Terminated Logic for 3.3V, or SSTL3 standard is a general purpose 3.3V memory bus standard also sponsored by Hitachi and IBM (JESD8-8). This standard has two classes, I and II. SelectI/O devices support both classes for the SSTL3 standard. This standard requires a Differential Amplifier input buffer and an Push-Pull output buffer.

SSTL2 — Stub Series Terminated Logic for 2.5V

The Stub Series Terminated Logic for 2.5V, or SSTL2 standard is a general purpose 2.5V memory bus standard sponsored by Hitachi and IBM (JESD8-9). This standard has two classes, I and II. SelectI/O devices support both classes for the SSTL2 standard. This standard requires a Differential Amplifier input buffer and an Push-Pull output buffer.

CTT — Center Tap Terminated

The Center Tap Terminated, or CTT standard is a 3.3V memory bus standard sponsored by Fujitsu (JESD8-4). This standard requires a Differential Amplifier input buffer and a Push-Pull output buffer.

AGP-2X — Advanced Graphics Port

The Intel AGP standard is a 3.3V Advanced Graphics Port-2X bus standard used with the Pentium II processor for graphics applications. This standard requires a Push-Pull output buffer and a Differential Amplifier input buffer.

LVDS — Low Voltage Differential Signal

LVDS is a differential I/O standard. It requires that one data bit is carried through two signal lines. As with all differential signaling standards, LVDS has an inherent noise immunity over single-ended I/O standards. The voltage swing between two signal lines is approximately 350mV. The use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}) is not required. LVDS requires the use of two pins per input or output. LVDS requires external resistor termination.

BLVDS — Bus LVDS

This standard allows for bidirectional LVDS communication between two or more devices. The external resistor termination is different than the one for standard LVDS.

LVPECL — Low Voltage Positive Emitter Coupled Logic

LVPECL is another differential I/O standard. It requires two signal lines for transmitting one data bit. This standard specifies two pins per input or output. The voltage swing between these two signal lines is approximately 850 mV. The use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}) is not required. The LVPECL standard requires external resistor termination.

Library Symbols

The Xilinx library includes an extensive list of symbols designed to provide support for the variety of SelectI/O features. Most of these symbols represent variations of the five generic SelectI/O symbols.

- IBUF (input buffer)
- IBUFG (global clock input buffer)
- OBUF (output buffer)
- OBUFT (3-state output buffer)
- IOBUF (input/output buffer)

IBUF

Signals used as inputs to the Virtex-E device must source an input buffer (IBUF) via an external input port. The generic Virtex-E IBUF symbol appears in Figure 37. The extension

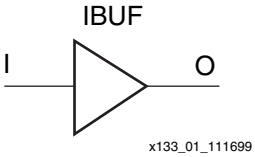

Figure 37: **Input Buffer (IBUF) Symbols**

to the base name defines which I/O standard the IBUF uses. The assumed standard is LVTTL when the generic IBUF has no specified extension.

The following list details the variations of the IBUF symbol:

- IBUF
- IBUF_LVCMOS2
- IBUF_PCI33_3
- IBUF_PCI66_3
- IBUF_GTL
- IBUF_GTLP
- IBUF_HSTL_I
- IBUF_HSTL_III
- IBUF_HSTL_IV
- IBUF_SSTL3_I
- IBUF_SSTL3_II
- IBUF_SSTL2_I
- IBUF_SSTL2_II
- IBUF_CTT
- IBUF_AGP
- IBUF_LVCMOS18
- IBUF_LVDS
- IBUF_LVPECL

When the IBUF symbol supports an I/O standard that requires a V_{REF}, the IBUF automatically configures as a differential amplifier input buffer. The V_{REF} voltage must be supplied on the V_{REF} pins. In the case of LVDS, LVPECL, and BLVDS, V_{REF} is not required.

The voltage reference signal is “banked” within the Virtex-E device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 38 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

IBUF placement restrictions require that any differential amplifier input signals within a bank be of the same standard. How to specify a specific location for the IBUF via the LOC property is described below. Table 19 summarizes the Virtex-E input standards compatibility requirements.

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element by default activates to ensure a zero hold-time requirement. The NODELAY=TRUE property overrides this default.

When the IBUF does not drive a flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

Table 19: **Xilinx Input Standards Compatibility Requirements**

Rule 1	Standards with the same input V_{CCO}, output V_{CCO}, and V_{REF} can be placed within the same bank.

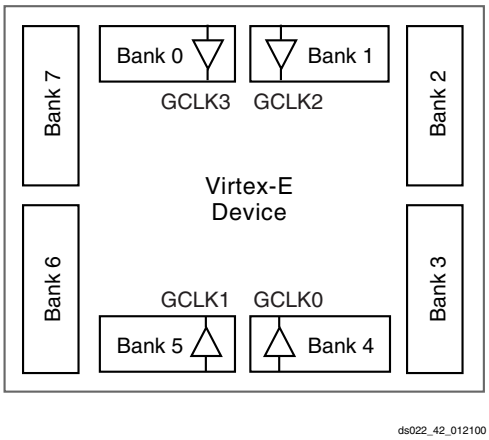

Figure 38: **Virtex-E I/O Banks**

IBUFG

Signals used as high fanout clock inputs to the Virtex-E device should drive a global clock input buffer (IBUFG) via an external input port in order to take advantage of one of the four dedicated global clock distribution networks. The output of the IBUFG should only drive a CLKDLL, CLKDLLHF, or BUFG symbol. The generic Virtex-E IBUFG symbol appears in Figure 39.

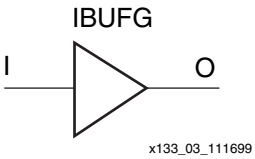

Figure 39: **Virtex-E Global Clock Input Buffer (IBUFG) Symbol**

The extension to the base name determines which I/O standard is used by the IBUFG. With no extension specified for the generic IBUFG symbol, the assumed standard is LVTTL.

The following list details variations of the IBUFG symbol.

- IBUFG
- IBUFG_LVCMOS2
- IBUFG_PCI33_3
- IBUFG_PCI66_3
- IBUFG_GTL
- IBUFG_GTLP
- IBUFG_HSTL_I
- IBUFG_HSTL_III
- IBUFG_HSTL_IV
- IBUFG_SSTL3_I
- IBUFG_SSTL3_II
- IBUFG_SSTL2_I
- IBUFG_SSTL2_II
- IBUFG_CTT
- IBUFG_AGP
- IBUFG_LVCMOS18
- IBUFG_LVDS
- IBUFG_LVPECL

When the IBUFG symbol supports an I/O standard that requires a differential amplifier input, the IBUFG automatically configures as a differential amplifier input buffer. The low-voltage I/O standards with a differential amplifier input require an external reference voltage input V_{REF}.

The voltage reference signal is “banked” within the Virtex-E device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 38 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

IBUFG placement restrictions require any differential amplifier input signals within a bank be of the same standard. The LOC property can specify a location for the IBUFG.

As an added convenience, the BUFGP can be used to instantiate a high fanout clock input. The BUFGP symbol

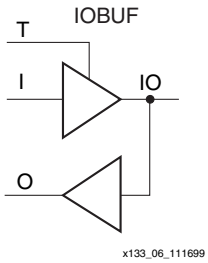

Figure 42: **Input/Output Buffer Symbol (IOBUF)**

The following list details variations of the IOBUF symbol.

- IOBUF
- IOBUF_S_2
- IOBUF_S_4
- IOBUF_S_6
- IOBUF_S_8
- IOBUF_S_12
- IOBUF_S_16
- IOBUF_S_24
- IOBUF_F_2
- IOBUF_F_4
- IOBUF_F_6
- IOBUF_F_8
- IOBUF_F_12
- IOBUF_F_16
- IOBUF_F_24
- IOBUF_LVCMOS2
- IOBUF_PCI33_3
- IOBUF_PCI66_3
- IOBUF_GTL
- IOBUF_GTLP
- IOBUF_HSTL_I
- IOBUF_HSTL_III
- IOBUF_HSTL_IV
- IOBUF_SSTL3_I
- IOBUF_SSTL3_II
- IOBUF_SSTL2_I
- IOBUF_SSTL2_II
- IOBUF_CTT
- IOBUF_AGP
- IOBUF_LVCMOS18
- IOBUF_LVDS
- IOBUF_LVPECL

When the IOBUF symbol used supports an I/O standard that requires a differential amplifier input, the IOBUF automatically configures with a differential amplifier input buffer.

The low-voltage I/O standards with a differential amplifier input require an external reference voltage input V_{REF}.

The voltage reference signal is “banked” within the Virtex-E device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 38, page 34 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

IOBUF placement restrictions require any differential amplifier input signals within a bank be of the same standard.

The Virtex-E series supports eight banks for the HQ and PQ packages. The CS package supports four V_{CCO} banks.

Additional restrictions on the Virtex-E SelectI/O IOBUF placement require that within a given V_{CCO} bank each IOBUF must share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within the same V_{CCO} bank. The LOC property can specify a location for the IOBUF.

An optional delay element is associated with the input path in each IOBUF. When the IOBUF drives an input flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Override this default with the NODELAY=TRUE property.

In the case when the IOBUF does not drive an input flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak “keeper” circuit. Control this feature by adding the appropriate symbol to the output net of the IOBUF (PULLUP, PULLDOWN, or KEEPER).

SelectI/O Properties

Access to some of the SelectI/O features (for example, location constraints, input delay, output drive strength, and slew rate) is available through properties associated with these features.

Input Delay Properties

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Use the NODELAY=TRUE property to override this default.

In the case when the IBUF does not drive a flip-flop within the IOB, the delay element by default de-activates to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

The register elements can be packed in the IOB using the IOB property to TRUE on the register or by using the “map -pr [i|o|b]” where “i” is inputs only, “o” is outputs only and “b” is both inputs and outputs.

To improve design coding times VHDL and Verilog synthesis macro libraries have been developed to explicitly create these structures. The input library macros are listed below. The 3-state is configured to be 3-stated at GSR and when the PRE,CLR,S or R is asserted and shares it's clock enable with the output register. If this is not desirable then the library can be updated by the user for the desired functionality. The O and OB inputs to the macros are the external net connections.

Creating a LVDS Bidirectional Buffer

LVDS bidirectional buffers can be placed in a wide number of IOB locations. The exact locations are dependent on the package used. The Virtex-E package information lists the possible locations as IO_L#P for the P-side and IO_L#N for the N-side, where # is the pair number.

HDL Instantiation

Both bidirectional buffers are required to be instantiated in the design and placed on the correct IO_L#P and IO_L#N locations. The IOB must have the same net source the following pins, clock (C), set/reset (SR), 3-state (T), 3-state clock enable (TCE), output (O), output clock enable (OCE). In addition, the output (O) pins must be inverted with respect to each other, and if output registers are used, the INIT states must be opposite values (one HIGH and one LOW). If 3-state registers are used, they must be initialized to the same state. Failure to follow these rules leads to DRC errors in the software.

VHDL Instantiation

```
data0_p:   IOBUF_LVDS port map
(I=>data_out(0), T=>data_tri,
IO=>data_p(0), O=>data_int(0));

data0_inv: INV        port map
(I=>data_out(0),   O=>data_n_out(0));

data0_n  : IOBUF_LVDS port map
(I=>data_n_out(0), T=>data_tri,
IO=>data_n(0), O=>open);
```

Verilog Instantiation

```
IOBUF_LVDS data0_p(.I(data_out[0]),
.T(data_tri), .IO(data_p[0]),
.O(data_int[0]);

INV        data0_inv (.I(data_out[0],
.O(data_n_out[0]);

IOBUF_LVDS
data0_n(.I(data_n_out[0]),.T(data_tri),.
IO(data_n[0]).O());
```

Location Constraints

All LVDS buffers must be explicitly placed on a device. For the output buffers this can be done with the following constraint in the .ucf or .ncf file.

```
NET data_p<0> LOC = D28; # IO_L0P

NET data_n<0> LOC = B29; # IO_L0N
```

Synchronous vs. Asynchronous Bidirectional Buffers

If the output side of the bidirectional buffers are synchronous (registered in the IOB), then any IO_L#PIN pair can be used. If the output side of the bidirectional buffers are asynchronous (no output register), then they must use one of the pairs that is a part of the asynchronous LVDS IOB group. This applies for either the 3-state pin or the data out pin.

The LVDS pairs that can be used as asynchronous bidirectional buffers are listed in the Virtex-E pinout tables. Some pairs are marked as asynchronous capable for all devices in that package, and others are marked as available only for that device in the package. If the device size might change at some point in the product’s lifetime, then only the common pairs for all packages should be used.

Adding Output and 3-State Registers

All LVDS buffers can have an output and input registers in the IOB. The output registers must be in both the P-side and N-side IOBs, the input register is only in the P-side. All the normal IOB register options are available (FD, FDE, FDC, FDCE, FDP, FDPE, FDR, FDRE, FDS, FDSE, LD, LDE, LDC, LDCE, LDP, LDPE). The register elements can be inferred or explicitly instantiated in the HDL code. Special care must be taken to insure that the D pins of the registers are inverted and that the INIT states of the registers are opposite. The 3-state (T), 3-state clock enable (CE), clock pin (C), output clock enable (CE), and set/reset (CLR/PRE or S/R) pins must connect to the same source. Failure to do this leads to a DRC error in the software.

The register elements can be packed in the IOB using the IOB property to TRUE on the register or by using the “map -pr [i|o|b]” where “i” is inputs only, “o” is outputs only and “b” is both inputs and outputs. To improve design coding times VHDL and Verilog synthesis macro libraries have been developed to explicitly create these structures. The bidirectional I/O library macros are listed in Table 44. The 3-state is configured to be 3-stated at GSR and when the PRE,CLR,S or R is asserted and shares its clock enable with the output and input register. If this is not desirable then the library can be updated be the user for the desired functionality. The I/O and IOB inputs to the macros are the external net connections.

IOB Input Switching Characteristics Standard Adjustments

Description	Symbol	Standard	Speed Grade(1)				Units
			Min	-8	-7	-6	
Data Input Delay Adjustments							
Standard-specific data input delay adjustments	T_{ILVTTL}	LVTTL	0.0	0.0	0.0	0.0	ns
	$T_{ILVCMOS2}$	LVCMOS2	–0.02	0.0	0.0	0.0	ns
	$T_{ILVCMOS18}$	LVCMOS18	0.12	+0.20	+0.20	+0.20	ns
	T_{ILVDS}	LVDS	0.00	+0.15	+0.15	+0.15	ns
	$T_{ILVPECL}$	LVPECL	0.00	+0.15	+0.15	+0.15	ns
	T_{IPCI33_3}	PCI, 33 MHz, 3.3 V	–0.05	+0.08	+0.08	+0.08	ns
	T_{IPCI66_3}	PCI, 66 MHz, 3.3 V	–0.05	–0.11	–0.11	–0.11	ns
	T_{IGTL}	GTL	+0.10	+0.14	+0.14	+0.14	ns
	$T_{IGTLPLUS}$	GTL+	+0.06	+0.14	+0.14	+0.14	ns
	T_{IHSTL}	HSTL	+0.02	+0.04	+0.04	+0.04	ns
	T_{ISSTL2}	SSTL2	–0.04	+0.04	+0.04	+0.04	ns
	T_{ISSTL3}	SSTL3	–0.02	+0.04	+0.04	+0.04	ns
	T_{ICTT}	CTT	+0.01	+0.10	+0.10	+0.10	ns
	T_{IAGP}	AGP	–0.03	+0.04	+0.04	+0.04	ns

Notes:
1. Input timing i for LVTTL is measured at 1.4 V. For other I/O standards, see Table 4.

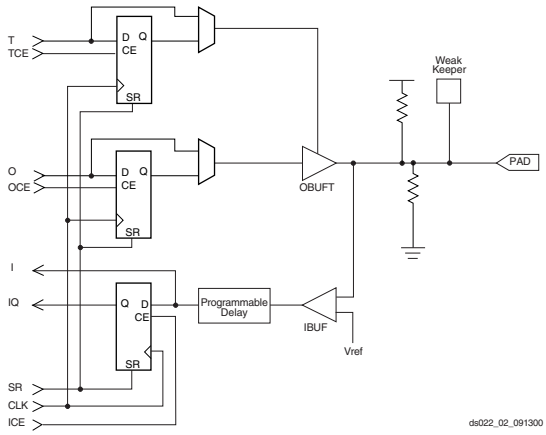

Figure 1: **Virtex-E Input/Output Block (IOB)**

Clock Distribution Switching Characteristics

Description	Symbol	Speed Grade				Units
		Min	-8	-7	-6	
GCLK IOB and Buffer						
Global Clock PAD to output.	T_{GPIO}	0.38	0.7	0.7	0.7	ns, max
Global Clock Buffer I input to O output	T_{GIO}	0.11	0.20	0.45	0.50	ns, max

I/O Standard Global Clock Input Adjustments

Description	Symbol[1]	Standard	Speed Grade				Units
			Min	-8	-7	-6	
Data Input Delay Adjustments							
Standard-specific global clock input delay adjustments	$T_{GPLVTTL}$	LVTTL	0.0	0.0	0.0	0.0	ns, max
	$T_{GPLVCMOS2}$	LVCMOS2	–0.02	0.0	0.0	0.0	ns, max
	$T_{GPLVCMOS18}$	LVCMOS18	0.12	0.20	0.20	0.20	ns, max
	T_{GLVDS}	LVDS	0.23	0.38	0.38	0.38	ns, max
	$T_{GLVPECL}$	LVPECL	0.23	0.38	0.38	0.38	ns, max
	$T_{GPPCI33\_3}$	PCI, 33 MHz, 3.3 V	–0.05	0.08	0.08	0.08	ns, max
	$T_{GPPCI66\_3}$	PCI, 66 MHz, 3.3 V	–0.05	–0.11	–0.11	–0.11	ns, max
	T_{GPGTL}	GTL	0.20	0.37	0.37	0.37	ns, max
	T_{GPGTLP}	GTL+	0.20	0.37	0.37	0.37	ns, max
	T_{GPHSTL}	HSTL	0.18	0.27	0.27	0.27	ns, max
	$T_{GPSSTL2}$	SSTL2	0.21	0.27	0.27	0.27	ns, max
	$T_{GPSSTL3}$	SSTL3	0.18	0.27	0.27	0.27	ns, max
	T_{GPCTT}	CTT	0.22	0.33	0.33	0.33	ns, max
	T_{GPAGP}	AGP	0.21	0.27	0.27	0.27	ns, max

Notes:
1. Input timing for GPLVTTL is measured at 1.4 V. For other I/O standards, see Table 4.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/7/99	1.0	Initial Xilinx release.
1/10/00	1.1	Re-released with spd.txt v. 1.18, FG860/900/1156 package information, and additional DLL, Select RAM and SelectI/O information.
1/28/00	1.2	Added Delay Measurement Methodology table, updated SelectI/O section, Figures 30, 54, & 55, text explaining Table 5, T_{BYP} values, buffered Hex Line info, p. 8, I/O Timing Measurement notes, notes for Tables 15, 16, and corrected F1156 pinout table footnote references.
2/29/00	1.3	Updated pinout tables, V_{CC} page 20, and corrected Figure 20.
5/23/00	1.4	Correction to table on p. 22.
7/10/00	1.5	• Numerous minor edits. • Data sheet upgraded to Preliminary. • Preview -8 numbers added to **Virtex-E Electrical Characteristics** tables.
8/1/00	1.6	• Reformatted entire document to follow new style guidelines. • Changed speed grade values in tables on pages 35-37.
9/20/00	1.7	• Min values added to **Virtex-E Electrical Characteristics** tables. • XCV2600E and XCV3200E numbers added to **Virtex-E Electrical Characteristics** tables (Module 3). • Corrected user I/O count for XCV100E device in Table 1 (Module 1). • Changed several pins to “No Connect in the XCV100E“ and removed duplicate V_{CCINT} pins in Table ~ (Module 4). • Changed pin J10 to “No connect in XCV600E” in Table 74 (Module 4). • Changed pin J30 to “VREF option only in the XCV600E” in Table 74 (Module 4). • Corrected pair 18 in Table 75 (Module 4) to be “AO in the XCV1000E, XCV1600E“.
11/20/00	1.8	• Upgraded speed grade -8 numbers in **Virtex-E Electrical Characteristics** tables to Preliminary. • Updated minimums in Table 13 and added notes to Table 14. • Added to note 2 to **Absolute Maximum Ratings**. • Changed speed grade -8 numbers for $T_{SHCKO32}$, T_{REG}, T_{BCCS}, and T_{ICKOF} • Changed all minimum hold times to –0.4 under **Global Clock Set-Up and Hold for LVTTL Standard, with DLL**. • Revised maximum T_{DLLPW} in -6 speed grade for **DLL Timing Parameters**. • Changed GCLK0 to BA22 for FG860 package in Table 46.
2/12/01	1.9	• Revised footnote for Table 14. • Added numbers to **Virtex-E Electrical Characteristics** tables for XCV1000E and XCV2000E devices. • Updated Table 27 and Table 78 to include values for XCV400E and XCV600E devices. • Revised Table 62 to include pinout information for the XCV400E and XCV600E devices in the BG560 package. • Updated footnotes 1 and 2 for Table 76 to include XCV2600E and XCV3200E devices.
4/02/01	2.0	• Updated numerous values in **Virtex-E Switching Characteristics** tables. • Converted data sheet to modularized format. See the **Virtex-E Data Sheet** section.
4/19/01	2.1	• Updated values in **Virtex-E Switching Characteristics** tables.

CS144 Chip-Scale Package

XCV50E, XCV100E, XCV200E, XCV300E and XCV400E devices in CS144 Chip-scale packages have footprint compatibility. In the CS144 package, bank pairs that share a side are internally interconnected, permitting four choices for V_{CCO}. See Table 3.

Table 3: **I/O Bank Pairs and Shared Vcco Pins**

Paired Banks	Shared V_{CCO} Pins
Banks 0 & 1	A2, A13, D7
Banks 2 & 3	B12, G11, M13
Banks 4 & 5	N1, N7, N13
Banks 6 & 7	B2, G2, M2

Pins labeled I0_VREF can be used as either in all parts unless device-dependent, as indicated in the footnotes. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 4, see Table 5 is Differential Pair information.

Table 4: **CS144 — XCV50E, XCV100E, XCV200E**

Bank	Pin Description	Pin #
0	GCK3	A6
0	IO	B3
0	IO_VREF_L0N_YY	B4[2]
0	IO_L0P_YY	A4
0	IO_L1N_YY	B5
0	IO_L1P_YY	A5
0	IO_LVDS_DLL_L2N	C6
0	IO_VREF	A3[1]
0	IO_VREF	C4
0	IO_VREF	D6
1	GCK2	A7
1	IO	A8
1	IO_LVDS_DLL_L2P	B7
1	IO_L3N_YY	C8
1	IO_L3P_YY	D8
1	IO_L4N_YY	C9
1	IO_VREF_L4P_YY	D9[2]
1	IO_WRITE_L5N_YY	C10
1	IO_CS_L5P_YY	D10
1	IO_VREF	A10
1	IO_VREF	B8
1	IO_VREF	B10[1]
2	IO	D12
2	IO	F12
2	IO_DOUT_BUSY_L6P_YY	C11
2	IO_DIN_D0_L6N_YY	C12
2	IO_D1_L7N	E10
2	IO_VREF_L7P	D13[2]
2	IO_L8N_YY	E13
2	IO_D2_L8P_YY	E12
2	IO_D3_L9N	F11
2	IO_VREF_L9P	F10
2	IO_L10P	F13
2	IO_VREF	C13[1]
2	IO_VREF	D11
3	IO	H13
3	IO	K13
3	IO_L10N	G13
3	IO_VREF_L11N	H11
3	IO_D4_L11P	H12
3	IO_D5_L12N_YY	J13
3	IO_L12P_YY	H10
3	IO_VREF_L13N	J10[2]
3	IO_D6_L13P	J11
3	IO_INIT_L14N_YY	L13
3	IO_D7_L14P_YY	K10
3	IO_VREF	K11[1]
3	IO_VREF	K12
4	GCK0	K7
4	IO	M8
4	IO	M10

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P66	IO_VREF_L46P	5
P65	IO_L46N	5
P64	IO_L47P_YY	5
P63	IO_L47N_YY	5
P62	M2	NA
P61	VCCO	5
P60	M0	NA
P59	GND	NA
P58	M1	NA
P57	IO_L48N_YY	6
P56	IO_L48P_YY	6
P55	VCCO	6
P54	IO_VREF	6
P53	IO_L49N_Y	6
P52	IO_L49P_Y	6
P51	GND	NA
P50	IO_VREF_L50N_Y	6
P49	IO_L50P_Y	6
P48	IO_VREF	6
P47	IO_VREF_L51N_Y	6
P46	IO_L51P_Y	6
P45	GND	NA
P44	VCCO	6
P43	VCCINT	NA
P42	IO_L52N_YY	6
P41	IO_L52P_YY	6
P40[1]	IO_VREF	6
P39	IO_L53N_Y	6
P38	IO_L53P_Y	6
P37	GND	NA
P36	IO_VREF_L54N_Y	6
P35	IO_L54P_Y	6
P34	IO_L55N_Y	6
P33	IO_VREF_L55P_Y	6
P32	VCCINT	NA
P31	IO	6

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P30	VCCO	6
P29	GND	NA
P28	IO_L56N_YY	7
P27	IO_L56P_YY	7
P26	IO_VREF	7
P25	VCCO	7
P24	IO_L57N_Y	7
P23	IO_VREF_L57P_Y	7
P22	GND	NA
P21	IO_L58N_Y	7
P20	IO_L58P_Y	7
P19[1]	IO_VREF	7
P18	IO_L59N_YY	7
P17	IO_L59P_YY	7
P16	VCCINT	NA
P15	VCCO	7
P14	GND	NA
P13	IO_L60N_Y	7
P12	IO_VREF_L60P_Y	7
P11	IO_VREF	7
P10	IO_L61N_Y	7
P9	IO_VREF_L61P_Y	7
P8	GND	NA
P7	IO_L62N_Y	7
P6	IO_L62P_Y	7
P5	IO_VREF_L63N_Y	7
P4	IO_L63P_Y	7
P3	IO	7
P2	TMS	NA
P1	GND	NA

Notes:
1. V_{REF} or I/O option only in the XCV1000E; otherwise, I/O option only.

Table 13: **BG432 Differential Pin Pair Summary XCV300E, XCV400E, XC600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
48	2	N1	P4	√	D3
49	2	P3	P2	4	-
50	2	R3	R4	1	VREF
51	2	R1	T3	√	-
52	3	U4	U2	1	VREF
53	3	U1	V3	4	-
54	3	V4	V2	√	VREF
55	3	W3	W4	1	-
56	3	Y1	Y3	1	-
57	3	Y4	Y2	4	-
58	3	AA3	AB1	√	D5
59	3	AB3	AB4	√	VREF
60	3	AD1	AC3	1	VREF
61	3	AC4	AD2	4	-
62	3	AD3	AD4	√	VREF
63	3	AF2	AE3	1	-
64	3	AE4	AG1	5	-
65	3	AG2	AF3	1	VREF
66	3	AF4	AH1	4	-
67	3	AH2	AG3	3	-
68	3	AG4	AJ2	√	INIT
69	4	AJ4	AK3	√	-
70	4	AH5	AK4	1	-
71	4	AJ5	AH6	√	-
72	4	AL4	AK5	√	VREF
73	4	AJ6	AH7	2	-
74	4	AL5	AK6	√	-
75	4	AJ7	AL6	√	VREF
76	4	AH9	AJ8	1	-
77	4	AK8	AJ9	1	VREF
78	4	AL8	AK9	√	VREF
79	4	AK10	AL10	√	-

Table 13: **BG432 Differential Pin Pair Summary XCV300E, XCV400E, XC600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
80	4	AH12	AK11	√	-
81	4	AJ12	AK12	√	-
82	4	AH13	AJ13	√	-
83	4	AL13	AK14	√	VREF
84	4	AH14	AJ14	1	-
85	4	AK15	AJ15	1	VREF
86	5	AH15	AL17	NA	IO_LVDS_DLL
87	5	AK17	AJ17	1	VREF
88	5	AH17	AK18	1	-
89	5	AL19	AJ18	√	VREF
90	5	AH18	AL20	√	-
91	5	AK20	AH19	√	-
92	5	AJ20	AK21	√	-
93	5	AJ21	AL22	√	-
94	5	AJ22	AK23	√	VREF
95	5	AH22	AL24	1	VREF
96	5	AK24	AH23	1	-
97	5	AK25	AJ25	√	VREF
98	5	AL26	AK26	√	-
99	5	AH25	AL27	2	-
100	5	AJ26	AK27	√	VREF
101	5	AH26	AL28	√	-
102	5	AJ27	AK28	1	-
103	6	AH30	AJ30	√	-
104	6	AH31	AG28	3	-
105	6	AG30	AG29	4	-
106	6	AG31	AF28	1	VREF
107	6	AF30	AF29	5	-
108	6	AF31	AE28	1	-
109	6	AD28	AE30	√	VREF
110	6	AD31	AD30	4	-
111	6	AC29	AC28	1	VREF

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
3	IO_D4_L73P_YY	W4	
3	IO_VREF_L73N_YY	W5	
3	IO_L74P_Y	Y3	
3	IO_L74N_Y	Y4	
3	IO_L75P_Y	AA1	
3	IO_L75N_Y	Y5	
3	IO_L76P_Y	AA3	
3	IO_VREF_L76N_Y	AA4	3
3	IO_L77P_Y	AB3	
3	IO_L77N_Y	AA5	
3	IO_L78P_Y	AC1	
3	IO_L78N_Y	AB4	
3	IO_L79P_YY	AC3	
3	IO_D5_L79N_YY	AB5	
3	IO_D6_L80P_YY	AC4	
3	IO_VREF_L80N_YY	AD3	
3	IO_L81P_Y	AE1	
3	IO_L81N_Y	AC5	
3	IO_L82P_Y	AD4	
3	IO_VREF_L82N_Y	AF1	4
3	IO_L83P_Y	AF2	
3	IO_L83N_Y	AD5	
3	IO_L84P_Y	AG2	
3	IO_VREF_L84N_Y	AE4	1
3	IO_L85P_YY	AH1	
3	IO_VREF_L85N_YY	AE5	
3	IO_L86P_Y	AF4	
3	IO_L86N_Y	AJ1	
3	IO_L87P_Y	AJ2	
3	IO_L87N_Y	AF5	
3	IO_L88P_Y	AG4	
3	IO_VREF_L88N_Y	AK2	
3	IO_L89P_Y	AJ3	
3	IO_L89N_Y	AG5	
3	IO_L90P_Y	AL1	

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
3	IO_VREF_L90N_Y	AH4	3
3	IO_D7_L91P_YY	AJ4	
3	IO_INIT_L91N_YY	AH5	
3	IO	U4	
4	GCK0	AL17	
4	IO	AJ8	
4	IO	AJ11	
4	IO	AK6	
4	IO	AK9	
4	IO_L92P_YY	AL4	
4	IO_L92N_YY	AJ6	
4	IO_L93P_Y	AK5	
4	IO_VREF_L93N_Y	AN3	3
4	IO_L94P_YY	AL5	
4	IO_L94N_YY	AJ7	
4	IO_VREF_L95P_YY	AM4	
4	IO_L95N_YY	AM5	
4	IO_L96P_Y	AK7	
4	IO_L96N_Y	AL6	
4	IO_L97P_YY	AM6	
4	IO_L97N_YY	AN6	
4	IO_VREF_L98P_YY	AL7	
4	IO_L98N_YY	AJ9	
4	IO_L99P_Y	AN7	
4	IO_VREF_L99N_Y	AL8	1
4	IO_L100P_Y	AM8	
4	IO_L100N_Y	AJ10	
4	IO_VREF_L101P_Y	AL9	4
4	IO_L101N_Y	AM9	
4	IO_L102P_Y	AK10	
4	IO_L102N_Y	AN9	
4	IO_VREF_L103P_YY	AL10	
4	IO_L103N_YY	AM10	
4	IO_L104P_YY	AL11	

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
NA	VCCINT	N29	
NA	VCCINT	N33	
NA	VCCINT	U5	
NA	VCCINT	U30	
NA	VCCINT	Y2	
NA	VCCINT	Y31	
NA	VCCINT	AB2	
NA	VCCINT	AB32	
NA	VCCINT	AD2	
NA	VCCINT	AD32	
NA	VCCINT	AG3	
NA	VCCINT	AG31	
NA	VCCINT	AJ13	
NA	VCCINT	AK8	
NA	VCCINT	AK11	
NA	VCCINT	AK17	
NA	VCCINT	AK20	
NA	VCCINT	AL14	
NA	VCCINT	AL22	
NA	VCCINT	AL27	
NA	VCCINT	AN25	
0	VCCO	A22	
0	VCCO	A26	
0	VCCO	A30	
0	VCCO	B19	
0	VCCO	B32	
1	VCCO	A10	
1	VCCO	A16	
1	VCCO	B13	
1	VCCO	C3	
1	VCCO	E5	
2	VCCO	B2	
2	VCCO	D1	
2	VCCO	H1	

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
2	VCCO	M1	
2	VCCO	R2	
3	VCCO	V1	
3	VCCO	AA2	
3	VCCO	AD1	
3	VCCO	AK1	
3	VCCO	AL2	
4	VCCO	AN4	
4	VCCO	AN8	
4	VCCO	AN12	
4	VCCO	AM2	
4	VCCO	AM15	
5	VCCO	AL31	
5	VCCO	AM21	
5	VCCO	AN18	
5	VCCO	AN24	
5	VCCO	AN30	
6	VCCO	W32	
6	VCCO	AB33	
6	VCCO	AF33	
6	VCCO	AK33	
6	VCCO	AM32	
7	VCCO	C32	
7	VCCO	D33	
7	VCCO	K33	
7	VCCO	N32	
7	VCCO	T33	
NA	GND	A1	
NA	GND	A7	
NA	GND	A12	
NA	GND	A14	
NA	GND	A18	
NA	GND	A20	
NA	GND	A24	

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
NA	VCCINT	T15
NA	VCCINT	T16
NA	VCCINT	U6
NA	VCCINT	U17
NA	VCCINT	V5
NA	VCCINT	V18
NA	VCCO_7	L7
NA	VCCO_7	K7
NA	VCCO_7	K6
NA	VCCO_7	J6
NA	VCCO_7	H6
NA	VCCO_7	G6
NA	VCCO_6	N7
NA	VCCO_6	M7
NA	VCCO_6	T6
NA	VCCO_6	R6
NA	VCCO_6	P6
NA	VCCO_6	N6
NA	VCCO_5	U10
NA	VCCO_5	U9
NA	VCCO_5	U8
NA	VCCO_5	U7
NA	VCCO_5	T11
NA	VCCO_5	T10
NA	VCCO_4	U16
NA	VCCO_4	U15
NA	VCCO_4	U14
NA	VCCO_4	U13
NA	VCCO_4	T13
NA	VCCO_4	T12
NA	VCCO_3	T17
NA	VCCO_3	R17
NA	VCCO_3	P17
NA	VCCO_3	N17
NA	VCCO_3	N16
NA	VCCO_3	M16

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
NA	VCCO_2	K17
NA	VCCO_2	J17
NA	VCCO_2	H17
NA	VCCO_2	G17
NA	VCCO_2	L16
NA	VCCO_2	K16
NA	VCCO_1	G13
NA	VCCO_1	G12
NA	VCCO_1	F16
NA	VCCO_1	F15
NA	VCCO_1	F14
NA	VCCO_1	F13
NA	VCCO_0	G11
NA	VCCO_0	G10
NA	VCCO_0	F10
NA	VCCO_0	F9
NA	VCCO_0	F8
NA	VCCO_0	F7
NA	GND	AB22
NA	GND	AB1
NA	GND	AA21
NA	GND	AA2
NA	GND	Y20
NA	GND	Y3
NA	GND	P14
NA	GND	P13
NA	GND	P12
NA	GND	P11
NA	GND	P10
NA	GND	P9
NA	GND	N14
NA	GND	N13
NA	GND	N12
NA	GND	N11
NA	GND	N10
NA	GND	N9

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
NA	GND	M14
NA	GND	M13
NA	GND	M12
NA	GND	M11
NA	GND	M10
NA	GND	M9
NA	GND	L14
NA	GND	L13
NA	GND	L12
NA	GND	L11
NA	GND	L10
NA	GND	L9
NA	GND	K14
NA	GND	K13
NA	GND	K12
NA	GND	K11
NA	GND	K10
NA	GND	K9
NA	GND	J14
NA	GND	J13
NA	GND	J12
NA	GND	J11
NA	GND	J10
NA	GND	J9
NA	GND	C20
NA	GND	C3
NA	GND	B21
NA	GND	B2
NA	GND	A22
NA	GND	A1

Note 1: NC in the XCV200E device.

FG456 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 19: **FG456 Differential Pin Pair Summary XCV200E, XCV300E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	W12	U12	NA	IO_DLL_L75P
1	5	Y11	AA11	NA	IO_DLL_L75N
2	1	A11	D11	NA	IO_DLL_L13P
3	0	C11	B11	NA	IO_DLL_L13N
IO LVDS Total Pairs: 119, Asynchronous Output Pairs: 69					
0	0	B3	D5	NA	-
1	0	E6	B4	√	VREF
2	0	E7	A4	NA	-
3	0	D6	C6	√	VREF
4	0	B6	A5	1	-
5	0	C7	D7	1	-
6	0	B7	E8	√	VREF
7	0	E9	A7	√	-
8	0	B8	C8	1	-
9	0	A8	D9	1	-
10	0	E10	C9	NA	-
11	0	C10	A9	√	VREF
12	0	B10	F11	2	-
13	1	D11	B11	NA	IO_LVDS_DLL
14	1	D12	C12	2	-
15	1	A13	B12	2	-
16	1	B13	E12	√	VREF
17	1	D13	C13	√	-

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
2	IO_L63N	G4
2	IO_L64P	G3
2	IO_L64N	E2
2	IO_VREF_L65P_Y	H4
2	IO_L65N_Y	E1
2	IO_L66P_YY	H3
2	IO_L66N_YY	F2
2	IO_L67P	J4
2	IO_L67N	F1
2	IO_L68P_Y	J3
2	IO_L68N_Y	G2
2	IO_VREF_L69P_YY	G1
2	IO_L69N_YY	K4
2	IO_L70P_YY	H2
2	IO_L70N_YY	K3
2	IO_VREF_L71P	H1[3]
2	IO_L71N	L4
2	IO_L72P	J2
2	IO_L72N	L3
2	IO_VREF_L73P_YY	J1
2	IO_L73N_YY	M3
2	IO_L74P_YY	K2
2	IO_L74N_YY	N4
2	IO_L75P	K1
2	IO_L75N	N3
2	IO_VREF_L76P_YY	L2
2	IO_D1_L76N_YY	P4
2	IO_D2_L77P_YY	P3
2	IO_L77N_YY	L1
2	IO_L78P_Y	R4
2	IO_L78N_Y	M2
2	IO_L79P	R3
2	IO_L79N	M1
2	IO_L80P	T4
2	IO_L80N	N2
2	IO_VREF_L81P_Y	N1[1]

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
2	IO_L81N_Y	T3
2	IO_L82P_YY	P2
2	IO_L82N_YY	U5
2	IO_L83P	P1
2	IO_L83N	U4
2	IO_L84P_Y	R2
2	IO_L84N_Y	U3
2	IO_VREF_L85P_YY	V5
2	IO_D3_L85N_YY	R1
2	IO_L86P_YY	V4
2	IO_L86N_YY	T2
2	IO_L87P	V3
2	IO_L87N	T1
2	IO_L88P	W4
2	IO_L88N	U2
2	IO_VREF_L89P_YY	W3
2	IO_L89N_YY	U1
2	IO_L90P_YY	AA3
2	IO_L90N_YY	V2
2	IO_VREF_L91P	AA4[2]
2	IO_L91N	V1
2	IO_L92P_YY	AB2
2	IO_L92N_YY	W2
3	IO	AP3
3	IO	AT3
3	IO	AB3
3	IO_L93P	AB4
3	IO_VREF_L93N	W1[2]
3	IO_L94P_YY	AB5
3	IO_L94N_YY	Y2
3	IO_L95P_YY	AC2
3	IO_VREF_L95N_YY	Y1
3	IO_L96P	AC3
3	IO_L96N	AA1
3	IO_L97P	AC4

Table 25: **FG860 Differential Pin Pair Summary XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
256	7	T38	T41	√	-
257	7	T42	R39	1	VREF
258	7	R38	R42	2	-
259	7	P39	R40	4	-
260	7	P38	R41	2	-
261	7	N39	P42	1	-
262	7	M39	P40	3	-
263	7	M38	P41	√	-
264	7	L39	N42	√	VREF
265	7	N41	L38	2	-
266	7	M42	K40	√	-
267	7	K38	M40	√	VREF
268	7	J40	M41	2	-
269	7	L40	J39	5	VREF
270	7	L41	J38	√	-
271	7	H39	K42	√	VREF
272	7	H38	K41	1	-
273	7	G40	J41	2	-
274	7	G39	H42	√	-
275	7	G42	G38	1	VREF
276	7	F40	G41	2	-
277	7	F41	F42	4	-
278	7	E42	F39	2	VREF
279	7	E41	E40	1	-
280	7	D41	E39	3	-

Notes:
1. AO in the XCV1000E, 2000E.
2. AO in the XCV1000E, 1600E.
3. AO in the XCV2000E.
4. AO in the XCV1600E.
5. AO in the XCV1000E.

FG900 Fine-Pitch Ball Grid Array Package

XCV600E, XCV1000E, and XCV1600E devices in the FG900 fine-pitch Ball Grid Array package have footprint compatibility. Pins labeled I0_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 26, see Table 27 for Differential Pair information.

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
0	GCK3	C15
0	IO	A7[4]
0	IO	A13[4]
0	IO	C5[4]
0	IO	C6[4]
0	IO	C14[4]
0	IO	D8[5]
0	IO	D10
0	IO	D13[4]
0	IO	E6
0	IO	E9[5]
0	IO	E14[5]
0	IO	F9[4]
0	IO	F14[5]
0	IO	G15
0	IO	K11[5]
0	IO	K12
0	IO	L13[4]
0	IO_L0N_YY	C4[4]
0	IO_L0P_YY	F7[3]
0	IO_L1N_Y	D5
0	IO_L1P_Y	G8
0	IO_VREF_L2N_Y	A3[1]
0	IO_L2P_Y	H9
0	IO_L3N_Y	B4[4]
0	IO_L3P_Y	J10[4]
0	IO_L4N_YY	A4
0	IO_L4P_YY	D6
0	IO_VREF_L5N_YY	E7
0	IO_L5P_YY	B5

Table 27: **FG900 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
52	1	A22	C21	√	VREF
53	1	B22	H19	4	-
54	1	D22	E21	4	-
55	1	C22	F21	√	VREF
56	1	E22	H20	√	-
57	1	A23	G21	2	-
58	1	K19	A24	2	-
59	1	B24	C24	√	VREF
60	1	G22	H21	√	-
61	1	C25	E23	1	-
62	1	A26	D24	1	-
63	1	K20	B26	√	VREF
64	1	J21	D25	√	-
65	1	F23	C26	2	-
66	1	G23	B27	2	VREF
67	1	F24	A27	2	-
68	1	A28	B28	4	-
69	1	C27	K21	√	CS
70	2	J22	E27	√	DIN, D0
71	2	C29	D28	NA	-
72	2	G25	E25	1	-
73	2	E28	C30	4	VREF
74	2	K22	F27	3	-
75	2	D30	J23	4	-
76	2	L21	F28	1	VREF
77	2	G28	E30	√	-
78	2	G27	E29	4	-
79	2	K23	H26	1	-
80	2	F30	L22	√	VREF
81	2	H27	G29	√	-
82	2	G30	M21	2	-
83	2	J24	J26	4	-
84	2	H30	L23	4	VREF
85	2	K26	J28	4	-

Table 27: **FG900 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
86	2	J29	K24	4	-
87	2	K27	J30	4	VREF
88	2	M22	K29	NA	D2
89	2	K28	L25	4	-
90	2	N21	K25	1	-
91	2	L24	L27	4	-
92	2	L29	M23	3	-
93	2	L26	L28	4	-
94	2	L30	M27	1	VREF
95	2	M26	M29	√	-
96	2	N29	M30	4	-
97	2	N25	N27	1	-
98	2	N30	P21	√	D3
99	2	N26	P28	√	-
100	2	P29	N24	2	-
101	2	P22	R26	√	-
102	2	P25	R29	4	VREF
103	2	R21	R28	4	-
104	2	R25	T30	4	VREF
105	2	P24	R27	4	-
106	3	R24	U29	NA	
107	3	R22	T27	4	VREF
108	3	R23	T28	4	-
109	3	T21	T25	4	VREF
110	3	U28	U30	4	-
111	3	T23	U27	2	-
112	3	U25	V27	√	-
113	3	U24	V29	√	VREF
114	3	W30	U22	1	-
115	3	U21	W29	4	-
116	3	V26	W27	√	-
117	3	W26	Y29	1	VREF
118	3	W25	Y30	4	-
119	3	V24	Y28	3	-

Date	Version	Revision
4/2/01	2.0	• Updated numerous values in **Virtex-E Switching Characteristics** tables. • Changed pinout table footnotes from "V_{REF} option only" to "V_{REF} or I/O option only" to improve clarity. • Converted file to modularized format. See the **Virtex-E Data Sheet** section.
7/26/01	2.1	• Changed pinout table footnotes from "V_{REF} or I/O option only" to "V_{REF} or I/O option only; otherwise I/O only" to improve clarity. • Changed designation for pin pair 300 in Table 29 from AO to footnote 9.
10/25/01	2.2	• Changed Table 29 to clarify which devices in the FG1156 package can use each pin pair as an asynchronous output. • Updated references to the XCV3200E device in the FG1156 package.
11/15/01	2.3	• Fixed cosmetic error.
07/17/02	2.4	• Added “VREF” to the description for pin B15 in Table 12. • Changed designation for pin pair 129 in Table 15 from AO to “AO in the XCV1000E, 1600E, 2000E“. • Data sheet designation upgraded from Preliminary to Production.
03/14/03	2.5	• Removed the Virtex-E XCV300E section under **Pinout Differences Between Virtex and Virtex-E Families** (and revised Table 1), since these differences do not exist.

Virtex-E Data Sheet

The Virtex-E Data Sheet contains the following modules:

- DS022-1, Virtex-E 1.8V FPGAs:
  Introduction and Ordering Information (Module 1)
- DS022-2, Virtex-E 1.8V FPGAs:
  Functional Description (Module 2)
- DS022-3, Virtex-E 1.8V FPGAs:
  DC and Switching Characteristics (Module 3)
- DS022-4, Virtex-E 1.8V FPGAs:
  Pinout Tables (Module 4)