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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 3456 |
| Number of Logic Elements/Cells | 15552 |
| Total RAM Bits | 294912 |
| Number of I/O | 158 |
| Number of Gates | 985882 |
| Voltage - Supply | 1.71V ~ 1.89V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 240-BFQFP Exposed Pad |
| Supplier Device Package | 240-PQFP (32x32) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xcv600e-7hq240i |

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

### *Dedicated Routing*

Some classes of signal require dedicated routing resources to maximize performance. In the Virtex-E architecture, dedicated routing resources are provided for two classes of signal.

- Horizontal routing resources are provided for on-chip 3-state buses. Four partitionable bus lines are provided per CLB row, permitting multiple buses within a row, as shown in Figure 8.
- Two dedicated nets per CLB propagate carry signals vertically to the adjacent CLB.Global Clock Distribution Network
- DLL Location

### *Clock Routing*

Clock Routing resources distribute clocks and other signals with very high fanout throughout the device. Virtex-E devices include two tiers of clock routing resources referred to as global and local clock routing resources.

- The global routing resources are four dedicated global nets with dedicated input pins that are designed to distribute high-fanout clock signals with minimal skew. Each global clock net can drive all CLB, IOB, and block RAM clock pins. The global nets can be driven only by global buffers. There are four global buffers, one for each global net.
- The local clock routing resources consist of 24 backbone lines, 12 across the top of the chip and 12 across bottom. From these lines, up to 12 unique signals per column can be distributed via the 12 longlines in the column. These local resources are more flexible than the global resources since they are not restricted to routing only to clock pins.

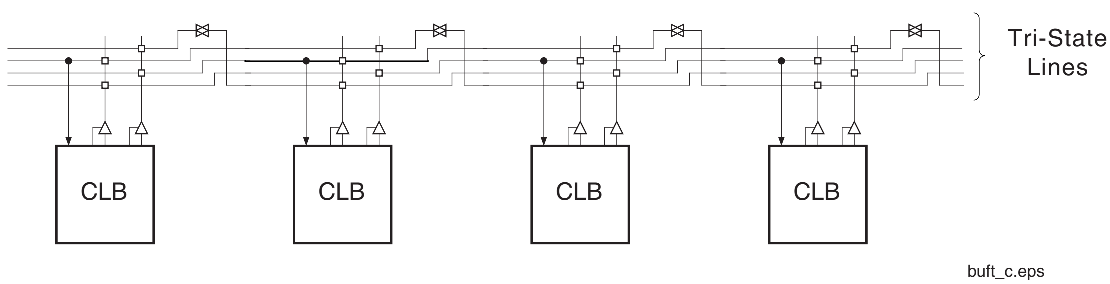


*Figure 8:* **BUFT Connections to Dedicated Horizontal Bus LInes**

## Global Clock Distribution

Virtex-E provides high-speed, low-skew clock distribution through the global routing resources described above. A typical clock distribution net is shown in Figure 9.

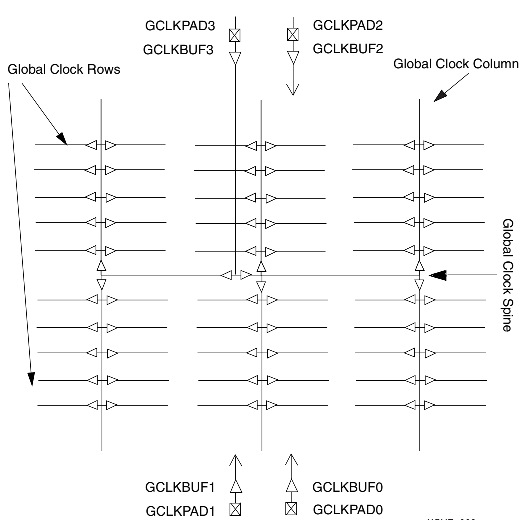


*Figure 9:* **Global Clock Distribution Network**

Four global buffers are provided, two at the top center of the device and two at the bottom center. These drive the four global nets that in turn drive any clock pin.

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is selected either from these pads or from signals in the general purpose routing.

### *Digital Delay-Locked Loops*

There are eight DLLs (Delay-Locked Loops) per device, with four located at the top and four at the bottom, Figure 10. The DLLs can be used to eliminate skew between the clock input pad and the internal clock input pins throughout the device. Each DLL can drive two global clock networks.The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element. Additional delay is introduced such that clock edges arrive at internal flip-flops synchronized with clock edges arriving at the input.

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock, and can double the clock or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

3. At the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock. If BUSY is High (from a previous write), the data is not accepted. Acceptance instead occurs on the first clock after BUSY goes Low, and the data must be held until this has happened.
4. Repeat steps 2 and 3 until all the data has been sent.
5. De-assert $\overline{CS}$ and $\overline{WRITE}$.

*Table 11:* **SelectMAP Write Timing Characteristics**

| | Description | | Symbol | | Units |
|---|---|---|---|---|---|
| CCLK | $D_{0-7}$ Setup/Hold | 1/2 | $T_{SMDCC}/T_{SMCCD}$ | 5.0 / 1.7 | ns, min |
| | $\overline{CS}$ Setup/Hold | 3/4 | $T_{SMCSCC}/T_{SMCCCS}$ | 7.0 / 1.7 | ns, min |
| | $\overline{WRITE}$ Setup/Hold | 5/6 | $T_{SMCCW}/T_{SMWCC}$ | 7.0 / 1.7 | ns, min |
| | BUSY Propagation Delay | 7 | $T_{SMCKBY}$ | 12.0 | ns, max |
| | Maximum Frequency | | $F_{CC}$ | 66 | MHz, max |
| | Maximum Frequency with no handshake | | $F_{CCNH}$ | 50 | MHz, max |

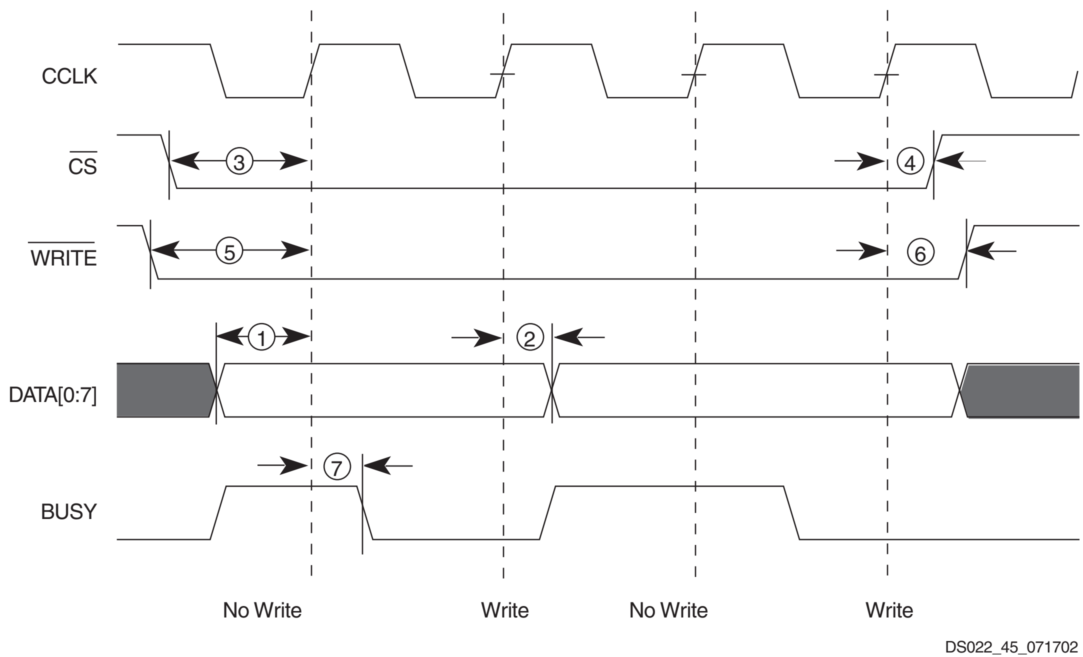


*Figure 17:* **Write Operations**

A flowchart for the write operation is shown in Figure 18. Note that if CCLK is slower than $f_{CCNH}$, the FPGA never asserts BUSY, In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.

### Abort

During a given assertion of $\overline{CS}$, the user cannot switch from a write to a read, or vice-versa. This action causes the current packet command to be aborted. The device remains BUSY until the aborted operation has completed. Following an abort, data is assumed to be unaligned to word boundaries, and the FPGA requires a new synchronization word prior to accepting any new packets.

To initiate an abort during a write operation, de-assert $\overline{WRITE}$. At the rising edge of CCLK, an abort is initiated, as shown in Figure 19.

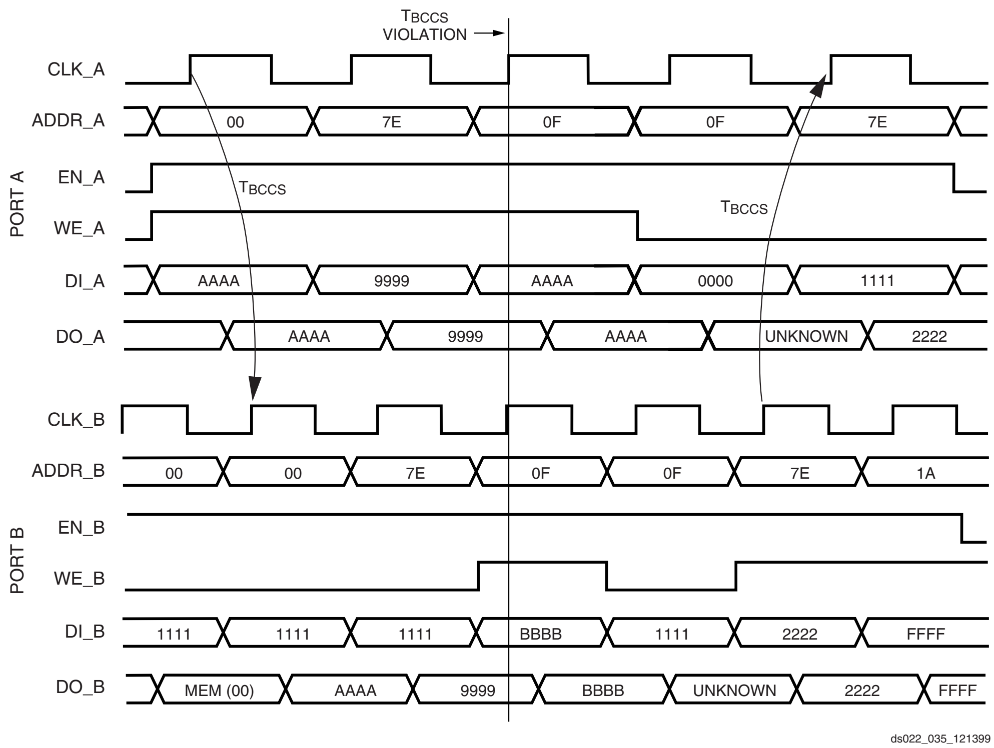


*Figure 34:* **Timing Diagram for a True Dual-port Read/Write Block SelectRAM+ Memory**

At the third rising edge of CLKA, the $T_{BCCS}$ parameter is violated with two writes to memory location 0x0F. The DOA and DOB buses reflect the contents of the DIA and DIB buses, but the stored value at 0x0F is invalid.

At the fourth rising edge of CLKA, a read operation is performed at memory location 0x0F and invalid data is present on the DOA bus. Port B also executes a read operation to memory location 0x0F and also reads invalid data.

At the fifth rising edge of CLKA a read operation is performed that does not violate the $T_{BCCS}$ parameter to the previous write of 0x7E by Port B. THe DOA bus reflects the recently written value by Port B.

## Initialization

The block SelectRAM+ memory can initialize during the device configuration sequence. The 16 initialization properties of 64 hex values each (a total of 4096 bits) set the initialization of each RAM. These properties appear in Table 17. Any initialization properties not explicitly set configure as zeros. Partial initialization strings pad with zeros. Initialization strings greater than 64 hex values generate an error. The RAMs can be simulated with the initialization values using generics in VHDL simulators and parameters in Verilog simulators.

## Initialization in VHDL and Synopsys

The block SelectRAM+ structures can be initialized in VHDL for both simulation and synthesis for inclusion in the EDIF output file. The simulation of the VHDL code uses a generic to pass the initialization. Synopsys FPGA compiler does not presently support generics. The initialization values instead attach as attributes to the RAM by a built-in Synopsys dc_script. The translate_off statement stops synthesis translation of the generic statements. The following code illustrates a module that employs these techniques.

*Table 17:* **RAM Initialization Properties**

| Property | Memory Cells |
|---|---|
| INIT_00 | 255 to 0 |
| INIT_01 | 511 to 256 |
| INIT_02 | 767 to 512 |
| INIT_03 | 1023 to 768 |
| INIT_04 | 1279 to 1024 |
| INIT_05 | 1535 to 1280 |
| INIT_06 | 1791 to 2047 |
| INIT_07 | 2047 to 1792 |
| INIT_08 | 2303 to 2048 |
| INIT_09 | 2559 to 2304 |
| INIT_0a | 2815 to 2560 |
| INIT_0b | 3071 to 2816 |
| INIT_0c | 3327 to 3072 |
| INIT_0d | 3583 to 3328 |
| INIT_0e | 3839 to 3584 |
| INIT_0f | 4095 to 3840 |

### *IOB Flip-Flop/Latch Property*

The Virtex-E series I/O Block (IOB) includes an optional register on the input path, an optional register on the output path, and an optional register on the 3-state control pin. The design implementation software automatically takes advantage of these registers when the following option for the Map program is specified.

map –pr b <filename>

Alternatively, the IOB = TRUE property can be placed on a register to force the mapper to place the register in an IOB.

### *Location Constraints*

Specify the location of each SelectI/O symbol with the location constraint LOC attached to the SelectI/O symbol. The external port identifier indicates the value of the location constrain. The format of the port identifier depends on the package chosen for the specific design.

The LOC properties use the following form:

LOC=A42

LOC=P37

### *Output Slew Rate Property*

As mentioned above, a variety of symbol names provide the option of choosing the desired slew rate for the output buffers. In the case of the LVTTL output buffers (OBUF, OBUFT, and IOBUF), slew rate control can be alternatively programed with the SLEW= property. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals. The SLEW= property has one of the two following values.

SLEW=SLOW

SLEW=FAST

### *Output Drive Strength Property*

The desired output drive strength can be additionally specified by choosing the appropriate library symbol. The Xilinx library also provides an alternative method for specifying this feature. For the LVTTL output buffers (OBUF, OBUFT, and IOBUF, the desired drive strength can be specified with the DRIVE= property. This property could have one of the following seven values.

DRIVE=2
DRIVE=4
DRIVE=6
DRIVE=8
DRIVE=12 (Default)
DRIVE=16
DRIVE=24

## Design Considerations

### *Reference Voltage ($V_{REF}$) Pins*

Low-voltage I/O standards with a differential amplifier input buffer require an input reference voltage ($V_{REF}$). Provide the $V_{REF}$ as an external signal to the device.

The voltage reference signal is "banked" within the device on a half-edge basis such that for all packages there are eight independent $V_{REF}$ banks internally. See Figure 38 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a $V_{REF}$ input. After placing a differential amplifier input signal within a given $V_{REF}$ bank, the same external source must drive all I/O pins configured as a $V_{REF}$ input.

Within each $V_{REF}$ bank, any input buffers that require a $V_{REF}$ signal must be of the same type. Output buffers of any type and input buffers can be placed without requiring a reference voltage within the same $V_{REF}$ bank.

### *Output Drive Source Voltage ($V_{CCO}$) Pins*

Many of the low voltage I/O standards supported by SelectI/O devices require a different output drive source voltage ($V_{CCO}$). As a result each device can often have to support multiple output drive source voltages.

The Virtex-E series supports eight banks for the HQ and PQ packages. The CS package supports four $V_{CCO}$ banks.

Output buffers within a given $V_{CCO}$ bank must share the same output drive source voltage. Input buffers for LVTTL, LVCMOS2, LVCMOS18, PCI33_3, and PCI 66_3 use the $V_{CCO}$ voltage for Input $V_{CCO}$ voltage.

### *Transmission Line Effects*

The delay of an electrical signal along a wire is dominated by the rise and fall times when the signal travels a short distance. Transmission line delays vary with inductance and capacitance, but a well-designed board can experience delays of approximately 180 ps per inch.

Transmission line effects, or reflections, typically start at 1.5" for fast (1.5 ns) rise and fall times. Poor (or non-existent) termination or changes in the transmission line impedance cause these reflections and can cause additional delay in longer traces. As system speeds continue to increase, the effect of I/O delays can become a limiting factor and therefore transmission line termination becomes increasingly more important.

### *Termination Techniques*

A variety of termination techniques reduce the impact of transmission line effects.

The following are output termination techniques:

- None
- Series
- Parallel (Shunt)
- Series and Parallel (Series-Shunt)

## Application Examples

Creating a design with the SelectI/O features requires the instantiation of the desired library symbol within the design code. At the board level, designers need to know the termination techniques required for each I/O standard.

This section describes some common application examples illustrating the termination techniques recommended by each of the standards supported by the SelectI/O features.

### *Termination Examples*

Circuit examples involving typical termination techniques for each of the SelectI/O standards follow. For a full range of accepted values for the DC voltage specifications for each standard, refer to the table associated with each figure.

The resistors used in each termination technique example and the transmission lines depicted represent board level components and are not meant to represent components on the device.

#### GTL

A sample circuit illustrating a valid termination technique for GTL is shown in Figure 44.

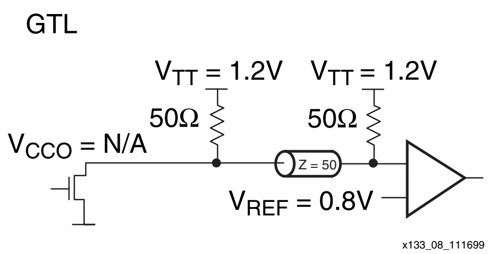


*Figure 44:* **Terminated GTL**

Table 23 lists DC voltage specifications.

*Table 23:* **GTL Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | - | N/A | - |
| $V_{REF} = N \times V_{TT}$[1] | 0.74 | 0.8 | 0.86 |
| $V_{TT}$ | 1.14 | 1.2 | 1.26 |
| $V_{IH} = V_{REF} + 0.05$ | 0.79 | 0.85 | - |
| $V_{IL} = V_{REF} - 0.05$ | - | 0.75 | 0.81 |
| $V_{OH}$ | - | - | - |
| $V_{OL}$ | - | 0.2 | 0.4 |
| $I_{OH}$ at $V_{OH}$(mA) | - | - | - |
| $I_{OL}$at $V_{OL}$(mA) at 0.4V | 32 | - | - |
| $I_{OL}$at $V_{OL}$(mA) at 0.2V | - | - | 40 |

**Notes:**

1. N must be greater than or equal to 0.653 and less than or equal to 0.68.

#### GTL+

A sample circuit illustrating a valid termination technique for GTL+ appears in Figure 45. DC voltage specifications appear in Table 24.

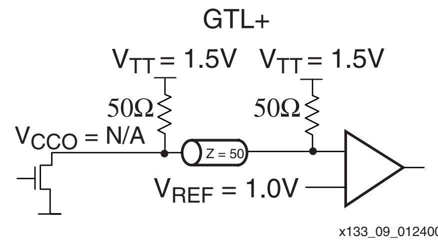


*Figure 45:* **Terminated GTL+**

*Table 24:* **GTL+ Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | - | - | - |
| $V_{REF} = N \times V_{TT}$[1] | 0.88 | 1.0 | 1.12 |
| $V_{TT}$ | 1.35 | 1.5 | 1.65 |
| $V_{IH} = V_{REF} + 0.1$ | 0.98 | 1.1 | - |
| $V_{IL} = V_{REF} - 0.1$ | - | 0.9 | 1.02 |
| $V_{OH}$ | - | - | - |
| $V_{OL}$ | 0.3 | 0.45 | 0.6 |
| $I_{OH}$ at $V_{OH}$ (mA) | - | - | - |
| $I_{OL}$at $V_{OL}$ (mA) at 0.6V | 36 | - | - |
| $I_{OL}$at $V_{OL}$ (mA) at 0.3V | - | - | 48 |

**Notes:**

1. N must be greater than or equal to 0.653 and less than or equal to 0.68.

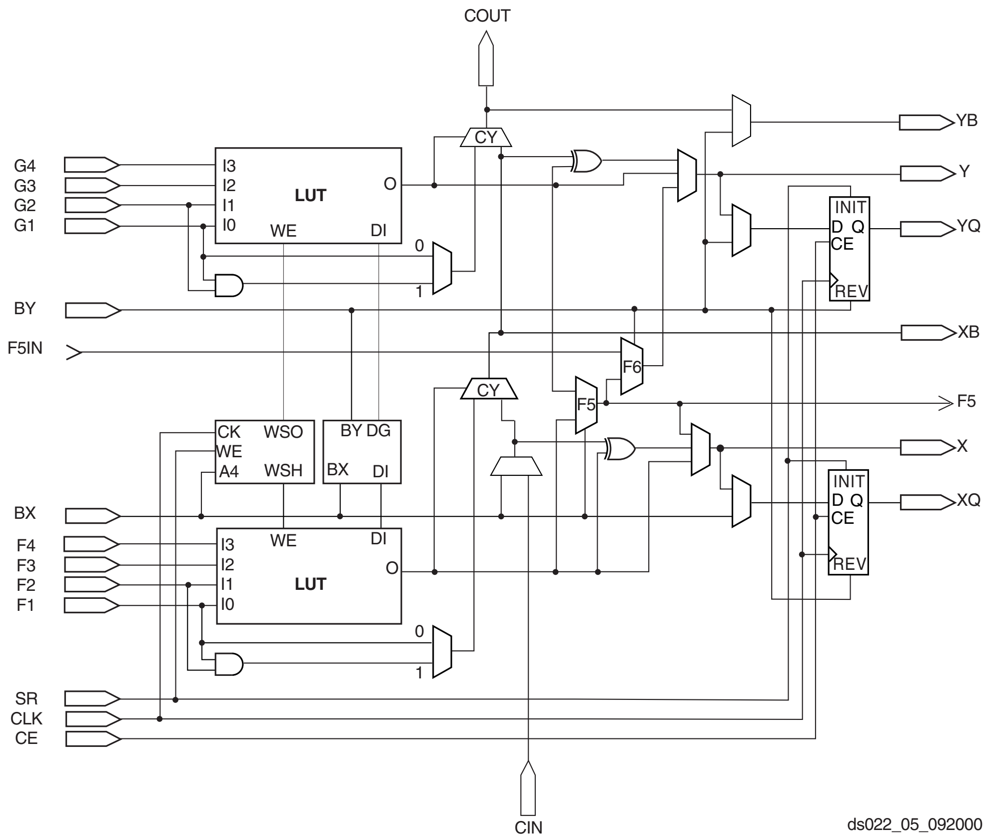


*Figure 2:* **Detailed View of Virtex-E Slice**

*Table 6:* **PQ240 — XCV50E, XCV100E, XCV200E, XCV300E, XCV400E**

| Pin # | Pin Description | Bank |
|---|---|---|
| P173 | IO_L16N_Y | 2 |
| P171 | IO_VREF_L17P_Y | 2 |
| P170 | IO_L17N_Y | 2 |
| P169 | IO | 2 |
| P168[1] | IO_VREF_L18P_Y | 2 |
| P167 | IO_D1_L18N_Y | 2 |
| P163 | IO_D2_L19P_YY | 2 |
| P162 | IO_L19N_YY | 2 |
| P161 | IO | 2 |
| P160 | IO_L20P_Y | 2 |
| P159 | IO_L20N_Y | 2 |
| P157 | IO_VREF_L21P_Y | 2 |
| P156 | IO_D3_L21N_Y | 2 |
| P155 | IO_L22P_Y | 2 |
| P154[3] | IO_VREF_L22N_Y | 2 |
| P153 | IO_L23P_YY | 2 |
| P152 | IO_L23N_YY | 2 |
| | | |
| P149 | IO | 3 |
| P147[3] | IO_VREF | 3 |
| P145 | IO_D4_L24P_Y | 3 |
| P144 | IO_VREF_L24N_Y | 3 |
| P142 | IO_L25P_Y | 3 |
| P141 | IO_L25N_Y | 3 |
| P140 | IO | 3 |
| P139 | IO_L26P_YY | 3 |
| P138 | IO_D5_L26N_YY | 3 |
| P134 | IO_D6_L27P_Y | 3 |
| P133[1] | IO_VREF_L27N_Y | 3 |
| P132 | IO | 3 |
| P131 | IO_L28P_Y | 3 |
| P130 | IO_VREF_L28N_Y | 3 |
| P128 | IO_L29P_Y | 3 |
| P127 | IO_L29N_Y | 3 |
| P126[2] | IO_VREF_L30P_Y | 3 |

*Table 6:* **PQ240 — XCV50E, XCV100E, XCV200E, XCV300E, XCV400E**

| Pin # | Pin Description | Bank |
|---|---|---|
| P125 | IO_L30N_Y | 3 |
| P124 | IO_D7_L31P_YY | 3 |
| P123 | IO_INIT_L31N_YY | 3 |
| | | |
| P118 | IO_L32P_YY | 4 |
| P117 | IO_L32N_YY | 4 |
| P115[2] | IO_VREF | 4 |
| P114 | IO_L33P_YY | 4 |
| P113 | IO_L33N_YY | 4 |
| P111 | IO_VREF_L34P_YY | 4 |
| P110 | IO_L34N_YY | 4 |
| P109 | IO | 4 |
| P108[1] | IO_VREF_L35P_YY | 4 |
| P107 | IO_L35N_YY | 4 |
| P103 | IO_L36P_YY | 4 |
| P102 | IO_L36N_YY | 4 |
| P101 | IO | 4 |
| P100 | IO_L37P_Y | 4 |
| P99 | IO_L37N_Y | 4 |
| P97 | IO_VREF_L38P_Y | 4 |
| P96 | IO_L38N_Y | 4 |
| P95 | IO_L39P_Y | 4 |
| P94[3] | IO_VREF_L39N_Y | 4 |
| P93 | IO_LVDS_DLL_L40P | 4 |
| P92 | GCK0 | 4 |
| | | |
| P89 | GCK1 | 5 |
| P87 | IO_LVDS_DLL_L40N | 5 |
| P86[3] | IO_VREF | 5 |
| P84 | IO_VREF_L41P_Y | 5 |
| P82 | IO_L41N_Y | 5 |
| P81 | IO | 5 |
| P80 | IO | 5 |
| P79 | IO_L42P_YY | 5 |
| P78 | IO_L42N_YY | 5 |

*Table 8:* **HQ240 — XCV600E, XCV1000E**

| Pin # | Pin Description | Bank |
|---|---|---|
| P138 | IO_D5_L26N_YY | 3 |
| P137 | VCCINT | NA |
| P136 | VCCO | 3 |
| P135 | GND | NA |
| P134 | IO_D6_L27P_Y | 3 |
| P133 | IO_VREF_L27N_Y | 3 |
| P132 | IO_VREF | 3 |
| P131 | IO_L28P_Y | 3 |
| P130 | IO_VREF_L28N_Y | 3 |
| P129 | GND | NA |
| P128 | IO_L29P_Y | 3 |
| P127 | IO_L29N_Y | 3 |
| P126 | IO_VREF_L30P_Y | 3 |
| P125 | IO_L30N_Y | 3 |
| P124 | IO_D7_L31P_YY | 3 |
| P123 | IO_INIT_L31N_YY | 3 |
| P122 | PROGRAM | NA |
| P121 | VCCO | 3 |
| P120 | DONE | 3 |
| P119 | GND | NA |
| P118 | IO_L32P_YY | 4 |
| P117 | IO_L32N_YY | 4 |
| P116 | VCCO | 4 |
| P115 | IO_VREF | 4 |
| P114 | IO_L33P_YY | 4 |
| P113 | IO_L33N_YY | 4 |
| P112 | GND | NA |
| P111 | IO_VREF_L34P_YY | 4 |
| P110 | IO_L34N_YY | 4 |
| P109 | IO_VREF | 4 |
| P108 | IO_VREF_L35P_YY | 4 |
| P107 | IO_L35N_YY | 4 |
| P106 | GND | NA |
| P105 | VCCO | 4 |
| P104 | VCCINT | NA |
| P103 | IO_L36P_YY | 4 |

*Table 8:* **HQ240 — XCV600E, XCV1000E**

| Pin # | Pin Description | Bank |
|---|---|---|
| P102 | IO_L36N_YY | 4 |
| P101[1] | IO_VREF | 4 |
| P100 | IO_L37P_Y | 4 |
| P99 | IO_L37N_Y | 4 |
| P98 | GND | NA |
| P97 | IO_VREF_L38P_Y | 4 |
| P96 | IO_L38N_Y | 4 |
| P95 | IO_L39P | 4 |
| P94 | IO_VREF_L39N | 4 |
| P93 | IO_LVDS_DLL_L40P | 4 |
| P92 | GCK0 | 4 |
| P91 | GND | NA |
| P90 | VCCO | 4 |
| P89 | GCK1 | 5 |
| P88 | VCCINT | NA |
| P87 | IO_LVDS_DLL_L40N | 5 |
| P86 | IO_VREF | 5 |
| P85 | VCCO | 5 |
| P84 | IO_VREF_L41P | 5 |
| P83 | GND | NA |
| P82 | IO_L41N | 5 |
| P81 | IO | 5 |
| P80[1] | IO_VREF | 5 |
| P79 | IO_L42P_YY | 5 |
| P78 | IO_L42N_YY | 5 |
| P77 | VCCINT | NA |
| P76 | VCCO | 5 |
| P75 | GND | NA |
| P74 | IO_L43P_YY | 5 |
| P73 | IO_VREF_L43N_YY | 5 |
| P72 | IO_VREF | 5 |
| P71 | IO_L44P_YY | 5 |
| P70 | IO_VREF_L44N_YY | 5 |
| P69 | GND | NA |
| P68 | IO_L45P_YY | 5 |
| P67 | IO_L45N_YY | 5 |

*Table 12:* **BG432 — XCV300E, XCV400E, XCV600E**

| Bank | Pin Description | Pin # |
|---|---|---|
| 2 | IO_L41N_Y | H2 |
| 2 | IO_VREF_L42P_Y | H1[1] |
| 2 | IO_L42N_Y | J4 |
| 2 | IO_VREF_L43P_YY | J2 |
| 2 | IO_D1_L43N_YY | K4 |
| 2 | IO_D2_L44P_YY | K2 |
| 2 | IO_L44N_YY | K1 |
| 2 | IO_L45P_Y | L2 |
| 2 | IO_L45N_Y | M4 |
| 2 | IO_L46P_Y | M3 |
| 2 | IO_L46N_Y | M2 |
| 2 | IO_L47P_Y | N4 |
| 2 | IO_L47N_Y | N3 |
| 2 | IO_VREF_L48P_YY | N1 |
| 2 | IO_D3_L48N_YY | P4 |
| 2 | IO_L49P_Y | P3 |
| 2 | IO_L49N_Y | P2 |
| 2 | IO_VREF_L50P_Y | R3[2] |
| 2 | IO_L50N_Y | R4 |
| 2 | IO_L51P_YY | R1 |
| 2 | IO_L51N_YY | T3 |
| | | |
| 3 | IO | AA2 |
| 3 | IO | AC2 |
| 3 | IO | AE2 |
| 3 | IO | U3 |
| 3 | IO | W1 |
| 3 | IO_L52P_Y | U4 |
| 3 | IO_VREF_L52N_Y | U2[2] |
| 3 | IO_L53P_Y | U1 |
| 3 | IO_L53N_Y | V3 |
| 3 | IO_D4_L54P_YY | V4 |
| 3 | IO_VREF_L54N_YY | V2 |
| 3 | IO_L55P_Y | W3 |
| 3 | IO_L55N_Y | W4 |
| 3 | IO_L56P_Y | Y1 |

*Table 12:* **BG432 — XCV300E, XCV400E, XCV600E**

| Bank | Pin Description | Pin # |
|---|---|---|
| 3 | IO_L56N_Y | Y3 |
| 3 | IO_L57P_Y | Y4 |
| 3 | IO_L57N_Y | Y2 |
| 3 | IO_L58P_YY | AA3 |
| 3 | IO_D5_L58N_YY | AB1 |
| 3 | IO_D6_L59P_YY | AB3 |
| 3 | IO_VREF_L59N_YY | AB4 |
| 3 | IO_L60P_Y | AD1 |
| 3 | IO_VREF_L60N_Y | AC3[1] |
| 3 | IO_L61P_Y | AC4 |
| 3 | IO_L61N_Y | AD2 |
| 3 | IO_L62P_YY | AD3 |
| 3 | IO_VREF_L62N_YY | AD4 |
| 3 | IO_L63P_Y | AF2 |
| 3 | IO_L63N_Y | AE3 |
| 3 | IO_L64P | AE4 |
| 3 | IO_L64N | AG1 |
| 3 | IO_L65P_Y | AG2 |
| 3 | IO_VREF_L65N_Y | AF3 |
| 3 | IO_L66P_Y | AF4 |
| 3 | IO_L66N_Y | AH1 |
| 3 | IO_L67P | AH2 |
| 3 | IO_L67N | AG3 |
| 3 | IO_D7_L68P_YY | AG4 |
| 3 | IO_INIT_L68N_YY | AJ2 |
| 3 | IO | T2 |
| | | |
| 4 | GCK0 | AL16 |
| 4 | IO | AH10 |
| 4 | IO | AJ11 |
| 4 | IO | AK7 |
| 4 | IO | AL12 |
| 4 | IO | AL15 |
| 4 | IO_L69P_YY | AJ4 |
| 4 | IO_L69N_YY | AK3 |
| 4 | IO_L70P_Y | AH5 |

*Table 12:* **BG432 — XCV300E, XCV400E, XCV600E**

| Bank | Pin Description | Pin # |
|---|---|---|
| 4 | IO_L70N_Y | AK4 |
| 4 | IO_L71P_YY | AJ5 |
| 4 | IO_L71N_YY | AH6 |
| 4 | IO_VREF_L72P_YY | AL4 |
| 4 | IO_L72N_YY | AK5 |
| 4 | IO_L73P_Y | AJ6 |
| 4 | IO_L73N_Y | AH7 |
| 4 | IO_L74P_YY | AL5 |
| 4 | IO_L74N_YY | AK6 |
| 4 | IO_VREF_L75P_YY | AJ7 |
| 4 | IO_L75N_YY | AL6 |
| 4 | IO_L76P_Y | AH9 |
| 4 | IO_L76N_Y | AJ8 |
| 4 | IO_VREF_L77P_Y | AK8[1] |
| 4 | IO_L77N_Y | AJ9 |
| 4 | IO_VREF_L78P_YY | AL8 |
| 4 | IO_L78N_YY | AK9 |
| 4 | IO_L79P_YY | AK10 |
| 4 | IO_L79N_YY | AL10 |
| 4 | IO_L80P_YY | AH12 |
| 4 | IO_L80N_YY | AK11 |
| 4 | IO_L81P_YY | AJ12 |
| 4 | IO_L81N_YY | AK12 |
| 4 | IO_L82P_YY | AH13 |
| 4 | IO_L82N_YY | AJ13 |
| 4 | IO_VREF_L83P_YY | AL13 |
| 4 | IO_L83N_YY | AK14 |
| 4 | IO_L84P_Y | AH14 |
| 4 | IO_L84N_Y | AJ14 |
| 4 | IO_VREF_L85P_Y | AK15[2] |
| 4 | IO_L85N_Y | AJ15 |
| 4 | IO_LVDS_DLL_L86P | AH15 |
| | | |
| 5 | GCK1 | AK16 |
| 5 | IO | AH20 |
| 5 | IO | AJ19 |

*Table 12:* **BG432 — XCV300E, XCV400E, XCV600E**

| Bank | Pin Description | Pin # |
|---|---|---|
| 5 | IO | AJ23 |
| 5 | IO | AJ24 |
| 5 | IO_LVDS_DLL_L86N | AL17 |
| 5 | IO_L87P_Y | AK17 |
| 5 | IO_VREF_L87N_Y | AJ17[2] |
| 5 | IO_L88P_Y | AH17 |
| 5 | IO_L88N_Y | AK18 |
| 5 | IO_L89P_YY | AL19 |
| 5 | IO_VREF_L89N_YY | AJ18 |
| 5 | IO_L90P_YY | AH18 |
| 5 | IO_L90N_YY | AL20 |
| 5 | IO_L91P_YY | AK20 |
| 5 | IO_L91N_YY | AH19 |
| 5 | IO_L92P_YY | AJ20 |
| 5 | IO_L92N_YY | AK21 |
| 5 | IO_L93P_YY | AJ21 |
| 5 | IO_L93N_YY | AL22 |
| 5 | IO_L94P_YY | AJ22 |
| 5 | IO_VREF_L94N_YY | AK23 |
| 5 | IO_L95P_Y | AH22 |
| 5 | IO_VREF_L95N_Y | AL24[1] |
| 5 | IO_L96P_Y | AK24 |
| 5 | IO_L96N_Y | AH23 |
| 5 | IO_L97P_YY | AK25 |
| 5 | IO_VREF_L97N_YY | AJ25 |
| 5 | IO_L98P_YY | AL26 |
| 5 | IO_L98N_YY | AK26 |
| 5 | IO_L99P_Y | AH25 |
| 5 | IO_L99N_Y | AL27 |
| 5 | IO_L100P_YY | AJ26 |
| 5 | IO_VREF_L100N_YY | AK27 |
| 5 | IO_L101P_YY | AH26 |
| 5 | IO_L101N_YY | AL28 |
| 5 | IO_L102P_Y | AJ27 |
| 5 | IO_L102N_Y | AK28 |
| | | |

*Table 14:* **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

| Bank | Pin Description | Pin# | See Note |
|---|---|---|---|
| 1 | IO_L43N_Y | C5 | |
| 1 | IO_VREF_L43P_Y | E7 | 3 |
| 1 | IO_WRITE_L44N_YY | D6 | |
| 1 | IO_CS_L44P_YY | A2 | |
| | | | |
| 2 | IO | D3 | |
| 2 | IO | F3 | |
| 2 | IO | G1 | |
| 2 | IO | J2 | |
| 2 | IO_DOUT_BUSY_L45P_YY | D4 | |
| 2 | IO_DIN_D0_L45N_YY | E4 | |
| 2 | IO_L46P_Y | F5 | |
| 2 | IO_VREF_L46N_Y | B3 | 3 |
| 2 | IO_L47P_Y | F4 | |
| 2 | IO_L47N_Y | C1 | |
| 2 | IO_VREF_L48P_Y | G5 | |
| 2 | IO_L48N_Y | E3 | |
| 2 | IO_L49P_Y | D2 | |
| 2 | IO_L49N_Y | G4 | |
| 2 | IO_L50P_Y | H5 | |
| 2 | IO_L50N_Y | E2 | |
| 2 | IO_VREF_L51P_YY | H4 | |
| 2 | IO_L51N_YY | G3 | |
| 2 | IO_L52P_Y | J5 | |
| 2 | IO_VREF_L52N_Y | F1 | 1 |
| 2 | IO_L53P_Y | J4 | |
| 2 | IO_L53N_Y | H3 | |
| 2 | IO_VREF_L54P_Y | K5 | 4 |
| 2 | IO_L54N_Y | H2 | |
| 2 | IO_L55P_Y | J3 | |
| 2 | IO_L55N_Y | K4 | |
| 2 | IO_VREF_L56P_YY | L5 | |
| 2 | IO_D1_L56N_YY | K3 | |
| 2 | IO_D2_L57P_YY | L4 | |
| 2 | IO_L57N_YY | K2 | |

*Table 14:* **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

| Bank | Pin Description | Pin# | See Note |
|---|---|---|---|
| 2 | IO_L58P_Y | M5 | |
| 2 | IO_L58N_Y | L3 | |
| 2 | IO_L59P_Y | L1 | |
| 2 | IO_L59N_Y | M4 | |
| 2 | IO_VREF_L60P_Y | N5 | 3 |
| 2 | IO_L60N_Y | M2 | |
| 2 | IO_L61P_Y | N4 | |
| 2 | IO_L61N_Y | N3 | |
| 2 | IO_L62P_Y | N2 | |
| 2 | IO_L62N_Y | P5 | |
| 2 | IO_VREF_L63P_YY | P4 | |
| 2 | IO_D3_L63N_YY | P3 | |
| 2 | IO_L64P_Y | P2 | |
| 2 | IO_L64N_Y | R5 | |
| 2 | IO_L65P_Y | R4 | |
| 2 | IO_L65N_Y | R3 | |
| 2 | IO_VREF_L66P_Y | R1 | |
| 2 | IO_L66N_Y | T4 | |
| 2 | IO_L67P_Y | T5 | |
| 2 | IO_VREF_L67N_Y | T3 | 2 |
| 2 | IO_L68P_YY | T2 | |
| 2 | IO_L68N_YY | U3 | |
| | | | |
| 3 | IO | AE3 | |
| 3 | IO | AF3 | |
| 3 | IO | AH3 | |
| 3 | IO | AK3 | |
| 3 | IO_VREF_L69P_Y | U1 | 2 |
| 3 | IO_L69N_Y | U2 | |
| 3 | IO_L70P_Y | V2 | |
| 3 | IO_VREF_L70N_Y | V4 | |
| 3 | IO_L71P_Y | V5 | |
| 3 | IO_L71N_Y | V3 | |
| 3 | IO_L72P_Y | W1 | |
| 3 | IO_L72N_Y | W3 | |

*Table 14:* **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

| Bank | Pin Description | Pin# | See Note |
|---|---|---|---|
| NA | GND | A29 | |
| NA | GND | A32 | |
| NA | GND | A33 | |
| NA | GND | B1 | |
| NA | GND | B6 | |
| NA | GND | B9 | |
| NA | GND | B15 | |
| NA | GND | B23 | |
| NA | GND | B27 | |
| NA | GND | B31 | |
| NA | GND | C2 | |
| NA | GND | E1 | |
| NA | GND | F32 | |
| NA | GND | G2 | |
| NA | GND | G33 | |
| NA | GND | J32 | |
| NA | GND | K1 | |
| NA | GND | L2 | |
| NA | GND | M33 | |
| NA | GND | P1 | |
| NA | GND | P33 | |
| NA | GND | R32 | |
| NA | GND | T1 | |
| NA | GND | V33 | |
| NA | GND | W2 | |
| NA | GND | Y1 | |
| NA | GND | Y33 | |
| NA | GND | AB1 | |
| NA | GND | AC32 | |
| NA | GND | AD33 | |
| NA | GND | AE2 | |
| NA | GND | AG1 | |
| NA | GND | AG32 | |
| NA | GND | AH2 | |
| NA | GND | AJ33 | |

*Table 14:* **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

| Bank | Pin Description | Pin# | See Note |
|---|---|---|---|
| NA | GND | AL32 | |
| NA | GND | AM3 | |
| NA | GND | AM7 | |
| NA | GND | AM11 | |
| NA | GND | AM19 | |
| NA | GND | AM25 | |
| NA | GND | AM28 | |
| NA | GND | AM33 | |
| NA | GND | AN1 | |
| NA | GND | AN2 | |
| NA | GND | AN5 | |
| NA | GND | AN10 | |
| NA | GND | AN14 | |
| NA | GND | AN16 | |
| NA | GND | AN20 | |
| NA | GND | AN22 | |
| NA | GND | AN27 | |
| NA | GND | AN33 | |

**Notes:**

1. $V_{REF}$ or I/O option only in the XCV2000E; otherwise, I/O option only.
2. $V_{REF}$ or I/O option only in the XCV1600E & 2000E; otherwise, I/O option only.
3. $V_{REF}$ or I/O option only in the XCV1000E, 1600E, & 2000E; otherwise, I/O option only.
4. $V_{REF}$ or I/O option only in the XCV600E, 1000E, 1600E, & 2000E; otherwise, I/O option only.

*Table 15:* **BG560 Differential Pin Pair Summary XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

| Pair | Bank | P Pin | N Pin | AO | Other Functions |
|---|---|---|---|---|---|
| 171 | 7 | J33 | M29 | √ | - |
| 172 | 7 | K31 | L30 | √ | VREF |
| 173 | 7 | H33 | L29 | 4 | - |
| 174 | 7 | H32 | J31 | 18 | VREF |
| 175 | 7 | H31 | K29 | 14 | - |
| 176 | 7 | G32 | J30 | 20 | VREF |
| 177 | 7 | G31 | J29 | √ | VREF |
| 178 | 7 | E32 | E33 | 15 | - |
| 179 | 7 | F31 | H29 | 14 | - |
| 180 | 7 | E31 | D32 | 15 | VREF |
| 181 | 7 | C33 | G29 | 14 | - |
| 182 | 7 | D31 | F30 | 14 | VREF |

**Notes:**
1. AO in the XCV1600E.
2. AO in the XCV2000E.
3. AO in the XCV1600E, 2000E.
4. AO in the XCV1000E, 1600E.
5. AO in the XCV1000E, 2000E.
6. AO in the XCV1000E.
7. AO in the XCV1000E, 1600E, 2000E.
8. AO in the XCV600E, 1600E.
9. AO in the XCV400E, 600E, 1600E.
10. AO in the XCV400E, 600E, 1000E, 2000E.
11. AO in the XCV400E, 600E, 1000E.
12. AO in the XCV400E, 1000E, 2000E.
13. AO in the XCV400E, 600E, 1000E, 1600E.
14. AO in the XCV400E, 1000E, 1600E.
15. AO in the XCV600E, 1000E, 2000E.
16. AO in the XCV600E, 2000E.
17. AO in the XCV400E, 600E, 1600E, 2000E.
18. AO in the XCV600E, 1000E, 1600E, 2000E.
19. AO in the XCV400E, 600E, 2000E.
20. AO in the XCV400E, 1000E.

## FG256 Fine-Pitch Ball Grid Array Packages

XCV50E, XCV100E, XCV200E, and XCV300E devices in FG256 fine-pitch Ball Grid Array packages have footprint compatibility. Pins labeled I0_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as $V_{REF}$, it can be used as general I/O. Immediately following Table 16, see Table 17 for Differential Pair information.

*Table 16:* **FG256 Package — XCV50E, XCV100E, XCV200E, XCV300E**

| Bank | Pin Description | Pin # |
|---|---|---|
| 0 | GCK3 | B8 |
| 0 | IO | B3 |
| 0 | IO | E7 |
| 0 | IO | D8 |
| 0 | IO_L0N_Y | C5 |
| 0 | IO_VREF_L0P_Y | A3[2] |
| 0 | IO_L1N_YY | D5 |
| 0 | IO_L1P_YY | E6 |
| 0 | IO_VREF_L2N_YY | B4 |
| 0 | IO_L2P_YY | A4 |
| 0 | IO_L3N_Y | D6 |
| 0 | IO_L3P_Y | B5 |
| 0 | IO_VREF_L4N_YY | C6[1] |
| 0 | IO_L4P_YY | A5 |
| 0 | IO_L5N_YY | B6 |
| 0 | IO_L5P_YY | C7 |
| 0 | IO_L6N_Y | D7 |
| 0 | IO_L6P_Y | C8 |
| 0 | IO_VREF_L7N_Y | B7 |
| 0 | IO_L7P_Y | A6 |
| 0 | IO_LVDS_DLL_L8N | A7 |
| | | |
| 1 | GCK2 | C9 |
| 1 | IO | B10 |
| 1 | IO_LVDS_DLL_L8P | A8 |
| 1 | IO_L9N_Y | D9 |
| 1 | IO_L9P_Y | A9 |
| 1 | IO_L10N_Y | E10 |
| 1 | IO_VREF_L10P_Y | B9 |

## FG676 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

*Table 21:* **FG676 Differential Pin Pair Summary XCV400E, XCV600E**

| Pair | Bank | P Pin | N Pin | AO | Other Functions |
|---|---|---|---|---|---|
| Global Differential Clock | | | | | |
| 3 | 0 | E13 | B13 | NA | IO_DLL_L21N |
| 2 | 1 | C13 | F14 | NA | IO_DLL_L21P |
| 1 | 5 | AB13 | AF13 | NA | IO_DLL_L115N |
| 0 | 4 | AA14 | AC14 | NA | IO_DLL_L115P |
| IOLVDS<br>Total Pairs: 183, Asynchronous Output Pairs: 97 | | | | | |
| 0 | 0 | F7 | C4 | 1 | - |
| 1 | 0 | C5 | G8 | √ | - |
| 2 | 0 | E7 | D6 | √ | VREF |
| 3 | 0 | F8 | A4 | NA | - |
| 4 | 0 | D7 | B5 | NA | - |
| 5 | 0 | G9 | E8 | √ | VREF |
| 6 | 0 | F9 | A5 | √ | - |
| 7 | 0 | C7 | D8 | 1 | - |
| 8 | 0 | E9 | B7 | 1 | VREF |
| 9 | 0 | D9 | A7 | NA | - |
| 10 | 0 | G10 | B8 | NA | VREF |
| 11 | 0 | F10 | C9 | √ | - |
| 12 | 0 | E10 | A8 | 1 | - |
| 13 | 0 | D10 | G11 | √ | - |
| 14 | 0 | F11 | B10 | √ | - |
| 15 | 0 | E11 | C10 | NA | - |
| 16 | 0 | D11 | G12 | √ | - |
| 17 | 0 | F12 | C11 | √ | VREF |
| 18 | 0 | E12 | A11 | √ | - |
| 19 | 0 | C12 | D12 | 1 | - |
| 20 | 0 | H13 | A12 | 1 | VREF |
| 21 | 1 | F14 | B13 | NA | IO_LVDS_DLL |
| 22 | 1 | F13 | E14 | NA | - |
| 23 | 1 | A14 | D14 | 1 | VREF |
| 24 | 1 | H14 | C14 | 1 | - |
| 25 | 1 | C15 | G14 | √ | - |
| 26 | 1 | D15 | E15 | √ | VREF |
| 27 | 1 | F15 | C16 | √ | - |
| 28 | 1 | D16 | G15 | - | - |
| 29 | 1 | A17 | E16 | √ | - |
| 30 | 1 | E17 | C17 | √ | - |
| 31 | 1 | D17 | F16 | 1 | - |
| 32 | 1 | C18 | F17 | √ | - |
| 33 | 1 | G16 | A18 | √ | VREF |
| 34 | 1 | G17 | C19 | √ | - |
| 35 | 1 | B19 | D18 | 1 | VREF |
| 36 | 1 | E18 | D19 | 1 | - |
| 37 | 1 | B20 | F18 | √ | - |
| 38 | 1 | C20 | G19 | √ | VREF |
| 39 | 1 | E19 | G18 | √ | - |
| 40 | 1 | D20 | A21 | √ | - |
| 41 | 1 | C21 | F19 | √ | VREF |
| 42 | 1 | E20 | B22 | √ | - |
| 43 | 1 | D21 | A23 | 2 | - |
| 44 | 1 | E21 | C22 | √ | CS |
| 45 | 2 | E23 | F22 | √ | DIN, D0 |
| 46 | 2 | E24 | F20 | √ | - |
| 47 | 2 | G21 | G22 | 2 | - |
| 48 | 2 | F24 | H20 | 1 | VREF |
| 49 | 2 | E25 | H21 | 1 | - |
| 50 | 2 | F23 | G23 | √ | - |
| 51 | 2 | H23 | J20 | √ | VREF |

*Table 22:* **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

| Bank | Pin Description | Pin # |
|---|---|---|
| 3 | IO_L97N | AA2 |
| 3 | IO_L98P_YY | AC5 |
| 3 | IO_L98N_YY | AB1 |
| 3 | IO_D4_L99P_YY | AD3 |
| 3 | IO_VREF_L99N_YY | AC1 |
| 3 | IO_L100P_Y | AD1 |
| 3 | IO_L100N_Y | AD4 |
| 3 | IO_L101P | AD2 |
| 3 | IO_L101N | AE3 |
| 3 | IO_L102P_YY | AE1 |
| 3 | IO_L102N_YY | AE4 |
| 3 | IO_L103P_Y | AE2 |
| 3 | IO_VREF_L103N_Y | AF3[1] |
| 3 | IO_L104P | AF4 |
| 3 | IO_L104N | AF1 |
| 3 | IO_L105P | AG3 |
| 3 | IO_L105N | AF2 |
| 3 | IO_L106P_Y | AG4 |
| 3 | IO_L106N_Y | AG1 |
| 3 | IO_L107P_YY | AH3 |
| 3 | IO_D5_L107N_YY | AG2 |
| 3 | IO_D6_L108P_YY | AH1 |
| 3 | IO_VREF_L108N_YY | AJ2 |
| 3 | IO_L109P | AH2 |
| 3 | IO_L109N | AJ3 |
| 3 | IO_L110P_YY | AJ1 |
| 3 | IO_L110N_YY | AJ4 |
| 3 | IO_L111P_YY | AK1 |
| 3 | IO_VREF_L111N_YY | AK3 |
| 3 | IO_L112P | AK2 |
| 3 | IO_L112N | AK4 |
| 3 | IO_L113P | AL1 |
| 3 | IO_VREF_L113N | AL2[3] |
| 3 | IO_L114P_YY | AM1 |
| 3 | IO_L114N_YY | AL3 |
| 3 | IO_L115P_YY | AM2 |
| 3 | IO_VREF_L115N_YY | AL4 |
| 3 | IO_L116P_Y | AM3 |
| 3 | IO_L116N_Y | AN1 |
| 3 | IO_L117P | AM4 |
| 3 | IO_L117N | AP1 |
| 3 | IO_L118P_YY | AN2 |
| 3 | IO_L118N_YY | AP2 |
| 3 | IO_L119P_Y | AN3 |
| 3 | IO_VREF_L119N_Y | AR1 |
| 3 | IO_L120P | AN4 |
| 3 | IO_L120N | AT1 |
| 3 | IO_L121P | AR2 |
| 3 | IO_VREF_L121N | AP4[1] |
| 3 | IO_L122P_Y | AT2 |
| 3 | IO_L122N_Y | AR3 |
| 3 | IO_D7_L123P_YY | AR4 |
| 3 | IO_INIT_L123N_YY | AU2 |
| | | |
| 4 | GCK0 | AW19 |
| 4 | IO | AV3 |
| 4 | IO_L124P_YY | AU4 |
| 4 | IO_L124N_YY | AV5 |
| 4 | IO_L125P_Y | AT6 |
| 4 | IO_L125N_Y | AV4 |
| 4 | IO_VREF_L126P_Y | AU6[1] |
| 4 | IO_L126N_Y | AW4 |
| 4 | IO_L127P_YY | AT7 |
| 4 | IO_L127N_YY | AW5 |
| 4 | IO_VREF_L128P_YY | AU7 |
| 4 | IO_L128N_YY | AV6 |
| 4 | IO_L129P_Y | AT8 |
| 4 | IO_L129N_Y | AW6 |
| 4 | IO_L130P_Y | AU8 |
| 4 | IO_L130N_Y | AV7 |
| 4 | IO_L131P_YY | AT9 |
| 4 | IO_L131N_YY | AW7 |

## FG680 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

*Table 23:* **FG680 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E, XCV2000E**

| Pair | Bank | P Pin | N Pin | AO | Other Functions |
|---|---|---|---|---|---|
| GCLK LVDS | | | | | |
| 3 | 0 | A20 | C22 | NA | IO_DLL_L29N |
| 2 | 1 | D21 | A19 | NA | IO_DLL_L29P |
| 1 | 5 | AU22 | AT22 | NA | IO_DLL_L155N |
| 0 | 4 | AW19 | AT21 | NA | IO_DLL_L155P |
| IO LVDS<br>Total Pairs: 247, Asynchronous Output Pairs: 111 | | | | | |
| 0 | 0 | A36 | C35 | 5 | - |
| 1 | 0 | B35 | D34 | 5 | VREF |
| 2 | 0 | A35 | C34 | √ | - |
| 3 | 0 | B34 | D33 | √ | VREF |
| 4 | 0 | A34 | C33 | 3 | - |
| 5 | 0 | B33 | D32 | 3 | - |
| 6 | 0 | D31 | C32 | √ | - |
| 7 | 0 | C31 | A33 | √ | VREF |
| 8 | 0 | B31 | B32 | 5 | - |
| 9 | 0 | D30 | A32 | 5 | VREF |
| 10 | 0 | C30 | A31 | √ | - |
| 11 | 0 | D29 | B30 | √ | VREF |
| 12 | 0 | C29 | A30 | 2 | - |
| 13 | 0 | B29 | A29 | 2 | - |
| 14 | 0 | A28 | B28 | √ | VREF |
| 15 | 0 | B27 | C28 | √ | - |
| 16 | 0 | A27 | D27 | 5 | - |
| 17 | 0 | B26 | C27 | 5 | - |
| 18 | 0 | C26 | D26 | √ | - |
| 19 | 0 | D25 | A26 | √ | VREF |
| 20 | 0 | C25 | B25 | 3 | - |
| 21 | 0 | D24 | A25 | 3 | - |
| 22 | 0 | B23 | A24 | √ | - |
| 23 | 0 | A23 | C24 | √ | VREF |
| 24 | 0 | B22 | B24 | 5 | - |
| 25 | 0 | A22 | E23 | 5 | - |
| 26 | 0 | B21 | D23 | √ | - |
| 27 | 0 | A21 | C23 | √ | VREF |
| 28 | 0 | B20 | E22 | 2 | - |
| 29 | 1 | A19 | C22 | NA | IO_LVDS_DLL |
| 30 | 1 | B19 | C21 | 2 | VREF |
| 31 | 1 | A18 | C19 | 2 | - |
| 32 | 1 | B18 | D19 | √ | VREF |
| 33 | 1 | A17 | C18 | √ | - |
| 34 | 1 | B17 | D18 | 5 | - |
| 35 | 1 | A16 | E18 | 5 | - |
| 36 | 1 | D17 | C17 | √ | VREF |
| 37 | 1 | E17 | B16 | √ | - |
| 38 | 1 | C16 | A15 | 3 | - |
| 39 | 1 | D16 | B15 | 3 | - |
| 40 | 1 | B14 | A14 | √ | VREF |
| 41 | 1 | A13 | C15 | √ | - |
| 42 | 1 | B13 | D15 | 5 | - |
| 43 | 1 | A12 | C14 | 5 | - |
| 44 | 1 | C13 | D14 | √ | - |
| 45 | 1 | D13 | B12 | √ | VREF |
| 46 | 1 | C12 | A11 | 2 | - |
| 47 | 1 | C11 | B11 | 2 | - |
| 48 | 1 | D11 | A10 | √ | VREF |
| 49 | 1 | C10 | B10 | √ | - |
| 50 | 1 | D10 | A9 | 5 | VREF |
| 51 | 1 | C9 | B9 | 5 | - |

*Table 24:* **FG860 — XCV1000E, XCV1600E, XCV2000E**

| Bank | Pin Description | Pin # |
|---|---|---|
| 1 | IO_L57N_Y | D9 |
| 1 | IO_VREF_L57P_Y | A12[2] |
| 1 | IO_L58N_Y | E9 |
| 1 | IO_L58P_Y | C12 |
| 1 | IO_L59N_YY | B12 |
| 1 | IO_VREF_L59P_YY | D8 |
| 1 | IO_L60N_YY | A11 |
| 1 | IO_L60P_YY | E8 |
| 1 | IO_L61N_Y | C7 |
| 1 | IO_L61P_Y | A10 |
| 1 | IO_L62N_Y | C6 |
| 1 | IO_L62P_Y | B10 |
| 1 | IO_L63N_YY | A9 |
| 1 | IO_VREF_L63P_YY | B9 |
| 1 | IO_L64N_YY | A8 |
| 1 | IO_L64P_YY | E7 |
| 1 | IO_L65N_Y | B8 |
| 1 | IO_L65P_Y | C5 |
| 1 | IO_L66N_Y | A7 |
| 1 | IO_VREF_L66P_Y | A6 |
| 1 | IO_L67N_Y | B7 |
| 1 | IO_L67P_Y | D6 |
| 1 | IO_L68N_Y | A5 |
| 1 | IO_L68P_Y | C4 |
| 1 | IO_WRITE_L69N_YY | B6 |
| 1 | IO_CS_L69P_YY | E6 |
| | | |
| 2 | IO | H2 |
| 2 | IO | H3 |
| 2 | IO | J1 |
| 2 | IO | K5 |
| 2 | IO | M2 |
| 2 | IO | N1 |
| 2 | IO | R5 |
| 2 | IO | U1 |
| 2 | IO | U4 |
| 2 | IO | W3 |

*Table 24:* **FG860 — XCV1000E, XCV1600E, XCV2000E**

| Bank | Pin Description | Pin # |
|---|---|---|
| 2 | IO | Y3 |
| 2 | IO | AA3 |
| 2 | IO_DOUT_BUSY_L70P_YY | F5 |
| 2 | IO_DIN_D0_L70N_YY | D2 |
| 2 | IO_L71P_Y | E4 |
| 2 | IO_L71N_Y | E2 |
| 2 | IO_L72P_Y | D3 |
| 2 | IO_L72N_Y | F2 |
| 2 | IO_VREF_L73P_Y | E1 |
| 2 | IO_L73N_Y | F4 |
| 2 | IO_L74P | G2 |
| 2 | IO_L74N | E3 |
| 2 | IO_L75P_Y | F1 |
| 2 | IO_L75N_Y | G5 |
| 2 | IO_VREF_L76P_Y | G1 |
| 2 | IO_L76N_Y | F3 |
| 2 | IO_L77P_YY | G4 |
| 2 | IO_L77N_YY | H1 |
| 2 | IO_L78P_Y | J2 |
| 2 | IO_L78N_Y | G3 |
| 2 | IO_L79P_Y | H5 |
| 2 | IO_L79N_Y | K2 |
| 2 | IO_VREF_L80P_YY | H4 |
| 2 | IO_L80N_YY | K1 |
| 2 | IO_L81P_YY | L2 |
| 2 | IO_L81N_YY | L3 |
| 2 | IO_VREF_L82P_Y | L1[2] |
| 2 | IO_L82N_Y | J5 |
| 2 | IO_L83P_Y | J4 |
| 2 | IO_L83N_Y | M3 |
| 2 | IO_VREF_L84P_YY | J3 |
| 2 | IO_L84N_YY | M1 |
| 2 | IO_L85P_YY | N2 |
| 2 | IO_L85N_YY | K4 |
| 2 | IO_L86P_Y | N3 |
| 2 | IO_L86N_Y | K3 |
| 2 | IO_VREF_L87P_YY | L5 |

*Table 28:* **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

*Table 28:* **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

| Bank | Pin Description | Pin # |
|---|---|---|
| 4 | IO_L212N_YY | AP18 |
| 4 | IO_L213P_Y | AF18 |
| 4 | IO_L213N_Y | AP17 |
| 4 | IO_VREF_L214P_Y | AJ18[1] |
| 4 | IO_L214N_Y | AL18 |
| 4 | IO_LVDS_DLL_L215P | AM18 |
| | | |
| 5 | GCK1 | AL19 |
| 5 | IO | AF17[3] |
| 5 | IO | AG12[3] |
| 5 | IO | AH12 |
| 5 | IO | AJ10[3] |
| 5 | IO | AJ11[3] |
| 5 | IO | AK7[3] |
| 5 | IO | AK13[3] |
| 5 | IO | AL13[3] |
| 5 | IO | AM4[3] |
| 5 | IO | AN9 |
| 5 | IO | AN10[3] |
| 5 | IO | AN16 |
| 5 | IO | AN17[3] |
| 5 | IO_LVDS_DLL_L215N | AL17 |
| 5 | IO_L216P_Y | AH17 |
| 5 | IO_VREF_L216N_Y | AM17[1] |
| 5 | IO_L217P_Y | AJ17 |
| 5 | IO_L217N_Y | AG17 |
| 5 | IO_L218P_YY | AP16 |
| 5 | IO_VREF_L218N_YY | AL16 |
| 5 | IO_L219P_YY | AJ16 |
| 5 | IO_L219N_YY | AM16 |
| 5 | IO_L220P | AK16[5] |
| 5 | IO_L220N | AP15[4] |
| 5 | IO_L221P_Y | AL15 |
| 5 | IO_L221N_Y | AH16 |
| 5 | IO_L222P_Y | AN15 |
| 5 | IO_L222N_Y | AF16 |
| 5 | IO_L223P_Y | AP14[5] |
| 5 | IO_L223N_Y | AE16[4] |
| 5 | IO_L224P_YY | AK15 |
| 5 | IO_VREF_L224N_YY | AJ15 |
| 5 | IO_L225P_YY | AH15 |
| 5 | IO_L225N_YY | AN14 |
| 5 | IO_L226P | AK14[5] |
| 5 | IO_L226N | AG15[4] |
| 5 | IO_L227P_Y | AM13 |
| 5 | IO_L227N_Y | AF15 |
| 5 | IO_L228P_Y | AG14 |
| 5 | IO_L228N_Y | AP13 |
| 5 | IO_L229P_YY | AE14[5] |
| 5 | IO_L229N_YY | AE15[4] |
| 5 | IO_L230P_YY | AN13 |
| 5 | IO_VREF_L230N_YY | AG13 |
| 5 | IO_L231P_YY | AH14 |
| 5 | IO_L231N_YY | AP12 |
| 5 | IO_L232P_Y | AJ14 |
| 5 | IO_L232N_Y | AL14 |
| 5 | IO_L233P_Y | AF13 |
| 5 | IO_L233N_Y | AN12 |
| 5 | IO_L234P_Y | AF14 |
| 5 | IO_L234N_Y | AP11 |
| 5 | IO_L235P_Y | AN11 |
| 5 | IO_L235N_Y | AH13 |
| 5 | IO_L236P_YY | AM12 |
| 5 | IO_L236N_YY | AL12 |
| 5 | IO_L237P_YY | AJ13 |
| 5 | IO_VREF_L237N_YY | AP10 |
| 5 | IO_L238P_Y | AK12 |
| 5 | IO_L238N_Y | AM10 |

*Table 29:* **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

| Pair | Bank | P Pin | N Pin | AO | Other Functions |
|---|---|---|---|---|---|
| 111 | 2 | M31 | R26 | 2600 1600 | - |
| 112 | 2 | N30 | P28 | 3200 1600 1000 | - |
| 113 | 2 | N29 | N33 | 2600 2000 1000 | VREF |
| 114 | 2 | T25 | N34 | 3200 2600 2000 1600 | - |
| 115 | 2 | P34 | R27 | 3200 2600 2000 1600 1000 | - |
| 116 | 2 | P29 | P31 | 3200 2600 1600 1000 | - |
| 117 | 2 | P33 | T26 | 3200 2600 2000 | - |
| 118 | 2 | R34 | R28 | 2600 2000 1000 | - |
| 119 | 2 | N31 | N32 | 2000 1600 1000 | D3 |
| 120 | 2 | P30 | R33 | 2000 1600 | - |
| 121 | 2 | R29 | T34 | 3200 2600 2000 1600 1000 | - |
| 122 | 2 | R30 | T30 | 1000 | - |
| 123 | 2 | T28 | R31 | 3200 1600 | - |
| 124 | 2 | T29 | U27 | 3200 2600 1600 1000 | - |
| 125 | 2 | T31 | T33 | 2000 1600 1000 | VREF |
| 126 | 2 | U28 | T32 | 2000 1600 1000 | - |
| 127 | 2 | U29 | U33 | 3200 2600 1600 1000 | VREF |
| 128 | 2 | V33 | U31 | 3200 2600 2000 1600 1000 | - |
| 129 | 3 | V26 | V30 | 3200 2600 1600 1000 | VREF |
| 130 | 3 | W34 | V28 | 2000 1600 1000 | - |
| 131 | 3 | W32 | W30 | 2000 1600 1000 | VREF |

*Table 29:* **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

| Pair | Bank | P Pin | N Pin | AO | Other Functions |
|---|---|---|---|---|---|
| 132 | 3 | V29 | Y34 | 3200 2600 1600 1000 | - |
| 133 | 3 | W29 | Y33 | 3200 1600 | - |
| 134 | 3 | W26 | W28 | 1000 | - |
| 135 | 3 | Y31 | Y30 | 3200 2600 2000 1600 1000 | - |
| 136 | 3 | AA34 | W31 | 2000 1600 | - |
| 137 | 3 | AA33 | Y29 | 2000 1600 1000 | VREF |
| 138 | 3 | W25 | AB34 | 2600 2000 1000 | - |
| 139 | 3 | Y28 | AB33 | 3200 2600 2000 | - |
| 140 | 3 | AA30 | Y26 | 3200 2600 1600 1000 | - |
| 141 | 3 | Y27 | AA31 | 3200 2600 2000 1600 1000 | - |
| 142 | 3 | AA27 | AA29 | 3200 2600 2000 1600 | - |
| 143 | 3 | AB32 | AB29 | 2600 2000 1000 | VREF |
| 144 | 3 | AA28 | AC34 | 3200 1600 1000 | - |
| 145 | 3 | Y25 | AD34 | 2600 1600 | - |
| 146 | 3 | AB30 | AC33 | 3200 2600 1600 1000 | - |
| 147 | 3 | AA26 | AC32 | 2000 1000 | - |
| 148 | 3 | AD33 | AB28 | 3200 2600 2000 | - |
| 149 | 3 | AE34 | AB27 | 3200 2600 2000 1600 1000 | D5 |
| 150 | 3 | AE33 | AC30 | 2000 1600 1000 | VREF |
| 151 | 3 | AA25 | AE32 | 3200 1600 1000 | - |
| 152 | 3 | AE31 | AD29 | 3200 2600 2000 1600 1000 | - |

*Table 29:* **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

| Pair | Bank | P Pin | N Pin | AO | Other Functions |
|---|---|---|---|---|---|
| 153 | 3 | AD31 | AF33 | 3200 2600 2000 1600 1000 | VREF |
| 154 | 3 | AC28 | AF31 | 3200 2600 1600 1000 | - |
| 155 | 3 | AC27 | AF32 | 3200 2600 1600 | - |
| 156 | 3 | AE29 | AD28 | 2600 1000 | VREF |
| 157 | 3 | AD30 | AG32 | 3200 2600 2000 1600 1000 | - |
| 158 | 3 | AC26 | AH33 | 2000 1600 | - |
| 159 | 3 | AD26 | AF30 | 3200 2600 2000 1600 1000 | VREF |
| 160 | 3 | AC25 | AH32 | 2600 2000 1000 | - |
| 161 | 3 | AE28 | AL34 | 3200 2600 2000 | - |
| 162 | 3 | AG30 | AD27 | 3200 2600 1600 1000 | - |
| 163 | 3 | AF29 | AK34 | 3200 2600 2000 1600 1000 | - |
| 164 | 3 | AD25 | AE27 | 3200 2600 2000 1600 | - |
| 165 | 3 | AJ33 | AH31 | 2600 2000 1000 | VREF |
| 166 | 3 | AE26 | AL33 | 3200 2600 1600 1000 | - |
| 167 | 3 | AF28 | AL32 | 2600 1600 | - |
| 168 | 3 | AJ31 | AF27 | 3200 2600 1600 1000 | VREF |
| 169 | 3 | AG29 | AJ32 | 2600 2000 1000 | - |
| 170 | 3 | AK33 | AH30 | 3200 2600 2000 | - |
| 171 | 3 | AK32 | AK31 | 3200 2600 2000 1600 1000 | INIT |

*Table 29:* **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

| Pair | Bank | P Pin | N Pin | AO | Other Functions |
|---|---|---|---|---|---|
| 172 | 4 | AP31 | AK29 | 3200 2600 2000 1600 1000 | - |
| 173 | 4 | AP30 | AN31 | 3200 1600 1000 | - |
| 174 | 4 | AH27 | AN30 | 3200 2000 1000 | - |
| 175 | 4 | AM30 | AK28 | 3200 2000 1000 | VREF |
| 176 | 4 | AG26 | AN29 | 3200 2600 1000 | - |
| 177 | 4 | AF25 | AM29 | 3200 2600 2000 1600 1000 | - |
| 178 | 4 | AL29 | AL28 | 3200 2600 2000 1600 1000 | VREF |
| 179 | 4 | AE24 | AN28 | 2000 1600 | - |
| 180 | 4 | AJ27 | AH26 | 3200 1000 | - |
| 181 | 4 | AG25 | AK27 | 3200 1000 | - |
| 182 | 4 | AM28 | AF24 | 3200 2600 | - |
| 183 | 4 | AJ26 | AP27 | 3200 2600 2000 1600 1000 | - |
| 184 | 4 | AK26 | AN27 | 3200 2600 2000 1600 1000 | VREF |
| 185 | 4 | AE23 | AM27 | 3200 1600 | - |
| 186 | 4 | AL26 | AP26 | 3200 2000 1000 | - |
| 187 | 4 | AN26 | AJ25 | 3200 2000 1000 | VREF |
| 188 | 4 | AG24 | AP25 | 3200 2600 | - |
| 189 | 4 | AF23 | AM26 | 3200 2600 2000 1600 1000 | - |
| 190 | 4 | AJ24 | AN25 | 3200 2600 2000 1600 1000 | VREF |
| 191 | 4 | AE22 | AM25 | 2600 1600 1000 | - |