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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	3456
Number of Logic Elements/Cells	15552
Total RAM Bits	294912
Number of I/O	512
Number of Gates	985882
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	680-LBGA Exposed Pad
Supplier Device Package	680-FTEBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv600e-8fg680c

Table 1: Virtex-E Field-Programmable Gate Array Family Members

Device	System Gates	Logic Gates	CLB Array	Logic Cells	Differential I/O Pairs	User I/O	BlockRAM Bits	Distributed RAM Bits
XCV50E	71,693	20,736	16 x 24	1,728	83	176	65,536	24,576
XCV100E	128,236	32,400	20 x 30	2,700	83	196	81,920	38,400
XCV200E	306,393	63,504	28 x 42	5,292	119	284	114,688	75,264
XCV300E	411,955	82,944	32 x 48	6,912	137	316	131,072	98,304
XCV400E	569,952	129,600	40 x 60	10,800	183	404	163,840	153,600
XCV600E	985,882	186,624	48 x 72	15,552	247	512	294,912	221,184
XCV1000E	1,569,178	331,776	64 x 96	27,648	281	660	393,216	393,216
XCV1600E	2,188,742	419,904	72 x 108	34,992	344	724	589,824	497,664
XCV2000E	2,541,952	518,400	80 x 120	43,200	344	804	655,360	614,400
XCV2600E	3,263,755	685,584	92 x 138	57,132	344	804	753,664	812,544
XCV3200E	4,074,387	876,096	104 x 156	73,008	344	804	851,968	1,038,336

Virtex-E Compared to Virtex Devices

The Virtex-E family offers up to 43,200 logic cells in devices up to 30% faster than the Virtex family.

I/O performance is increased to 622 Mb/s using Source Synchronous data transmission architectures and synchronous system performance up to 240 MHz using singled-ended SelectI/O technology. Additional I/O standards are supported, notably LVPECL, LVDS, and BLVDS, which use two pins per signal. Almost all signal pins can be used for these new standards.

Virtex-E devices have up to 640 Kb of faster (250 MHz) block SelectRAM, but the individual RAMs are the same size and structure as in the Virtex family. They also have eight DLLs instead of the four in Virtex devices. Each individual DLL is slightly improved with easier clock mirroring and 4x frequency multiplication.

V_{CCINT} , the supply voltage for the internal logic and memory, is 1.8 V, instead of 2.5 V for Virtex devices. Advanced processing and 0.18 μ m design rules have resulted in smaller dice, faster speed, and lower power consumption.

I/O pins are 3 V tolerant, and can be 5 V tolerant with an external 100 Ω resistor. PCI 5 V is not supported. With the addition of appropriate external resistors, any pin can tolerate any voltage desired.

Banking rules are different. With Virtex devices, all input buffers are powered by V_{CCINT} . With Virtex-E devices, the LVTTTL, LVCMOS2, and PCI input buffers are powered by the I/O supply voltage V_{CCO} .

The Virtex-E family is not bitstream-compatible with the Virtex family, but Virtex designs can be compiled into equivalent Virtex-E devices.

The same device in the same package for the Virtex-E and Virtex families are pin-compatible with some minor exceptions. See the data sheet pinout section for details.

General Description

The Virtex-E FPGA family delivers high-performance, high-capacity programmable logic solutions. Dramatic increases in silicon efficiency result from optimizing the new architecture for place-and-route efficiency and exploiting an aggressive 6-layer metal 0.18 μ m CMOS process. These advances make Virtex-E FPGAs powerful and flexible alternatives to mask-programmed gate arrays. The Virtex-E family includes the nine members in Table 1.

Building on experience gained from Virtex FPGAs, the Virtex-E family is an evolutionary step forward in programmable logic design. Combining a wide variety of programmable system features, a rich hierarchy of fast, flexible interconnect resources, and advanced process technology, the Virtex-E family delivers a high-speed and high-capacity programmable logic solution that enhances design flexibility while reducing time-to-market.

Virtex-E Architecture

Virtex-E devices feature a flexible, regular architecture that comprises an array of configurable logic blocks (CLBs) surrounded by programmable input/output blocks (IOBs), all interconnected by a rich hierarchy of fast, versatile routing

Data Registers

The primary data register is the Boundary Scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out, and 3-State Control. Non-IOB pins have appropriate partial bit population if input-only or output-only. Each EXTEST CAPTURED-OR state captures all In, Out, and 3-state pins.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream Boundary Scan device.

The FPGA supports up to two additional internal scan chains that can be specified using the BSCAN macro. The macro provides two user pins (SEL1 and SEL2) which are decodes of the USER1 and USER2 instructions respectively. For these instructions, two corresponding pins (TDO1 and TDO2) allow user scan data to be shifted out of TDO.

Likewise, there are individual clock pins (DRCK1 and DRCK2) for each user register. There is a common input pin (TDI) and shared output pins that represent the state of the TAP controller (RESET, SHIFT, and UPDATE).

Bit Sequence

The order within each IOB is: In, Out, 3-State. The input-only pins contribute only the In bit to the Boundary Scan I/O data register, while the output-only pins contribute all three bits.

From a cavity-up view of the chip (as shown in EPIC), starting in the upper right chip corner, the Boundary Scan data-register bits are ordered as shown in [Figure 12](#).

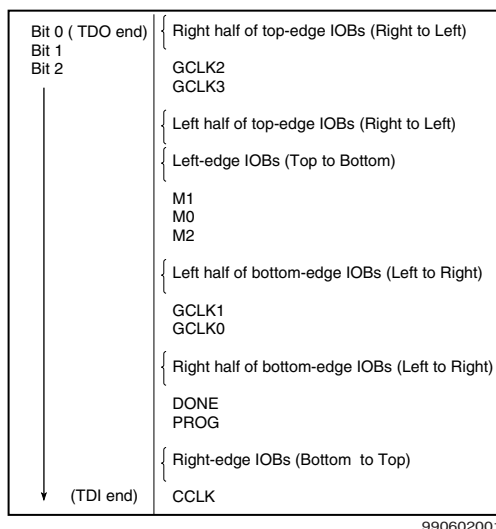


Figure 12: Boundary Scan Bit Sequence

BSDL (Boundary Scan Description Language) files for Virtex-E Series devices are available on the Xilinx web site in the File Download area.

Identification Registers

The IDCODE register is supported. By using the IDCODE, the device connected to the JTAG port can be determined.

The IDCODE register has the following binary format:

vvvv:ffff:ffa:aaaa:aaaa:cccc:cccc:ccc1

where

v = the die version number

f = the family code (05 for Virtex-E family)

a = the number of CLB rows (ranges from 16 for XCV50E to 104 for XCV3200E)

c = the company code (49h for Xilinx)

The USERCODE register is supported. By using the USERCODE, a user-programmable identification code can be loaded and shifted out for examination. The identification code (see [Table 7](#)) is embedded in the bitstream during bitstream generation and is valid only after configuration.

Table 7: IDCODEs Assigned to Virtex-E FPGAs

FPGA	IDCODE
XCV50E	v0A10093h
XCV100E	v0A14093h
XCV200E	v0A1C093h
XCV300E	v0A20093h
XCV400E	v0A28093h
XCV600E	v0A30093h
XCV1000E	v0A40093h
XCV1600E	v0A48093h
XCV2000E	v0A50093h
XCV2600E	v0A5C093h
XCV3200E	v0A68093h

Note:

Attempting to load an incorrect bitstream causes configuration to fail and can damage the device.

Including Boundary Scan in a Design

Since the Boundary Scan pins are dedicated, no special element needs to be added to the design unless an internal data register (USER1 or USER2) is desired.

If an internal data register is used, insert the Boundary Scan symbol and connect the necessary pins as appropriate.

Table 9 lists the total number of bits required to configure each device.

Table 9: Virtex-E Bitstream Lengths

Device	# of Configuration Bits
XCV50E	630,048
XCV100E	863,840
XCV200E	1,442,016
XCV300E	1,875,648
XCV400E	2,693,440
XCV600E	3,961,632
XCV1000E	6,587,520
XCV1600E	8,308,992
XCV2000E	10,159,648
XCV2600E	12,922,336
XCV3200E	16,283,712

Slave-Serial Mode

In slave-serial mode, the FPGA receives configuration data in bit-serial form from a serial PROM or other source of serial configuration data. The serial bitstream must be set up at the DIN input pin a short time before each rising edge of an externally generated CCLK.

Table 10: Master/Slave Serial Mode Programming Switching

	Description	Figure References	Symbol	Values	Units
CCLK	DIN setup/hold, slave mode	1/2	T_{DCC}/T_{CCD}	5.0 / 0.0	ns, min
	DIN setup/hold, master mode	1/2	T_{DSCK}/T_{CKDS}	5.0 / 0.0	ns, min
	DOUT	3	T_{CCO}	12.0	ns, max
	High time	4	T_{CCH}	5.0	ns, min
	Low time	5	T_{CCL}	5.0	ns, min
	Maximum Frequency		F_{CC}	66	MHz, max
	Frequency Tolerance, master mode with respect to nominal			+45% –30%	

For more detailed information on serial PROMs, see the PROM data sheet at <http://www.xilinx.com/bvdocs/publications/ds026.pdf>.

Multiple FPGAs can be daisy-chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed to the DOUT pin. The maximum capacity for a single LOUT/DOUT write is $2^{20}-1$ (1,048,575) 32-bit words, or 33,554,400 bits. The data on the DOUT pin changes on the rising edge of CCLK.

The change of DOUT on the rising edge of CCLK differs from previous families, but does not cause a problem for mixed configuration chains. This change was made to improve serial configuration rates for Virtex and Virtex-E only chains.

Figure 13 shows a full master/slave system. A Virtex-E device in slave-serial mode should be connected as shown in the right-most device.

Slave-serial mode is selected by applying <111> or <011> to the mode pins (M2, M1, M0). A weak pull-up on the mode pins makes slave serial the default mode if the pins are left unconnected. However, it is recommended to drive the configuration mode pins externally. Figure 14 shows slave-serial mode programming switching characteristics.

Table 10 provides more detail about the characteristics shown in Figure 14. Configuration must be delayed until the INIT pins of all daisy-chained FPGAs are High.

Configuration through the TAP uses the CFG_IN instruction. This instruction allows data input on TDI to be converted into data packets for the internal configuration bus.

The following steps are required to configure the FPGA through the Boundary Scan port (when using TCK as a start-up clock).

1. Load the CFG_IN instruction into the Boundary Scan instruction register (IR).
2. Enter the Shift-DR (SDR) state.
3. Shift a configuration bitstream into TDI.
4. Return to Run-Test-Idle (RTI).
5. Load the JSTART instruction into IR.
6. Enter the SDR state.
7. Clock TCK through the startup sequence.
8. Return to RTI.

Configuration and readback via the TAP is always available. The Boundary Scan mode is selected by a <101> or <001> on the mode pins (M2, M1, M0). For details on TAP characteristics, refer to XAPP139.

Configuration Sequence

The configuration of Virtex-E devices is a three-phase process. First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user, as described below. The configuration process can also be initiated by asserting $\overline{\text{PROGRAM}}$. The end of the memory-clearing phase is signalled by $\overline{\text{INIT}}$ going High, and the completion of the entire process is signalled by DONE going High.

The power-up timing of configuration signals is shown in Figure 20.

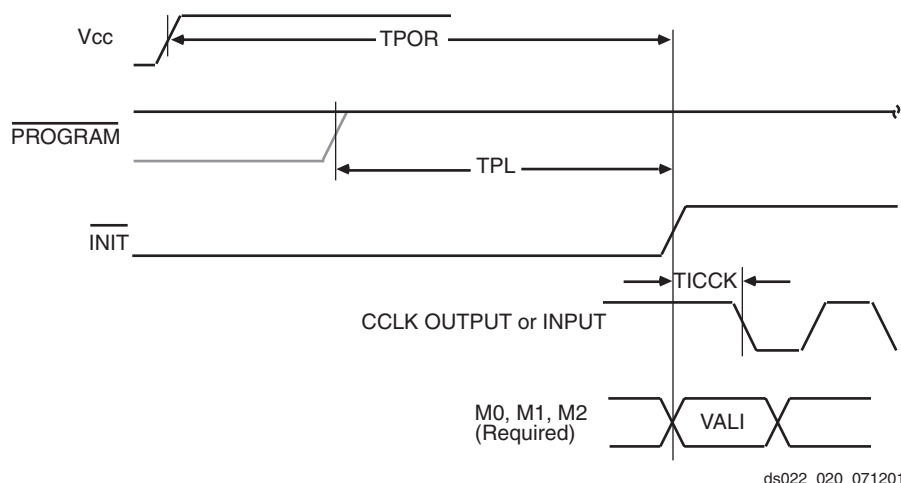


Figure 20: Power-Up Timing Configuration Signals

The corresponding timing characteristics are listed in Table 12.

Table 12: Power-up Timing Characteristics

Description	Symbol	Value	Units
Power-on Reset ¹	T_{POR}	2.0	ms, max
Program Latency	T_{PL}	100.0	μs , max
CCLK (output) Delay	T_{ICCK}	0.5	μs , min
		4.0	μs , max
Program Pulse Width	T_{PROGRAM}	300	ns, min

Notes:

1. T_{POR} delay is the initialization time required after V_{CCINT} and V_{CCO} in Bank 2 reach the recommended operating voltage.

Delaying Configuration

$\overline{\text{INIT}}$ can be held Low using an open-drain driver. An open-drain is required since $\overline{\text{INIT}}$ is a bidirectional open-drain pin that is held Low by the FPGA while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

Start-Up Sequence

The default Start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary.

One CCLK cycle later, the Global Set/Reset (GSR) and Global Write Enable (GWE) signals are released. This permits

SSTL2_II

A sample circuit illustrating a valid termination technique for SSTL2_II appears in Figure 52. DC voltage specifications appear in Table 31.

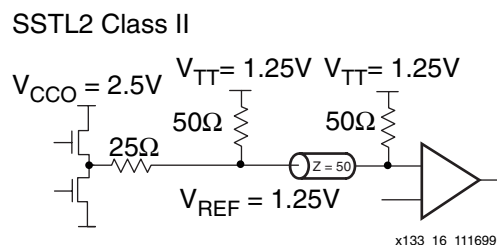


Figure 52: Terminated SSTL2 Class II

Table 31: SSTL2_II Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
$V_{REF} = 0.5 \times V_{CCO}$	1.15	1.25	1.35
$V_{TT} = V_{REF} + N^{(1)}$	1.11	1.25	1.39
$V_{IH} = V_{REF} + 0.18$	1.33	1.43	3.0 ⁽²⁾
$V_{IL} = V_{REF} - 0.18$	-0.3 ⁽³⁾	1.07	1.17
$V_{OH} = V_{REF} + 0.8$	1.95	-	-
$V_{OL} = V_{REF} - 0.8$	-	-	0.55
I_{OH} at V_{OH} (mA)	-15.2	-	-
I_{OL} at V_{OL} (mA)	15.2	-	-

Notes:

1. N must be greater than or equal to -0.04 and less than or equal to 0.04.
2. V_{IH} maximum is $V_{CCO} + 0.3$.
3. V_{IL} minimum does not conform to the formula.

CTT

A sample circuit illustrating a valid termination technique for CTT appear in Figure 53. DC voltage specifications appear in Table 32.

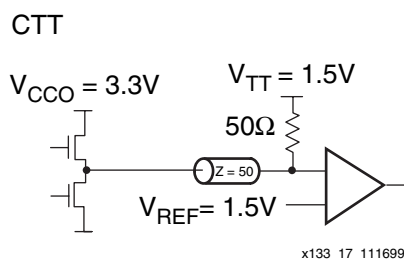


Figure 53: Terminated CTT

Table 32: CTT Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	2.05 ⁽¹⁾	3.3	3.6
V_{REF}	1.35	1.5	1.65
V_{TT}	1.35	1.5	1.65
$V_{IH} = V_{REF} + 0.2$	1.55	1.7	-
$V_{IL} = V_{REF} - 0.2$	-	1.3	1.45
$V_{OH} = V_{REF} + 0.4$	1.75	1.9	-
$V_{OL} = V_{REF} - 0.4$	-	1.1	1.25
I_{OH} at V_{OH} (mA)	-8	-	-
I_{OL} at V_{OL} (mA)	8	-	-

Notes:

1. Timing delays are calculated based on V_{CCO} min of 3.0V.

PCI33_3 & PCI66_3

PCI33_3 or PCI66_3 require no termination. DC voltage specifications appear in Table 33.

Table 33: PCI33_3 and PCI66_3 Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
V_{REF}	-	-	-
V_{TT}	-	-	-
$V_{IH} = 0.5 \times V_{CCO}$	1.5	1.65	$V_{CCO} + 0.5$
$V_{IL} = 0.3 \times V_{CCO}$	-0.5	0.99	1.08
$V_{OH} = 0.9 \times V_{CCO}$	2.7	-	-
$V_{OL} = 0.1 \times V_{CCO}$	-	-	0.36
I_{OH} at V_{OH} (mA)	Note 1	-	-
I_{OL} at V_{OL} (mA)	Note 1	-	-

Notes:

1. Tested according to the relevant specification.

Table 42: Input Library Macros

Name	Inputs	Outputs
IBUFDS_FD_LVDS	I, IB, C	Q
IBUFDS_FDE_LVDS	I, IB, CE, C	Q
IBUFDS_FDC_LVDS	I, IB, C, CLR	Q
IBUFDS_FDCE_LVDS	I, IB, CE, C, CLR	Q
IBUFDS_FDP_LVDS	I, IB, C, PRE	Q
IBUFDS_FDPE_LVDS	I, IB, CE, C, PRE	Q
IBUFDS_FDR_LVDS	I, IB, C, R	Q
IBUFDS_FDRE_LVDS	I, IB, CE, C, R	Q
IBUFDS_FDS_LVDS	I, IB, C, S	Q
IBUFDS_FDSE_LVDS	I, IB, CE, C, S	Q
IBUFDS_LD_LVDS	I, IB, G	Q
IBUFDS_LDE_LVDS	I, IB, GE, G	Q
IBUFDS_LDC_LVDS	I, IB, G, CLR	Q
IBUFDS_LDCE_LVDS	I, IB, GE, G, CLR	Q
IBUFDS_LDP_LVDS	I, IB, G, PRE	Q
IBUFDS_LDPE_LVDS	I, IB, GE, G, PRE	Q

Creating LVDS Output Buffers

LVDS output buffers can be placed in a wide number of IOB locations. The exact locations are dependent on the package used. The Virtex-E package information lists the possible locations as IO_L#P for the P-side and IO_L#N for the N-side, where # is the pair number.

HDL Instantiation

Both output buffers are required to be instantiated in the design and placed on the correct IO_L#P and IO_L#N locations. The IOB must have the same net source the following pins, clock (C), set/reset (SR), output (O), output clock enable (OCE). In addition, the output (O) pins must be inverted with respect to each other, and if output registers are used, the INIT states must be opposite values (one HIGH and one LOW). Failure to follow these rules leads to DRC errors in software.

VHDL Instantiation

```
data0_p : OBUF_LVDS port map
(I=>data_int(0), O=>data_p(0));

data0_inv: INV      port map
(I=>data_int(0), O=>data_n_int(0));

data0_n : OBUF_LVDS port map
(I=>data_n_int(0), O=>data_n(0));
```

Verilog Instantiation

```
OBUF_LVDS data0_p (.I(data_int[0]),
.O(data_p[0]));

INV      data0_inv (.I(data_int[0],
.O(data_n_int[0]));

OBUF_LVDS data0_n (.I(data_n_int[0]),
.O(data_n[0]));
```

Location Constraints

All LVDS buffers must be explicitly placed on a device. For the output buffers this can be done with the following constraint in the .ucf or .ncf file.

```
NET data_p<0> LOC = D28; # IO_L0P
NET data_n<0> LOC = B29; # IO_L0N
```

Synchronous vs. Asynchronous Outputs

If the outputs are synchronous (registered in the IOB) then any IO_L#PIN pair can be used. If the outputs are asynchronous (no output register), then they must use one of the pairs that are part of the same IOB group at the end of a ROW or COLUMN in the device.

The LVDS pairs that can be used as asynchronous outputs are listed in the Virtex-E pinout tables. Some pairs are marked as asynchronous-capable for all devices in that package, and others are marked as available only for that device in the package. If the device size might change at some point in the product lifetime, then only the common pairs for all packages should be used.

Adding an Output Register

All LVDS buffers can have an output register in the IOB. The output registers must be in both the P-side and N-side IOBs. All the normal IOB register options are available (FD, FDE, FDC, FDCE, FDP, FDPE, FDR, FDRE, FDS, FDSE, LD, LDE, LDC, LDCE, LDP, LDPE). The register elements can be inferred or explicitly instantiated in the HDL code.

Special care must be taken to insure that the D pins of the registers are inverted and that the INIT states of the registers are opposite. The clock pin (C), clock enable (CE) and set/reset (CLR/PRE or S/R) pins must connect to the same source. Failure to do this leads to a DRC error in the software.

The register elements can be packed in the IOB using the IOB property to TRUE on the register or by using the “map-pr [ilolb]” where “i” is inputs only, “o” is outputs only and “b” is both inputs and outputs.

To improve design coding times VHDL and Verilog synthesis macro libraries have been developed to explicitly create these structures. The output library macros are listed in Table 43. The O and OB inputs to the macros are the external net connections.

Table 2: IOB Input Switching Characteristics (Continued)

			Speed Grade ⁽¹⁾				Units
Description ⁽²⁾	Symbol	Device	Min	-8	-7	-6	
Sequential Delays							
Clock CLK							
Minimum Pulse Width, High	T _{CH}	All	0.56	1.2	1.3	1.4	ns, min
Minimum Pulse Width, Low	T _{CL}		0.56	1.2	1.3	1.4	ns, min
Clock CLK to output IQ	T _{IOCKIQ}		0.18	0.4	0.7	0.7	ns, max
Setup and Hold Times with respect to Clock at IOB Input Register							
Pad, no delay	T _{IOPICK} / T _{IOICKP}	All	0.69 / 0	1.3 / 0	1.4 / 0	1.5 / 0	ns, min
Pad, with delay	T _{IOPICKD} / T _{IOICKPD}	XCV50E	1.25 / 0	2.8 / 0	2.9 / 0	2.9 / 0	ns, min
		XCV100E	1.25 / 0	2.8 / 0	2.9 / 0	2.9 / 0	ns, min
		XCV200E	1.33 / 0	3.0 / 0	3.1 / 0	3.1 / 0	ns, min
		XCV300E	1.33 / 0	3.0 / 0	3.1 / 0	3.1 / 0	ns, min
		XCV400E	1.37 / 0	3.1 / 0	3.2 / 0	3.2 / 0	ns, min
		XCV600E	1.49 / 0	3.4 / 0	3.5 / 0	3.5 / 0	ns, min
		XCV1000E	1.49 / 0	3.4 / 0	3.5 / 0	3.5 / 0	ns, min
		XCV1600E	1.53 / 0	3.5 / 0	3.6 / 0	3.6 / 0	ns, min
		XCV2000E	1.53 / 0	3.5 / 0	3.6 / 0	3.6 / 0	ns, min
		XCV2600E	1.53 / 0	3.5 / 0	3.6 / 0	3.6 / 0	ns, min
XCV3200E	1.53 / 0	3.5 / 0	3.6 / 0	3.6 / 0	ns, min		
ICE input	T _{IOICECK} / T _{IOCKICE}	All	0.28 / 0.0	0.55 / 0.01	0.7 / 0.01	0.7 / 0.01	ns, min
SR input (IFF, synchronous)	T _{IOSRCKI}	All	0.38	0.8	0.9	1.0	ns, min
Set/Reset Delays							
SR input to IQ (asynchronous)	T _{IOSRIQ}	All	0.54	1.1	1.2	1.4	ns, max
GSR to output IQ	T _{GSRQ}	All	3.88	7.6	8.5	9.7	ns, max

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. Input timing t_i for LVTTTL is measured at 1.4 V. For other I/O standards, see Table 4.

Virtex-E Pin Definitions

Pin Name	Dedicated Pin	Direction	Description
GCK0, GCK1, GCK2, GCK3	Yes	Input	Clock input pins that connect to Global Clock Buffers.
M0, M1, M2	Yes	Input	Mode pins are used to specify the configuration mode.
CCLK	Yes	Input or Output	The configuration Clock I/O pin: it is an input for SelectMAP and slave-serial modes, and output in master-serial mode. After configuration, it is input only, logic level = Don't Care.
PROGRAM	Yes	Input	Initiates a configuration sequence when asserted Low.
DONE	Yes	Bidirectional	Indicates that configuration loading is complete, and that the start-up sequence is in progress. The output can be open drain.
INIT	No	Bidirectional (Open-drain)	When Low, indicates that the configuration memory is being cleared. The pin becomes a user I/O after configuration.
BUSY/DOUT	No	Output	In SelectMAP mode, BUSY controls the rate at which configuration data is loaded. The pin becomes a user I/O after configuration unless the SelectMAP port is retained. In bit-serial modes, DOUT provides preamble and configuration data to downstream devices in a daisy-chain. The pin becomes a user I/O after configuration.
D0/DIN, D1, D2, D3, D4, D5, D6, D7	No	Input or Output	In SelectMAP mode, D0-7 are configuration data pins. These pins become user I/Os after configuration unless the SelectMAP port is retained. In bit-serial modes, DIN is the single data input. This pin becomes a user I/O after configuration.
WRITE	No	Input	In SelectMAP mode, the active-low Write Enable signal. The pin becomes a user I/O after configuration unless the SelectMAP port is retained.
CS	No	Input	In SelectMAP mode, the active-low Chip Select signal. The pin becomes a user I/O after configuration unless the SelectMAP port is retained.
TDI, TDO, TMS, TCK	Yes	Mixed	Boundary-scan Test-Access-Port pins, as defined in IEEE1149.1.
DXN, DXP	Yes	N/A	Temperature-sensing diode pins. (Anode: DXP, cathode: DXN)
V _{CCINT}	Yes	Input	Power-supply pins for the internal core logic.
V _{CCO}	Yes	Input	Power-supply pins for the output drivers (subject to banking rules)
V _{REF}	No	Input	Input threshold voltage pins. Become user I/Os when an external threshold voltage is not needed (subject to banking rules).
GND	Yes	Input	Ground

Table 7: PQ240 Differential Pin Pair Summary
XCV50E, XCV100E, XCV200E, XCV300E, XCV400E

Pair	Bank	P Pin	N Pin	AO	Other Functions
48	6	P56	P57	√	-
49	6	P52	P53	2	-
50	6	P49	P50	3	VREF
51	6	P46	P47	4	VREF
52	6	P41	P42	√	-
53	6	P38	P39	2	-
54	6	P35	P36	4	VREF
55	6	P33	P34	5	VREF
56	7	P27	P28	√	-
57	7	P23	P24	4	VREF
58	7	P20	P21	2	-
59	7	P17	P18	√	-
60	7	P12	P13	4	VREF
61	7	P9	P10	3	VREF
62	7	P6	P7	2	-
63	7	P4	P5	6	VREF

Notes:

1. AO in the XCV50E.
2. AO in the XCV50E, 100E, 200E, 300E.
3. AO in the XCV50E, 200E, 300E, 400E.
4. AO in the XCV50E, 300E, 400E.
5. AO in the XCV100E, 200E, 400E.
6. AO in the XCV100E, 400E.
7. AO in the XCV50E, 200E, 400E.
8. AO in the XCV100E.

HQ240 High-Heat Quad Flat-Pack Packages

XCV600E and XCV1000E devices in High-heat dissipation Quad Flat-pack packages have footprint compatibility. Pins labeled IO_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF} it can be used as general I/O. Immediately following Table 8, see Table 9 for Differential Pair information.

Table 8: HQ240 — XCV600E, XCV1000E

Pin #	Pin Description	Bank
P240	VCCO	7
P239	TCK	NA
P238	IO	0
P237	IO_L0N	0
P236	IO_VREF_L0P	0
P235	IO_L1N_YY	0
P234	IO_L1P_YY	0
P233	GND	NA
P232	VCCO	0
P231	IO_VREF	0
P230	IO_VREF	0
P229	IO_VREF_L2N_YY	0
P228	IO_L2P_YY	0
P227	GND	NA
P226	VCCO	0
P225	VCCINT	NA
P224	IO_L3N_YY	0
P223	IO_L3P_YY	0
P222	IO_VREF	0 ¹
P221	IO_L4N_Y	0
P220	IO_L4P_Y	0
P219	GND	NA
P218	IO_VREF_L5N_Y	0
P217	IO_L5P_Y	0
P216	IO_VREF	0
P215	IO_LVDS_DLL_L6N	0
P214	VCCINT	NA
P213	GCK3	0
P212	VCCO	0
P211	GND	NA

HQ240 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A ✓ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

**Table 9: HQ240 Differential Pin Pair Summary
XCV600E, XCV1000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	P92	P93	NA	IO_DLL_L40P
1	5	P89	P87	NA	IO_DLL_L40N
2	1	P210	P209	NA	IO_DLL_L6P
3	0	P213	P215	NA	IO_DLL_L6N
IO LVDS					
Total Pairs: 64, Asynchronous Output Pairs: 53					
0	0	P236	P237	NA	VREF
1	0	P234	P235	✓	-
2	0	P228	P229	✓	VREF
3	0	P223	P224	✓	-
4	0	P220	P221	✓	-
5	0	P217	P218	✓	VREF
6	1	P209	P215	NA	IO_LVDS_DLL
7	1	P205	P206	✓	VREF
8	1	P202	P203	✓	-
9	1	P199	P200	✓	-
10	1	P194	P195	✓	VREF
11	1	P191	P192	✓	VREF
12	1	P188	P189	✓	-
13	1	P186	P187	NA	VREF
14	1	P184	P185	✓	CS
15	2	P178	P177	✓	DIN, D0

**Table 9: HQ240 Differential Pin Pair Summary
XCV600E, XCV1000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
16	2	P174	P173	✓	-
17	2	P171	P170	✓	VREF
18	2	P168	P167	✓	D1
19	2	P163	P162	✓	D2
20	2	P160	P159	✓	-
21	2	P157	P156	✓	D3
22	2	P155	P154	1	VREF
23	2	P153	P152	✓	-
24	3	P145	P144	✓	D4, VREF
25	3	P142	P141	✓	-
26	3	P139	P138	✓	D5
27	3	P134	P133	✓	VREF
28	3	P131	P130	✓	VREF
29	3	P128	P127	✓	-
30	3	P126	P125	1	VREF
31	3	P124	P123	✓	INIT
32	4	P118	P117	✓	-
33	4	P114	P113	✓	-
34	4	P111	P110	✓	VREF
35	4	P108	P107	✓	VREF
36	4	P103	P102	✓	-
37	4	P100	P99	✓	-
38	4	P97	P96	✓	VREF
39	4	P95	P94	NA	VREF
40	5	P93	P87	NA	IO_LVDS_DLL
41	5	P84	P82	NA	VREF
42	5	P79	P78	✓	-
43	5	P74	P73	✓	VREF
44	5	P71	P70	✓	VREF
45	5	P68	P67	✓	-
46	5	P66	P65	NA	VREF
47	5	P64	P63	✓	-

Table 12: BG432 — XCV300E, XCV400E, XCV600E

Bank	Pin Description	Pin #
4	IO_L70N_Y	AK4
4	IO_L71P_YY	AJ5
4	IO_L71N_YY	AH6
4	IO_VREF_L72P_YY	AL4
4	IO_L72N_YY	AK5
4	IO_L73P_Y	AJ6
4	IO_L73N_Y	AH7
4	IO_L74P_YY	AL5
4	IO_L74N_YY	AK6
4	IO_VREF_L75P_YY	AJ7
4	IO_L75N_YY	AL6
4	IO_L76P_Y	AH9
4	IO_L76N_Y	AJ8
4	IO_VREF_L77P_Y	AK8 ¹
4	IO_L77N_Y	AJ9
4	IO_VREF_L78P_YY	AL8
4	IO_L78N_YY	AK9
4	IO_L79P_YY	AK10
4	IO_L79N_YY	AL10
4	IO_L80P_YY	AH12
4	IO_L80N_YY	AK11
4	IO_L81P_YY	AJ12
4	IO_L81N_YY	AK12
4	IO_L82P_YY	AH13
4	IO_L82N_YY	AJ13
4	IO_VREF_L83P_YY	AL13
4	IO_L83N_YY	AK14
4	IO_L84P_Y	AH14
4	IO_L84N_Y	AJ14
4	IO_VREF_L85P_Y	AK15 ²
4	IO_L85N_Y	AJ15
4	IO_LVDS_DLL_L86P	AH15
5	GCK1	AK16
5	IO	AH20
5	IO	AJ19

Table 12: BG432 — XCV300E, XCV400E, XCV600E

Bank	Pin Description	Pin #
5	IO	AJ23
5	IO	AJ24
5	IO_LVDS_DLL_L86N	AL17
5	IO_L87P_Y	AK17
5	IO_VREF_L87N_Y	AJ17 ²
5	IO_L88P_Y	AH17
5	IO_L88N_Y	AK18
5	IO_L89P_YY	AL19
5	IO_VREF_L89N_YY	AJ18
5	IO_L90P_YY	AH18
5	IO_L90N_YY	AL20
5	IO_L91P_YY	AK20
5	IO_L91N_YY	AH19
5	IO_L92P_YY	AJ20
5	IO_L92N_YY	AK21
5	IO_L93P_YY	AJ21
5	IO_L93N_YY	AL22
5	IO_L94P_YY	AJ22
5	IO_VREF_L94N_YY	AK23
5	IO_L95P_Y	AH22
5	IO_VREF_L95N_Y	AL24 ¹
5	IO_L96P_Y	AK24
5	IO_L96N_Y	AH23
5	IO_L97P_YY	AK25
5	IO_VREF_L97N_YY	AJ25
5	IO_L98P_YY	AL26
5	IO_L98N_YY	AK26
5	IO_L99P_Y	AH25
5	IO_L99N_Y	AL27
5	IO_L100P_YY	AJ26
5	IO_VREF_L100N_YY	AK27
5	IO_L101P_YY	AH26
5	IO_L101N_YY	AL28
5	IO_L102P_Y	AJ27
5	IO_L102N_Y	AK28

Table 12: BG432 — XCV300E, XCV400E, XCV600E

Bank	Pin Description	Pin #
6	VCCO	AL31
7	VCCO	A31
7	VCCO	L28
7	VCCO	L31
NA	GND	A2
NA	GND	A3
NA	GND	A7
NA	GND	A9
NA	GND	A14
NA	GND	A18
NA	GND	A23
NA	GND	A25
NA	GND	A29
NA	GND	A30
NA	GND	B1
NA	GND	B2
NA	GND	B30
NA	GND	B31
NA	GND	C1
NA	GND	C31
NA	GND	D16
NA	GND	G1
NA	GND	G31
NA	GND	J1
NA	GND	J31
NA	GND	P1
NA	GND	P31
NA	GND	T4
NA	GND	T28
NA	GND	V1
NA	GND	V31
NA	GND	AC1
NA	GND	AC31
NA	GND	AE1
NA	GND	AE31

Table 12: BG432 — XCV300E, XCV400E, XCV600E

Bank	Pin Description	Pin #
NA	GND	AH16
NA	GND	AJ1
NA	GND	AJ31
NA	GND	AK1
NA	GND	AK2
NA	GND	AK30
NA	GND	AK31
NA	GND	AL2
NA	GND	AL3
NA	GND	AL7
NA	GND	AL9
NA	GND	AL14
NA	GND	AL18
NA	GND	AL23
NA	GND	AL25
NA	GND	AL29
NA	GND	AL30

Notes:

1. V_{REF} or I/O option only in the XCV600E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV400E, XCV600E; otherwise, I/O option only.

Table 14: BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin#	See Note
7	IO_L165N_YY	P32	
7	IO_VREF_L165P_YY	P31	
7	IO_L166N_Y	P30	
7	IO_L166P_Y	P29	
7	IO_L167N_Y	M32	
7	IO_L167P_Y	N31	
7	IO_L168N_Y	N30	
7	IO_VREF_L168P_Y	L33	3
7	IO_L169N_Y	M31	
7	IO_L169P_Y	L32	
7	IO_L170N_Y	M30	
7	IO_L170P_Y	L31	
7	IO_L171N_YY	M29	
7	IO_L171P_YY	J33	
7	IO_L172N_YY	L30	
7	IO_VREF_L172P_YY	K31	
7	IO_L173N_Y	L29	
7	IO_L173P_Y	H33	
7	IO_L174N_Y	J31	
7	IO_VREF_L174P_Y	H32	4
7	IO_L175N_Y	K29	
7	IO_L175P_Y	H31	
7	IO_L176N_Y	J30	
7	IO_VREF_L176P_Y	G32	1
7	IO_L177N_YY	J29	
7	IO_VREF_L177P_YY	G31	
7	IO_L178N_Y	E33	
7	IO_L178P_Y	E32	
7	IO_L179N_Y	H29	
7	IO_L179P_Y	F31	
7	IO_L180N_Y	D32	
7	IO_VREF_L180P_Y	E31	
7	IO_L181N_Y	G29	
7	IO_L181P_Y	C33	
7	IO_L182N_Y	F30	

Table 14: BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin#	See Note
7	IO_VREF_L182P_Y	D31	3
2	CCLK	C4	
3	DONE	AJ5	
NA	DXN	AK29	
NA	DXP	AJ28	
NA	M0	AJ29	
NA	M1	AK30	
NA	M2	AN32	
NA	PROGRAM	AM1	
NA	TCK	E29	
NA	TDI	D5	
2	TDO	E6	
NA	TMS	B33	
NA	NC	C31	
NA	NC	AC2	
NA	NC	AK4	
NA	NC	AL3	
NA	VCCINT	A21	
NA	VCCINT	B12	
NA	VCCINT	B14	
NA	VCCINT	B18	
NA	VCCINT	B28	
NA	VCCINT	C22	
NA	VCCINT	C24	
NA	VCCINT	E9	
NA	VCCINT	E12	
NA	VCCINT	F2	
NA	VCCINT	H30	
NA	VCCINT	J1	
NA	VCCINT	K32	
NA	VCCINT	M3	
NA	VCCINT	N1	

Table 14: BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin#	See Note
NA	GND	A29	
NA	GND	A32	
NA	GND	A33	
NA	GND	B1	
NA	GND	B6	
NA	GND	B9	
NA	GND	B15	
NA	GND	B23	
NA	GND	B27	
NA	GND	B31	
NA	GND	C2	
NA	GND	E1	
NA	GND	F32	
NA	GND	G2	
NA	GND	G33	
NA	GND	J32	
NA	GND	K1	
NA	GND	L2	
NA	GND	M33	
NA	GND	P1	
NA	GND	P33	
NA	GND	R32	
NA	GND	T1	
NA	GND	V33	
NA	GND	W2	
NA	GND	Y1	
NA	GND	Y33	
NA	GND	AB1	
NA	GND	AC32	
NA	GND	AD33	
NA	GND	AE2	
NA	GND	AG1	
NA	GND	AG32	
NA	GND	AH2	
NA	GND	AJ33	

Table 14: BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin#	See Note
NA	GND	AL32	
NA	GND	AM3	
NA	GND	AM7	
NA	GND	AM11	
NA	GND	AM19	
NA	GND	AM25	
NA	GND	AM28	
NA	GND	AM33	
NA	GND	AN1	
NA	GND	AN2	
NA	GND	AN5	
NA	GND	AN10	
NA	GND	AN14	
NA	GND	AN16	
NA	GND	AN20	
NA	GND	AN22	
NA	GND	AN27	
NA	GND	AN33	

Notes:

1. V_{REF} or I/O option only in the XCV2000E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV1600E & 2000E; otherwise, I/O option only.
3. V_{REF} or I/O option only in the XCV1000E, 1600E, & 2000E; otherwise, I/O option only.
4. V_{REF} or I/O option only in the XCV600E, 1000E, 1600E, & 2000E; otherwise, I/O option only.

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
1	IO_L40P_YY	D20
1	IO_L41N_YY	F19
1	IO_VREF_L41P_YY	C21
1	IO_L42N_YY	B22
1	IO_L42P_YY	E20
1	IO_L43N_Y	A23
1	IO_L43P_Y	D21
1	IO_WRITE_L44N_YY	C22
1	IO_CS_L44P_YY	E21
2	IO	D25 ¹
2	IO	D26
2	IO	E26
2	IO	F26
2	IO	H26 ¹
2	IO	K26 ¹
2	IO	M25 ¹
2	IO	N26 ¹
2	IO_D1	K24
2	IO_DOUT_BUSY_L45P_YY	E23
2	IO_DIN_D0_L45N_YY	F22
2	IO_L46P_YY	E24
2	IO_L46N_YY	F20
2	IO_L47P_Y	G21
2	IO_L47N_Y	G22
2	IO_VREF_L48P_Y	F24
2	IO_L48N_Y	H20
2	IO_L49P_Y	E25
2	IO_L49N_Y	H21
2	IO_L50P_YY	F23
2	IO_L50N_YY	G23
2	IO_VREF_L51P_YY	H23
2	IO_L51N_YY	J20
2	IO_L52P_YY	G24
2	IO_L52N_YY	H22
2	IO_L53P_Y	J21
2	IO_L53N_Y	G25

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
2	IO_VREF_L54P_Y	G26 ²
2	IO_L54N_Y	J22
2	IO_L55P_YY	H24
2	IO_L55N_YY	J23
2	IO_L56P_YY	J24
2	IO_VREF_L56N_YY	K20
2	IO_D2_L57P_YY	K22
2	IO_L57N_YY	K21
2	IO_L58P_YY	H25
2	IO_L58N_YY	K23
2	IO_L59P_Y	L20
2	IO_L59N_Y	J26
2	IO_L60P_Y	K25
2	IO_L60N_Y	L22
2	IO_L61P_Y	L21
2	IO_L61N_Y	L23
2	IO_L62P_Y	M20
2	IO_L62N_Y	L24
2	IO_VREF_L63P_YY	M23
2	IO_D3_L63N_YY	M22
2	IO_L64P_YY	L26
2	IO_L64N_YY	M21
2	IO_L65P_Y	N19
2	IO_L65N_Y	M24
2	IO_VREF_L66P_Y	M26
2	IO_L66N_Y	N20
2	IO_L67P_YY	N24
2	IO_L67N_YY	N21
2	IO_L68P_YY	N23
2	IO_L68N_YY	N22
3	IO	P24
3	IO	P26 ¹
3	IO	R26 ¹
3	IO	T26 ¹
3	IO	U26 ¹
3	IO	W25

FG860 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A ✓ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 25: FG860 Differential Pin Pair Summary
XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
3	0	C22	A22	NA	IO_DLL_L34N
2	1	B22	D22	NA	IO_DLL_L34P
1	5	AY22	AW21	NA	IO_DLL_L176N
0	4	BA22	AW20	NA	IO_DLL_L176P
IO LVDS					
Total Pairs: 281, Asynchronous Output Pairs: 111					
0	0	D38	A38	2	-
1	0	E37	B37	1	-
2	0	C39	A37	1	VREF
3	0	C38	B36	1	-
4	0	B35	A36	✓	-
5	0	D37	A35	✓	VREF
6	0	A34	C37	5	-
7	0	B33	E36	5	-
8	0	C32	A33	✓	-
9	0	B32	C36	✓	VREF
10	0	D35	A32	1	-
11	0	C35	C31	1	VREF
12	0	A31	E34	✓	-
13	0	C30	D34	✓	VREF
14	0	E33	B30	2	-
15	0	D33	A30	2	-
16	0	B29	C33	✓	VREF
17	0	A29	E32	✓	-

Table 25: FG860 Differential Pin Pair Summary
XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
18	0	C28	D32	2	-
19	0	B28	E31	1	-
20	0	A28	D31	1	-
21	0	C27	D30	5	-
22	0	B27	E29	✓	-
23	0	A27	D29	✓	VREF
24	0	D28	C26	5	-
25	0	F27	B26	5	-
26	0	C25	E27	✓	-
27	0	B25	D27	✓	VREF
28	0	D26	A25	1	-
29	0	E25	A24	1	-
30	0	B24	D25	✓	-
31	0	A23	E24	✓	VREF
32	0	E23	C23	2	-
33	0	D23	B23	2	VREF
34	1	D22	A22	NA	IO_LVDS_DLL
35	1	B21	D21	2	VREF
36	1	A21	D20	2	-
37	1	D19	C20	✓	VREF
38	1	E19	B20	✓	-
39	1	A19	D18	1	-
40	1	C19	E18	1	-
41	1	E17	B19	✓	VREF
42	1	D16	A18	✓	-
43	1	B18	E16	5	-
44	1	A17	F16	5	-
45	1	E15	C17	✓	VREF
46	1	D14	B17	✓	-
47	1	E14	A16	5	-
48	1	D13	C16	1	-
49	1	D12	B16	1	-
50	1	E12	A15	2	-
51	1	C11	C15	✓	-

Table 26: FG900 — XCV600E, XCV1000E, XCV1600E

Bank	Pin Description	Pin #
5	IO_L182N	AF13
5	IO_L183P	AH14
5	IO_L183N	AJ14
5	IO_L184P_YY	AE14
5	IO_VREF_L184N_YY	AG13
5	IO_L185P_YY	AK13
5	IO_L185N_YY	AD13
5	IO_L186P	AE13
5	IO_L186N	AF12
5	IO_L187P	AC13
5	IO_L187N	AA13
5	IO_L188P_YY	AA12
5	IO_VREF_L188N_YY	AJ12 ¹
5	IO_L189P_YY	AB12
5	IO_L189N_YY	AE11
5	IO_L190P	AK12 ⁴
5	IO_L190N	Y13 ⁴
5	IO_L191P	AG11
5	IO_L191N	AF11
5	IO_L192P	AH11
5	IO_L192N	AJ11
5	IO_L193P_YY	AE12 ⁴
5	IO_L193N_YY	AG10 ⁴
5	IO_L194P_YY	AD12
5	IO_L194N_YY	AK11
5	IO_L195P_YY	AJ10
5	IO_VREF_L195N_YY	AC12
5	IO_L196P_YY	AK10
5	IO_L196N_YY	AD11
5	IO_L197P_YY	AJ9
5	IO_L197N_YY	AE9
5	IO_L198P_YY	AH10
5	IO_VREF_L198N_YY	AF9
5	IO_L199P_YY	AH9
5	IO_L199N_YY	AK9
5	IO_L200P	AF8
5	IO_L200N	AB11

Table 26: FG900 — XCV600E, XCV1000E, XCV1600E

Bank	Pin Description	Pin #
5	IO_L201P	AC11
5	IO_L201N	AG8
5	IO_L202P_YY	AK8
5	IO_VREF_L202N_YY	AF7
5	IO_L203P_YY	AG7
5	IO_L203N_YY	AK7
5	IO_L204P	AJ7
5	IO_L204N	AD10
5	IO_L205P	AH6
5	IO_L205N	AC10
5	IO_L206P_YY	AD9
5	IO_VREF_L206N_YY	AG6
5	IO_L207P_YY	AB10
5	IO_L207N_YY	AJ5
5	IO_L208P	AD8 ⁴
5	IO_L208N	AK5 ⁴
5	IO_L209P	AC9
5	IO_VREF_L209N	AJ4 ¹
5	IO_L210P	AG5
5	IO_L210N	AK4
5	IO_L211P_YY	AH5 ³
5	IO_L211N_YY	AG3 ⁴
6	IO	T2 ⁴
6	IO	T10 ⁴
6	IO	U1
6	IO	U4 ⁵
6	IO	U6 ⁴
6	IO	U7 ⁴
6	IO	V1 ⁴
6	IO	V5 ⁵
6	IO	V8
6	IO	Y10 ⁴
6	IO	AA4 ⁴
6	IO	AB5 ⁵
6	IO	AB7 ⁴
6	IO	AC3 ⁵

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
111	2	M31	R26	2600 1600	-
112	2	N30	P28	3200 1600 1000	-
113	2	N29	N33	2600 2000 1000	VREF
114	2	T25	N34	3200 2600 2000 1600	-
115	2	P34	R27	3200 2600 2000 1600 1000	-
116	2	P29	P31	3200 2600 1600 1000	-
117	2	P33	T26	3200 2600 2000	-
118	2	R34	R28	2600 2000 1000	-
119	2	N31	N32	2000 1600 1000	D3
120	2	P30	R33	2000 1600	-
121	2	R29	T34	3200 2600 2000 1600 1000	-
122	2	R30	T30	1000	-
123	2	T28	R31	3200 1600	-
124	2	T29	U27	3200 2600 1600 1000	-
125	2	T31	T33	2000 1600 1000	VREF
126	2	U28	T32	2000 1600 1000	-
127	2	U29	U33	3200 2600 1600 1000	VREF
128	2	V33	U31	3200 2600 2000 1600 1000	-
129	3	V26	V30	3200 2600 1600 1000	VREF
130	3	W34	V28	2000 1600 1000	-
131	3	W32	W30	2000 1600 1000	VREF

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
132	3	V29	Y34	3200 2600 1600 1000	-
133	3	W29	Y33	3200 1600	-
134	3	W26	W28	1000	-
135	3	Y31	Y30	3200 2600 2000 1600 1000	-
136	3	AA34	W31	2000 1600	-
137	3	AA33	Y29	2000 1600 1000	VREF
138	3	W25	AB34	2600 2000 1000	-
139	3	Y28	AB33	3200 2600 2000	-
140	3	AA30	Y26	3200 2600 1600 1000	-
141	3	Y27	AA31	3200 2600 2000 1600 1000	-
142	3	AA27	AA29	3200 2600 2000 1600	-
143	3	AB32	AB29	2600 2000 1000	VREF
144	3	AA28	AC34	3200 1600 1000	-
145	3	Y25	AD34	2600 1600	-
146	3	AB30	AC33	3200 2600 1600 1000	-
147	3	AA26	AC32	2000 1000	-
148	3	AD33	AB28	3200 2600 2000	-
149	3	AE34	AB27	3200 2600 2000 1600 1000	D5
150	3	AE33	AC30	2000 1600 1000	VREF
151	3	AA25	AE32	3200 1600 1000	-
152	3	AE31	AD29	3200 2600 2000 1600 1000	-

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
231	5	AH14	AP12	3200 2600 2000 1600 1000	-
232	5	AJ14	AL14	3200 2600 1000	-
233	5	AF13	AN12	3200 2000 1000	-
234	5	AF14	AP11	3200 2000 1000	-
235	5	AN11	AH13	3200 1600 1000	-
236	5	AM12	AL12	3200 2600 2000 1600 1000	-
237	5	AJ13	AP10	3200 2600 2000 1600 1000	VREF
238	5	AK12	AM10	2600 1600 1000	-
239	5	AP9	AK11	2600 1600 1000	-
240	5	AL11	AL10	3200 2600 2000 1600 1000	VREF
241	5	AE13	AM9	3200 2600 2000 1600 1000	-
242	5	AF12	AP8	3200 2600	-
243	5	AL9	AH11	3200 2000 1000	VREF
244	5	AF11	AN8	3200 2000 1000	-
245	5	AM8	AG11	3200 1600	-
246	5	AL8	AK9	3200 2600 2000 1600 1000	VREF
247	5	AH10	AN7	3200 2600 2000 1600 1000	-
248	5	AE12	AJ9	3200 2600	-
249	5	AM7	AL7	3200 1000	-
250	5	AG10	AN6	3200 1000	-

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
251	5	AK8	AH9	2000 1600	-
252	5	AP5	AJ8	3200 2600 2000 1600 1000	VREF
253	5	AE11	AN5	3200 2600 2000 1600 1000	-
254	5	AF10	AM6	3200 2600 1000	-
255	5	AL6	AG9	3200 2000 1000	VREF
256	5	AH8	AP4	3200 2000 1000	-
257	5	AN4	AJ7	3200 1600 1000	-
258	5	AM5	AK6	3200 2600 2000 1600 1000	-
259	6	AF8	AH6	3200 2600 2000 1600 1000	-
260	6	AK3	AE9	3200 2600 2000	-
261	6	AL2	AD10	2600 2000 1000	-
262	6	AH4	AL1	3200 2600 1600 1000	VREF
263	6	AK1	AG6	2600 1600	-
264	6	AK2	AF7	3200 2600 1600 1000	-
265	6	AG5	AJ3	2600 2000 1000	VREF
266	6	AJ2	AD9	3200 2600 2000 1600	-
267	6	AH2	AC10	3200 2600 2000 1600 1000	-
268	6	AF5	AH3	3200 2600 1600 1000	-
269	6	AG3	AE8	3200 2600 2000	-

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/7/99	1.0	Initial Xilinx release.
1/10/00	1.1	Re-released with spd.txt v. 1.18, FG860/900/1156 package information, and additional DLL, Select RAM and SelectI/O information.
1/28/00	1.2	Added Delay Measurement Methodology table, updated SelectI/O section, Figures 30, 54, & 55, text explaining Table 5, T_{BYP} values, buffered Hex Line info, p. 8, I/O Timing Measurement notes, notes for Tables 15, 16, and corrected F1156 pinout table footnote references.
2/29/00	1.3	Updated pinout tables, V_{CC} page 20, and corrected Figure 20.
5/23/00	1.4	Correction to table on p. 22.
7/10/00	1.5	- Numerous minor edits. - Data sheet upgraded to Preliminary. - Preview -8 numbers added to Virtex-E Electrical Characteristics tables.
8/1/00	1.6	- Reformatted entire document to follow new style guidelines. - Changed speed grade values in tables on pages 35-37.
9/20/00	1.7	- Min values added to Virtex-E Electrical Characteristics tables. - XCV2600E and XCV3200E numbers added to Virtex-E Electrical Characteristics tables (Module 3). - Corrected user I/O count for XCV100E device in Table 1 (Module 1). - Changed several pins to "No Connect in the XCV100E" and removed duplicate V_{CCINT} pins in Table ~ (Module 4). - Changed pin J10 to "No connect in XCV600E" in Table 74 (Module 4). - Changed pin J30 to "V_{REF} or I/O option only in the XCV600E" in Table 74 (Module 4). - Corrected pair 18 in Table 75 (Module 4) to be "AO in the XCV1000E, XCV1600E".
11/20/00	1.8	- Upgraded speed grade -8 numbers in Virtex-E Electrical Characteristics tables to Preliminary. - Updated minimums in Table 13 and added notes to Table 14. - Added to note 2 to Absolute Maximum Ratings. - Changed speed grade -8 numbers for $T_{SHCKO32}$, T_{REG}, T_{BCCS}, and T_{ICKOF} - Changed all minimum hold times to -0.4 under Global Clock Set-Up and Hold for LVTTTL Standard, with DLL. - Revised maximum T_{DLLPW} in -6 speed grade for DLL Timing Parameters. - Changed GCLK0 to BA22 for FG860 package in Table 46.
2/12/01	1.9	- Revised footnote for Table 14. - Added numbers to Virtex-E Electrical Characteristics tables for XCV1000E and XCV2000E devices. - Updated Table 27 and Table 78 to include values for XCV400E and XCV600E devices. - Revised Table 62 to include pinout information for the XCV400E and XCV600E devices in the BG560 package. - Updated footnotes 1 and 2 for Table 76 to include XCV2600E and XCV3200E devices.