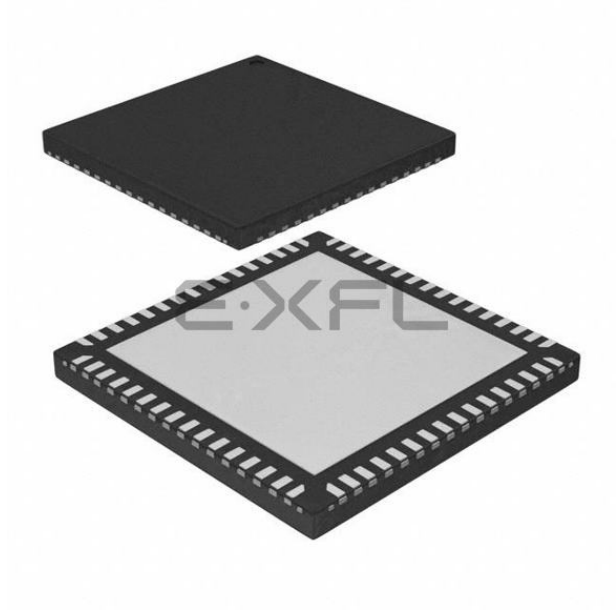

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega128a3-mh

7.4 Data Memory

The Data Memory consist of the I/O Memory, EEPROM and SRAM memories, all within one linear address space, see Figure 7-2 on page 11. To simplify development, the memory map for all devices in the family is identical and with empty, reserved memory space for smaller devices.

Figure 7-2. Data Memory Map (Hexadecimal address)

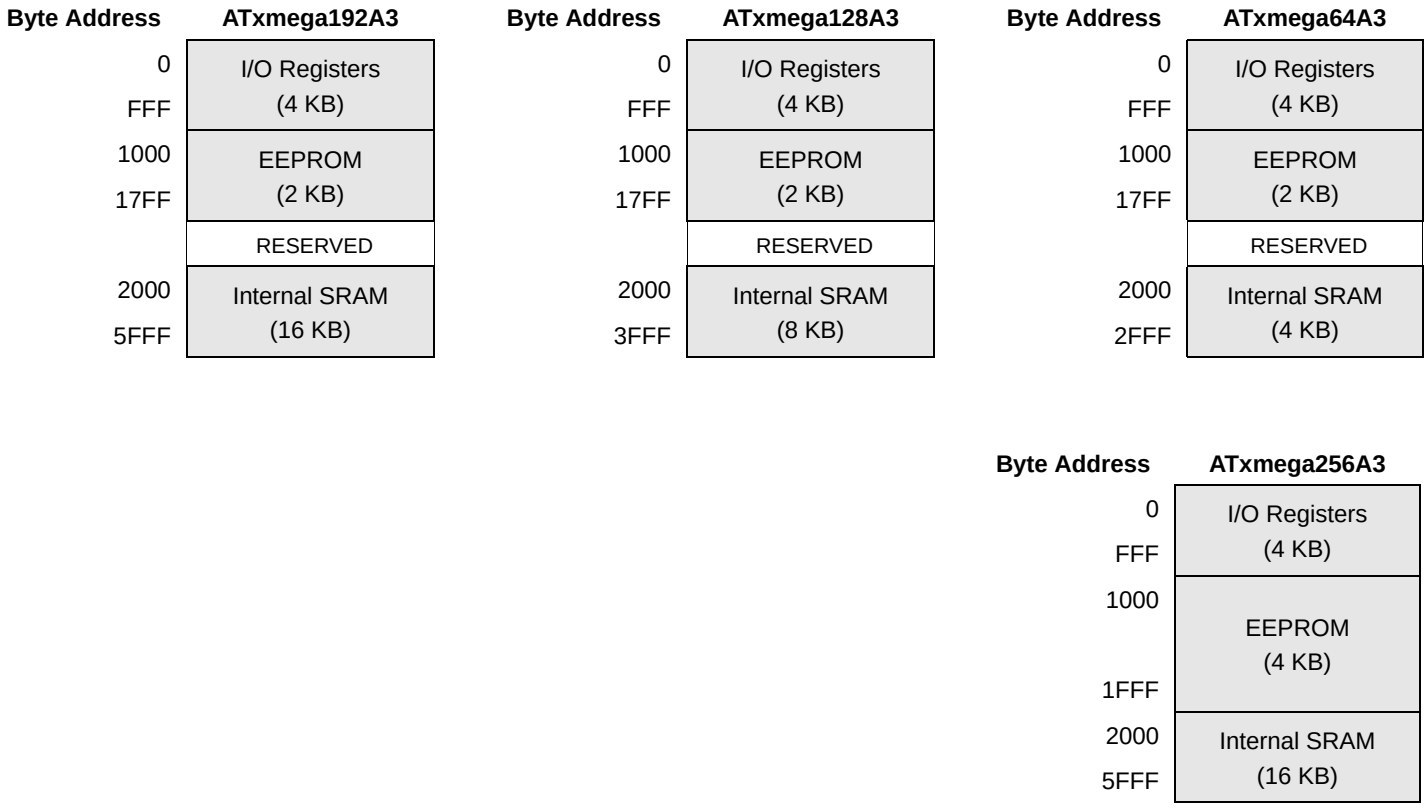
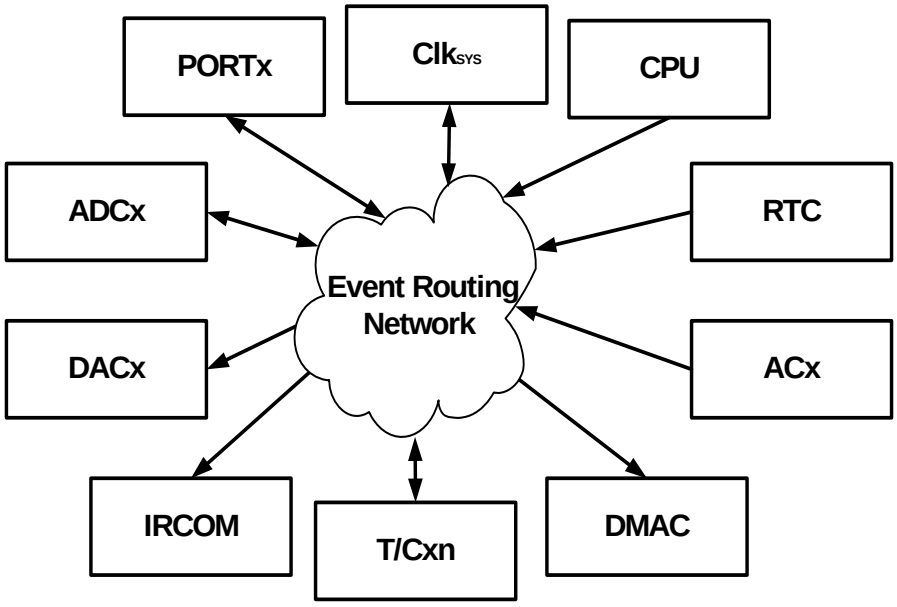


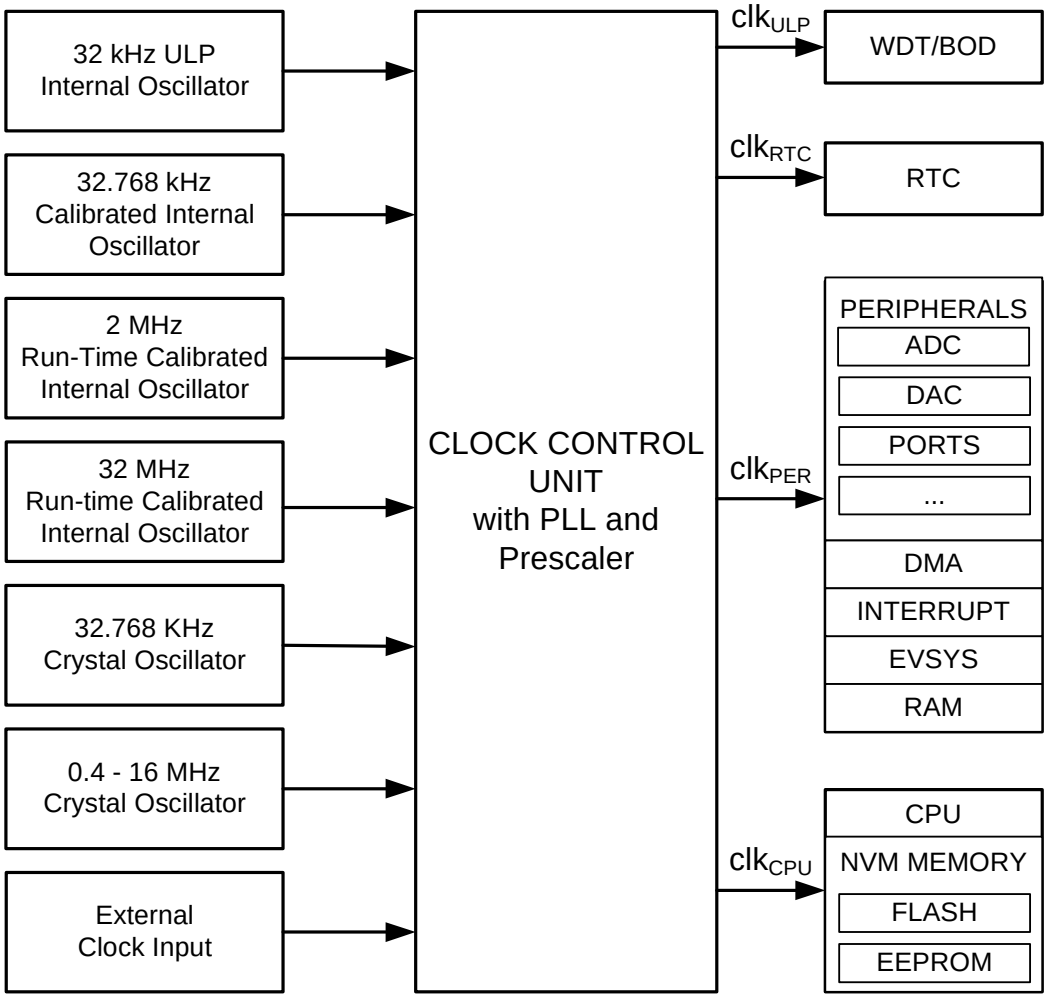
Figure 9-1. Event system block diagram.



The Event Routing Network can directly connect together ADCs, DACs, Analog Comparators (ACx), I/O ports (PORTx), the Real-time Counter (RTC), Timer/Counters (T/C) and the IR Communication Module (IRCOM). Events can also be generated from software (CPU).

All events from all peripherals are always routed into the Event Routing Network. This consist of eight multiplexers where each can be configured in software to select which event to be routed into that event channel. All eight event channels are connected to the peripherals that can use events, and each of these peripherals can be configured to use events from one or more event channels to automatically trigger a software selectable action.

Figure 10-1. Clock system overview



Each clock source is briefly described in the following sub-sections.

10.3 Clock Options

10.3.1 32 kHz Ultra Low Power Internal Oscillator

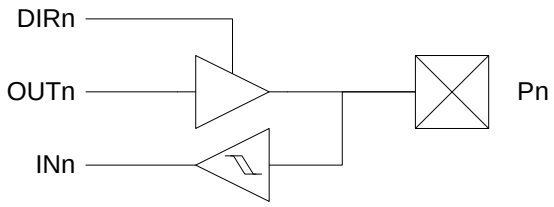
The 32 kHz Ultra Low Power (ULP) Internal Oscillator is a very low power consumption clock source. It is used for the Watchdog Timer, Brown-Out Detection and as an asynchronous clock source for the Real Time Counter. This oscillator cannot be used as the system clock source, and it cannot be directly controlled from software.

10.3.2 32.768 kHz Calibrated Internal Oscillator

The 32.768 kHz Calibrated Internal Oscillator is a high accuracy clock source that can be used as the system clock source or as an asynchronous clock source for the Real Time Counter. It is calibrated during production to provide a default frequency which is close to its nominal frequency.

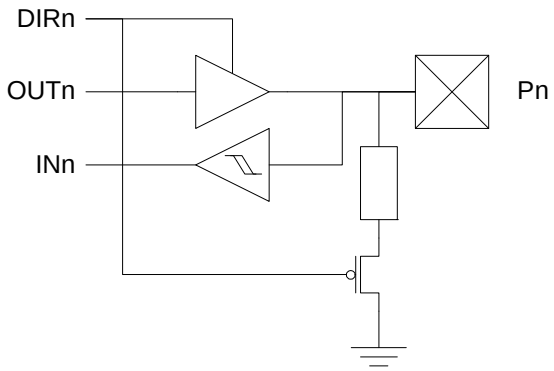
15.3.1 Push-pull

Figure 15-1. I/O configuration - Totem-pole



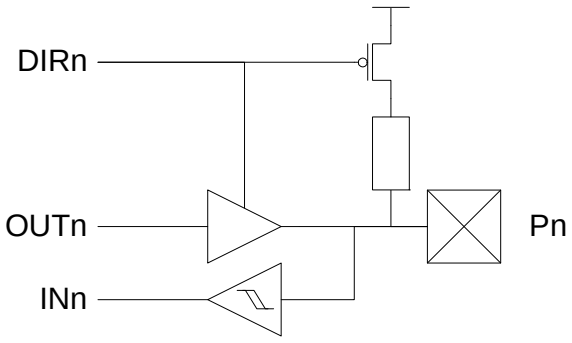
15.3.2 Pull-down

Figure 15-2. I/O configuration - Totem-pole with pull-down (on input)



15.3.3 Pull-up

Figure 15-3. I/O configuration - Totem-pole with pull-up (on input)



15.3.4 Bus-keeper

The bus-keeper's weak output produces the same logical level as the last output level. It acts as a pull-up if the last level was '1', and pull-down if the last level was '0'.

21. SPI - Serial Peripheral Interface

21.1 Features

- **Three Identical SPI peripherals**
- **Full-duplex, Three-wire Synchronous Data Transfer**
- **Master or Slave Operation**
- **LSB First or MSB First Data Transfer**
- **Seven Programmable Bit Rates**
- **End of Transmission Interrupt Flag**
- **Write Collision Flag Protection**
- **Wake-up from Idle Mode**
- **Double Speed (CK/2) Master SPI Mode**

21.2 Overview

The Serial Peripheral Interface (SPI) allows high-speed full-duplex, synchronous data transfer between different devices. Devices can communicate using a master-slave scheme, and data is transferred both to and from the devices simultaneously.

PORTC, PORTD, and PORTE each has one SPI. Notation of these peripherals are SPIC, SPID, and SPIE respectively.

30. Pinout and Pin Functions

The pinout of XMEGA A3 is shown "" on page 2. In addition to general I/O functionality, each pin may have several function. This will depend on which peripheral is enabled and connected to the actual pin. Only one of the alternate pin functions can be used at time.

30.1 Alternate Pin Function Description

The tables below show the notation for all pin functions available and describe its function.

30.1.1 Operation/Power Supply

VCC	Digital supply voltage
AVCC	Analog supply voltage
GND	Ground

30.1.2 Port Interrupt functions

SYNC	Port pin with full synchronous and limited asynchronous interrupt function
ASYNC	Port pin with full synchronous and full asynchronous interrupt function

30.1.3 Analog functions

ACn	Analog Comparator input pin n
AC0OUT	Analog Comparator 0 Output
ADCn	Analog to Digital Converter input pin n
DACn	Digital to Analog Converter output pin n
AREF	Analog Reference input pin

30.1.4 Timer/Counter and AWEX functions

OCnx	Output Compare Channel x for Timer/Counter n
$\overline{\text{OCnx}}$	Inverted Output Compare Channel x for Timer/Counter n
OCnxLS	Output Compare Channel x Low Side for Timer/Counter n
OCnxHS	Output Compare Channel x High Side for Timer/Counter n

30.1.5 Communication functions

SCL	Serial Clock for TWI
SDA	Serial Data for TWI
SCLIN	Serial Clock In for TWI when external driver interface is enabled
SCLOUT	Serial Clock Out for TWI when external driver interface is enabled
SDAIN	Serial Data In for TWI when external driver interface is enabled
SDAOUT	Serial Data Out for TWI when external driver interface is enabled
XCKn	Transfer Clock for USART n
RXDn	Receiver Data for USART n
TXDn	Transmitter Data for USART n
$\overline{SS}$	Slave Select for SPI
MOSI	Master Out Slave In for SPI
MISO	Master In Slave Out for SPI
SCK	Serial Clock for SPI

30.1.6 Oscillators, Clock and Event

TOSCn	Timer Oscillator pin n
XTALn	Input/Output for inverting Oscillator pin n
CLKOUT	Peripheral Clock Output
EVOUT	Event Channel 0 Output

30.1.7 Debug/System functions

$\overline{RESET}$	Reset pin
PDI_CLK	Program and Debug Interface Clock pin
PDI_DATA	Program and Debug Interface Data pin
TCK	JTAG Test Clock
TDI	JTAG Test Data In
TDO	JTAG Test Data Out
TMS	JTAG Test Mode Select

Table 30-6. Port F - Alternate functions

PORT F	PIN #	INTERRUPT	TCF0	USARTF0
PF0	46	SYNC	OC0A	
PF1	47	SYNC	OC0B	XCK0
PF2	48	SYNC/ASYNC	OC0C	RXD0
PF3	49	SYNC	OC0D	TXD0
PF4	50	SYNC		
PF5	51	SYNC		
PF6	54	SYNC		
PF7	55	SYNC		
GND	52			
VCC	53			

Table 30-7. Port R- Alternate functions

PORT R	PIN #	INTERRUPT	PROGR	XTAL
PDI	56		PDI_DATA	
$\overline{\text{RESET}}$	57		PDI_CLOCK	
PRO	58	SYNC		XTAL2
PR1	59	SYNC		XTAL1

Table 30-8. ATxmega256/192/128/64A3 Boundary Scan Order

Bit Number	Signal Name	Module
149	PQ3.Bidir	PORT Q
148	PQ3.Control	
147	PQ2.Bidir	
146	PQ2.Control	
145	PQ1.Bidir	
144	PQ1.Control	
143	PQ0.Bidir	
142	PQ0.Control	
141	PK7.Bidir	PORT K
140	PK7.Control	
139	PK6.Bidir	
138	PK6.Control	
137	PK5.Bidir	
136	PK5.Control	
135	PK4.Bidir	
134	PK4.Control	
133	PK3.Bidir	
132	PK3.Control	
131	PK2.Bidir	
130	PK2.Control	
129	PK1.Bidir	
128	PK1.Control	
127	PK0.Bidir	
126	PK0.Control	

34.9 Brownout Detection Characteristics

Table 34-10. Brownout Detection Characteristics[1]

Symbol	Parameter	Condition	Min	Typ	Max	Units
	BOD level 0 falling Vcc		1.62	1.63	1.7	V
	BOD level 1 falling Vcc			1.9		
	BOD level 2 falling Vcc			2.17		
	BOD level 3 falling Vcc			2.43		
	BOD level 4 falling Vcc			2.68		
	BOD level 5 falling Vcc			2.96		
	BOD level 6 falling Vcc			3.22		
	BOD level 7 falling Vcc			3.49		
	Hysteresis	BOD level 0-5		1		%

Note: 1. BOD is calibrated at 85°C within BOD level 0 values, and BOD level 0 is the default level.

34.10 PAD Characteristics

Table 34-11. PAD Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input High Voltage	V_{CC} = 2.4 - 3.6V	0.7*V_{CC}		V_{CC}+0.5	V
		V_{CC} = 1.6 - 2.4V	0.8*V_{CC}		V_{CC}+0.5	
V_{IL}	Input Low Voltage	V_{CC} = 2.4 - 3.6V	-0.5		0.3*V_{CC}	
		V_{CC} = 1.6 - 2.4V	-0.5		0.2*V_{CC}	
V_{OL}	Output Low Voltage GPIO	I_{OH} = 15 mA, V_{CC} = 3.3V		0.4	0.76	
		I_{OH} = 10 mA, V_{CC} = 3.0V		0.3	0.64	
		I_{OH} = 5 mA, V_{CC} = 1.8V		0.2	0.46	
V_{OH}	Output High Voltage GPIO	I_{OH} = -8 mA, V_{CC} = 3.3V	2.6	2.9		
		I_{OH} = -6 mA, V_{CC} = 3.0V	2.1	2.7		
		I_{OH} = -2 mA, V_{CC} = 1.8V	1.4	1.6		
I_{IL}	Input Leakage Current I/O pin			<0.001	1	µA
I_{IH}	Input Leakage Current I/O pin			<0.001	1	
R_P	I/O pin Pull/Buss keeper Resistor			20		kΩ
R_{RST}	Reset pin Pull-up Resistor			20		
	Input hysteresis			0.5		V

Figure 35-5. Active Supply Current vs. Vcc

f_{SYS} = 2.0 MHz internal RC

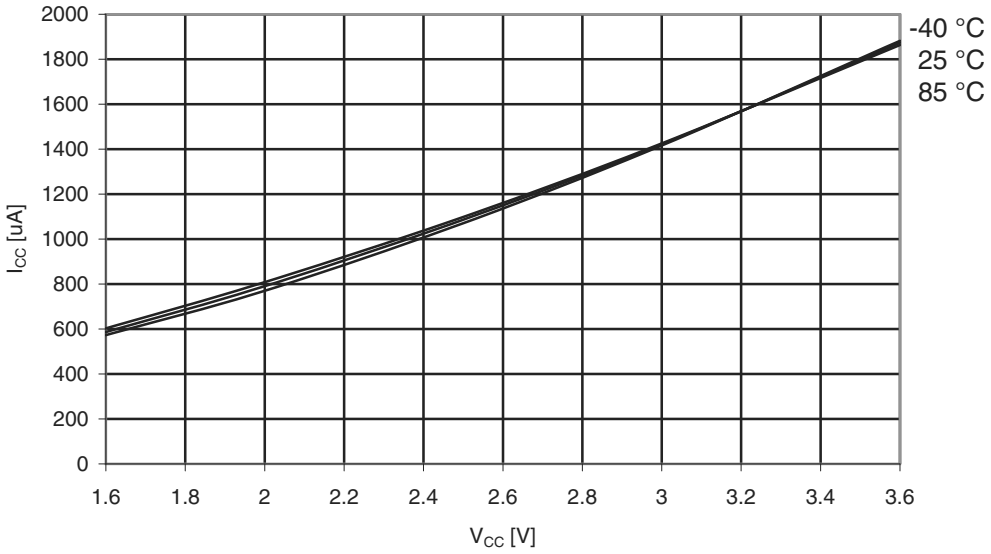
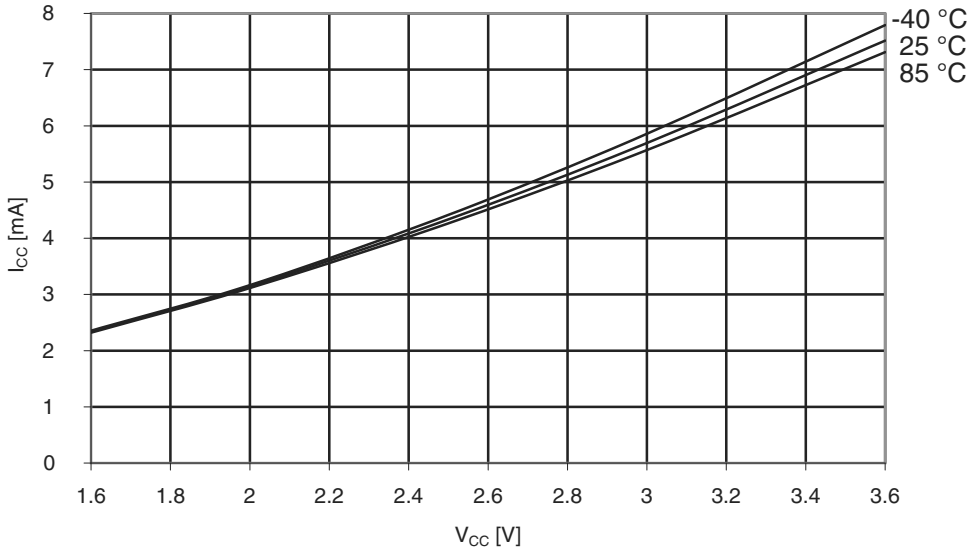


Figure 35-6. Active Supply Current vs. Vcc

f_{SYS} = 32 MHz internal RC prescaled to 8 MHz



35.3 Power-down Supply Current

Figure 35-15. Power-down Supply Current vs. Temperature

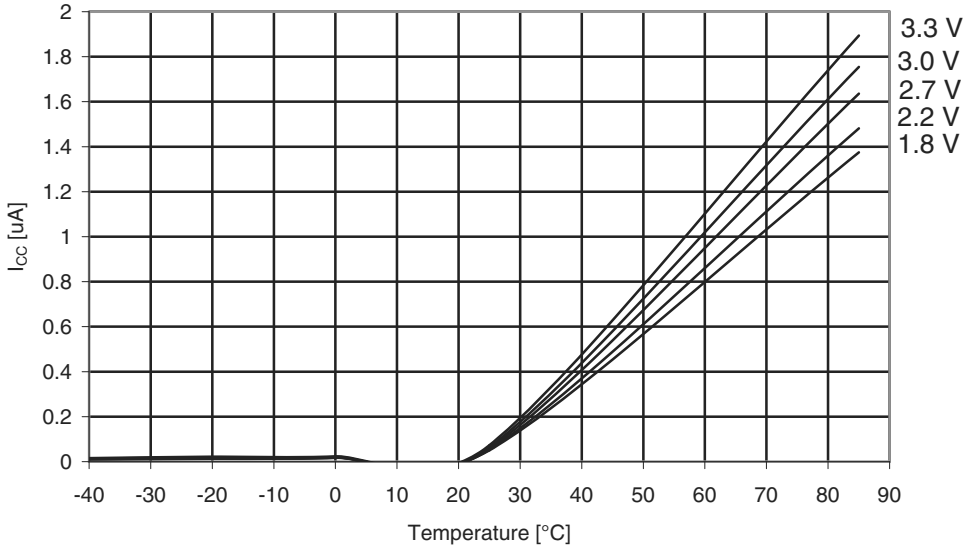
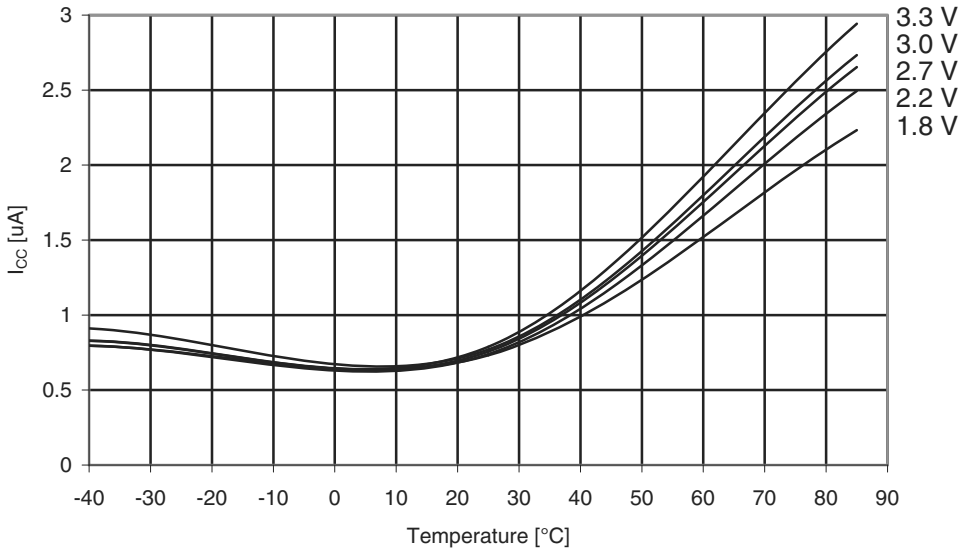


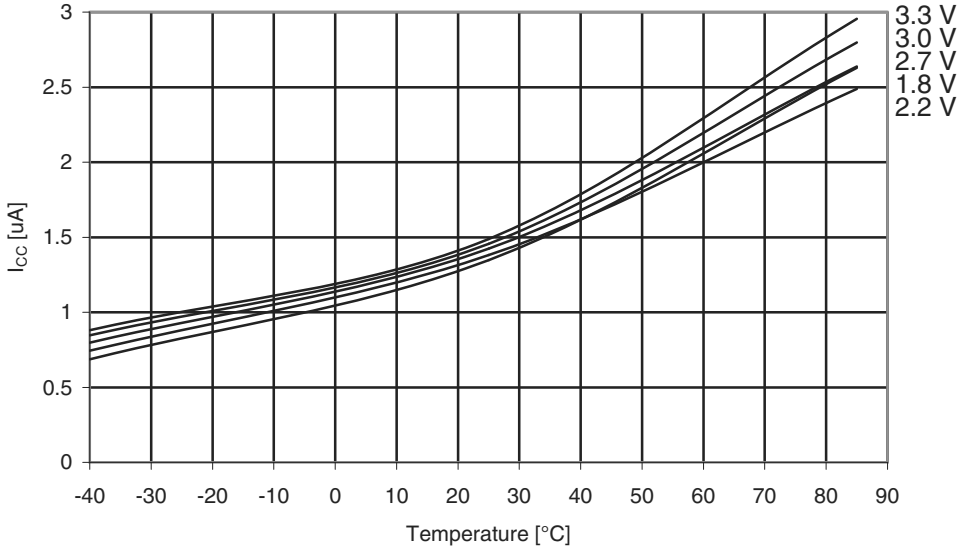
Figure 35-16. Power-down Supply Current vs. Temperature

With WDT and sampled BOD enabled.



35.4 Power-save Supply Current

Figure 35-17. Power-save Supply Current vs. Temperature
With WDT, sampled BOD and RTC from ULP enabled



35.5 Pin Pull-up

Figure 35-18. Reset Pull-up Resistor Current vs. Reset Pin Voltage
V_{CC} = 1.8V

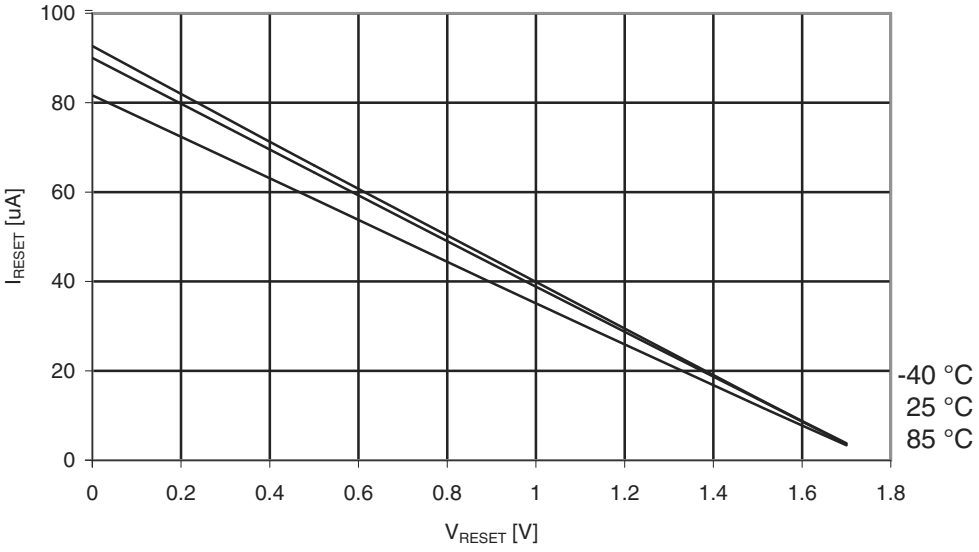


Figure 35-23. I/O Pin Output Voltage vs. Source Current

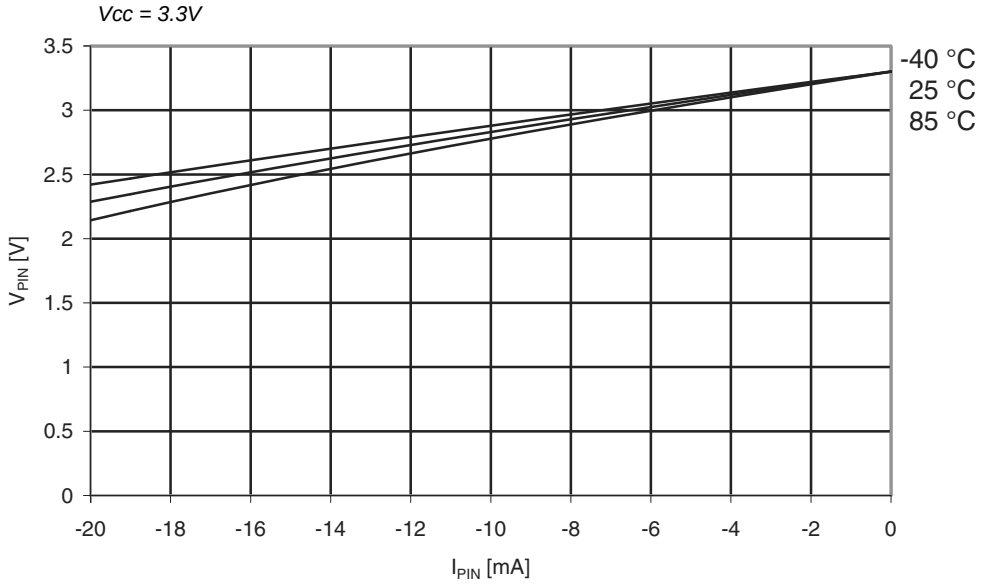
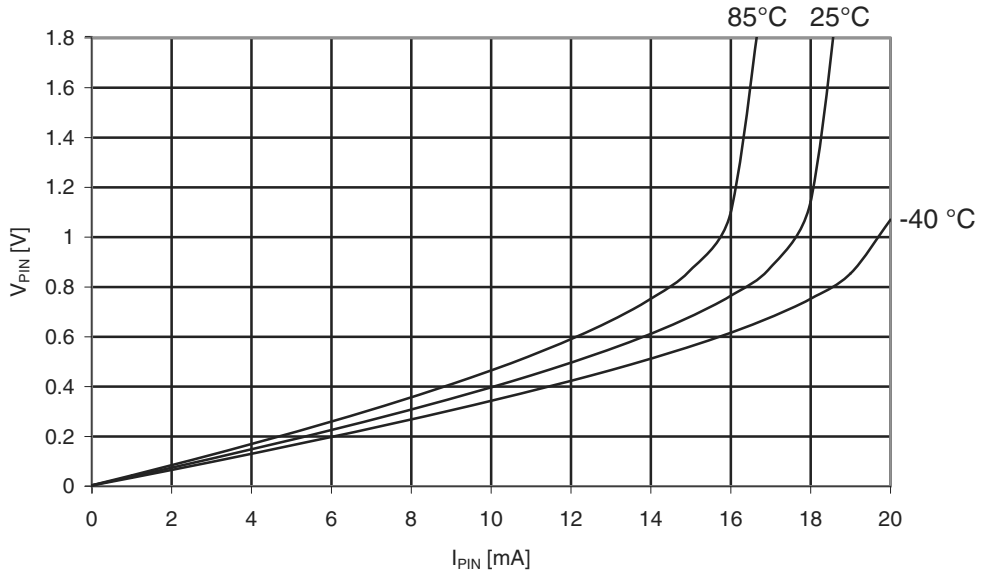


Figure 35-24. I/O Pin Output Voltage vs. Sink Current



35.9.2 Internal 2 MHz Oscillator

Figure 35-35. Internal 2 MHz Oscillator CALA Calibration Step Size

T = -40 to 85°C, V_{CC} = 3V

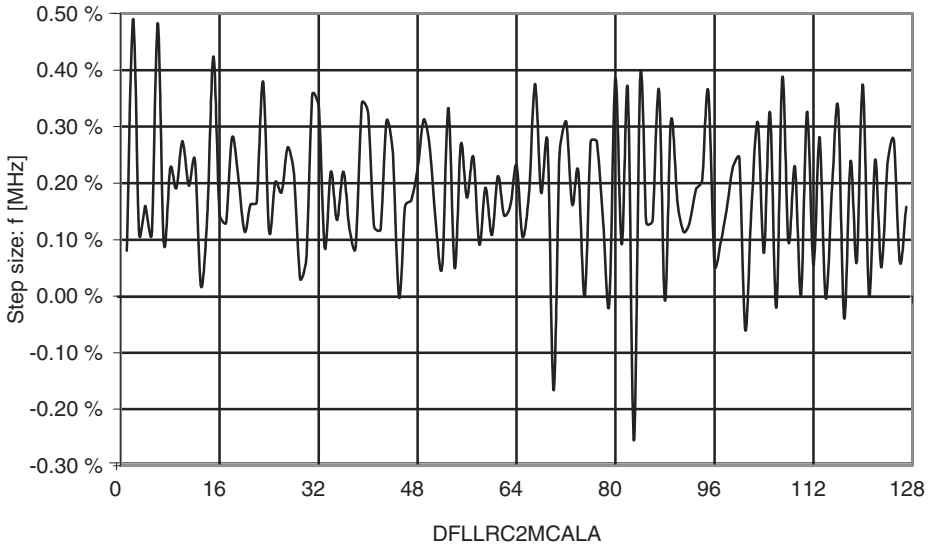


Figure 35-36. Internal 2 MHz Oscillator CALB Calibration Step Size

T = -40 to 85°C, V_{CC} = 3V

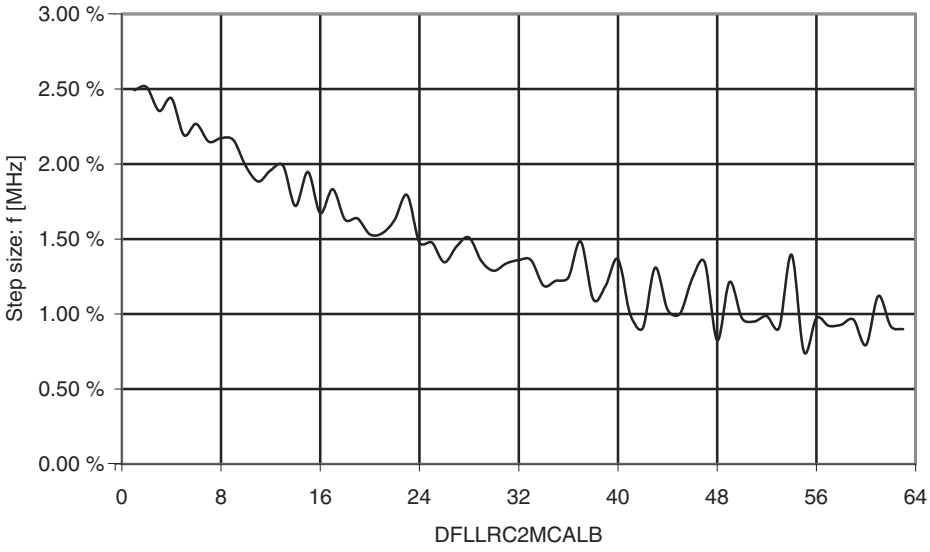
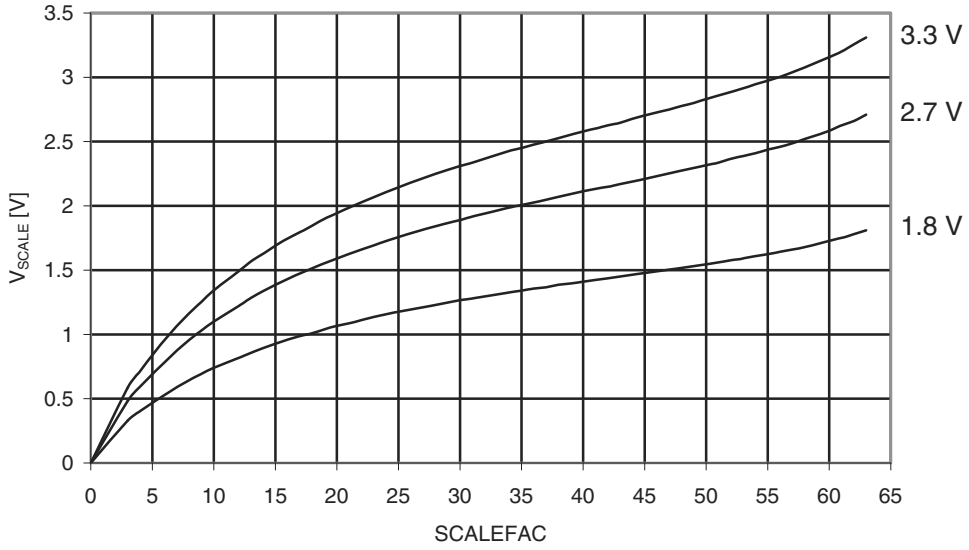


Figure 36-1. Analog Comparator Voltage Scaler vs. Scalefac
T = 25°C



Problem fix/Workaround

Use external voltage input for the analog comparator if accurate voltage levels are needed

3. ADC has increased INL error for some operating conditions

Some ADC configurations or operating condition will result in increased INL error.

In signed mode INL is increased to:

– 6LSB for sample rates above 1Msps, and up to 8 LSB for 2Msps sample rate.

– 6LSB for reference voltage below 1.1V when VCC is above 3.0V.

– 20LSB for ambient temperature below 0 degree C and reference voltage below 1.3V.

In unsigned mode, the INL error cannot be guaranteed, and this mode should not be used.

Problem fix/Workaround

None, avoid using the ADC in the above configurations in order to prevent increased INL error. Use the ADC in signed mode also for single ended measurements.

4. ADC gain stage output range is limited to 2.4 V

The amplified output of the ADC gain stage will never go above 2.4 V, hence the differential input will only give correct output when below 2.4 V/gain. For the available gain settings, this gives a differential input range of:

– 1x gain: 2.4 V

– 2x gain: 1.2 V

– 4x gain: 0.6 V

– 8x gain: 300 mV

– 16x gain: 150 mV

– 32x gain: 75 mV

– 64x gain: 38 mV

22. TWI Transmit collision flag not cleared on repeated start

The TWI transmit collision flag should be automatically cleared on start and repeated start, but is only cleared on start.

Problem fix/Workaround

Clear the flag in software after address interrupt.

23. Clearing TWI Stop Interrupt Flag may lock the bus

If software clears the STOP Interrupt Flag (APIF) on the same Peripheral Clock cycle as the hardware sets this flag due to a new address received, CLKHOLD is not cleared and the SCL line is not released. This will lock the bus.

Problem fix/Workaround

Check if the bus state is IDLE. If this is the case, it is safe to clear APIF. If the bus state is not IDLE, wait for the SCL pin to be low before clearing APIF.

Code:

```
/* Only clear the interrupt flag if within a "safe zone". */
while ( /* Bus not IDLE: */
       ((COMMS_TWI.MASTER.STATUS & TWI_MASTER_BUSSTATE_gm) !=
         TWI_MASTER_BUSSTATE_IDLE_gc)) &&
         /* SCL not held by slave: */
         !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm)
      )
{
    /* Ensure that the SCL line is low */
    if ( !(COMMS_PORT.IN & PIN1_bm) )
        if ( !(COMMS_PORT.IN & PIN1_bm) )
            break;
}
/* Check for an pending address match interrupt */
if ( !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm) )
{
    /* Safely clear interrupt flag */
    COMMS_TWI.SLAVE.STATUS |= (uint8_t)TWI_SLAVE_APIF_bm;
}
```

24. TWI START condition at bus timeout will cause transaction to be dropped

If Bus Timeout is enabled and a timeout occurs on the same Peripheral Clock cycle as a START is detected, the transaction will be dropped.

Problem fix/Workaround

None.

25. TWI Data Interrupt Flag erroneously read as set

When issuing the TWI slave response command CMD=0b11, it takes 1 Peripheral Clock cycle to clear the data interrupt flag (DIF). A read of DIF directly after issuing the command will show the DIF still set.

Problem fix/Workaround

Add one NOP instruction before checking DIF.

36.1.2 rev. B

- **Bandgap voltage input for the ACs can not be changed when used for both ACs simultaneously**
- **VCC voltage scaler for AC is non-linear**
- **ADC has increased INL error for some operating conditions**
- **ADC gain stage output range is limited to 2.4 V**
- **ADC Event on compare match non-functional**
- **Bandgap measurement with the ADC is non-functional when VCC is below 2.7V**
- **Accuracy lost on first three samples after switching input to ADC gain stage**
- **Configuration of PGM and CWCM not as described in XMEGA A Manual**
- **PWM is not restarted properly after a fault in cycle-by-cycle mode**
- **BOD will be enabled at any reset**
- **DAC is nonlinear and inaccurate when reference is above 2.4V or VCC - 0.6V**
- **DAC has increased INL or noise for some operating conditions**
- **DAC refresh may be blocked in S/H mode**
- **Conversion lost on DAC channel B in event triggered mode**
- **EEPROM page buffer always written when NVM DATA0 is written**
- **Pending full asynchronous pin change interrupts will not wake the device**
- **Pin configuration does not affect Analog Comparator Output**
- **NMI Flag for Crystal Oscillator Failure automatically cleared**
- **Writing EEPROM or Flash while reading any of them will not work**
- **Crystal start-up time required after power-save even if crystal is source for RTC**
- **RTC Counter value not correctly read after sleep**
- **Pending asynchronous RTC-interrupts will not wake up device**
- **TWI Transmit collision flag not cleared on repeated start**
- **Clearing TWI Stop Interrupt Flag may lock the bus**
- **TWI START condition at bus timeout will cause transaction to be dropped**
- **TWI Data Interrupt Flag (DIF) erroneously read as set**
- **WDR instruction inside closed window will not issue reset**

1. Bandgap voltage input for the ACs cannot be changed when used for both ACs simultaneously

If the Bandgap voltage is selected as input for one Analog Comparator (AC) and then selected/deselected as input for another AC, the first comparator will be affected for up to 1 µs and could potentially give a wrong comparison result.

Problem fix/Workaround

If the Bandgap is required for both ACs simultaneously, configure the input selection for both ACs before enabling any of them.

2. VCC voltage scaler for AC is non-linear

The 6-bit VCC voltage scaler in the Analog Comparators is non-linear.

Problem fix/Workaround

None.

26. TWI Data Interrupt Flag erroneously read as set

When issuing the TWI slave response command CMD=0b11, it takes 1 Peripheral Clock cycle to clear the data interrupt flag (DIF). A read of DIF directly after issuing the command will show the DIF still set.

Problem fix/Workaround

Add one NOP instruction before checking DIF.

27. WDR instruction inside closed window will not issue reset

When a WDR instruction is execute within one ULP clock cycle after updating the window control register, the counter can be cleared without giving a system reset.

Problem fix/Workaround

Wait at least one ULP clock cycle before executing a WDR instruction.

36.2.3 rev. A

Not sampled.

37.9 8068M – 09/09

1. Updated ”Electrical Characteristics” on page 63.
2. Added ”Flash and EEPROM Memory Characteristics” on page 66.
3. Added Errata for ”ATxmega192A3, ATxmega128A3, ATxmega64A3” on page 110.

37.10 8068L – 06/09

1. Updated ”Ordering Information” on page 2.
2. Updated ”Features” on page 39.
3. Updated ”Overview” on page 43.
4. Updated ”Overview” on page 48.
5. Added ”Electrical Characteristics” on page 63.
6. Added ”Typical Characteristics” on page 72.
7. Updated “”Errata” on page 93.

37.11 8068K – 02/09

1. Added ”Errata” on page 93 for ATxmega256A3 rev B.

37.12 8068J – 12/08

1. Added ”Errata” on page 93 for ATxmega256A3 rev A.

37.13 8068I – 11/08

1. Updated Featurelist in ”Memories” on page 9.

37.14 8068H – 10/08

1. Updated Table 14-1 on page 25.

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