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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	192KB (96K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega192a3-aur

4. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on http://www.atmel.com/avr.

4.1 Recommended reading

- XMEGA Manual
- XMEGA Application Notes

This device data sheet only contains part specific information and a short description of each peripheral and module. The XMEGA Manual describes the modules and peripherals in depth. The XMEGA application notes contain example code and show applied use of the modules and peripherals.

The XMEGA Manual and Application Notes are available from http://www.atmel.com/avr.

5. Disclaimer

For devices that are not available yet, typical values contained in this datasheet are based on simulations and characterization of other AVR XMEGA microcontrollers manufactured on the same process technology. Min. and Max values will be available after the device is characterized.

12. System Control and Reset

12.1 Features

- **Multiple reset sources for safe operation and device reset**
  - **Power-On Reset**
  - **External Reset**
  - **Watchdog Reset**
    The Watchdog Timer runs from separate, dedicated oscillator
  - **Brown-Out Reset**
    Accurate, programmable Brown-Out levels
  - **PDI reset**
  - **Software reset**
- **Asynchronous reset**
  - **No running clock in the device is required for reset**
- **Reset status register**

12.2 Resetting the AVR

During reset, all I/O registers are set to their initial values. The SRAM content is not reset. Application execution starts from the Reset Vector. The instruction placed at the Reset Vector should be an Absolute Jump (JMP) instruction to the reset handling routine. By default the Reset Vector address is the lowest Flash program memory address, ‘0’, but it is possible to move the Reset Vector to the first address in the Boot Section.

The I/O ports of the AVR are immediately tri-stated when a reset source goes active. The reset functionality is asynchronous, so no running clock is required to reset the device. After the device is reset, the reset source can be determined by the application by reading the Reset Status Register.

12.3 Reset Sources

12.3.1 Power-On Reset

The MCU is reset when the supply voltage VCC is below the Power-on Reset threshold voltage.

12.3.2 External Reset

The MCU is reset when a low level is present on the RESET pin.

12.3.3 Watchdog Reset

The MCU is reset when the Watchdog Timer period expires and the Watchdog Reset is enabled. The Watchdog Timer runs from a dedicated oscillator independent of the System Clock. For more details see ”WDT - Watchdog Timer” on page 24.

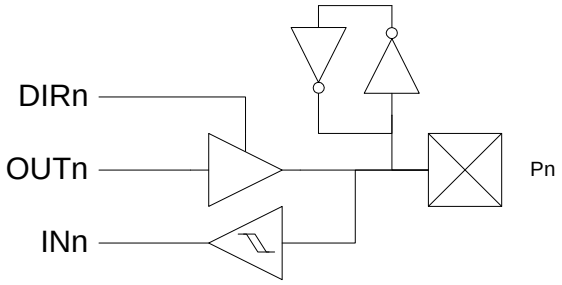
12.3.4 Brown-Out Reset

The MCU is reset when the supply voltage VCC is below the Brown-Out Reset threshold voltage and the Brown-out Detector is enabled. The Brown-out threshold voltage is programmable.

12.3.5 PDI reset

The MCU can be reset through the Program and Debug Interface (PDI).

Figure 15-4. I/O configuration - Totem-pole with bus-keeper



15.3.5 Others

Figure 15-5. Output configuration - Wired-OR with optional pull-down

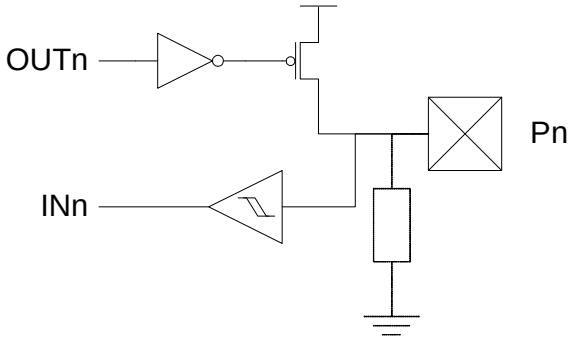
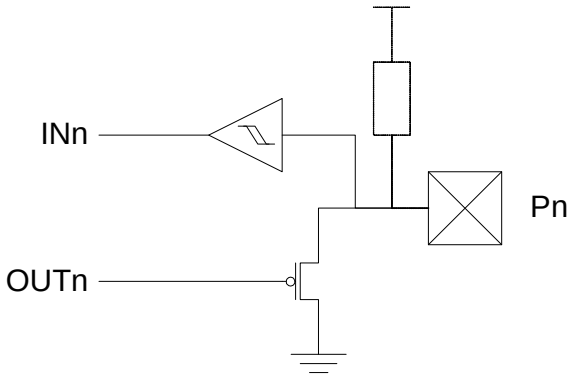


Figure 15-6. I/O configuration - Wired-AND with optional pull-up



16. T/C - 16-bits Timer/Counter with PWM

16.1 Features

- **Seven 16-bit Timer/Counters**
  - **Four Timer/Counters of type 0**
  - **Three Timer/Counters of type 1**
- **Four Compare or Capture (CC) Channels in Timer/Counter 0**
- **Two Compare or Capture (CC) Channels in Timer/Counter 1**
- **Double Buffered Timer Period Setting**
- **Double Buffered Compare or Capture Channels**
- **Waveform Generation:**
  - **Single Slope Pulse Width Modulation**
  - **Dual Slope Pulse Width Modulation**
  - **Frequency Generation**
- **Input Capture:**
  - **Input Capture with Noise Cancelling**
  - **Frequency capture**
  - **Pulse width capture**
  - **32-bit input capture**
- **Event Counter with Direction Control**
- **Timer Overflow and Timer Error Interrupts and Events**
- **One Compare Match or Capture Interrupt and Event per CC Channel**
- **Supports DMA Operation**
- **Hi-Resolution Extension (Hi-Res)**
- **Advanced Waveform Extension (AWEX)**

16.2 Overview

XMEGA A3 has seven Timer/Counters, four Timer/Counter 0 and three Timer/Counter 1. The difference between them is that Timer/Counter 0 has four Compare/Capture channels, while Timer/Counter 1 has two Compare/Capture channels.

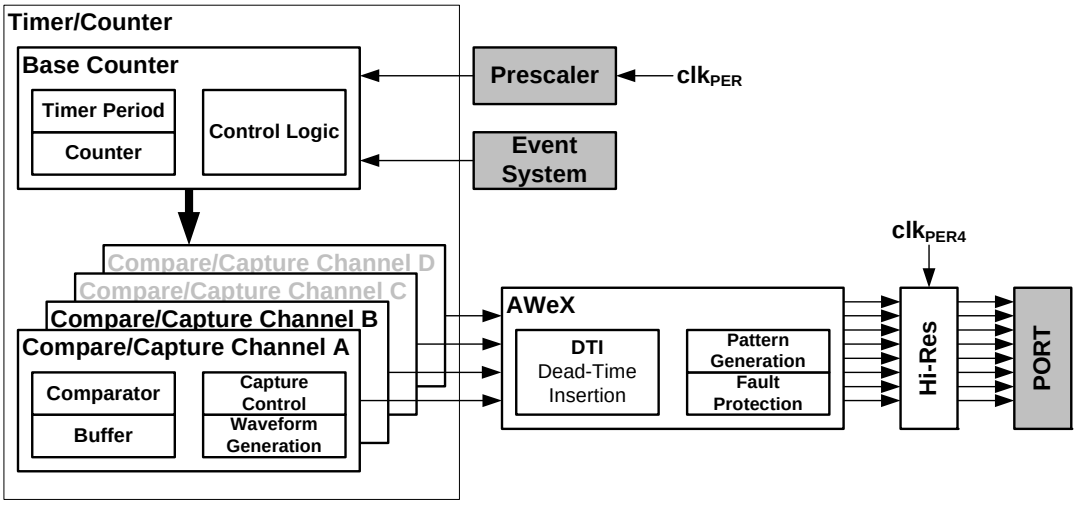
The Timer/Counters (T/C) are 16-bit and can count any clock, event or external input in the microcontroller. A programmable prescaler is available to get a useful T/C resolution. Updates of Timer and Compare registers are double buffered to ensure glitch free operation. Single slope PWM, dual slope PWM and frequency generation waveforms can be generated using the Compare Channels.

Through the Event System, any input pin or event in the microcontroller can be used to trigger input capture, hence no dedicated pins is required for this. The input capture has a noise canceller to avoid incorrect capture of the T/C, and can be used to do frequency and pulse width measurements.

A wide range of interrupt or event sources are available, including T/C Overflow, Compare match and Capture for each Compare/Capture channel in the T/C.

PORTC, PORTD and PORTE each has one Timer/Counter 0 and one Timer/Counter1. PORTF has one Timer/Counter 0. Notation of these are TCC0 (Time/Counter C0), TCC1, TCD0, TCD1, TCE0, TCE1 and TCF0, respectively.

Figure 16-1. Overview of a Timer/Counter and closely related peripherals



The Hi-Resolution Extension can be enabled to increase the waveform generation resolution by 2 bits (4x). This is available for all Timer/Counters. See ”Hi-Res - High Resolution Extension” on page 34 for more details.

The Advanced Waveform Extension can be enabled to provide extra and more advanced features for the Timer/Counter. This are only available for Timer/Counter 0. See ”AWEX - Advanced Waveform Extension” on page 33 for more details.

24. Crypto Engine

24.1 Features

- **Data Encryption Standard (DES) CPU instruction**
- **Advanced Encryption Standard (AES) Crypto module**
- **DES Instruction**
  - **Encryption and Decryption**
  - **Single-cycle DES instruction**
  - **Encryption/Decryption in 16 clock cycles per 8-byte block**
- **AES Crypto Module**
  - **Encryption and Decryption**
  - **Support 128-bit keys**
  - **Support XOR data load mode to the State memory for Cipher Block Chaining**
  - **Encryption/Decryption in 375 clock cycles per 16-byte block**

24.2 Overview

The Advanced Encryption Standard (AES) and Data Encryption Standard (DES) are two commonly used encryption standards. These are supported through an AES peripheral module and a DES CPU instruction. All communication interfaces and the CPU can optionally use AES and DES encrypted communication and data storage.

DES is supported by a DES instruction in the AVR XMEGA CPU. The 8-byte key and 8-byte data blocks must be loaded into the Register file, and then DES must be executed 16 times to encrypt/decrypt the data block.

The AES Crypto Module encrypts and decrypts 128-bit data blocks with the use of a 128-bit key. The key and data must be loaded into the key and state memory in the module before encryption/decryption is started. It takes 375 peripheral clock cycles before the encryption/decryption is done and decrypted/encrypted data can be read out, and an optional interrupt can be generated. The AES Crypto Module also has DMA support with transfer triggers when encryption/decryption is done and optional auto-start of encryption/decryption when the state memory is fully loaded.

30. Pinout and Pin Functions

The pinout of XMEGA A3 is shown "" on page 2. In addition to general I/O functionality, each pin may have several function. This will depend on which peripheral is enabled and connected to the actual pin. Only one of the alternate pin functions can be used at time.

30.1 Alternate Pin Function Description

The tables below show the notation for all pin functions available and describe its function.

30.1.1 Operation/Power Supply

VCC	Digital supply voltage
AVCC	Analog supply voltage
GND	Ground

30.1.2 Port Interrupt functions

SYNC	Port pin with full synchronous and limited asynchronous interrupt function
ASYNC	Port pin with full synchronous and full asynchronous interrupt function

30.1.3 Analog functions

ACn	Analog Comparator input pin n
AC0OUT	Analog Comparator 0 Output
ADCn	Analog to Digital Converter input pin n
DACn	Digital to Analog Converter output pin n
AREF	Analog Reference input pin

30.1.4 Timer/Counter and AWEX functions

OCnx	Output Compare Channel x for Timer/Counter n
$\overline{\text{OCnx}}$	Inverted Output Compare Channel x for Timer/Counter n
OCnxLS	Output Compare Channel x Low Side for Timer/Counter n
OCnxHS	Output Compare Channel x High Side for Timer/Counter n

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ROL	Rd	Rotate Left Through Carry	Rd(0) ← C, Rd(n+1) ← Rd(n), C ← Rd(7)	Z,C,N,V,H	1
ROR	Rd	Rotate Right Through Carry	Rd(7) ← C, Rd(n) ← Rd(n+1), C ← Rd(0)	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=0..6	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(3..0) ↔ Rd(7..4)	None	1
BSET	s	Flag Set	SREG(s) ← 1	SREG(s)	1
BCLR	s	Flag Clear	SREG(s) ← 0	SREG(s)	1
SBI	A, b	Set Bit in I/O Register	I/O(A, b) ← 1	None	1
CBI	A, b	Clear Bit in I/O Register	I/O(A, b) ← 0	None	1
BST	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
BLD	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1
SEC		Set Carry	C ← 1	C	1
CLC		Clear Carry	C ← 0	C	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	I	1
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Two’s Complement Overflow	V ← 1	V	1
CLV		Clear Two’s Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1
CLH		Clear Half Carry Flag in SREG	H ← 0	H	1
MCU Control Instructions					
BREAK		Break	(See specific descr. for BREAK)	None	1
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR)	None	1

Notes: 1. Cycle times for Data memory accesses assume internal memory accesses, and are not valid for accesses via the external RAM interface.
2. One extra cycle must be added when accessing Internal SRAM.

Table 34-1. Current Consumption (Continued)

Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{CC}	Power-save mode	RTC 1 kHz from Low Power 32kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.5	4	µA
			V_{CC} = 3.0V		0.7	4	
		RTC from Low Power 32kHz TOSC	V_{CC} = 3.0V		1.16		
	Reset Current Consumption	without Reset pull-up resistor current	V_{CC} = 3.0V		1300		
Module current consumption(2)							
I_{CC}	RC32M				460		µA
	RC32M w/DFLL	Internal 32.768kHz oscillator as DFLL source			594		
	RC2M				101		
	RC2M w/DFLL	Internal 32.768kHz oscillator as DFLL source			134		
	RC32K				27		
	PLL	Multiplication factor = 10x			202		
	Watchdog normal mode				1		
	BOD Continuous mode				128		
	BOD Sampled mode				1		
	Internal 1.00 V ref				80		
	Temperature reference				74		
	RTC with int. 32kHz RC as source	No prescaling			27		
	RTC with ULP as source	No prescaling			1		
	ADC	250 kS/s - Int. 1V Ref			2.9		mA
	DAC Normal Mode	1000 kS/s, Single channel, Int. 1V Ref			1.8		
	DAC Low-Power Mode	1000 KS/s, Single channel, Int. 1V Ref			0.95		
	DAC S/H Normal Mode	Int.1.1V Ref, Refresh 16CLK			2.9		
	DAC Low-Power Mode S/H	Int. 1.1V Ref, Refresh 16CLK			1.1		
	AC High-speed				195		µA
	AC Low-power				103		
	USART	Rx and Tx enabled, 9600 BAUD			5.4		
	DMA				128		
	Timer/Counter	Prescaler DIV1			20		
	AES				223		
	Flash/EEPROM Programming	Vcc = 2V			25		mA
		Vcc = 3V			33		

Notes: 1. All Power Reduction Registers set.
2. All parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1MHz External clock with no prescaling.

34.9 Brownout Detection Characteristics

Table 34-10. Brownout Detection Characteristics[1]

Symbol	Parameter	Condition	Min	Typ	Max	Units
	BOD level 0 falling Vcc		1.62	1.63	1.7	V
	BOD level 1 falling Vcc			1.9		
	BOD level 2 falling Vcc			2.17		
	BOD level 3 falling Vcc			2.43		
	BOD level 4 falling Vcc			2.68		
	BOD level 5 falling Vcc			2.96		
	BOD level 6 falling Vcc			3.22		
	BOD level 7 falling Vcc			3.49		
	Hysteresis	BOD level 0-5		1		%

Note: 1. BOD is calibrated at 85°C within BOD level 0 values, and BOD level 0 is the default level.

34.10 PAD Characteristics

Table 34-11. PAD Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input High Voltage	V_{CC} = 2.4 - 3.6V	0.7*V_{CC}		V_{CC}+0.5	V
		V_{CC} = 1.6 - 2.4V	0.8*V_{CC}		V_{CC}+0.5	
V_{IL}	Input Low Voltage	V_{CC} = 2.4 - 3.6V	-0.5		0.3*V_{CC}	
		V_{CC} = 1.6 - 2.4V	-0.5		0.2*V_{CC}	
V_{OL}	Output Low Voltage GPIO	I_{OH} = 15 mA, V_{CC} = 3.3V		0.4	0.76	
		I_{OH} = 10 mA, V_{CC} = 3.0V		0.3	0.64	
		I_{OH} = 5 mA, V_{CC} = 1.8V		0.2	0.46	
V_{OH}	Output High Voltage GPIO	I_{OH} = -8 mA, V_{CC} = 3.3V	2.6	2.9		
		I_{OH} = -6 mA, V_{CC} = 3.0V	2.1	2.7		
		I_{OH} = -2 mA, V_{CC} = 1.8V	1.4	1.6		
I_{IL}	Input Leakage Current I/O pin			<0.001	1	µA
I_{IH}	Input Leakage Current I/O pin			<0.001	1	
R_P	I/O pin Pull/Buss keeper Resistor			20		kΩ
R_{RST}	Reset pin Pull-up Resistor			20		
	Input hysteresis			0.5		V

Figure 35-3. Active Supply Current vs. Vcc

f_{SYS} = 1.0 MHz External Clock

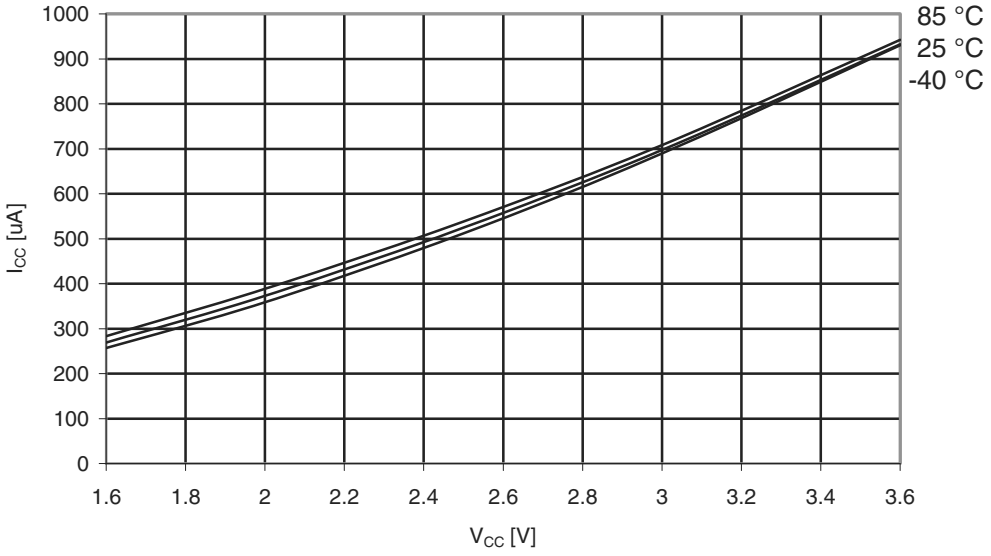


Figure 35-4. Active Supply Current vs. VCC

f_{SYS} = 32.768 kHz internal RC

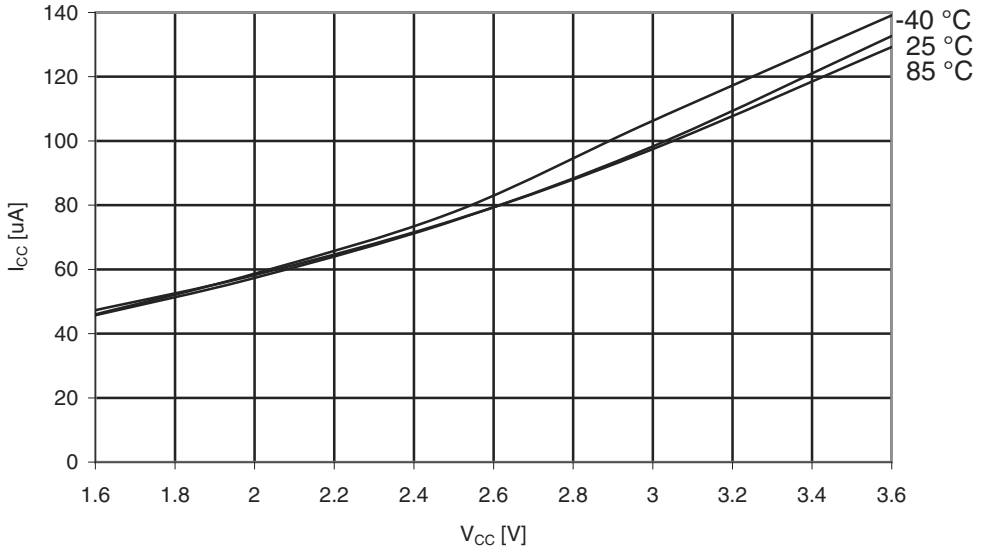
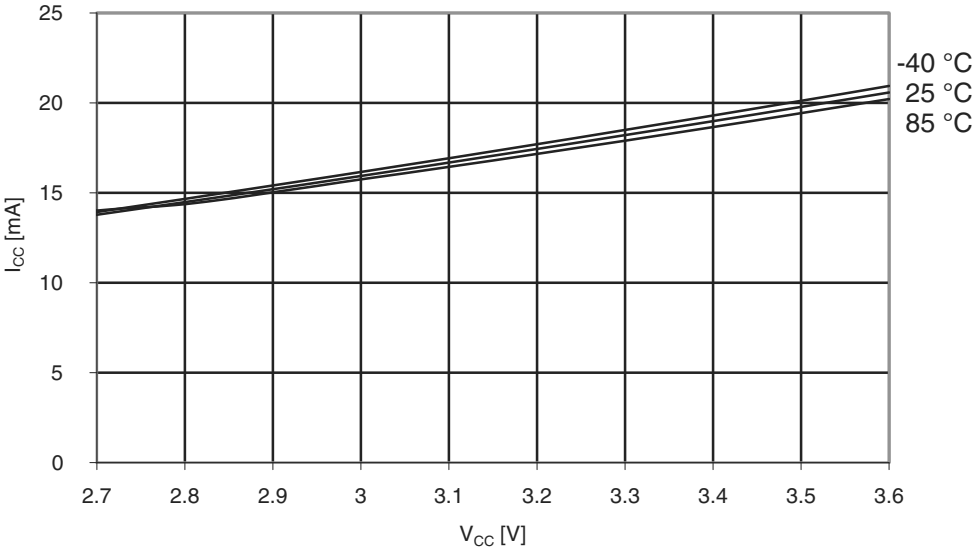


Figure 35-7. Active Supply Current vs. Vcc

f_{SYS} = 32 MHz internal RC



35.2 Idle Supply Current

Figure 35-8. Idle Supply Current vs. Frequency

f_{SYS} = 0 - 1.0 MHz, T = 25°C

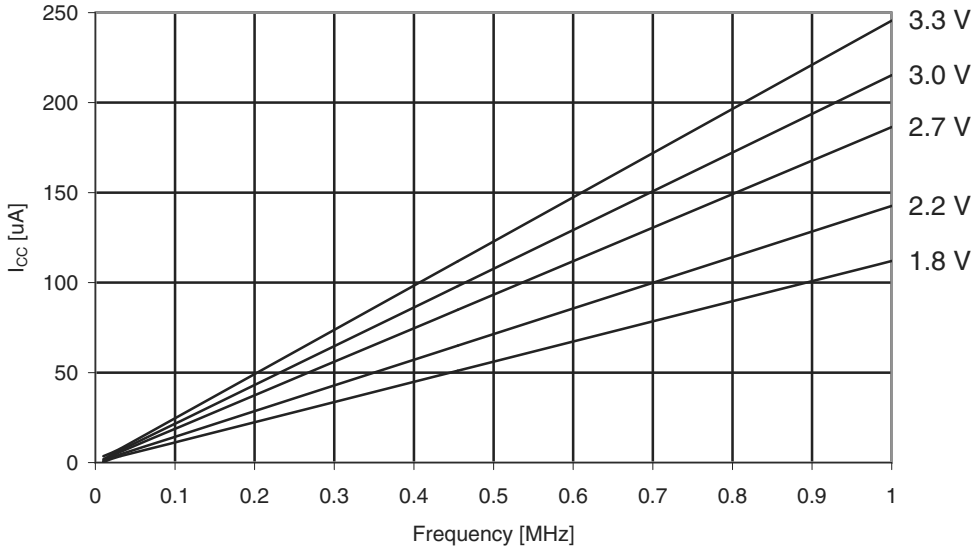


Figure 35-13. Idle Supply Current vs. Vcc

f_{SYS} = 32 MHz internal RC prescaled to 8 MHz

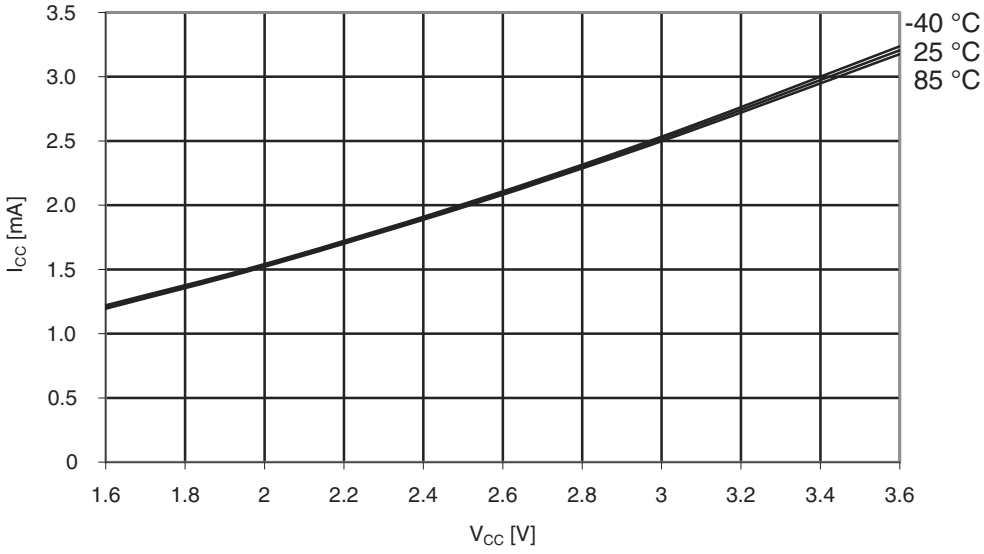


Figure 35-14. Idle Supply Current vs. Vcc

f_{SYS} = 32 MHz internal RC

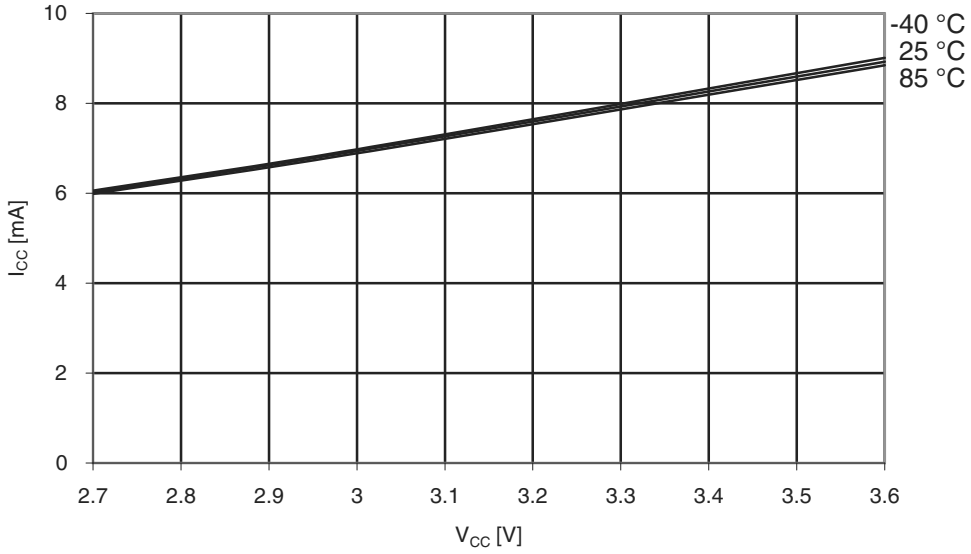


Figure 35-23. I/O Pin Output Voltage vs. Source Current

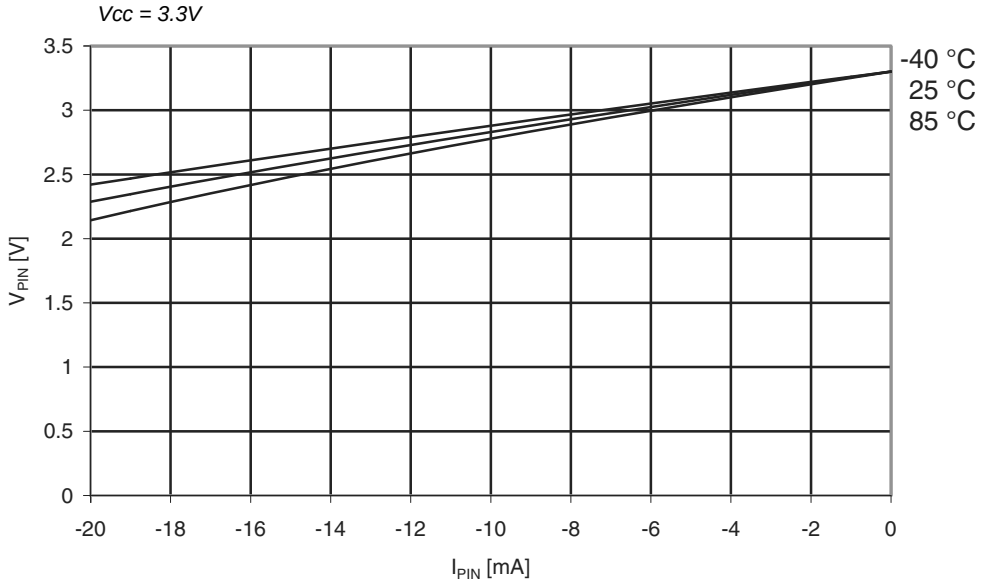
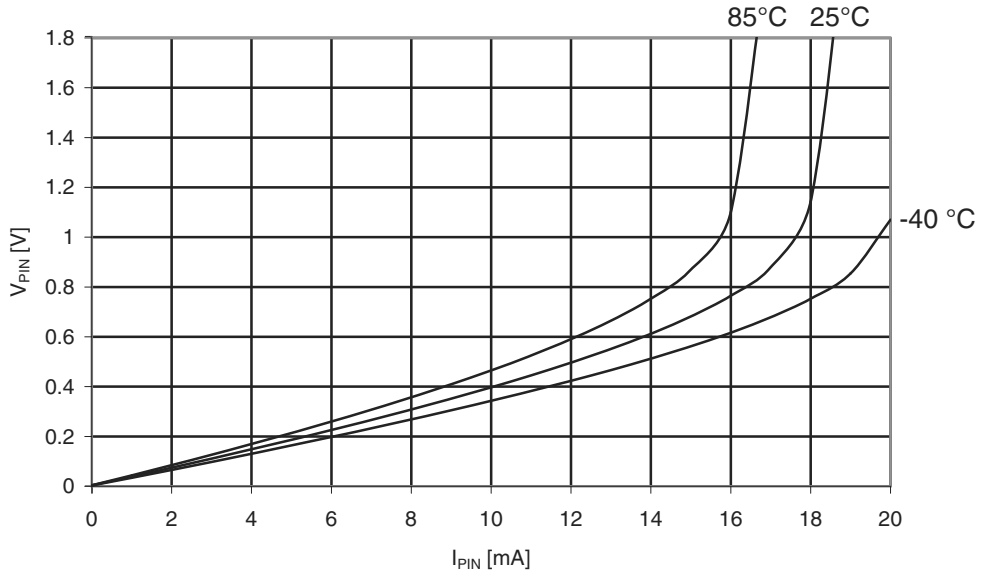


Figure 35-24. I/O Pin Output Voltage vs. Sink Current



35.9.2 Internal 2 MHz Oscillator

Figure 35-35. Internal 2 MHz Oscillator CALA Calibration Step Size

T = -40 to 85°C, V_{CC} = 3V

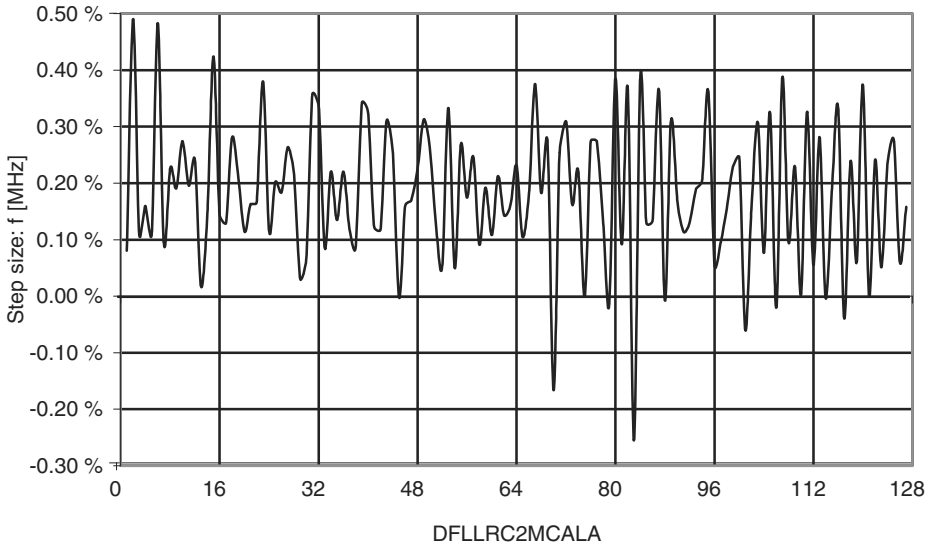
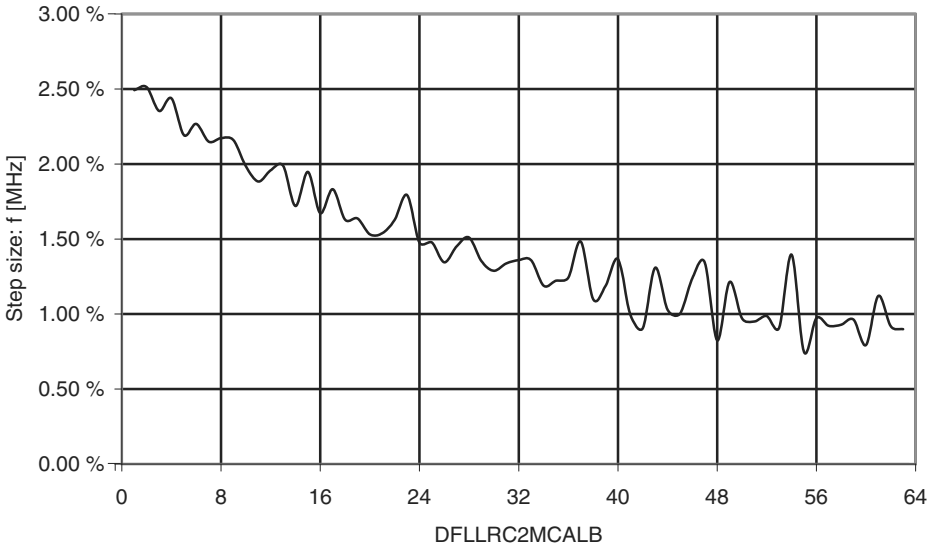


Figure 35-36. Internal 2 MHz Oscillator CALB Calibration Step Size

T = -40 to 85°C, V_{CC} = 3V



35.9.3 Internal 32 MHZ Oscillator

Figure 35-37. Internal 32 MHz Oscillator CALA Calibration Step Size

T = -40 to 85°C, V_{CC} = 3V

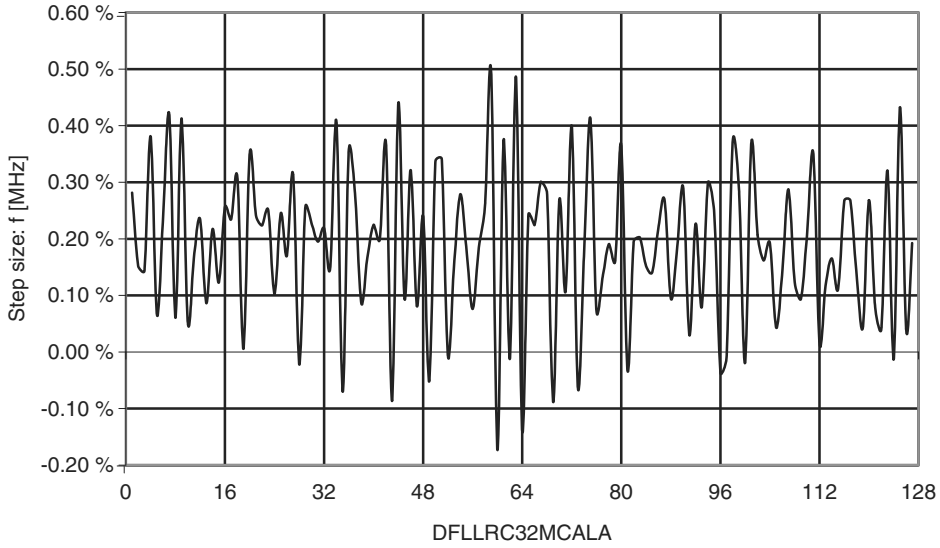


Figure 35-38. Internal 32 MHz Oscillator CALB Calibration Step Size

T = -40 to 85°C, V_{CC} = 3V

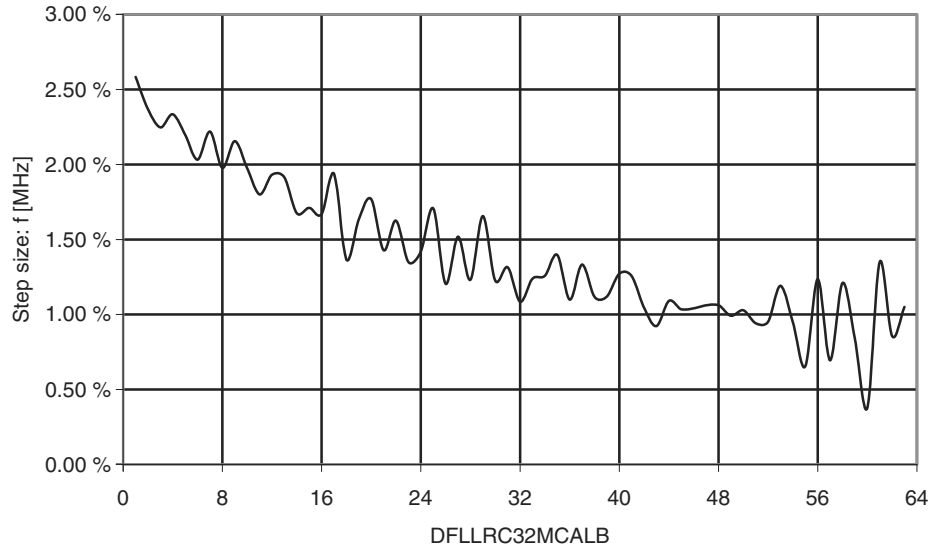
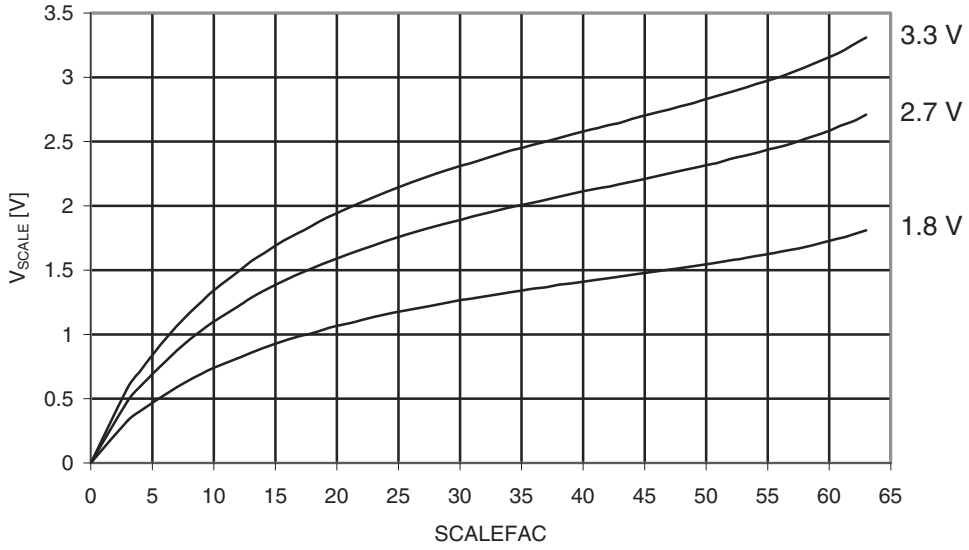


Figure 36-1. Analog Comparator Voltage Scaler vs. Scalefac
T = 25°C



Problem fix/Workaround

Use external voltage input for the analog comparator if accurate voltage levels are needed

3. ADC has increased INL error for some operating conditions

Some ADC configurations or operating condition will result in increased INL error.

In signed mode INL is increased to:

– 6LSB for sample rates above 1Msps, and up to 8 LSB for 2Msps sample rate.

– 6LSB for reference voltage below 1.1V when VCC is above 3.0V.

– 20LSB for ambient temperature below 0 degree C and reference voltage below 1.3V.

In unsigned mode, the INL error cannot be guaranteed, and this mode should not be used.

Problem fix/Workaround

None, avoid using the ADC in the above configurations in order to prevent increased INL error. Use the ADC in signed mode also for single ended measurements.

4. ADC gain stage output range is limited to 2.4 V

The amplified output of the ADC gain stage will never go above 2.4 V, hence the differential input will only give correct output when below 2.4 V/gain. For the available gain settings, this gives a differential input range of:

– 1x gain: 2.4 V

– 2x gain: 1.2 V

– 4x gain: 0.6 V

– 8x gain: 300 mV

– 16x gain: 150 mV

– 32x gain: 75 mV

– 64x gain: 38 mV

36.2.2 rev. B

- **Bandgap voltage input for the ACs can not be changed when used for both ACs simultaneously**
- **VCC voltage scaler for AC is non-linear**
- **ADC has increased INL error for some operating conditions**
- **ADC gain stage output range is limited to 2.4 V**
- **ADC Event on compare match non-functional**
- **Bandgap measurement with the ADC is non-functional when VCC is below 2.7V**
- **Accuracy lost on first three samples after switching input to ADC gain stage**
- **Configuration of PGM and CWCM not as described in XMEGA A Manual**
- **PWM is not restarted properly after a fault in cycle-by-cycle mode**
- **BOD will be enabled at any reset**
- **DAC is nonlinear and inaccurate when reference is above 2.4V or VCC - 0.6V**
- **DAC has increased INL or noise for some operating conditions**
- **DAC refresh may be blocked in S/H mode**
- **Conversion lost on DAC channel B in event triggered mode**
- **EEPROM page buffer always written when NVM DATA0 is written**
- **Pending full asynchronous pin change interrupts will not wake the device**
- **Pin configuration does not affect Analog Comparator Output**
- **NMI Flag for Crystal Oscillator Failure automatically cleared**
- **Writing EEPROM or Flash while reading any of them will not work**
- **Crystal start-up time required after power-save even if crystal is source for RTC**
- **RTC Counter value not correctly read after sleep**
- **Pending asynchronous RTC-interrupts will not wake up device**
- **TWI Transmit collision flag not cleared on repeated start**
- **Clearing TWI Stop Interrupt Flag may lock the bus**
- **TWI START condition at bus timeout will cause transaction to be dropped**
- **TWI Data Interrupt Flag (DIF) erroneously read as set**
- **WDR instruction inside closed window will not issue reset**

1. Bandgap voltage input for the ACs cannot be changed when used for both ACs simultaneously

If the Bandgap voltage is selected as input for one Analog Comparator (AC) and then selected/deselected as input for another AC, the first comparator will be affected for up to 1 µs and could potentially give a wrong comparison result.

Problem fix/Workaround

If the Bandgap is required for both ACs simultaneously, configure the input selection for both ACs before enabling any of them.

2. VCC voltage scaler for AC is non-linear

The 6-bit VCC voltage scaler in the Analog Comparators is non-linear.

8. Updated ”DAC Characteristics” on page 68. Removed DC output impedence.
9. Updated Figure 35-6 on page 74. Replaced the figure by a correct one.
10. Fixed typo in “Errata” section.

37.5 8068Q – 02/10

1. Added ”PDI Speed” on page 92.

37.6 8068P – 02/10

1. Updated the device pin-out Figure 2-1 on page 3. PDI_CLK and PDI_DATA renamed only PDI.
2. Removed JTAG Reset from the datasheet.
3. Updated ”DAC - 12-bit Digital to Analog Converter” on page 43. DAC uses internal 1.0 voltage.
4. Added Table 34-19 on page 71.
5. Updated ”Timer/Counter and AWEX functions” on page 49.
6. Updated ”Alternate Pin Function Description” on page 49.
7. Updated all ”Electrical Characteristics” on page 63.
8. Updated ”PAD Characteristics” on page 69.
9. Changed Internal Oscillator Speed to ”Oscillators and Wake-up Time” on page 88.
10. Updated ”Errata” on page 93

37.7 8068O – 11/09

1. Updated Table 34-3 on page 66, Endurance and Data Retention.
2. Updated Table 34-11 on page 69, Input hysteresis is in V and not in mV.
3. Updated ”Errata” on page 93.

37.8 8068N – 10/09

1. Updated ”Errata” on page 93.

37.9 8068M – 09/09

1. Updated ”Electrical Characteristics” on page 63.
2. Added ”Flash and EEPROM Memory Characteristics” on page 66.
3. Added Errata for ”ATxmega192A3, ATxmega128A3, ATxmega64A3” on page 110.

37.10 8068L – 06/09

1. Updated ”Ordering Information” on page 2.
2. Updated ”Features” on page 39.
3. Updated ”Overview” on page 43.
4. Updated ”Overview” on page 48.
5. Added ”Electrical Characteristics” on page 63.
6. Added ”Typical Characteristics” on page 72.
7. Updated “”Errata” on page 93.

37.11 8068K – 02/09

1. Added ”Errata” on page 93 for ATxmega256A3 rev B.

37.12 8068J – 12/08

1. Added ”Errata” on page 93 for ATxmega256A3 rev A.

37.13 8068I – 11/08

1. Updated Featurelist in ”Memories” on page 9.

37.14 8068H – 10/08

1. Updated Table 14-1 on page 25.