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What is "Embedded - Microcontrollers"?

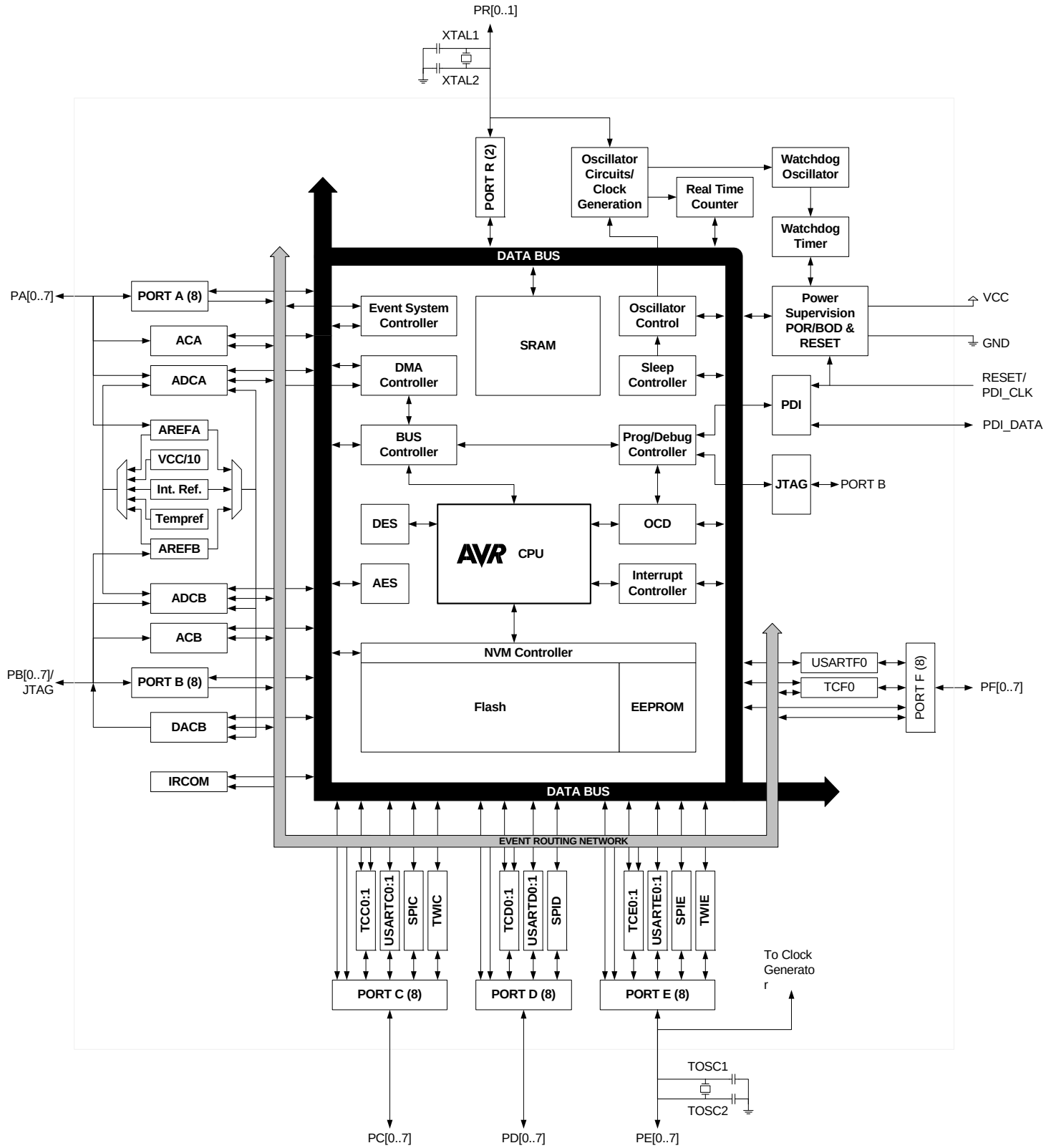
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	256KB (128K x 16)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega256a3-au

3.1 Block Diagram

Figure 3-1. XMEGA A3 Block Diagram



7.4.1 I/O Memory

All peripherals and modules are addressable through I/O memory locations in the data memory space. All I/O memory locations can be accessed by the Load (LD/LDS/LDD) and Store (ST/STS/STD) instructions, transferring data between the 32 general purpose registers in the CPU and the I/O Memory.

The IN and OUT instructions can address I/O memory locations in the range 0x00 - 0x3F directly.

I/O registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. The value of single bits can be checked by using the SBIS and SBIC instructions on these registers.

The I/O memory address for all peripherals and modules in XMEGA A3 is shown in the ”Peripheral Module Address Map” on page 56.

7.4.2 SRAM Data Memory

The XMEGA A3 devices have internal SRAM memory for data storage.

7.4.3 EEPROM Data Memory

The XMEGA A3 devices have internal EEPROM memory for non-volatile data storage. It is addressable either in a separate data space or it can be memory mapped into the normal data memory space. The EEPROM memory supports both byte and page access.

9. Event System

9.1 Features

- **Inter-peripheral communication and signalling with minimum latency**
- **CPU and DMA independent operation**
- **8 Event Channels allows for up to 8 signals to be routed at the same time**
- **Events can be generated by**
  - **Timer/Counters (TCxn)**
  - **Real Time Counter (RTC)**
  - **Analog to Digital Converters (ADCx)**
  - **Analog Comparators (ACx)**
  - **Ports (PORTx)**
  - **System Clock (Clk_{SYS})**
  - **Software (CPU)**
- **Events can be used by**
  - **Timer/Counters (TCxn)**
  - **Analog to Digital Converters (ADCx)**
  - **Digital to Analog Converters (DACx)**
  - **Ports (PORTx)**
  - **DMA Controller (DMAC)**
  - **IR Communication Module (IRCOM)**
- **The same event can be used by multiple peripherals for synchronized timing**
- **Advanced Features**
  - **Manual Event Generation from software (CPU)**
  - **Quadrature Decoding**
  - **Digital Filtering**
- **Functions in Active and Idle mode**

9.2 Overview

The Event System is a set of features for inter-peripheral communication. It enables the possibility for a change of state in one peripheral to automatically trigger actions in one or more peripherals. What changes in a peripheral that will trigger actions in other peripherals are configurable by software. It is a simple, but powerful system as it allows for autonomous control of peripherals without any use of interrupts, CPU or DMA resources.

The indication of a change in a peripheral is referred to as an event, and is usually the same as the interrupt conditions for that peripheral. Events are passed between peripherals using a dedicated routing network called the Event Routing Network. Figure 9-1 on page 17 shows a basic block diagram of the Event System with the Event Routing Network and the peripherals to which it is connected. This highly flexible system can be used for simple routing of signals, pin functions or for sequencing of events.

The maximum latency is two CPU clock cycles from when an event is generated in one peripheral, until the actions are triggered in one or more other peripherals.

The Event System is functional in both Active and Idle modes.

11. Power Management and Sleep Modes

11.1 Features

- **5 sleep modes**
  - **Idle**
  - **Power-down**
  - **Power-save**
  - **Standby**
  - **Extended standby**
- **Power Reduction registers to disable clocks to unused peripherals**

11.2 Overview

The XMEGA A3 provides various sleep modes tailored to reduce power consumption to a minimum. All sleep modes are available and can be entered from Active mode. In Active mode the CPU is executing application code. The application code decides when and which sleep mode to enter. Interrupts from enabled peripherals and all enabled reset sources can restore the microcontroller from sleep to Active mode.

In addition, Power Reduction registers provide a method to stop the clock to individual peripherals from software. When this is done, the current state of the peripheral is frozen and there is no power consumption from that peripheral. This reduces the power consumption in Active mode and Idle sleep mode.

11.3 Sleep Modes

11.3.1 Idle Mode

In Idle mode the CPU and Non-Volatile Memory are stopped, but all peripherals including the Interrupt Controller, Event System and DMA Controller are kept running. Interrupt requests from all enabled interrupts will wake the device.

11.3.2 Power-down Mode

In Power-down mode all system clock sources, and the asynchronous Real Time Counter (RTC) clock source, are stopped. This allows operation of asynchronous modules only. The only interrupts that can wake up the MCU are the Two Wire Interface address match interrupts, and asynchronous port interrupts, e.g pin change.

11.3.3 Power-save Mode

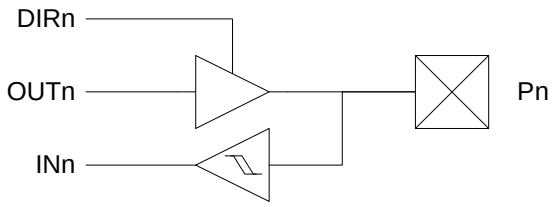
Power-save mode is identical to Power-down, with one exception: If the RTC is enabled, it will keep running during sleep and the device can also wake up from RTC interrupts.

11.3.4 Standby Mode

Standby mode is identical to Power-down with the exception that all enabled system clock sources are kept running, while the CPU, Peripheral and RTC clocks are stopped. This reduces the wake-up time when external crystals or resonators are used.

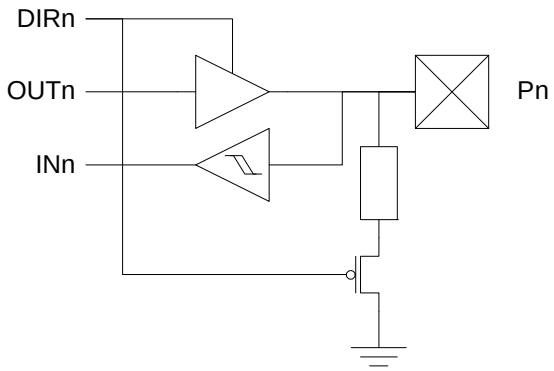
15.3.1 Push-pull

Figure 15-1. I/O configuration - Totem-pole



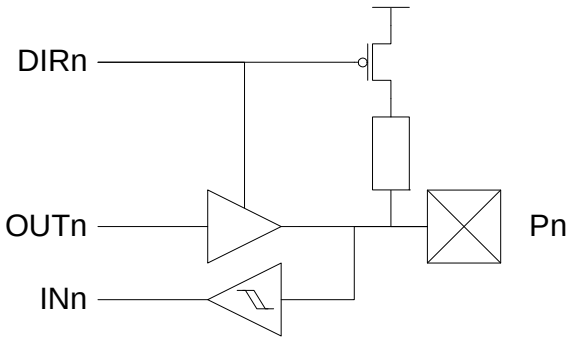
15.3.2 Pull-down

Figure 15-2. I/O configuration - Totem-pole with pull-down (on input)



15.3.3 Pull-up

Figure 15-3. I/O configuration - Totem-pole with pull-up (on input)



15.3.4 Bus-keeper

The bus-keeper's weak output produces the same logical level as the last output level. It acts as a pull-up if the last level was '1', and pull-down if the last level was '0'.

29. Program and Debug Interfaces

29.1 Features

- **PDI - Program and Debug Interface (Atmel proprietary 2-pin interface)**
- **JTAG Interface (IEEE std. 1149.1 compliant)**
- **Boundary-scan capabilities according to the IEEE Std. 1149.1 (JTAG)**
- **Access to the OCD system**
- **Programming of Flash, EEPROM, Fuses and Lock Bits**

29.2 Overview

The programming and debug facilities are accessed through the JTAG and PDI physical interfaces. The PDI physical interface uses one dedicated pin together with the Reset pin, and no general purpose pins are used. JTAG uses four general purpose pins on PORTB.

The PDI is an Atmel proprietary protocol for communication between the microcontroller and Atmel's or third party development tools.

29.3 IEEE 1149.1 (JTAG) Boundary-scan

The JTAG physical layer handles the basic low-level serial communication over four I/O lines named TMS, TCK, TDI, and TDO. It complies to the IEEE Std. 1149.1 for test access port and boundary scan.

29.3.1 Boundary-scan Order

Table 30-8 on page 53 shows the Scan order between TDI and TDO when the Boundary-scan chain is selected as data path. Bit 0 is the LSB; the first bit scanned in, and the first bit scanned out. The scan order follows the pin-out order. Bit 4, 5, 6 and 7 of Port B is not in the scan chain, since these pins constitute the TAP pins when the JTAG is enabled.

29.3.2 Boundary-scan Description Language Files

Boundary-scan Description Language (BSDL) files describe Boundary-scan capable devices in a standard format used by automated test-generation software. The order and function of bits in the Boundary-scan Data Register are included in this description. BSDL files are available for ATxmega256/192/128/64A3 devices.

See Table 30-8 on page 53 for ATxmega256/192/128/64A3 Boundary Scan Order.

30. Pinout and Pin Functions

The pinout of XMEGA A3 is shown "" on page 2. In addition to general I/O functionality, each pin may have several function. This will depend on which peripheral is enabled and connected to the actual pin. Only one of the alternate pin functions can be used at time.

30.1 Alternate Pin Function Description

The tables below show the notation for all pin functions available and describe its function.

30.1.1 Operation/Power Supply

VCC	Digital supply voltage
AVCC	Analog supply voltage
GND	Ground

30.1.2 Port Interrupt functions

SYNC	Port pin with full synchronous and limited asynchronous interrupt function
ASYNC	Port pin with full synchronous and full asynchronous interrupt function

30.1.3 Analog functions

ACn	Analog Comparator input pin n
AC0OUT	Analog Comparator 0 Output
ADCn	Analog to Digital Converter input pin n
DACn	Digital to Analog Converter output pin n
AREF	Analog Reference input pin

30.1.4 Timer/Counter and AWEX functions

OCnx	Output Compare Channel x for Timer/Counter n
$\overline{\text{OCnx}}$	Inverted Output Compare Channel x for Timer/Counter n
OCnxLS	Output Compare Channel x Low Side for Timer/Counter n
OCnxHS	Output Compare Channel x High Side for Timer/Counter n

30.2 Alternate Pin Functions

The tables below show the main and alternate pin functions for all pins on each port. They also show which peripheral that makes use of or enables the alternate pin function.

Table 30-1. Port A - Alternate functions

PORT A	PIN #	INTERRUPT	ADCA POS	ADCA NEG	ADCA GAINPOS	ADCA GAINNEG	ACA POS	ACA NEG	ACA OUT	REFA
GND	60									
AVCC	61									
PA0	62	SYNC	ADC0	ADC0	ADC0		AC0	AC0		AREF
PA1	63	SYNC	ADC1	ADC1	ADC1		AC1	AC1		
PA2	64	SYNC/ASYNC	ADC2	ADC2	ADC2		AC2			
PA3	1	SYNC	ADC3	ADC3	ADC3		AC3	AC3		
PA4	2	SYNC	ADC4		ADC4	ADC4	AC4			
PA5	3	SYNC	ADC5		ADC5	ADC5	AC5	AC5		
PA6	4	SYNC	ADC6		ADC6	ADC6	AC6			
PA7	5	SYNC	ADC7		ADC7	ADC7		AC7	AC0 OUT	

Table 30-2. Port B - Alternate functions

PORT B	PIN #	INTERRUPT	ADCB POS	ADCB NEG	ADCB GAINPOS	ADCB GAINNEG	ACB POS	ACB NEG	ACB OUT	DACB	REFB	JTAG
PB0	6	SYNC	ADC0	ADC0	ADC0		AC0	AC0			AREF	
PB1	7	SYNC	ADC1	ADC1	ADC1		AC1	AC1				
PB2	8	SYNC/ASYNC	ADC2	ADC2	ADC2		AC2			DAC0		
PB3	9	SYNC	ADC3	ADC3	ADC3		AC3	AC3		DAC1		
PB4	10	SYNC	ADC4		ADC4	ADC4	AC4					TMS
PB5	11	SYNC	ADC5		ADC5	ADC5	AC5	AC5				TDI
PB6	12	SYNC	ADC6		ADC6	ADC6	AC6					TCK
PB7	13	SYNC	ADC7		ADC7	ADC7		AC7	AC0 OUT			TDO
GND	14											
VCC	15											

31. Peripheral Module Address Map

The address maps show the base address for each peripheral and module in XMEGA A3. For complete register description and summary for each peripheral module, refer to the XMEGA A Manual.

Base Address	Name	Description
0x0000	GPIO	General Purpose IO Registers
0x0010	VPORT0	Virtual Port 0
0x0014	VPORT1	Virtual Port 1
0x0018	VPORT2	Virtual Port 2
0x001C	VPORT3	Virtual Port 2
0x0030	CPU	CPU
0x0040	CLK	Clock Control
0x0048	SLEEP	Sleep Controller
0x0050	OSC	Oscillator Control
0x0060	DFLLRC32M	DFLL for the 32 MHz Internal RC Oscillator
0x0068	DFLLRC2M	DFLL for the 2 MHz RC Oscillator
0x0070	PR	Power Reduction
0x0078	RST	Reset Controller
0x0080	WDT	Watch-Dog Timer
0x0090	MCU	MCU Control
0x00A0	PMIC	Programmable MUltilevel Interrupt Controller
0x00B0	PORTCFG	Port Configuration
0x00C0	AES	AES Module
0x0100	DMA	DMA Controller
0x0180	EVSYS	Event System
0x01C0	NVM	Non Volatile Memory (NVM) Controller
0x0200	ADCA	Analog to Digital Converter on port A
0x0240	ADCB	Analog to Digital Converter on port B
0x0320	DACB	Digital to Analog Converter on port B
0x0380	ACA	Analog Comparator pair on port A
0x0390	ACB	Analog Comparator pair on port B
0x0400	RTC	Real Time Counter
0x0480	TWIC	Two Wire Interface on port C
0x04A0	TWIE	Two Wire Interfaceon port E
0x0600	PORTA	Port A
0x0620	PORTB	Port B
0x0640	PORTC	Port C
0x0660	PORTD	Port D
0x0680	PORTE	Port E
0x06A0	PORTF	Port F
0x07E0	PORTR	Port R
0x0800	TCC0	Timer/Counter 0 on port C
0x0840	TCC1	Timer/Counter 1 on port C
0x0880	AWEXC	Advanced Waveform Extension on port C
0x0890	HIRESC	High Resolution Extension on port C
0x08A0	USARTC0	USART 0 on port C
0x08B0	USARTC1	USART 1 on port C
0x08C0	SPIC	Serial Peripheral Interface on port C
0x08F8	IRCOM	Infrared Communication Module
0x0900	TCD0	Timer/Counter 0 on port D
0x0940	TCD1	Timer/Counter 1 on port D
0x0990	HIRESD	High Resolution Extension on port D
0x09A0	USARTD0	USART 0 on port D
0x09B0	USARTD1	USART 1 on port D
0x09C0	SPID	Serial Peripheral Interface on port D
0x0A00	TCE0	Timer/Counter 0 on port E
0x0A40	TCE1	Timer/Counter 1 on port E
0x0A80	AWEXE	Advanced Waveform Extensionon port E
0x0A90	HIRESE	High Resolution Extension on port E
0x0AA0	USARTE0	USART 0 on port E
0x0AB0	USARTE1	USART 1 on oirt E
0x0AC0	SPIE	Serial Peripheral Interface on port E
0x0B00	TCF0	Timer/Counter 0 on port F
0x0B90	HIRESF	High Resolution Extension on port F
0x0BA0	USARTF0	USART 0 on port F

Mnemonics	Operands	Description	Operation	Flags	#Clocks
CALL	k	call Subroutine	PC ← k	None	3 / 4[1]
RET		Subroutine Return	PC ← STACK	None	4 / 5[1]
RETI		Interrupt Return	PC ← STACK	I	4 / 5[1]
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1 / 2 / 3
CP	Rd,Rr	Compare	Rd - Rr	Z,C,N,V,S,H	1
CPC	Rd,Rr	Compare with Carry	Rd - Rr - C	Z,C,N,V,S,H	1
CPI	Rd,K	Compare with Immediate	Rd - K	Z,C,N,V,S,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b) = 0) PC ← PC + 2 or 3	None	1 / 2 / 3
SBRS	Rr, b	Skip if Bit in Register Set	if (Rr(b) = 1) PC ← PC + 2 or 3	None	1 / 2 / 3
SBIC	A, b	Skip if Bit in I/O Register Cleared	if (I/O(A,b) = 0) PC ← PC + 2 or 3	None	2 / 3 / 4
SBIS	A, b	Skip if Bit in I/O Register Set	If (I/O(A,b) =1) PC ← PC + 2 or 3	None	2 / 3 / 4
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC ← PC + k + 1	None	1 / 2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC ← PC + k + 1	None	1 / 2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1 / 2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1 / 2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1 / 2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1 / 2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1 / 2
BRLT	k	Branch if Less Than, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1 / 2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1 / 2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1 / 2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1 / 2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1 / 2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1 / 2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1 / 2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1 / 2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1 / 2
Data Transfer Instructions					
MOV	Rd, Rr	Copy Register	Rd ← Rr	None	1
MOVW	Rd, Rr	Copy Register Pair	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LDS	Rd, k	Load Direct from data space	Rd ← (k)	None	2[1][2]
LD	Rd, X	Load Indirect	Rd ← (X)	None	1[1][2]
LD	Rd, X+	Load Indirect and Post-Increment	Rd ← (X) X ← X + 1	None	1[1][2]
LD	Rd, -X	Load Indirect and Pre-Decrement	X ← X - 1, ← X - 1 Rd ← (X) ← (X)	None	2[1][2]
LD	Rd, Y	Load Indirect	Rd ← (Y) ← (Y)	None	1[1][2]
LD	Rd, Y+	Load Indirect and Post-Increment	Rd ← (Y) Y ← Y + 1	None	1[1][2]

Figure 35-5. Active Supply Current vs. Vcc

f_{SYS} = 2.0 MHz internal RC

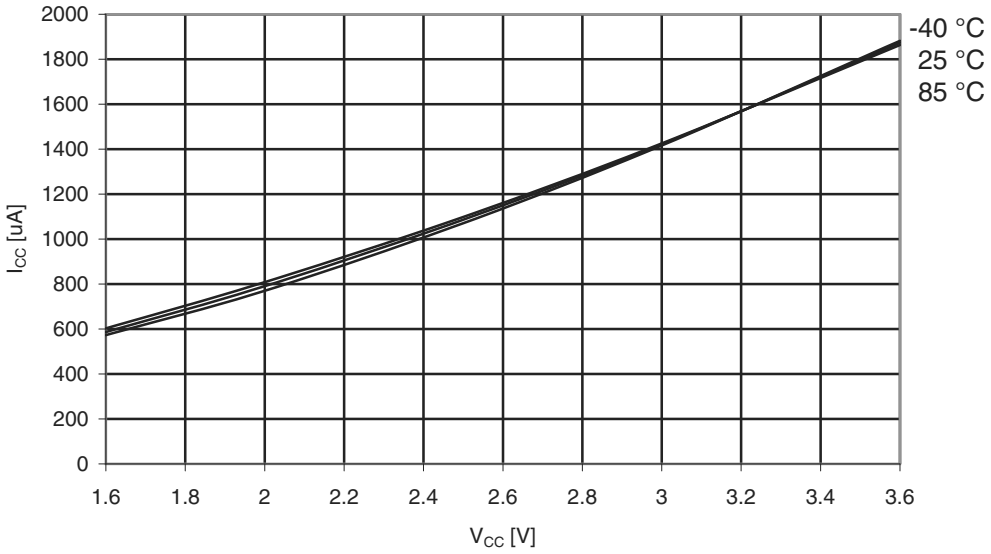


Figure 35-6. Active Supply Current vs. Vcc

f_{SYS} = 32 MHz internal RC prescaled to 8 MHz

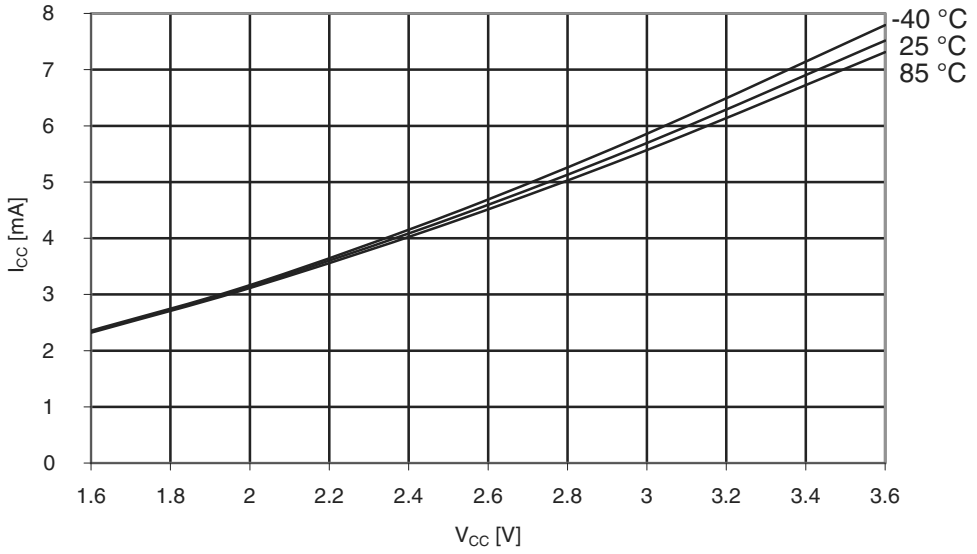
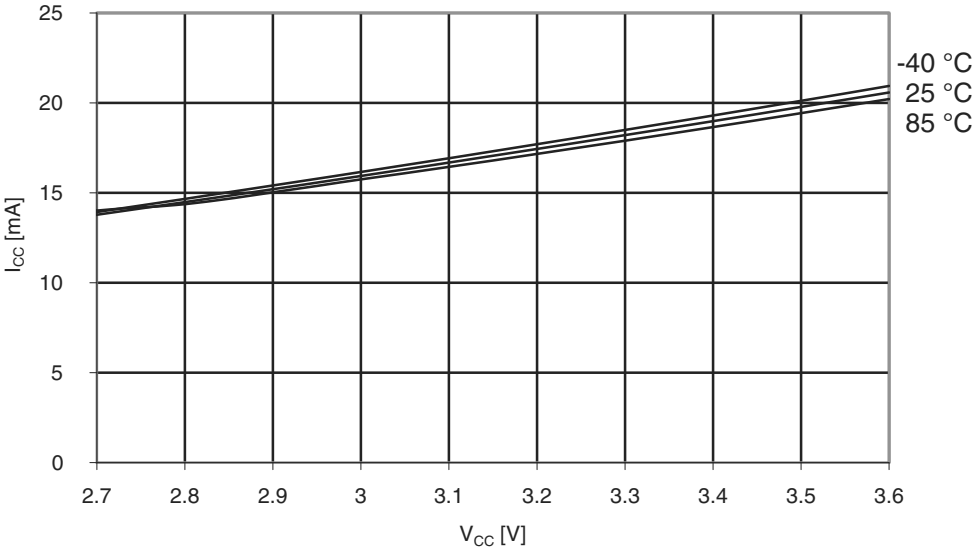


Figure 35-7. Active Supply Current vs. Vcc

f_{SYS} = 32 MHz internal RC



35.2 Idle Supply Current

Figure 35-8. Idle Supply Current vs. Frequency

f_{SYS} = 0 - 1.0 MHz, T = 25°C

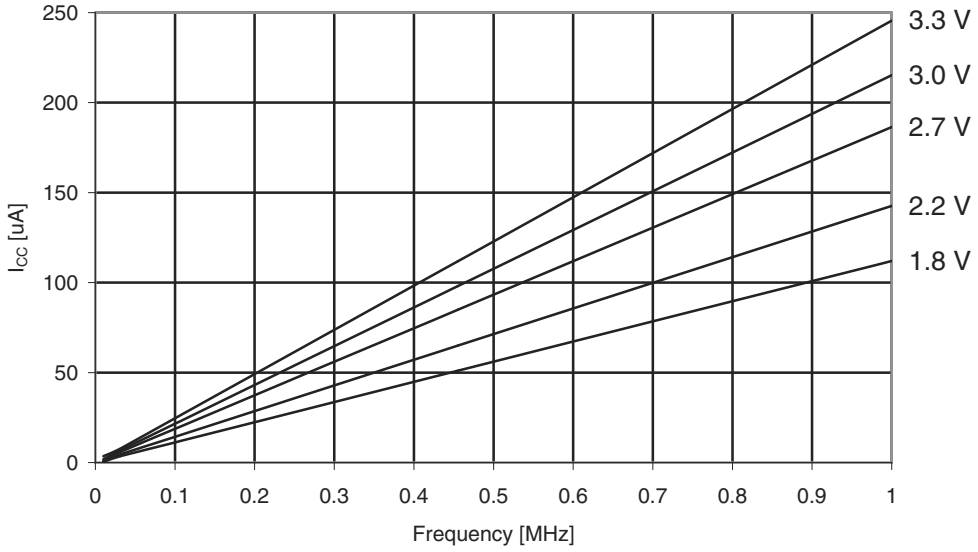


Figure 35-13. Idle Supply Current vs. Vcc

f_{SYS} = 32 MHz internal RC prescaled to 8 MHz

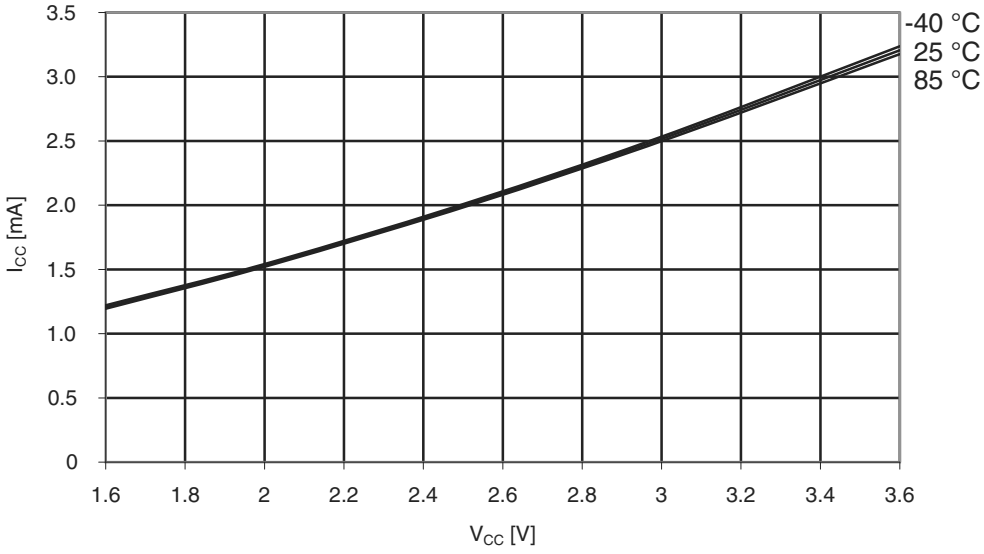
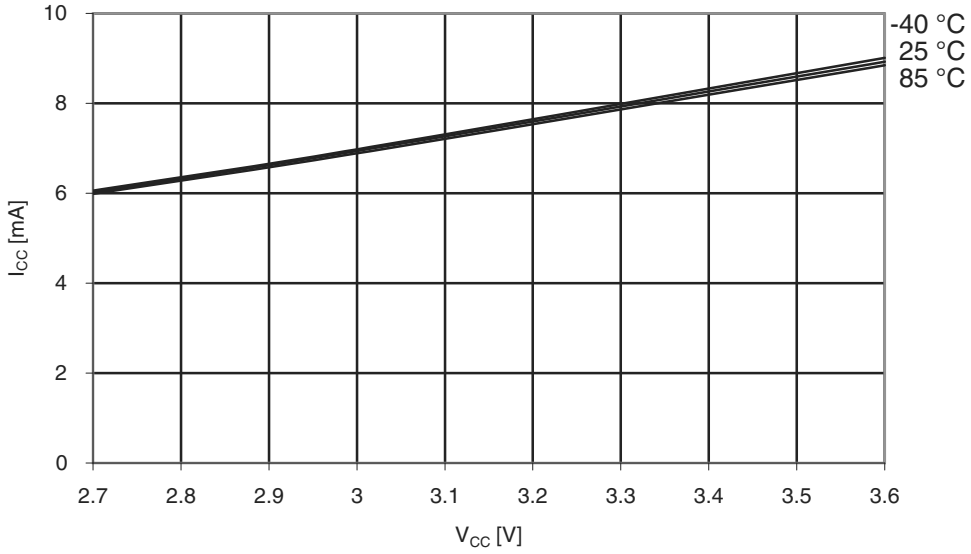


Figure 35-14. Idle Supply Current vs. Vcc

f_{SYS} = 32 MHz internal RC



35.6 Pin Output Voltage vs. Sink/Source Current

Figure 35-21. I/O Pin Output Voltage vs. Source Current

Vcc = 1.8V

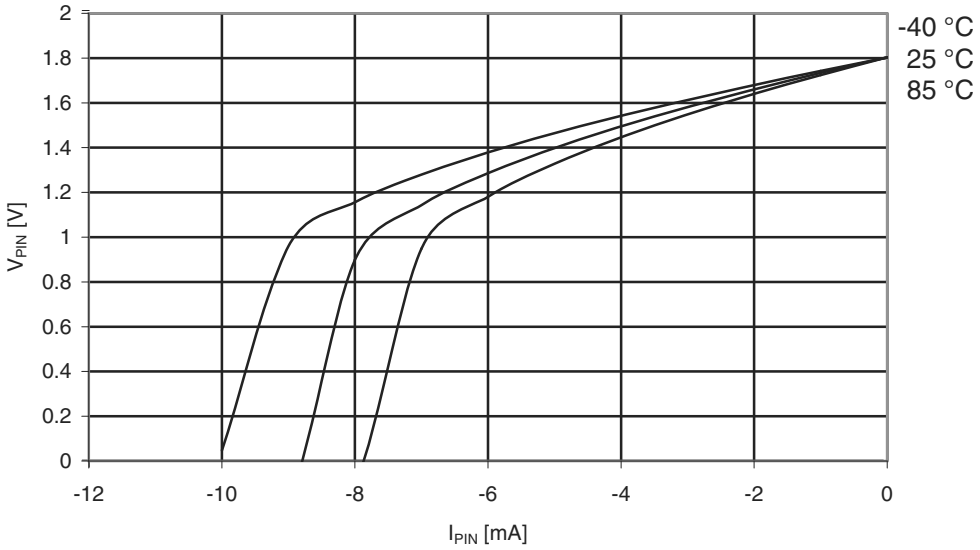
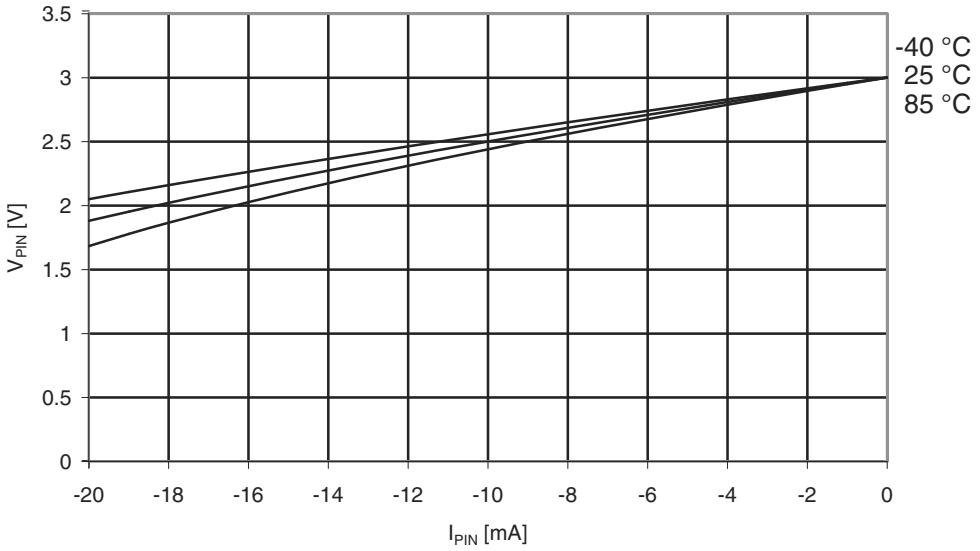


Figure 35-22. I/O Pin Output Voltage vs. Source Current

Vcc = 3.0V



Problem fix/Workaround

Wait at least one prescaled RTC clock cycle before reading the RTC CNT value.

22. Pending asynchronous RTC-interrupts will not wake up device

Asynchronous Interrupts from the Real-Time-Counter that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again.

Problem fix/Workaround

None.

23. TWI Transmit collision flag not cleared on repeated start

The TWI transmit collision flag should be automatically cleared on start and repeated start, but is only cleared on start.

Problem fix/Workaround

Clear the flag in software after address interrupt.

24. Clearing TWI Stop Interrupt Flag may lock the bus

If software clears the STOP Interrupt Flag (APIF) on the same Peripheral Clock cycle as the hardware sets this flag due to a new address received, CLKHOLD is not cleared and the SCL line is not released. This will lock the bus.

Problem fix/Workaround

Check if the bus state is IDLE. If this is the case, it is safe to clear APIF. If the bus state is not IDLE, wait for the SCL pin to be low before clearing APIF.

Code:

```
/* Only clear the interrupt flag if within a "safe zone". */
while ( /* Bus not IDLE: */
       ((COMMS_TWI.MASTER.STATUS & TWI_MASTER_BUSSTATE_gm) !=
         TWI_MASTER_BUSSTATE_IDLE_gc)) &&
         /* SCL not held by slave: */
         !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm)
      )
{
    /* Ensure that the SCL line is low */
    if ( !(COMMS_PORT.IN & PIN1_bm) )
        if ( !(COMMS_PORT.IN & PIN1_bm) )
            break;
}
/* Check for an pending address match interrupt */
if ( !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm) )
{
    /* Safely clear interrupt flag */
    COMMS_TWI.SLAVE.STATUS |= (uint8_t)TWI_SLAVE_APIF_bm;
}
```

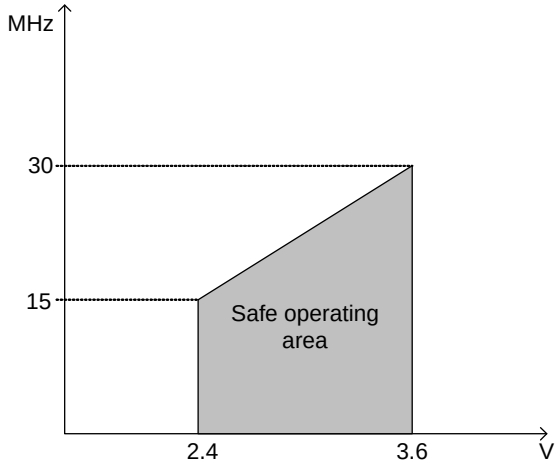
25. TWI START condition at bus timeout will cause transaction to be dropped

If Bus Timeout is enabled and a timeout occurs on the same Peripheral Clock cycle as a START is detected, the transaction will be dropped.

10. Operating Frequency and Voltage Limitation

To ensure correct operation, there is a limit on operating frequency and voltage. Figure 36-3 on page 109 shows the safe operating area.

Figure 36-3. Operating Frequnecy and Voltage Limitation



Problem fix/Workaround

None, avoid using the device outside these frequnecy and voltage limitations.

11. Inverted I/O enable does not affect Analog Comparator Output

The inverted I/O pin function does not affect the Analog Comparator output function.

Problem fix/Workarund

Configure the analog comparator setup to give a inverted result (i.e. connect positive input to the negative AC input and vice versa), or use and externel inverter to change polarity of Analog Comparator Output.

36.2 ATxmega192A3, ATxmega128A3, ATxmega64A3

36.2.1 rev. E

- **Bandgap voltage input for the ACs can not be changed when used for both ACs simultaneously**
- **VCC voltage scaler for AC is non-linear**
- **ADC has increased INL error for some operating conditions**
- **ADC gain stage output range is limited to 2.4 V**
- **ADC Event on compare match non-functional**
- **Bandgap measurement with the ADC is non-functional when VCC is below 2.7V**
- **Accuracy lost on first three samples after switching input to ADC gain stage**
- **Configuration of PGM and CWCM not as described in XMEGA A Manual**
- **PWM is not restarted properly after a fault in cycle-by-cycle mode**
- **BOD will be enabled at any reset**
- **DAC is nonlinear and inaccurate when reference is above 2.4V or VCC - 0.6V**
- **DAC has increased INL or noise for some operating conditions**
- **DAC refresh may be blocked in S/H mode**
- **Conversion lost on DAC channel B in event triggered mode**
- **EEPROM page buffer always written when NVM DATA0 is written**
- **Pending full asynchronous pin change interrupts will not wake the device**
- **Pin configuration does not affect Analog Comparator Output**
- **NMI Flag for Crystal Oscillator Failure automatically cleared**
- **Crystal start-up time required after power-save even if crystal is source for RTC**
- **RTC Counter value not correctly read after sleep**
- **Pending asynchronous RTC-interrupts will not wake up device**
- **TWI Transmit collision flag not cleared on repeated start**
- **Clearing TWI Stop Interrupt Flag may lock the bus**
- **TWI START condition at bus timeout will cause transaction to be dropped**
- **TWI Data Interrupt Flag (DIF) erroneously read as set**
- **WDR instruction inside closed window will not issue reset**

1. Bandgap voltage input for the ACs cannot be changed when used for both ACs simultaneously

If the Bandgap voltage is selected as input for one Analog Comparator (AC) and then selected/deselected as input for another AC, the first comparator will be affected for up to 1 µs and could potentially give a wrong comparison result.

Problem fix/Workaround

If the Bandgap is required for both ACs simultaneously, configure the input selection for both ACs before enabling any of them.

2. VCC voltage scaler for AC is non-linear

The 6-bit VCC voltage scaler in the Analog Comparators is non-linear.

26. WDR instruction inside closed window will not issue reset

When a WDR instruction is execute within one ULP clock cycle after updating the window control register, the counter can be cleared without giving a system reset.

Problem fix/Workaround

Wait at least one ULP clock cycle before executing a WDR instruction.

37. Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

37.1 8068U – 06/13

1. Not recommended for new designs - Use XMEGA A3U series.

37.2 8068T – 12/10

1. Datasheet status changed to complete: Preliminary removed from the front page.
2. Updated all tables in the “Electrical Characteristics” .
3. Updated ”Packaging information” on page 61.
4. Replaced Table 34-11 on page 69
5. Replaced Table 34-18 on page 71 and added the figure ”TOSC input capacitance” on page 71
6. Added ERRATA “rev. E” .
7. Added ERRATA “rev. B” .
8. Updated ERRATA for ADC (ADC has increased INL error for some operating conditions).
9. Updated the last page by Atmel new Brand Style Guide.

37.3 8068S – 09/10

10. Updated ”Errata” on page 93.

37.4 8068R – 08/10

1. Updated the Footnote 3 of ”Ordering Information” on page 2.
2. Updated Footnote 2 of Figure 2-1 on page 3.
3. Updated ”Data Memory Map (Hexadecimal address)” on page 11. 192A3 has 2 KB EEPROM.
4. Updated ”Features” on page 27. Event Channel 0 output on port pin 7.
5. Updated ”Absolute Maximum Ratings*” on page 63 by adding Icc for Flash/EEPROM Programming.
6. Added AVCC in ”ADC Characteristics” on page 67.
7. Updated Start up time in ”ADC Characteristics” on page 67.

37.15 8068G – 09/08

1. Updated ”Features” on page 1.
2. Updated ”Ordering Information” on page 2.
3. Updated ”Features” on page 9 by removing “External Memory...”.
4. Updated Figure 7-1 on page 10 and Figure 7-2 on page 11.
5. Updated Table 7-2 on page 14 and Table 7-3 on page 14.
6. Updated ”Features” on page 41 and ”Overview” on page 41.
7 Removed “Interrupt Vector Summary” section from datasheet.

37.16 8068F – 08/08

1. Changed Figure 2-1’s title to “Block diagram and pinout.”
2. Changed Package Type to “64M2” in ”Ordering Information” on page 2 and in ”Errata” on page 93.
3. Updated Table 30-5 on page 52.
4. Inserted a correct “64A” TQFP drawing on page 61.

37.17 8068E – 08/08

1. Updated ”Block Diagram” on page 5.
2. Inserted “Interrupt Vector Summary” on page 54.

37.18 8068D – 06/08

1. References to External Bus Interface (EBI) removed from ”Features” on page 1.

37.19 8068C – 06/08

1. Updated ”Features” on page 1.
2. Updated Figure 2-1 on page 3.
3. Updated ”Overview” on page 4.
4. Updated Table 7-2 on page 14.